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DIGITAL DEMODULATION TECHNIQUES FOR RADIO CHANNELS

A Thesis Submitted for fulfilment of the Degree of Master of Engineering (Electrical)

By

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Declaration

This thesis contains no material which has been accepted for the award of any other degree or diploma in any university. To the best of my knowledge and belief, it contains no material previously published or written by another person, except where due reference is made in the text of the thesis.



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Acknowledgments

The author gratefully acknowledges Philips Radio Communications Systems Ltd for providing financial assistance and access to equipment for this project. Financial assistance was also provided by the Australian Government through an Australian Postgraduate Industrial Research Award (APIRA), both these bodies made this work possible.

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Table

<u>SYNOPSIS</u>

The basis of this research is directed towards the Private Mobile Radio (PMR) networks, which play significant roles in Taxi, Police, Ambulance and other such Services. With an ever increasing need for data transmission, the current PMR systems which were designed for voice are not adequate. This research will examine a digital modulation scheme which can co-exist with an analog system.

The generation of the digital modulation will be examined in terms of Adjacent Channel Interference (ACI) requirements. Simulation techniques for the mobile radio channel are discussed, for evaluation of demodulator performance. Existing demodulation techniques were reviewed, with several of these simulated to find the most appropriate demodulation scheme for this application. This included the development of a new detection scheme. A test system using Digital Signal Processing (DSP) techniques was constructed.

1.0 Introduction

1.1 Overview

The development of cellular and related systems forming public mobile communications has had rapid growth over recent years. The concept of Personal Communications Networks (PCN), where a small and compact mobile terminal is used whereby the user can be contacted irrespective of location is becoming more realistic and has been an overall driving force behind cellular networks. The demand for the present analog cellular systems (AMPS used in both the US and Australia) is so high that the allocated radio spectrum has become saturated, hence severely reducing the grade of service [1,2]. To alleviate these problems future cellular systems will apply digital concepts which align neatly with the land digital systems, so that the mobile system becomes a natural extension of the already existing digital networks (such as ISDN, IBCN).

The dramatic advances in digital Very Large Scale Integration (VLSI) techniques allow miniaturisation with low power consumption devices, which lead to cheaper and smaller terminals thus become more attractive to potential users. The manufacturers had seen the potential market of such digital cellular systems and injected many dollars into developing this concept which far outstripped the progress of the traditional analog Private Mobile Radio (PMR). PMR systems play significant roles in Taxi, Police and Ambulance services, etc., and are presently based on Analog Narrowband Frequency Modulation (NBFM) techniques using Frequency Division Multiplexing (FDM)¹. There has been some proposed digital PMR systems such as Private Advanced Radio Service (PARS) in the UK [3] and a low bit rate packeting system developed in Sweden by Ericsson (Mobitex) with a higher rate version planned for release in the US [4].

Operators of PMR systems are charged for the radio spectrum they use and presently have much capital invested into the existing PMR mobile equipment. However these systems will have to advance in order to satisfy the need for efficient spectral usage and new/improved services, just as PMR has developed from the channel spacings of $120kHz \rightarrow 60kHz \rightarrow 50kHz$ (UHF) $\rightarrow 30kHz$ to the 12.5kHz channel spacings of today [1].

This research will describe the development of a digital mobile link which will co-

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¹ In this case there is one channel per carrier, which is termed Single Channel Per Carrier (SCPC).

exist with the present analog PMR with the full potential being realised once digital PMR specifications are produced. This would allow the development of present and future applications requiring a data link in a mobile environment to commence.

1.2 PMR of today

PMR systems generally work in a simplex mode as opposed to radio-telephone or the more recent cellular systems. The mobiles and base station registered all have access to one or several carriers which are assigned to a specific group of users. In this case all mobiles and bases tuned to the same channel, can hear each other, although only one can transmit at any given time. Although the system is limited in terms of public use its true market exists for organisations requiring fleet management where this type of system is a powerful tool. Since PMR generally runs in a broadcasting mode the closest mobile unit can respond rapidly.

The PMR network architecture is dependant on the operators' needs for coverage and/or availability. Public safety services such as Police, Ambulance and Fire Brigade all have large coverage areas, hence a need for a multi-site base station scheme with a multitude of channels. Whereas a dispatching service may operate in a small region which can adequately be serviced by one base-station, which if availability is not a major concern or traffic flow is low then the sharing of a single radio channel to conserve spectrum becomes a possibility. Some of the possible PMR architectures, including the extremes above, will now be briefly examined:

The multi-site configuration comes in two forms; i) Repeater type, where a base station would be set up on the fringes of the Central site coverage to receive and then regenerate at a higher power level and generally on a different channel to the Central site signal. Regeneration using the same channel would require 2 antennae, both of which would have to be directional to ensure 90dB isolation to eliminate feedback; ii) Isolated type, where the additional base-stations are placed, such that limits of coverage overlap the Central site coverage. The Central site would relay messages to the isolated site through a low power highly directional radio link. If outer most sites used the same frequency as the Central site, i.e. a quasi-synchronous mode, and large frequency offsets exist between the sites, poor quality voice would be received due to the FM capture effect [3].

Operators with low traffic could share frequencies through the use of Continuous Tone Controlled Signalling System (CTCSS) which uses sub-audible frequencies (60-500Hz) to

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indicate channel use by a particular operator. Consider two operators, each allowed the same channel allocation, but assigned A and B CTCSS tones. If the operator using tone A wishes to transmit, the operator would first check that the channel is free by checking for the B tone. Once satisfied the channel is free, A transmits the message which is received by all mobile transceivers. However, operator B mobile receivers mute the speaker if the A tone is received.

For operators requiring very little traffic, a large coverage and instant two-way communications, a single channel with multiple sites is available. Each site is polled for the specific mobile user using a sequence of five CTCSS tones (ZVEI, CIRR or NATEL mobile identification schemes [3]). Once all sites are polled the one with the greatest signal strength is used for communications between the Central office and the mobile unit. Alternatively if an instantaneous response is not required, a paging service may be sufficient.

1.3 Background

This research was initiated by Philips Radio Communication Systems whose worldwide design and development of PMR equipment is based in Australia². Philips required this research prior to the development in Australia of their range of digital mobile radio equipment. It was estimated that there were 300,000 users and a \$700 million market for PMR networks in Australia up to 1989³. Presently all these networks operate on techniques which have many limitations, with inefficient use of the spectral allocation being of prime concern (this is very expensive).

The reasons for upgrading the cellular systems to digital are also applicable for PMR, specifically [5,6]:

- DSP / Digital techniques (ASIC) are continually reducing in cost, thus decreasing end user terminal costs.
- Digital transmission air interface can tolerate more interference. This robustness in the mobile environment gives a consistent performance throughout the mobile network due to [1]:
 - a) Adjacent Channel Interference (ACI) can be higher which means higher capacities (A feature not fully exploited here).

² Once upon a time, left mid 1991

³ Lecture by Kevin Philips, Network Manager, MCS Telecom Australia, 8/2/89.

- b) Inherent threshold effect in digital signals allows more noise when compared to the analog counter part.
- c) Error Correction techniques are becoming more sophisticated and if applied correctly can dramatically improve the Bit Error Rate (BER). There will always be some trade off in throughput.
- Secure channels can be implemented using public key encryption techniques with minimal expense.
- Full duplex operation over a single carrier via the Ping-Pong technique (i.e. DECT system), simplifies handover in a cellular system as only one frequency channel assignment is required. Time-Duplex SCPC techniques do not require simultaneous transmission and reception, dispensing with a diplexer⁴.
- Flexible information transfer. All information formats can be encoded into a digital stream. Digital voice at toll grade quality is available for bit rates of 13kb/s⁵ which will no doubt reduce even further due to the world digital cellular drive. Reduced quality services using 4.8kb/s are presently being researched. These would be adequate for most PMR operators [3].
- Scope for increased capacity. Further channel splitting is easily achievable if TDM is applied. This would only require ROM and CODEC replacement in the terminal. Hence, upgrading of the network would be simple with minimal hardware modifications.

These advantages of digital have already led to the development of digital cellular radio in Europe (GSM system) and the USA. The European GSM system is based on a 270kb/s TDM system, while the planned US system operates on FDM (existing channel spacing of 30kHz) allocated into 3 channels using TDM, allowing compatibility with the existing AMPS system. The Japanese use a FDM digital modulation with slightly closer channel (25kHz) spacing compared to the US. These three digital standards are planned for release between 1992 and 1995, with the digitisation of PMR to follow. Presently the standards for PMR ACI are being reviewed by the Department of Transport and

⁴ Future low rate CODECs will make such a system possible for PMR.

⁵ As recommended in the Pan-European System (GSM-Rec 06.10)

Communications (DOTAC/Austel).

Due to the allocation of frequencies, the techniques used to enable the cellular network to become digital can not be adopted in PMR. The spectral usage in cellular systems often spreads outside the allocated channel. Applying similar techniques in PMR would result in excessive ACI. Any proposed system must co-exist with existing analog channels, hence ACI tests must conform to existing analog specifications which will severely limit the full potential of this intermediary digital system.

Any proposed digital PMR system must meet two important criteria; a) High spectral efficiency, which will minimise ACI and hence allow tight channel spacings (increasing the number of channels for a given bandwidth) and, b) Efficient power amplification which increases talk time (time between battery recharging) for portable equipment. Presently there are two schools of thought in the cellular world as both these criteria are contradictive with current technologies. The Europeans believed that simple high efficiency linear amplifiers could not be developed cheaply enough, hence they considered only Continuous Phase Modulation (CPM) schemes with Gaussian Minimum Shift Keying (GMSK) being the final choice. Whereas the $\pi/4$ shift DQPSK proposed for the US and Japan has higher spectral efficiency than GMSK. This uses Nyquist filtering (α =0.35) to control the spectrum which causes envelope variation hence requiring linear amplification to retain the benefits of Nyquist filtering⁶.

In addition to the above requirements, this work is further bound by the desire of Philips for a solution involving low developmental costs and minimum modifications to their existing PMR FM equipment, such that infrastructure costs are minimised for current operators. The modulation selected must be based around frequency or phase type modulation since the amplification stages used in existing equipment are class C. Gaussian Minimum Shift Keying (GMSK) is a phase modulation with a controllable side lobe to main lobe ratio which will be utilised in this research project. GMSK is further discussed in the next Chapter with the implementation of a general purpose CPM generator described.

In order to evaluate the various CPM detection schemes the mobile channel is modelled. This is covered in Chapter 3. Classical models for the mobile radio channel are presented, along with software implementation for the simulation of both the Classical model

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⁶ The $\pi/4$ shift eliminates zero crossing from the signal thereby reducing crossover distortion, however there is still the need for linear amplification.

and the multiple tapped delay line GSM model.

A literature survey of current detection techniques is presented in Chapter 4. A new scheme, Forward Estimation using Differential Feedback Equalisers (FEDFE), is simulated and compared to existing detection schemes suitable for this application, these comparisons are presented in Chapter 5. The new scheme has comparable performance to the more complex MLSE detector in a fading channel.

The specification of the CPM (Bit rate, BT and deviation) were obtained from extensive measurements which related the above three parameters to the eye openings and timing jitter windows. These measurements were performed under the constraint of meeting existing analog PMR ACI requirements. The new scheme together with 3 other data recovery schemes were implemented using the Texas Instruments TMS320c25, this also included a simple coding technique implemented using a Motorola 6809 to combat against deep fades. The system using FEDFE obtained a BER≈1e-2 at an $E_b/N_o=24.3$ dB, an improvement on existing schemes of 1.2dB over Conventional+DFE and 1.8dB over the Half Bit Offset technique. Further results are presented in Chapter 6.

2.0 Modulation

This chapter will briefly look at the historical development leading to GMSK, and presents the general signal modulation equations defining CPM. Regeneration of published diagrams relating to phase trees, phase cylinders and spectrums of various CPM schemes were performed to reinforce understanding.

A description of the hardware modulator designed to test the various GMSK demodulators is given, along with resulting spectral performance compared with theoretical truncated spectrums.

2.1 Background

In the mid 50's Frequency Shift Keying (FSK) for telegraph systems was the only real form of digital communications. At that stage there was very little in terms of digital components, and the advantages of digital were hard to define, because the technology did not exist.

In 1961 a U.S. patent relating to Minimum Shift Keying [7] (MSK, also referred to as Fast Frequency Shift Keying) was logged. This was a significant break through as it eliminated phase discontinuity in the signal, and so improved the spectral performance. Although the phase is continuous at the bit boundaries, the equivalent frequency response is still stepped producing spectral side lobes which are unacceptable in terms of Adjacent Channel Interference for this application.

Sinewave smoothed MSK eliminated the frequency step, and reduced the total number of side lobes. The spectral characteristics up to $(f-f_c)/f_{bit}=2.0$ were still approximately the same as MSK.

In 1978, DeJager [8] introduced Tamed Frequency Modulation (TFM) which made the phase transitions very smooth by considering the present and adjacent bits either side. The spectral properties were very good, quickly dropping to -70dB @ $(f-f_c)/f_{bit}=1.0$ with minimal sidelobes. The impulse response is of infinite length and so truncation is required. This can degrade the spectrum. DeJager also presented the ROM lookup table technique for the generation of TFM using in-phase and quadrature-phase signals.

The dominant technique to improving side lobe performance of MSK modulation is to use a premodulation filter. This produces significant intersymbol interference (ISI). This

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controlled ISI introduced at the transmitter can be removed with certain techniques at the receiver, since the interaction between adjacent symbols is known.

Murota [9] first demonstrated the use of Gaussian premodulation filter directed towards mobile radio communications, and showed that GMSK with BT=0.2 is equivalent to TFM. Other types of filtering include Raised Cosine, Spectrally Raised Cosine and Rectangular. All these schemes are part of the Continuous Phase Modulation¹ (CPM) group, which have been well documented by Sundberg & Aulin [10].

2.2 Mathematical Definition

Continuous Phase Modulation signals can be described by the following equations:

$$s(t) = \cos(2\pi f_c t + \mathbf{\phi}(t, \boldsymbol{\alpha})) \tag{2.1}$$

where, f_c carrier frequency α Bit sequence

t time

$$\phi(t,\alpha) = 2\pi h \sum_{i=-\infty}^{+\infty} \alpha_i q(t-iT)$$
(2.2)

where, h modulation index q cumulative phase of a single bit

and,
$$q(t) = \int_{-\infty}^{t} g(\tau) d\tau$$
 (2.3)

The smoothness and length of the g(t) pulse determines the spectral properties of the modulation. The q(t) must be normalised to give 1/2 for $t\rightarrow\infty$, hence for rational fraction modulation indexes the receiver can be coherent.

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¹ Also referred to as Digital Phase Modulation (DPM), or Constant Phase Frequency Shift Keying (CPFSK).

2.3 GMSK frequency and phase pulses

Published literature [10,36,11] defined the g(t) pulse for GMSK in many different forms. These were all mathematically shown to be equivalent. The form used here for g(t) generation is shown below [10]:

$$g(t) = \frac{1}{2T} \left(Q \left[2\pi B \frac{t - \frac{T}{2}}{\ln(2)^{\frac{1}{2}}} \right] - Q \left[2\pi B \frac{t + \frac{T}{2}}{\ln(2)^{\frac{1}{2}}} \right] \right)$$
(2.4)
where,
$$Q(t) = \int_{t}^{-\infty} \frac{1}{\sqrt{2\pi}} e^{\frac{-r^{2}}{2}} dr$$
$$B - 3dB \text{ bandwidth Gaussian filter}$$
$$T \text{ bit period}$$

The integration of Q(t) can not be solved analytically hence numerical integration techniques were required. In this work Simpson's rule for integration was used to evaluate Q(t) to an accuracy of 10⁻¹⁰, using Table 7.1 in [12] as the benchmark. Once the value of Q(t) was known, g(t) could be calculated, and using numerical integration many q(t) lookup tables were calculated for various BT products. The respective g(t) and q(t) pulses for GMSK are shown in Figure 2.1 and Figure 2.2 for a truncation length of four.

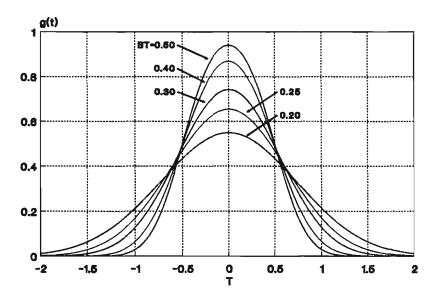


Figure 2.1 g(t) frequency pulse for GMSK

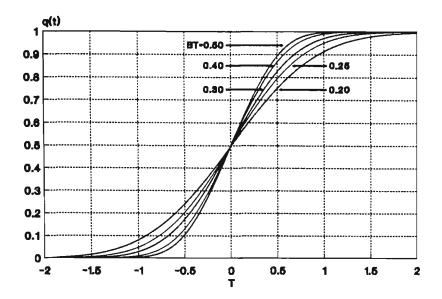
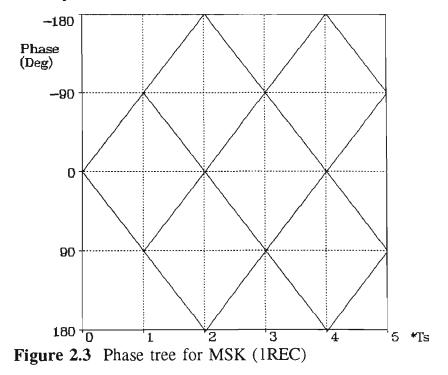


Figure 2.2 q(t) phase pulse for GMSK

2.4 Phase Trees/Cylinders

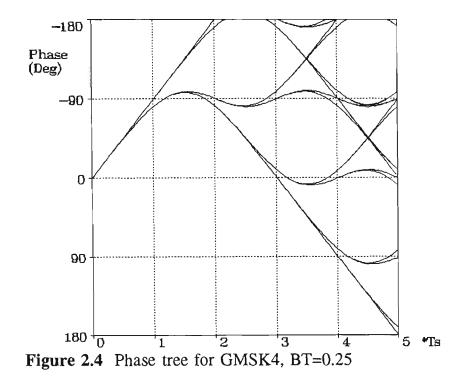
A phase tree shows, over a period of time, the effect of modulation on the carrier and gives an indication of the noise margin, hence the quality of transmitted data. The following trees were generated using Equation 2.2 and the appropriate q(t) pulse. Figure 2.3 illustrates the phase tree for MSK (1REC). During the first interval if a 1 is transmitted at time=Ts the phase shift is $\pi/2$. Alternatively, if a 0 is transmitted the resultant phase shift is $-\pi/2$ (assuming h=1/2). A bit only has influence on the phase over a one bit period, hence MSK is classed as a Full Response CPM scheme.



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A phase tree for GMSK is shown in Figure 2.4. The q(t) for GMSK is theoretically infinite; - for practical use they were truncated to a length of four symbols. A symbol now influences adjacent symbols. This type of CPM is classed as a partial response scheme. Previous bits before time=0 were assumed to be logic 1's. Since there is memory in the signal, several transmissions of logic 0's (-1) are required to bring the phase back to zero degrees (Note: not until 3*Ts does the phase=0 degrees).



The phase tree is allowed to build up over 7*Ts. For symbol intervals greater than 7*Ts all possible phase paths would be displayed (L_T =4, Binary signalling and h=1/2, there are 64 paths). If the display is now symbol synchronised, and symbols greater than 7*Ts are displayed on top of each other, a phase trellis would have been constructed. This is equivalent to eve diagrams displayed on an Oscilloscope, that are an aid in evaluating noise performance.

When the phase is greater than π , it will wrap around to $-\pi$ if the modulation index (h) is selected correctly. A phase cylinder is only appropriate for constant envelope modulation and is simply a wrapped phase trellis. Figure 2.5 shows a typical GMSK phase cylinder for BT=0.25 - phase is shown in the X-Y plane and time is into the page.

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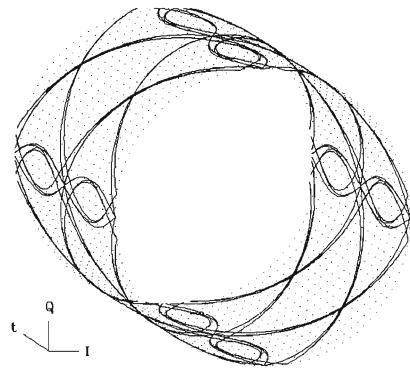


Figure 2.5 Phase cylinder for GMSK, BT=0.25

2.5 GMSK spectrum

GMSK spectra, using a truncation length of four symbols, are shown in Figure 2.6. The spectra were found by using the q(T) pulses found in section 2.3 and the algorithm developed by Sundberg [13] for calculating DPM spectrums.

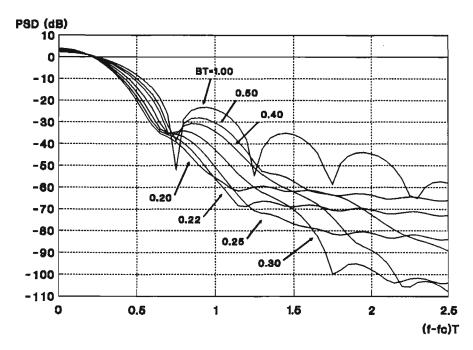


Figure 2.6 Truncated GMSK spectrums (L_T=4)

An interesting characteristic of these spectra shown in Figure 2.6, for relatively small BT products (≤ 0.3), is the truncation effect which causes a spectrum floor. As the BT product

for GMSK is reduced, the length of the g(t) and q(T) pulse increases, whereby the fixed truncation length has a more significant effect in increasing the spectrum floor. This is clearly visible for BT products of 0.25, 0.22 and 0.20.

2.6 Generation Techniques

The baseband GMSK signals given by Equation 2.2 can be translated to Radio Frequencies (RF) using either phase or frequency modulation (see Figure 2.7).

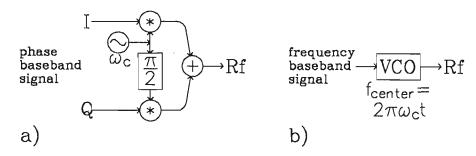


Figure 2.7 RF generation a) Phase b) Frequency

Coherent detection is only possible with phase modulation or a frequency modulation system with feedback to control the strict relationship between deviation frequency and bit rate (for a controlled deviation index). Both of these translation techniques require DC coupled circuits to make full use of spectrum allocation.

The original proposal by Murota [9] for the generation of GMSK, was to pass a NRZ sequence through a Gaussian filter and feed a VCO (Figure 2.7b). Although this technique was easy to implement, it would not be acceptable for coherent demodulation. The main reason being that conventional free-running VCO's do not have the frequency stability or linearity required by synchronisation schemes.

Other possibilities for the modulator implementation include:

- i) Full digital ROM based technique: DeJager [8], used a phase state machine and a shift register to access two ROM's to generate I/Q signals.
- PLL approach: This requires a PLL which is DC coupled. This is a serial modulator capable of very high data rates. Due to its complex design it can only be cost effective if used at high frequencies.
- iii) Band Pass filter and hard-limiter:
- iv) $\Sigma\Delta$ approach: This is a one bit DAC which is heavily oversampled, producing

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Pulse Width Modulation (PWM). A relatively new technique, which can achieve higher data rates than the ROM approach. This technique is still being researched, and has some minor problems relating to settling time.

Suzuki [14] developed a chip in 1984 using LSI techniques based on approach i). The chip generated I/Q GMSK signals for a BT=0.2, but this has not been referred to in recent papers. A generator using BT=0.2 would not be satisfactory for this project as the actual spectral requirements are not initially known, hence a GMSK generator was built which could handle a variety BT products, so that spectrum evaluations could be performed.

2.6.1 GMSK generator

This section describes the design and performance of the GMSK generator developed for this work. The design was based on a ROM approach which can accommodate a variety of CPM schemes and produce either phase or frequency baseband modulation signals depending on the ROM data. For practical circuits the q(t) pulse must be truncated (L_T) and with h=1/2, Equation 2.2 can be rewritten as Equation 2.5.

$$\phi(t,\alpha) = \frac{\pi}{2} \sum_{i=-\infty}^{n-L_T-1} \alpha_i + 2\pi h \sum_{i=n-L_T}^n \alpha_i q(t-iT)$$
(2.5)

The first term in Equation 2.5 can have one of four states 0, $\pi/2$, π and $3\pi/2$ over the interval [0,2 π). This would require a two bit state machine. When t=iT the first term either advances or retards by $\pi/2$, depending on the α_{n-Lt-1} th bit. The second term takes into account the partial cumulative phase contributions of bits (n-L_T) to n. Binary signalling with L_T=4 will be considered, hence there are 2⁴ phase paths which are bit dependant, so a memory of the previous four bits is required.

A total of six bits (2 state machine and 4 previous bit memory), is only capable of regenerating the signal at the sampling instant. A MOD16 counter gives 16 samples per symbol thereby reducing analog reconstruction requirements.

The block diagram of the modulator design is shown in Figure 2.8.

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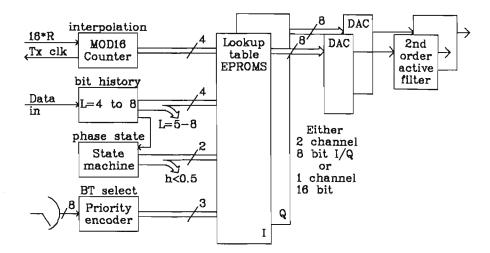


Figure 2.8 Modulator Block diagram

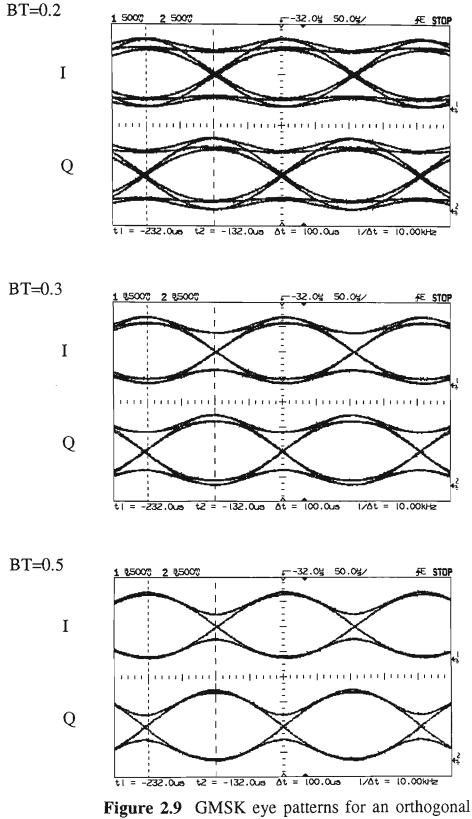
The final design can handle CPM schemes with the following specifications:

L=Truncation Length $4\rightarrow 8$ h=Modulation index 2/x where $x=2\rightarrow 16$ Up to eight CPM schemes can exist (h=1/2, L_T=4)

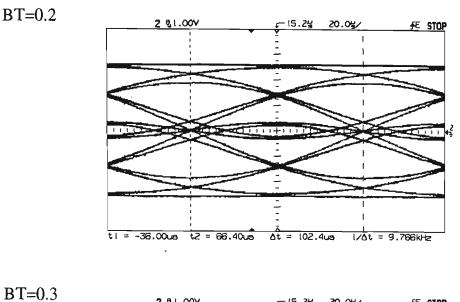
In addition, the same hardware can produce either Phase or Frequency modulation drive signals depending on the selected RF translation technique.

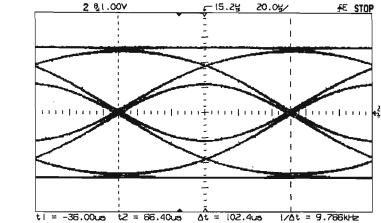
2.6.2 Baseband Characterisation

This section will observe the baseband signals for the generation of GMSK by both orthogonal (phase) and frequency modulation techniques. Figure 2.9 shows the orthogonal eye diagrams over five symbols for GMSK with a deviation of 1/2, bit rate of approximately 10kbits/sec (10M/1024) with various BT products. The I-phase and Q-phase signals are simply the Cosine and Sine respectively of $\phi(t,\alpha)$, which is given by Equation 2.2. The important trend to observe from Figure 2.9 is the reduction of the I and Q phase eyes as the BT product is reduced. This effect is further highlighted by observing the instantaneous frequency over two symbols for GMSK shown in Figure 2.10. This can be explained by the increase of ISI as the BT product is reduced.



generator, varying BT with R=10kb/s.







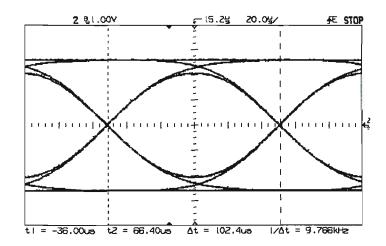


Figure 2.10 GMSK eye patterns of Instantaneous frequency, varying BT with R=10kb/s.

2.6.3 RF generation

A modified Philips PRM-80 transceiver was used to generate the RF signal, driven by the circuit described in section 2.6.1. The GMSK baseband signal is fed directly to the synthesiser section of the PRM-80, bypassing the voice conditioning circuitry required to minimise the spurious interference into adjacent channels. The PRM-80 synthesiser utilises a dual point modulation technique, as shown in the block diagram of Figure 2.11. One signal drives the RF VCO such as the traditional single point technique, this alone has the problem of DC signal removal from the modulation due to the inherent nature of the PLL. However, this is overcome in the PRM-80 by low pass filtering the modulation then using this signal to adjust the reference oscillator.

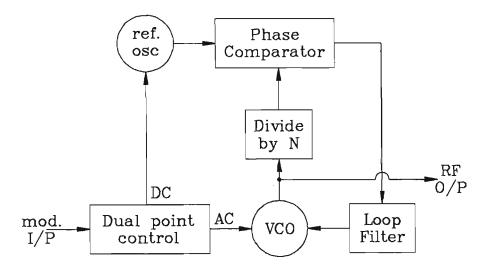


Figure 2.11 Synthesiser Block Diagram for a Philips PRM-80

Figure 2.12 shows GMSK spectra (at RF) produced by feeding the g(t) filtered data signal into the FM generator section of the PRM-80 transceiver (with a 2nd order reconstruction filter). The spectrum floor is caused by the internal noise floor of the RF carrier source as it exists when the modulating signal is removed.

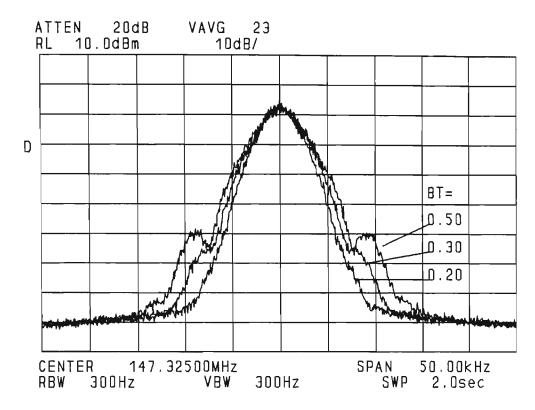


Figure 2.12 Practical FM generated GMSK spectrum (R=10kb/s, Deviation=±2.5kHz) using a Philips PRM-80 transceiver.

2.7 Conclusion

Phase trees and cylinders agreed with those published in [10]. The ROM table data for the generator agreed well with an equivalent generator scheme built by Philips UK [15]. The experimental eye diagrams for the orthogonal and frequency generation techniques (Figures 2.9 and 2.10) agreed well with those published by Murota [9].

The theoretical truncated spectrums agreed with those published by Murota [9] and a recent published DECT specification [16]. The generated RF spectrum of Figure 2.12 is slightly improved in terms of ACI when compared to theoretical, this may be due to: i) the cut off frequency of the reconstruction filter; ii) the roll off of the FM circuitry. Since, the spectrum can be forced to ≤ 60 dB, depending on the BT product, the hardware is satisfactory for Adjacent Channel Interference measurements and evaluation of the various demodulator schemes.

3.0 Channel Simulation

To evaluate various receiver schemes at the same comparative level, the signal degradation caused by the mobile channel under consideration must be emulated.

When simulating receivers the channel effects can be introduced either with:

- i) Data recordings of an actual received mobile signal. The problem with this approach is that many runs would have to be made relating to vehicle speed, modulation type, deviation, bit rate, BT product (for GMSK) and various terrains. Also, permission from the DOTAC would be required. The general problems associated with obtaining and setting up equipment would make this approach less attractive.
- ii) Simulation of the mathematical channel model. A much cheaper and more convenient solution.

This chapter will examine the main characteristics of the radio mobile channel. Section 3.1 presents fundamental concepts leading to the development of the basic building block of a mobile channel, the Clarke model [17,18,19]. The software simulation of the Clarke model which considers noise source generation and selection of a computational efficient method for filtering is presented in section 3.2. Section 3.3 presents the implementation of a Two-Ray and GSM¹ models in both the "C" language and a commercial product SPW², for processing load comparisons. A narrow-band implementation of the GSM model is suggested to reduce simulation times. This narrow-band GSM model was used for the remainder of this work.

3.1 Background

The mobile radio channel is the path between the fixed base station and the moving/stationary mobile, which generally in urban environments is not line of sight. The received signal at the mobile constitutes many versions of the original signal arriving at the omnidirectional antenna, with random carrier phase, arrival angle and amplitude. These components are caused by scattering and reflections of the local terrain (eg. buildings).

Multipath scattering causes an interference pattern of the signal strengths in a horizontal plane, which can consist of minima spaced at half the wavelength of the carrier

¹ GSM (Group Special Mobile), is a European group set-up to standardise the cellular mobile system.

² Signal Processing Workstation, by Comdisco Systems, INC.

frequency. A vehicle moving through this interference pattern has a received signal with rapid amplitude and phase variations. This is referred to as fading.

Each of these received components can also have a frequency shift (i.e. doppler shift) dependant on antenna type, carrier frequency and the received vector relative to the vehicle speed vector.

The concepts just described are known as short-term variations, which assumes the signal mean is constant over a given time period. After moving several hundred carrier wavelengths, the signal mean changes due to propagation losses. This is classed as long-term variations which is a result of shadowing.

Another property of the mobile channel is that of time dispersion, which if greater than the bit interval of the data, will introduce ISI.

3.1.1 Multipath Theory

The following treatment is brief with a full explanation available in [19,20]. First Ray A (see Figure 3.1), entered a local scattering area causing rays 1..N to be generated. Ray A does not directly intercept the mobile aerial.

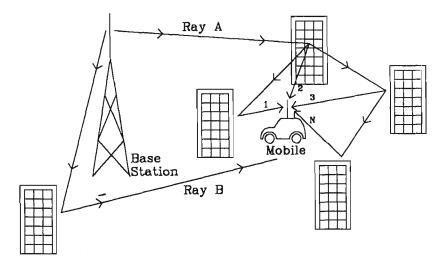
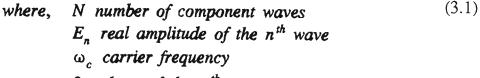


Figure 3.1 Multipath Example

The E field can be written for an omnidirectional antenna as:

$$E_o = \sum_{n=1}^{N} E_n \cdot \cos(\omega_c t + \theta_n)$$



 θ_n phase of the nth wave

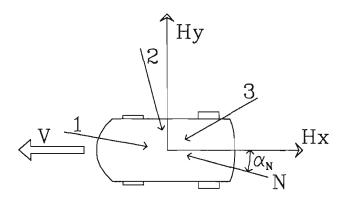


Figure 3.2 Top View of a mobile

By de-composing the respective En signals to magnetic I and Q components the following formulae are obtained:

$$H_{X}(t) = -\sum_{n=1}^{N} \frac{E_{n}}{\eta} \cos(\omega_{c} t + \theta_{n}) \cos(\alpha_{n})$$
(3.2)

$$H_{Y}(t) = \sum_{n=1}^{N} \frac{E_{n}}{\eta} \cos(\omega_{c} t + \theta_{n}) \sin(\alpha_{n})$$
(3.3)

where η free-space wave impedance α_n arrival angle of the nth wave

Since a single component can arrive from any angle with equal likelihood, α_n is uniformly distributed between 0 and 2π . The strength of each E_n is also uniformly distributed. H_x and H_y are, therefore, sums of uniformly distributed variables, and thus it be said from the Central Limit Theory that H_x and H_y are Gaussian distributed.

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Now,

$$H(t) = H_{\chi}(t) + jH_{\gamma}(t) \quad and \quad E_{o}(t) \propto \eta H(t) \quad (3.4)$$

The distributions for H_x and H_y are independent Gaussian sources with $\mu=0$ and $\sigma_x=\sigma_y=\sigma$, the joint probability becomes:

$$P_{X,Y}[X(t),Y(t)] = \frac{1}{2\pi\sigma^2} e^{-\frac{1}{2}\left(\frac{r}{\sigma}\right)^2}$$
(3.5)

where,
$$r(t) = \sqrt{x(t)^2 + y(t)^2}$$
 $r(t) \ge 0$ (3.6)

$$\phi(t) = \tan^{-1}\left(\frac{Y(y)}{X(t)}\right) \qquad 0 \le \phi \le 2\pi \tag{3.7}$$

$$X(t) = r(t)\cos(\phi(t)) \qquad Y(t) = r(t)\sin(\phi(t))$$
(3.8)

The amplitude and phase distributions of the received signal strength can be obtained by using the Jacobian transformation:

$$P_{r,\phi}(r,\phi) = P_{X,Y}[X,Y] | J |$$
(3.9)

where,
$$|J| = \begin{vmatrix} \frac{\partial X}{\partial r} & \frac{\partial X}{\partial \phi} \\ \frac{\partial Y}{\partial r} & \frac{\partial Y}{\partial \phi} \end{vmatrix} = \begin{vmatrix} \cos(\phi) & -r\sin(\phi) \\ \sin(\phi) & r\cos(\phi) \end{vmatrix}$$
 (3.10)

hence,
$$P_{r,\phi}(r,\phi) = \frac{r}{2\pi\sigma^2} e^{-\frac{r^2}{2\sigma^2}}$$
 (3.11)

Amplitude dist.
$$P_{r}(r) = \int_{0}^{2\pi} P_{r,\phi}(r,\phi) dt = \frac{r}{\sigma^{2}} e^{-\left(\frac{r}{2\sigma^{2}}\right)} \quad r \ge 0 \quad (3.12)$$

Phase dist.
$$P_{\phi}(\phi) = \int_{0}^{x} P_{r,\phi}(r,\phi) dr = \frac{1}{2\pi}$$
(3.13)

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Equation 3.12, is known as a Rayleigh distribution which has been shown to best fit actual measurements performed in built up areas. In open areas it is highly probably that direct line of sight between the transmitter and receiver occurs. This type of received signal has a Rician distribution.

3.1.2 Doppler Effects

Referring to Figure 3.2, each component arriving at the antenna has a doppler shift dependent on the intercepting angle α_n .

$$F_n = -\frac{V.\cos(\alpha_n)}{\lambda_c} \tag{3.14}$$

From this equation, the received components which undergo maximum doppler shift have α_n equal to 0 or 180 degrees, which corresponds to driving from and into the plane wave respectively. Hence, an unmodulated carrier can deviate in center frequency by a maximum of $\pm V/\lambda_c$.

The Energy spectral density $\propto dE/df$, and for uniform scatters $\propto \delta\theta/df$ [21]:

We can say,
$$S(f) \propto \frac{\delta\left(\cos^{-1}\left(\frac{f}{f_m}\right)\right)}{df} = \frac{-1}{\sqrt{1 - \left(\frac{f}{f_m}\right)^2}}$$
 (3.15)

This single ray fader can be physically realised as shown in Figure 3.3.

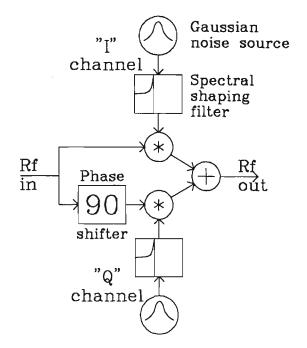


Figure 3.3 Clark model

3.1.3 Time dispersion

Ray B in Figure 3.1 shows an attenuated and delayed ray which will create its own local scattering, along with the main scattering of Ray A. For narrow band transmissions (i.e. low bit rates<50kbits/sec) the dispersion can be modelled by using another Rayleigh fader which has a delay (approximately 5μ S [22], see Figure 3.4a). This type of fading is generally referred to as flat Rayleigh fading, as all the received spectral components fade together. This can either be fast or slow depending on the vehicle speed.

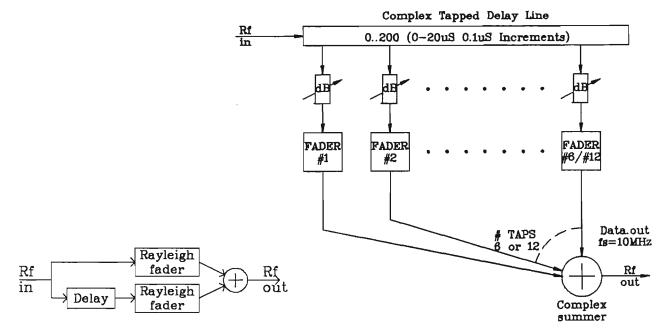


Figure 3.4 a) Simple 2 Ray model

b) GSM model

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For high bit rate signals the time dispersion over smaller intervals must be considered. This can occur over many bits causing severe ISI. The frequency components no longer fade coherently. Hence the term frequency selective fading. CEPT's (Conference of European Postal & Telecommunications Administrations) GSM group have recommended a channel for this system which consists of either 6 or 12 Rayleigh faders. The gain, delay and spectral parameters for each Rayleigh fader were estimated from actual measurements in various terrains.

3.2 Simulation of the Clarke model

This section will present the implementation and verification of software simulation of the Clarke model shown in Figure 3.3. The signals will be described using complex baseband representation to reduce simulation time. A Gaussian source regenerator capable of 24 independent sources will be presented and verified. The implementation of the spectral shaping filter³ shown in Figure 3.3 was performed utilising the overlap-save technique to reduce computations, with verification also presented.

3.2.1 Gaussian Sources

The general approach for generating Gaussian distributed sources, is to first generate a uniformly distributed source and then apply some form of non-linearity. The uniform source could be generated with a linear shift register, multiplicative generator or standard random number generators available in programming languages. Since there is a need for up to twenty four (24) such sources⁴, which must be independent, the random generator in "C" was rejected (since the generator was unknown, independency could not be guaranteed). A multiplicative generator of the form X_{i+1} =16807 X_i mod(2³¹-1) was selected with appropriate seeds, providing independency of 131,072 [23].

The generator was tested for uniformity using CHI-SQ test [23] at a significance level α =0.1% with 530 degrees of freedom, giving a critical value of 634.8. The average test result across the 24 sequences was 515.03 (no test was over 634.8) implying these sequences are adequately uniformly distributed.

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³ 'Classical' as shown in section 3.1.2, however these could be Gaussian, such as in the GSM model.

⁴ If the 12 tap GSM model is implemented.

The Gaussian sources could be generated by passing the uniform variables through the Cumulative probability distribution function of the Gaussian distribution and removing the mean. An alternative which is used here, is the Box-Miller algorithm which can generate two Gaussian variables $(n_1 \& n_2 \text{ output Gaussian}, u_1 \& u_2 \text{ input uniform between 0.0 and 1.0, see below}).$

$$n_1 = \cos(2\pi u_1) \cdot \sqrt{-2\log(u_2)}$$

$$n_2 = \sin(2\pi u_1) \cdot \sqrt{-2\log(u_2)}$$
(3.16)

The Box-Miller algorithm and the first two uniform random sequences were used to construct a test Rayleigh fader without the spectral shaping. The CDF was estimated for two run lengths, and plotted on Rayleigh paper⁵ for comparison, see Figure 3.5.

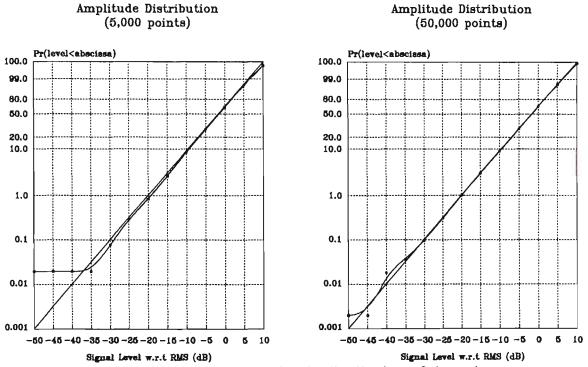


Figure 3.5 Rayleigh Plots showing amplitude distribution of the noise sources

As expected the longer run produced the best fit to the Rayleigh distribution.

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⁵ Rayleigh paper has the Y axis scaled so the theoretical Rayleigh distribution appears as a straight line.

3.2.2 Shaping filters

These filters are used in discrete time (i.e. simulation) hence, we can use existing theory for digital filter design. To cater for both the classical Clarke and GSM mobile channel models requires four types of shaping filters, classical spectrum (section 3.1.2), rician⁶ along with two baseband spectra based on Gaussian spectrums (GAUS1/GAUS2 in the GSM model, see section 3.3). The general approach in hardware implementation of the classical spectrum is to use a second order stage with a high Q to give the peak, followed by a single pole filter to achieve a rolloff of 18dB/oct for frequencies greater than f_{max} [24,25]. Making this Q too high, results in ringing of the filter at f_{max} , which in turn affects the Gaussian distributed input source, which forces the output of the simulator to no longer exhibit a Rayleigh distributed output.

IIR designs are based on analogue filters which are transformed from the S-domain to the Z-domain using transforms such as the Standard, Impulse Invariant and Bilinear. Existing analogue prototypes can not characterise arbitrary spectrum shapes. FIR design, by frequency sampling, will allow arbitrary frequency characteristics. Some frequency error occurs due to impulse truncation, however filter instability is eliminated if high Q filters are implemented.

The computational overhead in using an FIR for the shaping filter is greater than IIR counterparts, but the ability to have greater control over the spectral response is a more dominating factor. FIR implementation was chosen for this work.

3.2.2.1 Simulation time comparison (for shaping filters)

Once the impulse response is calculated this must be convolved with the signal to be filtered, generally implemented as a standard FIR filter. The alternative to using this direct convolution technique is to use Fast convolution implementing either Overlap-Save or Overlap-Add [24,25]. With certain combinations of L (truncation length) and N (FFT length), fast convolution has improved computational characteristics, compared with direct convolution. Overlap-Save was used as it offered a slightly easier implementation because the Overlap-Add method requires a further L additions.

The following is a derivation for the number of complex multiples required for direct

⁶ An attenuated classical spectrum with a doppler shifted direct component.

convolution and fast convolution techniques. They are based on the requirement of complex baseband filtering (i.e. spectrum can be non-symmetrical about DC).

let
$$2^{x} = N(16, 32, 64, ..., 1024, ...)$$
 $N > L$ (3.18)

Number of FFTs required for a sequence of [m] samples

$$=\frac{m}{(N-L)} \qquad round \ up \ nearest \ whole \tag{3.19}$$

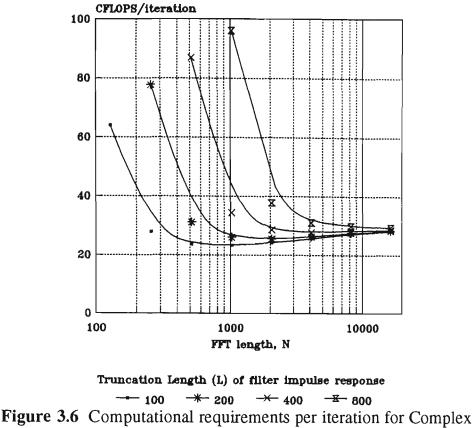
Number of complex *'s for one
$$FFT = N \log_2 N$$
 (3.20)

$$\Rightarrow \# of complex *'s (IFFT & FFT) = (2.N.\log_2 N) \frac{m}{(N-L)}$$
(3.21)

There are additionally
$$\frac{m}{(N-L)}$$
. N *'s for the filter process

Total number of complex multiples is
$$(2.\log_2(N)+1).\frac{mN}{N-L}$$
 (3.22)

Using Equations 3.17 and 3.22, for a given sequence length [m] a decision can be made whether to use direct FIR or FFT implementation for the filtering functions.



filtering using the Overlap-Save technique with FFT length N.

Figure 3.6 shows as N increases much greater than L, the overlapping loss of the FFT filtering is diminished. This graph would tend to suggest an N greater or equal to 4096 if L is less than 800, however N=1024 was selected. The main reason for selecting 1024 was that an FFT(1024) is relatively quick for initial program development and allows reasonably resolution for fs=2kHz. When L=800 and N=1024, 95 complex multiples are required which compares favourably against an equivalent FIR implementation of 800 complex multiples per iteration. In this case, the FFT approach has approximately an 8.4 times improvement over direct FIR implementation.

3.2.2.2 Overlap-Save Technique

Figure 3.7 shows the technique used to obtain the impulse response of the required shaping filter. An FFT length of N=1024 was selected using a sampling frequency of fs=2kHz, which gives an FFT resolution of 1.95hz. At stage A, the frequency response required is multiplied by an equivalent impulse spectrum. By performing the Inverse FFT (stage B) the impulse response of the filter is obtained. Note, that for non-symmetrical frequency responses on either side of DC, a complex impulse response is required.

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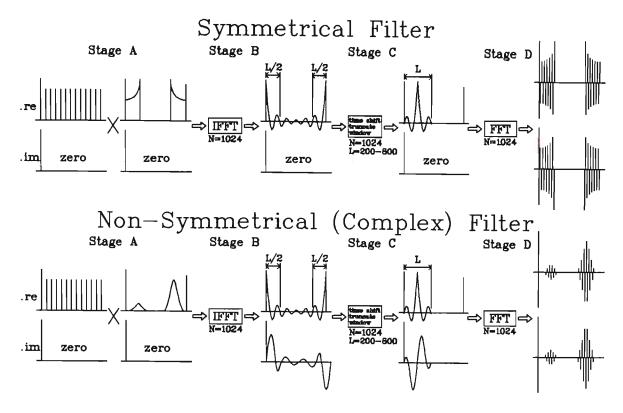


Figure 3.7 Filter template calculations.

When the impulse has reasonably small contributions at the middle of the output from stage B, there is a high possibility that the spectral requirements will be satisfied. Otherwise the FFT resolution must be increased. Stage C truncates the impulse to minimise the effects of circular convolution. The impulse is time delayed making it casual, to simplify the implementation of the Overlap-Save technique. A windowing function is applied to achieve low side lobes, for the various values of F_d (see section 3.1.2) which may be selected (especially for low F_d where truncation performs a severe rectangular window).

The final stage (D) performs a FFT to convert the impulse back to the frequency domain. This array is used in the Overlap-Save technique.

If a sequence is split into segments of FFT length (N), filtering can be performed by FFTing these segments and then multiplying these sequences by the pre-calculated response (from Figure 3.7) then Inverse FFTing, this would NOT produce the required result. The procedure just described would actually perform a cyclic (periodic) convolution instead of the desired linear convolution. This problem can be overcome by using the Overlap-Save⁷ technique which effectively forces the above mentioned process to be linear.

⁷ The Overlap-Add technique would work equally well

Figure 3.8 shows Overlap-Save FFT convolution process. Stage A, has the first Lo samples taken from the previous FFT filtering block and (N-Lo) new input samples are added. The last L samples are held in a temporary store. Stage B, performs the filtering using the initial calculated required spectrum response. The first L samples are discarded and replaced with temporary store ready for the next block conversion. The filtered sequence is available from the L^{th} to $(N-1)^{\text{th}}$ positions. Once all the (N-L) samples are used the next block conversion is commenced.

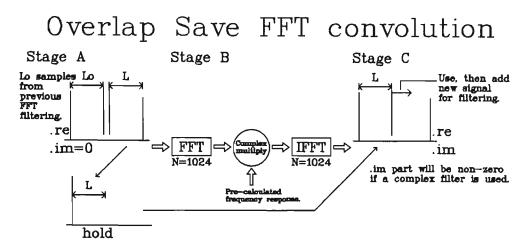


Figure 3.8 Overlap-Save Technique

3.2.2.3 Overlap-Save test

The performance of the Overlap-Save convolution technique was evaluated on a test system which could be frequency swept. Various spectrums were generated relating to window type and L (the impulse length). The side lobe rejection must be maximised to obtain the large attenuation required by the Classical shaping filter, as shown in Figure 3.9 and as expected the Blackman window gives the best side lobe rejection.

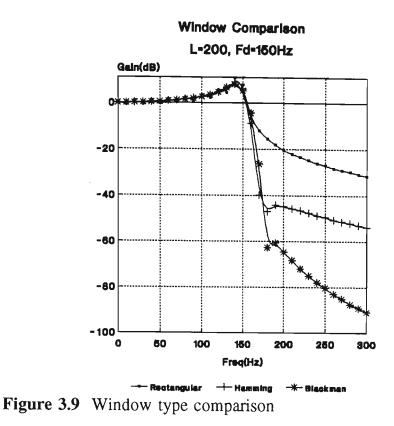
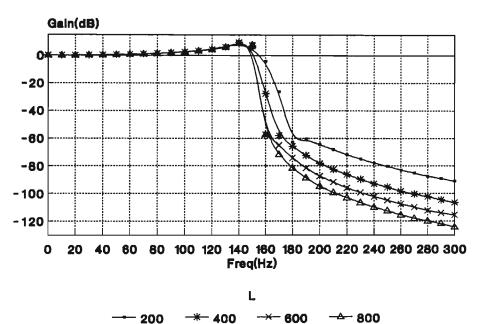


Figure 3.10, shows the variation of the spectrum for different truncation lengths (L). This clearly shows the improvement to the ideal spectrum as L is increased. As expected the Blackman window gave the lowest sidelobes, and was used for the remainder of this work.



FFT convolution (Blackman)

Figure 3.10 Effect of various truncation lengths (L), using a Blackman window.

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The Spectra are adequate for a fading frequency of 150Hz. However, when the fading frequency is reduced, keeping the same FFT resolution and truncation length causes spectral degradation. When comparing a receiver scheme at different maximum doppler frequencies, the Rayleigh amplitude characteristics would vary due to the peak on the classical response changing, which would produce non comparative results. This problem is not as critical in the Gaus1/Gaus2 type filters as their impulse responses for a given fading frequency are much shorter than that of the Classical filter. Hence this filter is the limiting factor.

The performance at fading frequencies of 75 and 150 hertz using the Blackman window with a fixed FFT sampling frequency of 2kHz, was simulated (see Figure 3.11). The Mean Square Error (MSE) is calculated between the ideal and simulated frequency spectrums. Thirty frequency sample points for each fading rate were used:

i) $F_d=75$ frequency sampled 0 to 150 steps 5Hz

ii) $F_d=150$ frequency sampled 0 to 300 steps 10Hz

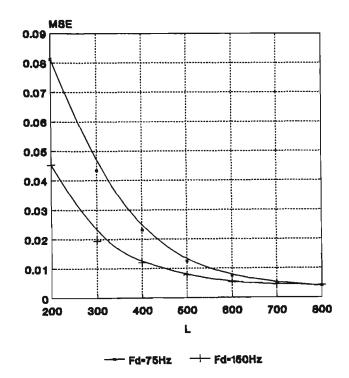


Figure 3.11 Frequency spectrum MSE for various F_d , with fixed f_s and N.

Figure 3.11 shows that to achieve the same MSE when the F_d is changed (f_s and N held constant), requires adjustment to the truncation length (L). This concept will be developed further in the next section.

3.3 Implementation of the GSM model

This section considers the software implementation of a channel simulator recommended by GSM [26], based on the wide sense stationary uncorrelated scattering (WSSUS) model. The GSM mobile system uses GMSK modulation at a high bit rate (270kbits/sec) with Time Division Multiplexing (TDM), which is a wideband signal. To simulate the frequency selective nature of fading which will occur for this system, delays in the order of the Bit period must be considered.

The model consists of a 0.1μ S tapped delay line of length 20μ S, with Rayleigh faders on each tap including a given doppler spectrum. For a given terrain the tap positions (delays), gains and doppler spectrums are defined. Three GSM models exist namely; i) rural area:RAxz, ii) hilly terrain:HTxz, iii) urban area:TUxz, where 'z' represents 6 or 12 taps.

The channel simulation was implemented in two ways:

- i) Full wideband implementation
- ii) Modified system, for narrower band signals to reduce simulation time.

3.3.1 Full wideband system

The code for the simulator was implemented in "C" on both IBM/AT and APOLLO 3500, the block diagram of the system is shown in Figure 3.12.

Description of this model (Figure 3.12) follows:

a) Source:

The pre-generated I/Q representation of the modulation is obtained from a file, initially designed for 16kBits/S with 5 times oversampling. Hence the signal must be bandlimited to 40kHz.

Interpolation, after the generation of the modulation data source and the I/Q fading sources, is required to bring the system to a common sampling frequency of 10MHz. This process is performed by a Low Pass Filter (LPF) which is designed at the new sampling frequency. The LPF has a maximal flat pass band equivalent to the bandwidth of the signal and has an attenuation of 60dB at the Nyquist frequency of the old sampling rate.

The input requires an interpolation of \uparrow 125, this filter was designed as a maximal flat Butterworth LPF, with and approximate linear phase response in the band of interest.

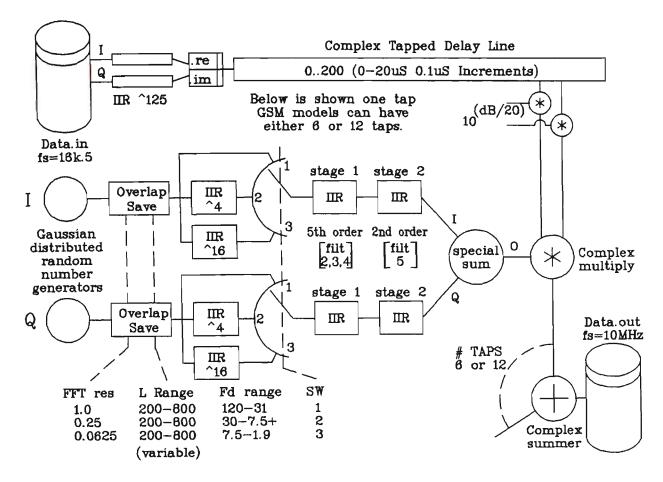


Figure 3.12 Block diagram of GSM channel model

b) Delay Line:

This has 200 tap positions with 0.1μ S steps. Since this will be operating for every iteration the shifting must be performed rapidly. A single direction linked list structure was adopted, where the next sample was added to the start of the list and the last element is dropped off.

c) Doppler Spectrum:

This was generated at a sample frequency of 2kHz, using the technique discussed in section 3.2. Referring to Figure 3.11, it is apparent that reducing the doppler frequency greatly increases the MSE when the FFT sampling frequency is fixed, especially at low truncation lengths. This is due to the increased impulse response length when F_d is reduced.

Figure 3.11 shows where if the FFT sampling rate is halved (i.e. 1kHz), the MSE curve for $F_d=75$ (fs=2kHz) would follow the curve for $F_d=150$ Hz with a FFT sampling rate of 2kHz. The only additional requirement is to interpolate by 2, so that the $F_d=75$ Hz signal

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has the same output sampling frequency as the $F_d=150$ Hz signal. We require F_d to be variable from 0 to 150Hz and to exhibit, as close as possible, the spectral characteristics and at the same time minimise simulation time. From this description the FFT sampling frequency can be varied with the output followed by an interpolation stage. This would require very stringent specifications at low values of F_d (i.e. $F_d=2$ Hz \Rightarrow FFT_{otd}=5.2Hz FFT_{new}=2kHz).

An alternative to this, is to use three FFT course sampling rates (2kHz,500Hz & 125Hz) then linearly adjust *L* for the required MSE. An MSE equal to 0.025 was selected for F_d =150Hz. Linearly increasing *L*, as F_d is decreased, improves the MSE. F_d is reduced until *L*=800 where the computational efficiency of the Overlap-Save is reduced (still 8 times quicker than the equivalent FIR implementation). Then the FFT sampling rate is reduced and an appropriate interpolation filter inserted (performed by the switch before Stage 1 in Figure 3.12). The final implementation allows doppler frequencies in the range of 1.9 to 120 Hz.

d) Interpolation:

An interpolation of \uparrow 5000 was required after the switching stage of the I/Q fading generators. A single filter used to perform this task would be impractical due to the quantisation errors of the poles close to DC point on the Z-domain unit circle. This problem was overcome by using a two stage interpolation scheme with \uparrow 125 for stage 1 and \uparrow 40 for stage 2, resulting in 5th and 2nd order IIR filters respectively.

e) Complex Addition:

Since the I/Q channels for the fading can each be represented as a complex signal (due to the GAUS1/GAUS2 filters), a special addition using the equation below was used:

O=I+jQ

where I and Q can be complex quantities

(3.23)

f) Gain;

These parameters are expressed as average relative power at each tap. Since there are three types of fading spectra, their 0dB points must all be the same at any given F_d . The accuracy of the 0dB point is dependent on the FFT sampling rate and the *L* used, which are both functions of F_d . The impulse response of the GAUS type filters can be easily found, and if compared to the length of the approximation of the CLASS filter they are much shorter.

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Hence the 0dB points of the GAUS filters are accurate. Simulations have shown that the truncation of the impulse response for the CLASS filter only effects the peak at F_d and that the 0dB point at DC is acceptable.

g) Sink;

The output sample rate is 10Mhz. This could generate an output file of 80M bytes (I&Q float, non-ASCII) for one second of simulation. If the modulation being tested is sufficiently bandlimited, decimation can be used to reduce file size.

3.3.2 Narrow-Band Modification to the GSM channel

The wideband channel model presented in section 3.3.1 required excessive simulation processing when used for the narrow-band application under consideration (due to the 10MHz interpolation). This section will show a GSM channel can be modified for narrow 25kHz channels. A thoroughly developed model which considers a variety of terrains and incorporating sub-bit signal delays, can then be used for BER performance simulations.

If the sampling frequency used by the modulation source (i.e. 80kHz) is selected as the new sampling frequency for the GSM model, 25kHz signal bandwidth can spread to 40kHz before aliasing becomes a problem. The tapped delay line is simulated by designing an interpolation (\uparrow 125) FIR poly-phase filter. To emulate a 1.3µS delay the 13th poly-phase branch would be used. Each poly-phase branch is implemented with a 10 tap FIR (1248 tap FIR/125 poly-phase branches) which can be calculated very rapidly. Delays greater than 12.5µS are performed by delaying the 80kHz sampled signal by a unit delay and making up the difference with a poly-phase branch. Example, 15.2µS \Rightarrow unit delay and (15.2-12.5=2.7) 27th poly-phase branch.

The sampling rate for the I/Q fading signals had to be converted from 2kHz to 80kHz. This was performed with a 240 tap poly-phase filter (\uparrow 40). This section now runs much faster than the stage 1 and stage 2 (\uparrow 5000) previously implemented. Hence simulation for narrow band signals can be performed much quicker. This narrowband system is shown in Figure 3.13.

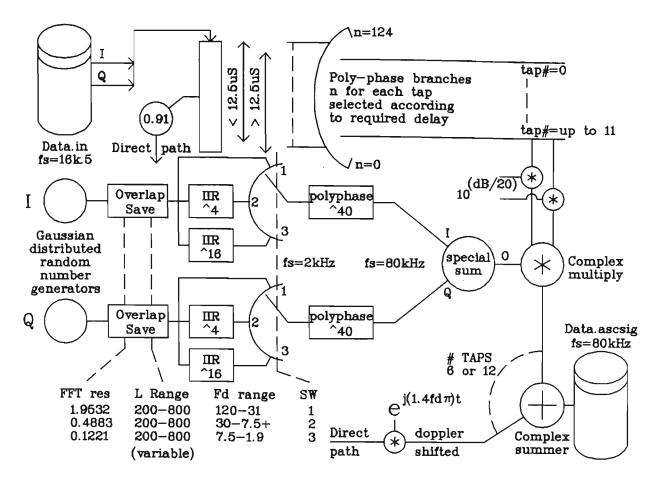


Figure 3.13 Block diagram of Narrowband GSM channel model, used for the remainder of this work.

3.3.3 Simulation run times

Table 3.1 shows simulation times for wideband and narrowband implementations of the GSM channel model on IBM/AT (with ITT 287) using Turbo C and APOLLO 3500 (with Wyntek floating point accelerator card) using "C" and SPW. The simulation times are for 1 second of real time data.

 Table 3.1
 Simulation time comparison

GSM MODEL (HTx12)	IBM/AT	Apollo	
	Turbo C	С	SPW
Wideband	20.4 hrs	14.2 hrs	N/A
Narrowband	N/A	20.8 mins	25.5 hrs

3.3.4 GSM results

The results here are related to the spectral properties of the shaping filters. The Gaussian sources were verified in section 3.2.1. Verifying the Gaussian sources after filtering would require very long simulations which produce impractical file sizes. All the following spectra (Figure 3.14) are for an unmodulated carrier, utilising the narrowband GSM implementation.

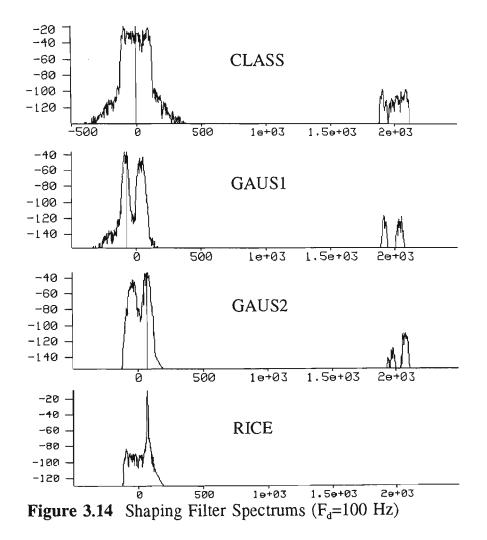


Figure 3.14 shows the four Spectrums required for implementation of the GSM model. The Rician shaping spectrum clearly shows the doppler shifted direct component. The images at 2kHz are due to the residue of the interpolation. These are less than -60dB and are acceptable.

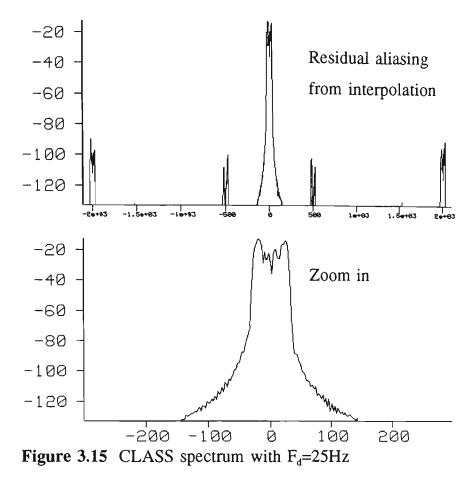
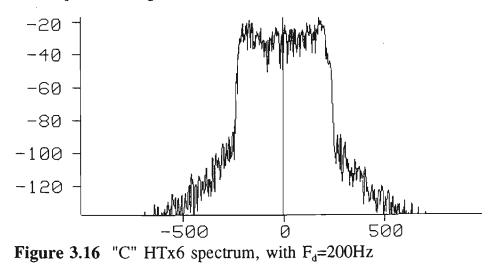


Figure 3.15 shows the Classical spectrum for $F_d=25$ Hz. This changes the FFT sampling frequency to 500Hz and inserts an IIR $\uparrow 4$ interpolation filter. The spectrum has images at ±500Hz are due to imperfect interpolation of the $\uparrow 4$ stage. The significant signal at 2kHz is due to the $\uparrow 40$ interpolation stage.



The final overall spectrum for the GSM hilly terrain 6 tap model (HTx6) implemented in "C" is shown in Figure 3.16. The Classical spectrum shaping is clearly dominant as the model suggests.

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3.4 Conclusion

The Channel model implemented in "C" on the Apollo will be used to evaluate the best demodulation system in Chapter 5. This implementation proved to have the minimum simulation time for one second of real time data (c.f. section 3.3.3). The final C program can also be easily configurated to simulate any combination of delays, gain and shaping spectra for up to 12 taps (eg. the simple two ray was implemented in this way).

This work found that a single version of the fader is not appropriate if the simulation time is to be minimised. In order to minimise the processing for simulation of the fading process, the Classical filter should be designed at a low sample rate (in the order of twice fading rate) then interpolated to the system sampling rate.

The amplitude distributions satisfied Rayleigh criteria and all spectrums were as required by GSM specifications.

If the description of the system is exactly known, using a language such as "C" will always result in faster simulation times. If ideas are to be tested then the SPW Block Diagram approach will result in quick implementation at the price of simulation time. But it must be stressed that full knowledge of the pre-defined blocks must be known for successful results.

4.0 GMSK Detection

This chapter will review existing detection schemes for GMSK demodulation and where possible give performance comparisons. Demodulation of GMSK signals has been an active area of mobile radio research since GMSK was first proposed by Murota and Hirade [9] in 1981. The numerous published detection schemes which can be classified into two groups; i) Coherent and ii) Non-Coherent, these will be covered in section 4.1 and 4.2 respectively. These two groups can be further sub-divided as shown in Figure 4.1. Section 4.3 will present tables comparing published material for GMSK detection in both AWGN and fading channels.

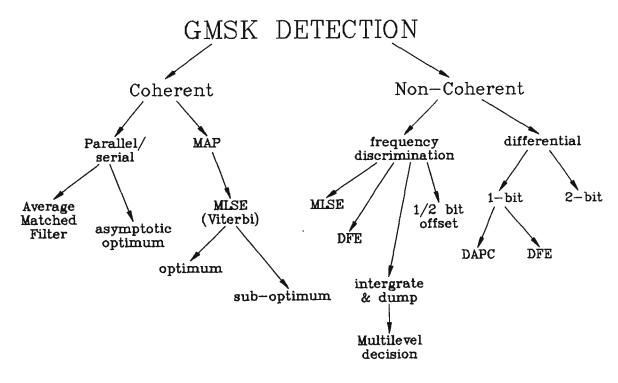


Figure 4.1 GMSK detection schemes

The choice between coherent and non-coherent detection schemes is dependant on the distortion caused by the channel. A coherent receiver will have a 3dB improvement in Eb/No over a simple distortion-less channel with AWGN, when compared with a Non-coherent receiver. However, as shown in Chapter 3 the main source of channel impairment in a mobile radio channel is fading. A phase locking scheme would loose lock, requiring an acquisition time before re-locking. During this time the received bit stream would have a burst of errors.

Fading also causes havoc to the phase of the received signal. There are both phase clicks during very deep fades and slow phase variations, termed static, which are much less

than the rate of the phase modulation.

The main purpose of this research is to adapt existing analog mobile equipment for digital modulations. Since the present radios use discriminator detectors, this will be the main area concentrated upon. These non-coherent based detection schemes have the advantage of no carrier phase recovery which would decrease burst error lengths.

A review of coherent detectors will also be provided (section 4.1) to serve as a guide for future systems which will consist of all digital systems. The true advantages of digital systems can only be exploited when all modulations are digital. Only then can high levels of co-channel interference be acceptable. Hence more dense use of available radio spectrum.

4.1 Coherent Receiver

Figure 4.2 shows the general block diagram for a coherent receiver. The received signal would be first translated to an IF frequency to enable good selectivity by the BPF. The recovered carrier would then be used to translate the IF signal to baseband, with I-phase and Q-phase components. The LPF are simply used to remove the $2\omega_{IF}$ components from the down conversion multipliers. The I and Q signals are then used for timing recovery which clock the required decision algorithm. The required decision algorithm may be either an MLSE or a Parallel/Serial scheme with either Average Matched Filters (AMF) or Asymptotically Optimum Filters (AOF). These will be discussed in the following sections [10].

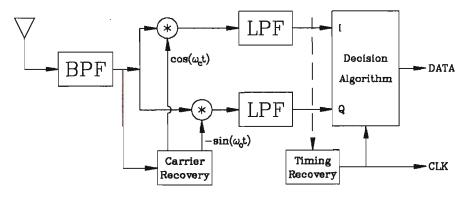


Figure 4.2 General block diagram for a coherent receiver

4.1.1 Optimum Receiver

Generally an optimum receiver would imply minimisation of the Bit Error Rate (BER), which can be directly applied to maximising the Signal to Noise Ratio (SNR) in Additive White Gaussian Noise (AWGN) channels. Digital schemes sample the received signal at the end of each bit interval, and during that interval perform functions on the received signal so that the SNR is maximised at the decision point.

A starting point for optimum detection used by many standard texts is Maximum A Posteriori (MAP) detection [27,28]. The objective is to find the conditional probability $Pr(\alpha_i | r)$, where r is the received signal and α_i is a possible transmitted bit stream, so that $Pr(\alpha_i | r)$ is maximised for all values of i. The term posteriori is used as $Pr(\alpha_i | r)$ is found after the event (after r is received). A MAP receiver would use the following criteria:

set,
$$\hat{\alpha} = \alpha_j$$
 for
 $Pr(\alpha_j | r) > Pr(\alpha_i | r)$ all $i \neq j$

$$(4.1)$$

Further following [27,28] the MAP criteria becomes:

$$\|v-s_{j}\|^{2} - \ln Pr(\alpha_{j}) < \|v-s_{i}\|^{2} - \ln Pr(\alpha_{i})$$
where, v received signal including noise
 s_{ij} possible signal vectors
 α_{ij} bit stream for S_{ij}

$$(4.2)$$

A receiver detection algorithm based on the detection rule of Equation 4.2 is shown below [27,28]:

$$z_{i} \doteq (r, s_{i}) - C_{i}$$

$$(r, s_{i}) = \int_{-\infty}^{\infty} r(t)s_{i}(t) dt$$

$$c_{i} = \begin{cases} \frac{1}{2}E_{i} & equiprobable \alpha_{i} \end{cases}$$

$$\left(4.3\right)$$

$$\left(\frac{1}{2}[E_{i} - \eta \ln Pr(\alpha_{i})] & otherwise \end{cases}$$

$$where, \quad E_{i} = ||s_{i}||^{2}$$

$$\eta \quad spectral \ noise \ density$$

$$\hat{\alpha} = \alpha_{i} \ with \ j \quad giving \ z_{i} > z_{i} \ for \ all \ i \neq j$$

$$(4.3)$$

The scalar (r,s_i) in Equation 4.3, is simply a correlation between the received signal and one possible transmitted sequence s_i . To perform the optimum receiver, all possible sequences in the transmitted signal set must be correlated at the receiver, with the highest

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correlation indicating the most likely transmitted signal. The block diagram of such a MAP receiver is shown in Figure 4.3. The constants c_i may be neglected if the data source is equiprobable, this also reduces the MAP criteria to that of maximum-likelihood detection.

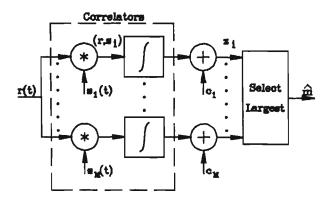


Figure 4.3 MAP receiver implemented with a bank of correlators

In general, practical systems require $s_i(t)$ to be of finite time, hence the correlators in Figure 4.3 can be replaced by matched filters [27]. These matched filters can be translated to baseband and hence be incorporated into the general coherent receiver of Figure 4.2.

4.1.1.1 Maximum Likelihood Sequence Estimation (MLSE)

Symbol by symbol detection is performed by Figure 4.3. The Intersymbol Interference (ISI) introduced by GMSK modulation at the transmitter for narrowing the bandwidth of the modulation is not utilised. Therefore better performance can be achieved by using optimum MLSE.

Referring to (r,s_i) of Equation 4.3 and following [10] for practical systems (where future time has no meaning) the equation can be written as:

$$(r,s_i) = \int_{-\infty}^{(n+1)T} r(t)s_i(t) dt$$
 (4.4)

Rewriting the above equation in a recursive form:

$$(r,s_i)_n = (r,s_i)_{n-1} + Met(s_i)_n$$

$$(n+1)T$$
(4.5)
where, $Met(s_i) = \int_{nT} r(t)\cos(w_o t + \phi(t,\alpha)) dt$

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Chapter 2 showed how GMSK can be generated by a finite state machine. Applying these concepts to the $Met(s_i)$ equation the following is obtained:

$$\boldsymbol{\phi}(t,\boldsymbol{\alpha}) = \boldsymbol{\phi}_{state} + \boldsymbol{\phi}(t,\boldsymbol{\alpha}_{0 \to (L-1)}) \tag{4.6}$$

GMSK, using a truncation length of 4 symbols and a modulation (h) index of 0.5, ϕ_{state} will take on one of 4 states [0,+/-pi/2,pi]. Also, $\phi(t,\alpha_{0-(L-1)})$, where $\alpha_{0-(L-1)}$ is the correlative state vector and $0 < t \le T$. $\phi(t,\alpha_{0-(L-1)})$ can take on one of possibly M^{L-1} [2³=8] states. Hence, the total number of possible sequences over one symbol is 64 (2*pM^{L-1}). For a binary scheme this means there are 32 possible phase states for GMSK4 with h=0.5.

Now consider (r,s_i) over 10 symbols, this would imply $64*2^{10}=64k$ path metrics with the minimum path metric indicating the optimum path. This is not a feasible proposition for practical implementation. However, close examination of the state trellis shown in Figure 4.4 reveals that two paths always merge to one state. Hence an intermediate decision can be made as to the best path (sequence) into each state. This is clearly visible in Figure 4.5, which shows the state diagram in a less cluttered form.

A recursive algorithm known as the Viterbi Algorithm (VA) [29,30] uses this concept of intermediate decisions to find the optimum sequence, and has been applied to the decoding of convolutional forward error correction coding for many years. Forney [30] was one of the earliest researchers to show how the VA could remove ISI from digital sequences. The basic concept is equivalent to GMSK signals, in that ISI (controlled in the case of GMSK) introduces a fixed number of states (memory) into the signal. If the portions of ISI can be estimated (these are known for GMSK) then ISI can be removed, hence a larger eye, which implies better signal detection capabilities.

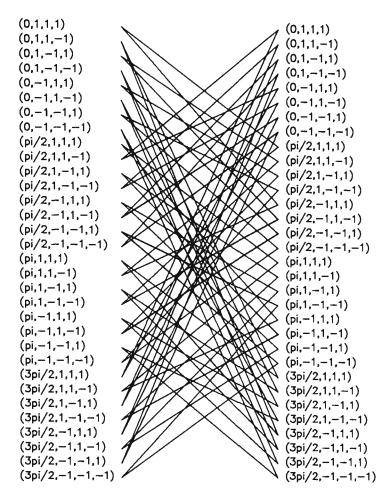


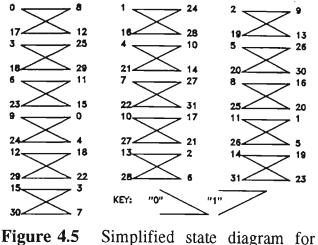
Figure 4.4 Full state trellis for L=4, h=0.5

The full VA implementation would require filters to find the branch metrics of Equation 4.5, 32 memories for state metric holds and 32 memories for bit sequence stores. For DSP implementation the branch metric (and state metric) would be quantised while the bit sequences would be contained in shift registers. The process (Add, Compare and Move) is repeated 32 times. As an example, consider the two states leading to state 0 in Figure 4.5. The new state metric for state 0 equals the larger of: i) state metric 9 plus the associated branch metric from state 9 to 0, ii) state metric 24 plus the associated branch metric from state 24 to 0. The shift register of the most likely last state is also copied across with a "1" (in this case) shifted to the most recent bit received position.

The theoretical VA requires that the shift registers be very long so that if the optimum path splits into two paths they will eventually merge to eliminate one. However in practical implementations, the shift register is of finite length with little loss in performance. The bit decision point is delayed to consider ISI in the forward direction of the decision point. So the received bit is taken from the end of the shift register with the largest state metric of the available 32 states, at the end of each symbol.

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L=4, h=0.5

ipinieu state utagrani

4.1.2 Parallel MSK for GMSK

Observing the MSK phase trellis in Figure 2.3, one can deduce that detection of a coherently received MSK signal can be achieved by sampling in the Q-phase during odd samples and the I-phase during even ones. If the LPF is replaced by a filter with an impulse response given by Equation 4.7 then the MSK receiver will be an optimum one [28].

$$a(t) = \begin{cases} \sin\left(\frac{\pi \cdot t}{2 \cdot T}\right) & 0 \le t \le 2\pi \\ 0 & otherwise \end{cases}$$
(4.7)

The parallel MSK receiver can be used for the detection of partial response CPM with minimal performance degradation for h=1/2. However the filter (Equation 4.7) must be optimised for a particular modulation. Svensson and Sundberg [10] presented algorithms to find the optimum filter for an arbitrary SNR. They also examined both the AWGN and Rayleigh fading environments.

Murota [9] also suggested the use of a parallel MSK type receiver for GMSK. However he did not attempt to optimise the detection filters. Murota achieved carrier recovery by using De Buda's technique for frequency shift keying with low deviation ratio [31].

4.1.3 Serial MSK receiver

The serial MSK receiver is less complex than Parallel MSK because the I and Q arms need not be alternatively sampled. Sundberg [10] found that serial detection is less sensitive to carrier recovery error, however more sensitive to timing jitter. The eye width in a parallel

detector is 2T while only T for the serial detector.

Although the serial receiver is less complex in terms of symbol timing, there is additional complexity required for the carrier recovery. Figure 4.6 shows a serial MSK-type receiver. Note that f_c -1/4T carrier is required.

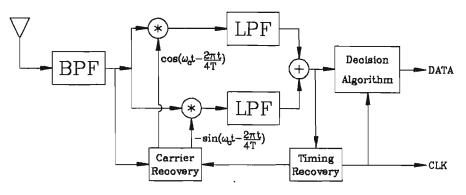


Figure 4.6 Serial MSK receiver

4.2 Non-Coherent Receivers

Another main form of detection is non-coherent detection which means that the exact carrier phase is not required for detection, only the timing clock needs regeneration. This has several advantages in flat fading as previously discussed in this chapter. Under the title of non-coherent (refer Figure 4.1) are two main groups, i) differential and ii) frequency discrimination detectors. Both types of detectors effectively differentiate the phase of the received signal. Hence phase state information is lost leaving a signal which is effectively generated by the g(t) pulse instead of the q(t) pulse (see Section 2.3). These two frequency detectors have numerous variations and additions to improve their overall performance which will be discussed in the following section.

4.2.1 Differential detection

The basic structure of a one-bit differential receiver is shown in Figure 4.7. A Band Pass Filter (BPF) selects a channel from a band at an Intermediate Frequency (IF), which is generally referred to as a pre-detection filter. This signal is then multiplied by a delayed (symbol) 90 degree phase shifted version of itself given by Equation 4.8.

$$\mathbf{y}(t) = \mathbf{R}(t)\cos[\omega_{a}t + \phi(t) + \eta(t)] * (-\mathbf{R}(t-T)\sin[\omega_{a}(t-T) + \phi(t-T) + \eta(t-T)])$$

$$(4.8)$$

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(1 0)

Expanding Equation 4.8 and assuming $\omega_{o}T=2\pi k$ (k=integer) with low pass filtering the following equation is obtained:

$$y(t) = \frac{R(t)R(t-T)}{2}\sin(\Delta\phi(T))$$
(4.9)
where, $\Delta\phi(T) = \phi(t) - \phi(t-T) + \eta(t) - \eta(t-T)$

Since R(T)R(t-T) is always positive the decision rule becomes:

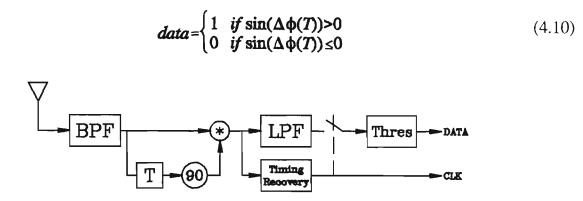


Figure 4.7 One-bit differential receiver

A further extension of this detection, is two bit-differential detection. Simon [32] showed two-bit differential detection to have a much wider eye and hence better detection properties. A non zero threshold point is required since a non-symmetrical eye is observed. An important addition is that the input data stream must be differentially encoded, as shown in Figure 4.8.

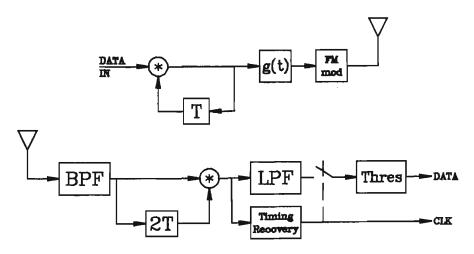


Figure 4.8 Two-bit differential receiver

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Makrakis *et al.* [33] have written many papers utilising decision feedback equaliser (DFE) to minimise the effect of ISI for both one and two bit differential detectors. They introduced the concept of Data-Aided Phase Control (DAPC) which is simply a baseband DFE implemented at IF. Instead of feeding back the g(t) ISI component of the last decision, the q(t) ISI component is used to phase rotate the delayed IF signal hence removing the effect of the last symbol.

4.2.2 Frequency Discriminator Detection

The basic structure of the frequency discriminator receiver is shown in Figure 4.9. The pre-detection and post-detection circuitry serve the same purpose as in differential detection. The only difference being a limiter discriminator which replaces the delay element and 90° phase shifter. The limiter discriminator produces an output voltage proportional to the input frequency. A frequency discriminator can be implemented in a number of ways [3,27]:

- a) Slope Detection This uses the edge of a filter, followed by an AM detector. Note this would require an input limiter to the filter, so that any received envelope variation is not perceived as signal information.
- b) Balanced discriminator An example would be the Foster-Seely radio detector. This uses two complemented tuned filters to convert an FM signal to an AM signal, followed by an envelope detector.
- c) Zero-crossing detector This finds the time between positive (or negative) going thresholds. Hence the instantaneous frequency of the signal.
- d) Phase-shift discriminators This type works on the principle of multiplying the received signal by a slight delayed version of itself. It effectively differentiates the phase to give the instantaneous frequency.

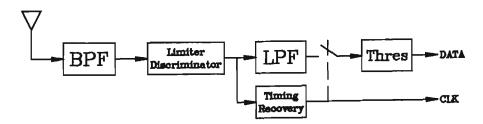


Figure 4.9 Frequency discriminator receiver

Technique b was generally used in the early stages of FM transmission. However with the advent of integrated circuits, single conversion (10.7Mhz to 455kHz) and detection of the baseband signal (using technique d) can be performed with a single 16 pin DIP IC. Also, technique d will obtain better linearity than technique b. Zero-crossing detectors (c) would achieve ultimate linearity with high speed digital devices. This is presently not cost effective when compared to the simplicity of technique d. Since a phase-shift discriminator is used in the VHF radios to be modified, analysis of this type of discriminator will be performed.

A lumped 90 degree phase shift is applied to the signal at IF, then multiplied by the original signal. This produces SIN sum and difference terms, where the sum is removed by low pass filtering. With no modulation the difference term would simply be zero (sin(0)). A sloped linear phase is required at IF, along with the lumped 90 degree phase shift, so that a \pm deviation from IF will produce \pm phase deviation from the 90 degrees at IF. As long as this phase deviation is small the approximation $\sin(\theta) \approx \theta$ can be made which gives the demodulated signal. This is shown mathematically in the following:

FM has,
$$\dot{\phi}(t) = 2\pi f_A x(t)$$
 (4.11)

$$\phi(t) - \phi(t - t_1) \approx \dot{\phi}(t) t_1 = 2\pi f_A t_1 x(t)$$
(4.12)

The output from the multiplication of the received signal and the modified version can be written as:

$$\cos(\omega_{o}t + \phi(t)) * [-\sin(\omega_{o}t + \phi(t - t_{1}))]$$
(4.13)

After low pass filtering and approximating for t_1 small:

$$-(\sin(\phi(t)-\phi(t-t_1)))\approx -(\phi(t)-\phi(t-t_1))$$

$$(4.14)$$

Substituting Equation 4.12 into Equation 4.14 the following is obtained:

$$y_{d}(t) \approx -2\pi f_{A} t_{1} x(t) \tag{4.15}$$

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As shown in Equation 4.15 the detected signal is only a function of the FM modulating signal x(t).

As in the case of differential detection, additional baseband processing can be performed to improve the bit error rate (BER). Adachi and Ohno [34] showed how the ISI in a GMSK signal can be removed to improve E_b/N_o for a given BER. A further extension (although developed before [34]) is the multilevel decision method published by Hirono *et al.* [35]. This technique removes the ISI introduced from the last two bits, by changing the threshold level dependent on the last two bits. This is equivalent to having a fixed threshold level of zero and using 2-bit DFE.

A technique called 1/2 bit offset detection published by Adachi and Ohno [36] does not have any feedback components. Hence on the surface it would appear to have better characteristics in flat fading because a deep fade results in total distortion of the signal guaranteeing a BER=0.5. This could give rise to error propagation when using decision feedback equalisers.

MLSE can also be applied to the detection of GMSK from the output of a frequency discriminator, with an instant four fold decrease in complexity since phase state information is lost. Chung [37] applied a simplification of the MLSE algorithm for GTFM. Ohno and Adachi [38] applied the same MLSE algorithm to GMSK by a simple modulation dependant coefficient change.

4.3 Comparison of existing schemes

The following tables compare published E_b/N_o values of various detection schemes for GMSK with BT=0.25. Tables for AGWN and flat fading cases are presented for BER=1e-3. However, it must be stressed that throughout all the papers reviewed some discrepancies exist due to the problems of obtaining consistent Pre-Post detection filtering.

A Pre-detection filter of BT=1.0 was chosen where possible. In general, the bit rate (16kBits/sec) was for narrow-band systems. Many papers only considered their proposed scheme in AWGN (see, note⁺ Table 4.1), which does not give a true indication of the scheme in a mobile radio channel. Also, due to the pre/post detection filtering discrepancies, direct comparison is not a fair indication of the best scheme. It only gives a feel for the order of magnitude for E_b/N_o .

SCHEME	E_{b}/N_{o} (dB)	REFERENCE
Differential		
1-bit	22.3	39+
1-bit, DFE	15.8	39+
1-bit, DAPC	16.1,15.2	40,41+
2-bit	15.5,14.6	41+,42
2-bit, DAPC	12.7	39+
Frequency discriminator		
Conventional	23.5	34
Conventional + 1 bit DFE	15.2,12.8,15.2	34,43+,44+
Multi-level		
$2 \text{ level} \equiv \text{Conv} + 1 \text{ bit DFE}$	13.5	35+
$4 \text{ level} \equiv \text{Conv} + 2 \text{ bit DFE}$	12.3	35+
1/2 bit offset	13.1,15.7	36,44+
MLSE	12.5	44
Coherent		
MSK, BL.T=0.0144*	10.1	45
MSK, BL.T=0.0288*	11.8	45
Ideal	8.6	45

Table 4.1 Eb/No performance, GMSK4 BT=0.25 h=0.5, BER=1.0e-3

Note:

⁺ Fading not considered

BL.T = Loop filter bandwidth for the Costas Loop, normalised to the bit rate.

The MSK adapted receiver [45] for GMSK performed well in AWGN, however performance is dependant on the loop filter bandwidth for the Costas loop implementation. As expected, a wide loop filter will allow more noise into the system thereby forcing the regenerated carrier to have a larger jitter variance leading to a degradation of $E_{\rm b}/N_{\rm o}$. However in fading, a wide loop filter is advantageous in decreasing the irreducible BER, by allowing the Costas Loop a larger lock-in range, hence faster carrier acquisition time.

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SCHEME	E_{b}/N_{o} (dB) BER=1e-3	Error floor fd=40Hz	REFERENCE
Differential			
1-bit	SNR=32.0	0.51e-4 (32)	46
1-bit	SNR=31.3	0.55e-3 (32)	47
2-bit	CNR=30.9	0.23e-3	42
2-bit	SNR=28.6	0.12e-3 (32)	48
2-bit	SNR=28.0	0.10e-3 (32)	47
Frequency discriminator			
Conventional	SNR=40.1	0.33e-4 (32)	47
Conventional	SNR=32.0	0.30e-4	49
Conventional	38.1	0.56e-3 ⁺	36
Conventional	SNR=41.1	0.35e-4 (32) ⁺	50
Convent.+DFE	30.7+	N/A	51
1/2 bit offset	29.2	0.12e-3+	36
Coherent			
MSK,BL.T=0.0144*	26.5	0.72e-3	45
MSK,BL.T=0.0288*	31.6	0.25e-3	45

Table 4.2 Eb/No performance in fading, GMSK4 BT=0.25 h=0.5, fd=40Hz

Notes

Estimates only

BL.T = Loop filter bandwidth for the Costas Loop, normalised to the bit rate.

Referring to Table 4.2 the MSK type receiver (BL.T=0.0144) performs best under static Rayleigh fading. However it has the worst irreducible error. In practice, the receiver could be running in a relatively high E_b/N_o (\geq 20dB) environment during some of the time, therefore the irreducible error does have some significance. To obtain an irreducible error in the order of 0.12e-3 (1/2 bit offset detection, frequency discriminator) the loop bandwidth would be very wide, hence increasing the static E_b/N_o . With the BL.T=0.0288, the irreducible

error floor for MSK coherent detection is only 0.24e-3 which a lower performance when compared with the 1/2 bit offset technique (0.12e-3) [36]. The 1/2 bit offset technique also has a 2.4dB improvement in the Static E_b/N_o .

The remainder of this work will examine discriminator detection methods, since this is the technique used in existing transceivers for PMR systems. Direct comparison of the various baseband processing schemes is difficult from published papers as the simulated or practical set-ups used seldom coincide. All relevant published detection schemes for frequency discrimination will be simulated under the same conditions for true comparison in Chapter 5.

5.0 Simulation of schemes

One of the major requirements of this work is to adapt existing PMR transceivers with minimum modifications for digital transmission. Discriminator schemes are therefore favoured.

The various discriminator based schemes presented in the previous chapter will be compared through the use of computer simulation. All the schemes will be simulated using the same operating conditions which have been chosen to emulate a real situation (i.e. IF filters with group delay). In this way good performance comparisons can be obtained. No previous published work has compared all these schemes under the same conditions. Five schemes in all will be evaluated for GMSK detection:

- i) Conventional with one threshold,
- ii) Conventional with DFE,
- iii) 1/2 bit offset technique,
- iv) MLSE proposed by Chung for GTFM, adapted for GMSK detection, and
- v) A new technique, Forward Estimation with Decision Feedback Equaliser (FEDFE).

Simulated BER will be performed by Monte Carlo techniques and will be the main criteria used for performance evaluation. Timing recovery will not be simulated but will have a fixed offset error within $\pm 1/80^{\text{th}}$ of the symbol period, with zero variance symbol timing jitter.

5.1 Simulation Technique

The system block diagram shown in Figure 5.1, illustrates the use of files for interfacing blocks. A file interface allows a single run of the pre-processing block, with the results used multiple times by the post-processing blocks. Computation overhead is reduced, since five different schemes can be evaluated with the two output files produced from one baseband system simulation. Initial implementation of this system using the above technique was developed in 'C'. This far outperformed (in terms of simulation time) the equivalent simulation which was developed using a commercial simulation package, COMDISCO's SPW.

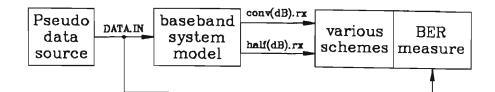


Figure 5.1 System block diagram, DATA.IN, conv(dB).rx and half(dB).rx are precomputed files used for the evaluation of various demodulation schemes.

Further speed improvements were achieved via a networked Apollo system (HP425's, or any networked Unix system), by distributing a whole BER graph over many machines. This was performed using a script file which created remote processes for various E_b/N_o values to obtain a ten point BER curve in approximately 3.5 hours (for 5 Apollos, using 40*symbol rate=sampling rate).

5.2 Baseband Model

As with the channel simulator presented in Chapter 3, the simulation will use complex envelope representation so that high sampling rates are not required. Equation 5.1 defines a RF signal at ω_c which has been phase modulated by $\phi(t)$. If the carrier is removed the modulation can be simulated by I-phase and Q-phase signals given in Equation 5.2. Representing the I and Q signals at baseband would require a minimum sampling frequency of twice the highest frequency component of the modulation, which is practical for simulation on existing computers.

$$s(t) = re\left\{e^{j\omega_c t}e^{j\phi(t)}\right\}$$
(3.1)

(5 1)

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$$I(t) = \cos(\phi(t))$$
(5.2)
$$Q(t) = \sin(\phi(t))$$

A symbol timing recovery algorithm is not simulated, hence ensuring accurate BER estimations at low E_b/N_o . There is no guarantee that the sampling point will be near optimum so high oversampling is utilised to give good timing resolution. High oversampling would also reduce the effect of aliasing, which may be caused by the low but finite out of band frequency components of GMSK or by hardlimiting of the signal which would spread the

modulation. A sampling rate of 40 times the symbol rate was selected which would allow a maximum offset error within $\pm 1.25\%$ (1/80) of the symbol period.

The fixed timing offset error reduces the effective E_b/N_o , by the losses shown in Table 5.1. This loss in E_b/N_o is estimated by the ratio of eye opening with the offset error to the eye opening with perfect timing recovery, using a bit stream (00100) which produces the minimum eye opening. Sampling 4 times the symbol rate produces errors in the order of 3dB, 10 times the symbol rate produces 0.5dB loss which is in the order of typical implementation losses. With sampling of 40 times the symbol rate the degradation is ≈ 0.03 dB, hence timing recovery effects are negligible.

GMSK	Sampling Frequency		
BT	4*R	10*R	40*R
0.20	-7.697	-0.581	-0.056
0.25	-3.510	-0.485	-0.028
0.30	-3.103	-0.445	-0.027
0.40	-2.937	-0.422	-0.026
0.50	-2.649	-0.366	-0.022

Table 5.1 Maximum E_{t}/N_{o} degradation in dB, caused by timing phase offset

The following sections will describe the blocks of the System, and the blocks used for the baseband model, shown in Figure 5.2.

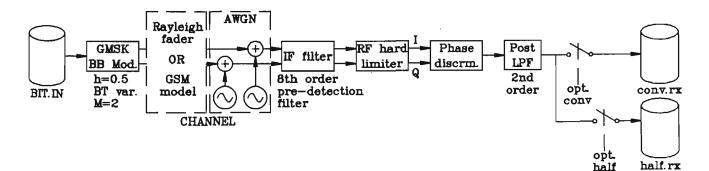


Figure 5.2 Block diagram for the Baseband model

PN sequence generator

Standard maximal length 16 bit PN sequence [52].

GMSK modulator

The theoretical basis for GMSK generation is shown in Chapter 2. The modulator is implemented by convolving the data stream with the q(t) pulse, given by Equations 2.3 and 2.4 (using convolution by Equation 2.2). This generates the phase modulating signal which is applied using the form of Equation 5.2.

Rayleigh Fader/AWGN

A simple one path Rayleigh fader was implemented as shown in Figure 3.3, but modelled at baseband (i.e. the I/Q modulation signal is complex multiplied with two filtered gaussian noise sources). BER performance deviated marginally when using either a complex 6 tap GSM model or a simple Rayleigh fader (~1dB in favour of GSM), with the latter chosen for reduced simulation times. The gaussian sources used for both the Rayleigh fader and AWGN were generated and tested as described in Section 3.2.1. The spectral shaping filters of the single Rayleigh fader were designed at a lower sampling frequency, with simple 2nd order filters designed directly in the Z-domain. Additional roll-off was achieved by the interpolating (^40) filters. To obtain correct E_t/N_o values for the simulation it was very important that the RMS level through the fader block was $1/\sqrt{2}$ (i.e. a gain of 0dB).

IF filter/Pre-detection filter

This block simulates the selective stages in a radio receiver used to reduce out of band signals which cause interference. A practical double conversion FM receiver would have the structure shown by Figure 5.3. The received signal from the aerial is initially band limited to the band of interest. A PLL frequency synthesiser and multiplier is used to translate the signal to the first IF frequency of 21.4Mhz, where some channel selectivity is performed by a crystal filter, which have good spurious characteristics. A crystal oscillator of 20.945Mhz and multiplier then translates the signal to an IF of 455kHz. Further selectivity is achieved by a crystal filter operating at this frequency. The cutoff edges of both BPFs produce severe group delay and phase distortions, which would be the main source of degradation to a digital signal before the limiter-discriminator.

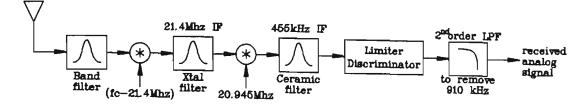


Figure 5.3 Practical FM receiver based on a Philips PRM-80

Published material generally simulates these selectivity filters using a Butterworth filter with idealised phase and group delay characteristics. This would be satisfactory if the existing radio transceivers used for this work contained expensive constant group delay selectivity filters, however this is not the case as standard analog filters exist. To accurately simulate the real situation, these poor group delay characteristics are included in this IF filter model.

The total selectivity filtering was modelled as an 8th order Butterworth IIR which is capable of generating similar group delay and phase distortion to that of the crystal filter. The crystal filter in the practical system had a narrower bandwidth hence had a more significant effect in distorting the modulated signal than caused by the ceramic filter. The practical filter pair had a -74dB stop band.

The simulated characteristics of the IF stage are shown in Figures 5.4a and 5.4b. The phase response of the filter introduced 1400 degrees across the band. These simulated results are similar to the measured results.

This Pre-detection filter and the Post-detection filter, which will be presented latter, are specified by the normalised BT product, which is the -3dB frequency of the filter (B) multiplied by the symbol period (T).

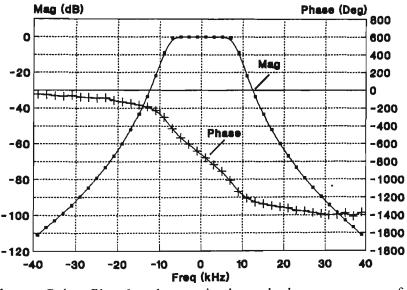


Figure 5.4a Simulated magnitude and phase responses for the IF filtering stage (BT=1.0, R=16kb/s).

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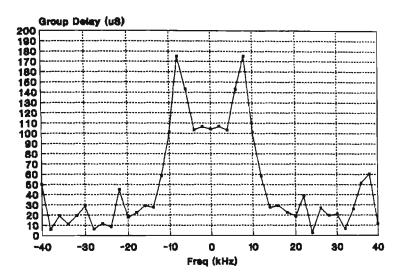


Figure 5.4b Simulated group delay response for the IF filtering stage (BT=1.0, R=16kb/s)

Hard-limiter/discriminator

The Hard-limiter ensures that envelope variations, which are caused by changes in the received signal strength, do not pass through to the discriminator and thus appear as demodulated received signal. The model used for the hard-limiter is shown in Figure 5.5.

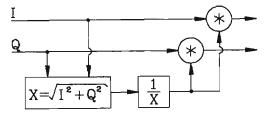


Figure 5.5 Hard-limiter model

Section 4.2.2 showed that the quadrature detector simply differentiates the phase of the IF signal. There are two general techniques for simulating the differentiation of the baseband phase:

i) The simulation is performed at baseband hence the difference between successive ARCTAN(Q/I)¹ samples will approximate differentiation when high sampling frequencies are used. A simple modulator-demodulator produces spikes in the received waveform, due to the inherent phase wrap problem. This was overcome with two modifications, using an ARCTAN function which works within $\pm \pi$ range (i.e. all 4 quadrants) and an algorithm which checks

¹ I and Q refer to the In-Phase and Quadrature-Phase respectively.

for positive and negative crossings of the π with a threshold when calculating the differentiation. The maximum rate of change of phase due to modulation for a CPM system with h=1/2 is 2.25 degrees (90 deg/40 times symbol sampling). Hence the spike should be removed if two consecutive samples are within the range of 180±2.25 degrees. Any transitions not in this range can be considered to be caused by deep fades which generate phase clicks. However it must be noted that there is a small but finite probability that the algorithm may be inadequate.

ii) The alternative is to mathematically differentiate the ARCTAN function as performed below:

$$\boldsymbol{\theta}(t) = \operatorname{arcTan}\left(\frac{\boldsymbol{Q}(t)}{\boldsymbol{I}(t)}\right) \tag{5.3}$$

$$\frac{d(\theta(t))}{dt} = \frac{d\left(arcTan\left(\frac{Q(t)}{I(t)}\right)\right)}{dt} = \frac{\frac{d\left(\frac{Q(t)}{I(t)}\right)}{dt}}{1 + \left(\frac{Q(t)}{I(t)}\right)^2}$$
(5.4)

$$\frac{d\theta}{dt} = \frac{I(t)\frac{dQ(t)}{dt} - Q(t)\frac{dI(t)}{dt}}{I^2(t) + Q^2(t)}$$
(5.5)

The differentiation approximation for either technique is totally dependent on the sample rate(fs). As fs is increased, Δt decreases and the approximation is improved. Both techniques were implemented for the frequency discriminator and both produced similar BER results. Technique i) was used in this work.

Post-detection LPF

In analog systems the Post-detection LPF is a simple one pole RC type network which has the main purpose of removing the 900kHz RF which is a by-product of the discriminator. A digital application has an additional requirement of maximising the SNR at the optimum sampling point. This requires more than one pole. However this could introduce distortion into the signal if a high order or low cutoff frequency filter is used. This filter was modelled as a 2nd order IIR butterworth.

Much of the literature does not use a standard LPF as described above, but instead an Integrate and Dump(I&D) filter with the same underlining notion of maximising the SNR at the sampling instant. The I&D filter integrates the signal over the symbol interval then dumps the results to a decision making system. The integration was simulated using Simpson's rule for numeric integration and synchronised (dump/reset) by offset optimum sampling points. Results using I&D filtering were compared with the 2nd order IIR system.

Sampler (Conventional, 1/2 bit offset)

There are two sampling positions required to implement the five different post discriminator detection schemes, see Figure 5.6 - the conventional sampling point where a 2-level eye exists and 1/2 bit offset eye which is a 3-level eye. Before the simulations are made, a test run of 1000 bits was performed with high E_b/N_o and no fading, graphically displaying the eye diagram to determine the best 2 and 3 level eye positions. These positions are totally dependent on the BT products of the modulation and Pre/Post detection filtering.

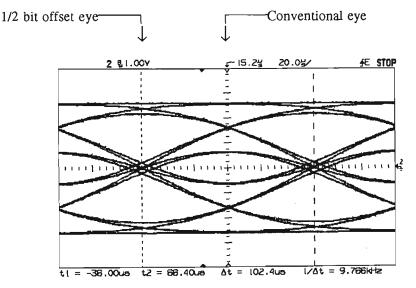


Figure 5.6 Sampling positions for GMSK BT=0.24

5.3 Post-detection processing (various schemes)

i) Conventional detector

A simple threshold is used to decide '1' or '0' at the optimum sample instant (2-level eye). The decided bit is compared with the delayed transmitted bit sequence, to obtain the number of bits in error. The transmitted sequence must be delayed to account for the effect of the filters and the modulation. This detector is shown in Figure 5.7.

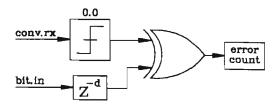


Figure 5.7 Conventional detector

ii) Conventional plus DFE

The main source of ISI when using a conventional detector is caused by the GMSK modulation, required to narrow the required spectrum. Since the receiver knows what type of modulation is being transmitted, it should be possible to remove the ISI effect caused by the previous received bits. By feeding back the last symbol detected and appropriately scaling it, depending on the ISI that it introduces, a Differential Feedback Equaliser (DFE) is obtained, as shown in Figure 5.8.

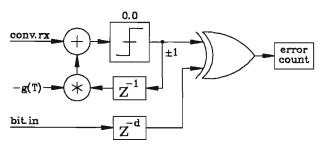


Figure 5.8 Conventional detector with DFE

iii) Half bit offset detection

Ohno and Adachi [36] observed that the eye at the half symbol sampling instant was open considerably more than that of conventional point. However there was ambiguity due to the 2 eyes. They devised a scheme using differential encoding in the transmitted bit stream so that transmitting a '1' resulted in a transition $(X_{n+1}=\bar{X}_n)$ and transmitting a '0' resulted in a hold $(X_{n+1}=X_n)$. This meant the detection process required absolute valuing the signal and a non-zero thresholder, as shown in Figure 5.9. Differential decoding is required for the transmitted sequence to obtain the correct bit stream for BER measurements.

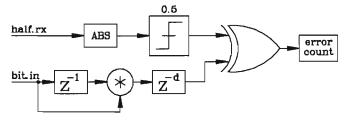


Figure 5.9 Half bit offset detector

iv) New detector (FEDFE)

A new detector for GMSK, Forward Estimation using Differential Feedback Equalisers (FEDFE), has been developed during this work. This extends the concept of DFE by estimating the subsequent bit. This is achieved by using two standard conventional plus DFE systems both fed with the input signal of which one is delayed by a symbol. The undelayed system Forward Estimates (FE) the subsequent bit of the delayed system and removes its ISI contribution. The DFE in the delayed system removes the ISI of the previous bit detected. Hence, the ISI introduced by the leading and trailing bits is removed. These bits are the major contributors to ISI, particularly for GMSK modulation with $BT \leq 0.25$. The block diagram for this scheme is shown in Figure 5.10.

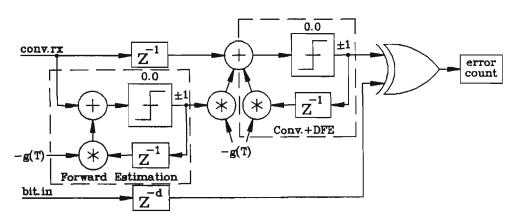


Figure 5.10 New detector (FEDFE) developed in this work, showing the conventional+DFE and new Forward Estimating section.

The Conventional + DFE section in Figure 5.10, makes the decision in the middle position (α_n) of Figure 5.11 with the ISI of the previous bit removed (α_{n-1}) . This new scheme delays the standard Conventional + DFE detector, and utilises another Conventional + DFE detector to "Forward Estimate" the subsequent bit (α_{n+1}) .

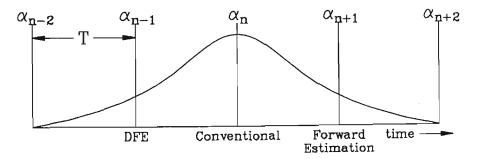


Figure 5.11 ISI removed with the New scheme (FEDFE), developed in this work.

v) Maximum Likelihood Sequence Estimation (MLSE)

Chung [37] developed a technique based on a two state MLSE for Generalised Tamed Frequency Modulation (GTFM). Chung used a state description with two states, which was achieved by reducing the impulse response length. The reduced impulse length introduced a 10dB degradation in power spectrum when compared to TFM at T Δf =1.0. By utilising the 1/2 bit offset sample point (3-level eye), Chung effectively reduced the impulse response to 3 symbol intervals, with the central 2 samples dominant. This is an approximate MLSE for a non-coherent receiver, in contrast to the optimum MLSE outlined in section 4.1.1.

The algorithm presented here follows Chung with a change to the modulation dependant constant $\{g(T/2)\}$ which is set for GMSK with BT=0.25. The impulse response for BT=0.25 spans 4 symbols, where the two farthest samples from the main central impulse are finite. This will cause a slight loss in performance which can be recovered by using a state description with more states, at the expense of increased complexity. The block diagram of this algorithm is shown in Figure 5.12.

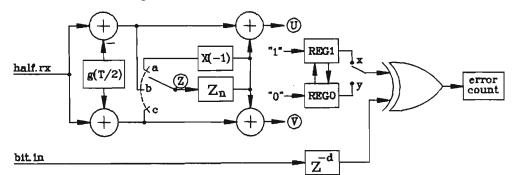


Figure 5.12 Approximate MLSE detector for a non-coherent receiver.

The output is based of one of the following three processing possibilities:

i)	if (U≥0.0)	{	$Z_n = half.rx - g(T_n)$	7/2)	
			REG1<<"1",	REG0<<"0"	
			output=MSB	of REG1	};
ii)	if (V<0.0)	{	Z _n =half.rx+g(Т/2)	
			REG1<<"1",	REG0<<"0"	
			output=MSB	of REG0	}; or,
iii)	if (U<0) & (V≥0)	{	$Z_n = -Z_n$,	$REG1 \Leftrightarrow REG0$	
			REG1<<"1",	REG0<<"0"	
			if $(Z_n > 0)$	output=MSB of REG	1
			else	output=MSB of REC	i0}.

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5.4 Simulation Results

The signal from the GMSK modulator shown in Figure 5.2 has an envelope of 1.0. This implies a baseband signal power of 1.0 Watt (RF power= $(1/\sqrt{2})^2=0.5$ W). The fader is designed such that its RMS= $1/\sqrt{2}$, when a baseband represented carrier (I=1.0 & Q=0.0) is passed. Hence the fader has no effect on the original power generated by the GMSK modulator. The required E_b/N_o can be obtained by suitably adjusting the σ^2 (variance) of the AWGN in both the I and Q channels.

To compare the simulation results with published material, E_b/N_o must be determined at the input to the hard limiter, where E_b is the Energy per symbol and N_o is the single sided noise spectral density. The gaussian noise is generated at the sampling frequency (40*f_b), so the high frequency components are folded back at the nyquist frequency (40*f_b/2). Therefore the noise spectral density generated by the AWGN block is constant to the nyquist frequency (i.e. \pm fn for baseband representation) with a total baseband noise power of 2* σ^2 (Watts), as shown by Equation 5.6.

$$N_{\sigma} = \frac{2\sigma^2}{2f_n} = \frac{\sigma^2 2}{40f_b}$$
(5.6)

Hence, the relationship between S/σ^2 and E_b/N_o is given by Equations 5.7 and 5.8.

$$\frac{E_b}{N_o} = \frac{S}{f_b} * \frac{40f_b}{2\sigma^2} = 20\frac{S}{\sigma^2}$$
(5.7)

$$\left(\frac{E_b}{N_o}\right)_{dB} = \left(\frac{S}{\sigma^2}\right)_{dB} + 13dB$$
(5.8)

By fixing S=1W (baseband representation), the setting of σ^2 to achieve the required E_b/N_o is found by:

$$\sigma^2 = 10^{-\frac{X-13}{10}} \quad \text{where} \quad X = \left(\frac{E_b}{N_o}\right)_{dB} \tag{5.9}$$

Simulations were performed by transmitting $5e^5$ bits, with the BER accepted for ≥ 50 errors. A combined AWGN and fading channel was then considered to estimate the best discriminator based detector under mobile radio conditions.

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5.4.1 AWGN Channel

The graphs below (Figure 5.13) show the BER performance of the five schemes outlined in section 5.3 using an AWGN channel. In general, published material uses a predetection filter of BT=1.0 with or without a post-detection filter, which could consist of a

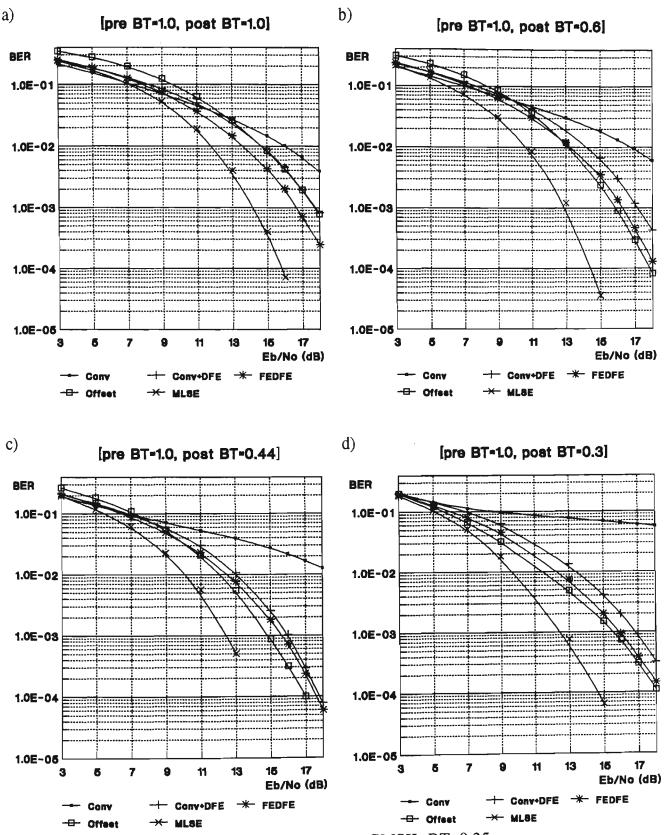


Figure 5.13a-d BER performance in AWGN for GMSK, BT=0.25

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Chapter 5

linear or Integrate and Dump filter.

Using BER performance curve for Post-detection filter with BT=0.44 (Figure 5.13c) the required E_b/N_o have been tabulated for a BER=1e-3 (see Table 5.2). The simulated performance was between 2-3dB worse than those published. This degradation was due to the IF simulation model which considered the poor phase and group delay characteristics of practical analog IF filters.

Scheme	Published (dB)	Simulated (dB)
Conv+DFE	12.8 [17]	16.0
Half	13.1 [10]	14.8

Table 5.2 Required E_b/N_o to achieve a BER=1e-3, for GMSK4, BT=0.25, h=1/2, Pre-filter BT=1.0 and Post-filter BT=0.44

A post detection filter with BT=0.44 was specified as optimum [43] when a predetection filter with BT=1.0 was used. Intuitively you would expect some optimum to exist, as a noisy digital signal poorly filtered (high BT) would be swamped by noise while to much filtering (low BT) would distort the original signal by the introduction of ISI. The general trends of the curves in Figure 5.13 indicate that increasing post detection BT actually improves BER especially at high Eb/No, this implies that there is little noise from the output of the discriminator hence near optimum pre-detection filtering in terms of AWGN rejection. The improvement of BER as post detection BT is increased can be explained by the reduced amount of ISI introduced.

Figure 5.14b clearly highlights the optimum post detection BT by allowing noise into the system at IF. This clearly shows a post-detection filter of $BT_{opt}=0.45-0.5$ to be optimum for conventional detection with Pre-detection BT=2.0. A optimum exists due to two dominating factors which occur for the extremes of BT products. For $BT>BT_{opt}$ the noise from the discriminator output is dominate, where for $BT<BT_{opt}$ the ISI introduced by the postdetection filter dominates. The difference in BER between the Figure 5.14a(5.5e-2) and 5.13b(2.4e-2) for a post detection BT=0.3 at a Eb/No=19dB is due to the increased predetection BT which reduces ISI.

Comparison of $E_b/N_o=15,19$ dB curves in Figures 5.14a and 5.14b, show that the BER is optimised for Conventional detection in an AWGN channel, when the Pre-detection BT=1.0 and Post-detection BT>1.0.

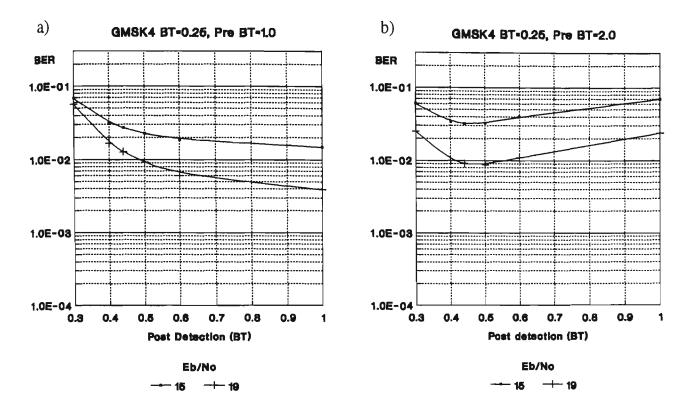


Figure 5.14 Optimum Post-Detection BT using conventional detection, GMSK4 BT=0.25 with a) Pre-detection BT=1.0, and b) Pre-detection BT=2.0.

5.4.2 Fading Channel

These simulations consider fading. This is the main source of signal degradation in a mobile radio channel. A specific configuration will be used for comparison;

- GMSK4, BT=0.25, h=1/2
- Pre-detection, BT=1.0
- Post-detection, BT=0.4

A straight comparison at BER=1e-3 does not give a unique curve. The fading rate should also be considered. A fading rate (f_d) of 40Hz (f_dT =0.0025) was selected as it is equivalent to a vehicle speed of 100km/hr at PMR frequencies (450MHz). The two main parameters for comparison will be the E_b/N_o at BER=1e-3 and the irreducible error rate. From Figure 5.15a and 5.15b the following points were measured;

i) Conventional for pre BT=1.0	pre BT=2.0
- $E_b/N_o=45.0$ dB at BER=1e-3	- $E_b/N_o=38.3$ dB at BER=1e-3
- error floor=0.690e-3	- error floor=0.268e-3
ii) Half offset detection	

- $E_{b}/N_{o}=36.0$ dB at BER=1e-3 - $E_{b}/N_{o}=35.0$ dB at BER=1e-3 - error floor=0.274e-3 - error floor=0.200e-3

An $E_{\nu}/N_{o}=38.1dB$ was required for BER=1e-3 with conventional detection [36]. This has a 7dB discrepancy with the simulated result (45.0). This is caused by the group delay of the IF stage. But in this case, even shallow fades have a dramatic effect on the small conventional eye. This is verified by using a wider IF stage which should decrease performance as more noise is allowed into the system, but in reality the severe group delay effects are moved away from the modulation. Figure 5.15b shows this significant improvement in $E_{\nu}/N_{o}=38.3$ which is similar to that published in [36]. With the pre-detection filter BT=1.0 the simulated irreducible error rate of 0.69e-3 was similar to the published [36] floor of 0.56e-3. The main dominating factor at high E_{ν}/N_{o} is the impulse response length of the IF filter which introduces additional ISI to the signal. Hence increasing the pre-detection BT should reduce the error floor, which is visible in Figure 15b giving BER=0.268e-3 for conventional detection.

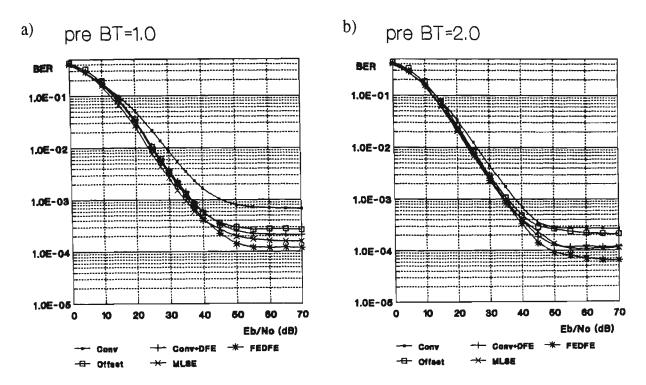


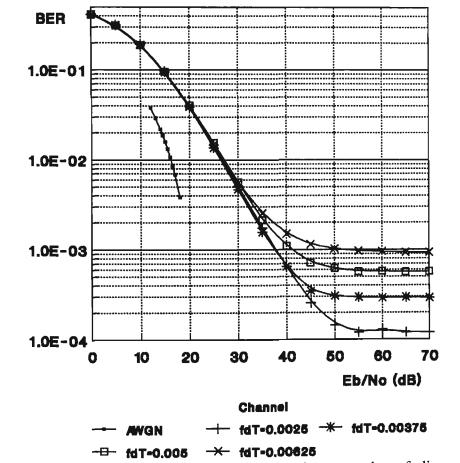
Figure 5.15 Performance in fading with GMSK BT=0.25, post BT=0.4 and f_d T=0.0025

There was a 1dB difference in E_b/N_o between the two pre-detection BT's for the offset technique, which verifies that the offset eye position has more tolerance to ISI degradation compared to a single threshold level at the conventional sampling instant.

The theoretical BER approach for conventional detection [47,49,50] in fading has E_b/N_o of 46.1dB, 37.0dB and 47.1dB with error floors of 0.33e-4, 0.30e-4 and 0.35e-4 respectively. The simulated static E_b/N_o =38.3dB was improved² whereas the error floor was increased to 0.268e-3. Both these effects can be explained by the absence of post-detection filtering in the theoretical model [47,49,50]. Under static fading, the post-detection filter performs similar to the AWGN case, i.e. improves the SNR at the sampling instant. Hence the simulated value of 38.3dB is improved as expected. The simulated error floor (0.268e-3) increased, due to the post-detection filter dispersing a phase click over several bits and the fact that the published paper used a slower fading rate (f_dT =0.002). In the proposed theoretical model [47,49,50] the effect of deep fades is only dependant on the fade characteristics. Hence, dispersion over several bits is limited.

² For a pre-detection BT=2.0 to minimise group delay distortion.

Figure 5.16 shows the effect of fading rate on the irreducible error rate, for conventional detection. The irreducible error rate is an error floor which can not be removed by increasing the transmitted signal strength. Fast fading increases the frequency of relatively deep fades which in turn increases the number of phase clicks over a given period of time. When this signal is frequency discriminator detected, the phase clicks produce a spike (due to the differentiation of the phase) or a smoothed superimposed pulse, depending on the depth of the fade. This non-gaussian noise has the potential to corrupt whole symbols. Therefore increasing the fading frequency, increases the number of symbols in error. Figure 5.16, shows that slow fading has a better irreducible error. The static fading part of the curve (E_{y}/N_{o} <30dB) shows a performance degradation of 10dB at BER=1e-2 when compared to a simple AWGN channel.



GMSK4 BT=0.25, pre BT=2.0, post BT=0.6

Figure 5.16 Performance of Conventional detection at various fading rates

5.4.3 Comparison of schemes in fading

Sections 5.4.1 and 5.4.2 compared the simulated performance with the results from published material. This section will select one scheme (from the five mentioned in section 5.3) which has the best performance in a mobile radio channel. Also taken into consideration are the effects of pre/post detection filtering. During some simulations, where the post-detection BT \leq 0.35, the ISI and group delay distortion was so severe that the optimum eye position for conventional sampling was difficult to distinguish. In these cases, ideal runs (no fading, high E_b/N_o) of 4000 bits were performed to determine (iterate to) the best sampling position.

The simulations were based on GMSK4(BT=0.25) with a bit rate of 16kb/s and fading rate of f_d T=0.00625³. A carrier frequency of between 400 to 500MHz corresponds to maximum vehicular speeds of 270 to 216km/hr respectively.

The modulation parameters are suitable for digital cellular system which has a higher tolerance to ACI. However, if the digital modulation is to be integrated into an existing analog PMR system then tight spectrum control is required to reduce leakage into the adjacent analog channel. This implies reducing either the bit rate or the GMSK BT, with the latter being the most preferred, as high bit rates are desirable. Reducing the GMSK BT results in a reduced eye (Figure 2.9) and hence degradation in BER. So PMR performance is expected to be less than that presented in this section.

Selecting a digital modulation suitable for present analog regulations will be covered in Chapter 6. From the curves outlined in Figure 5.13 for the AWGN case (no fading), MLSE showed a minimum 2dB improvement at BER=1e-3 for most combinations of pre/post detection filtering BT products when compared to the next best scheme. In a mobile fading environment this is diminished to 1dB for $E_{\rm p}/N_{\rm o}$ <40dB. The new FEDFE scheme has the lowest irreducible error floor - some 25% better than MLSE. An important observation found in Figure 5.15b is that the FEDFE scheme achieves the same $E_{\rm p}/N_{\rm o}$ at BER=1e-3 as MLSE.

The overall performance of conventional detection is much improved in Figure 5.15b when compared to Figure 5.15a. This is due to the group delay pre-detection filter effects. This highlights the effect of pre/post detection filtering on performance and suggests these two filters should be selected to minimise BER.

³ Although $f_d=100$ Hz is high for PMR frequencies, it aided in reducing simulation time.

5.4.4 Optimisation of Pre and Post detection filters

Due to the ease of theoretical analysis the published literature generally used an I&D filter for the post-detection filter. However, the I&D filter is primarily used for AWGN channels and, as will be shown, does not minimise the BER in a fading environment. Figure 5.17 shows the performance of conventional detection for various pre/post detection combinations with relatively static fading ($E_b/N_o=10dB$, 20dB) and irreducible error (high

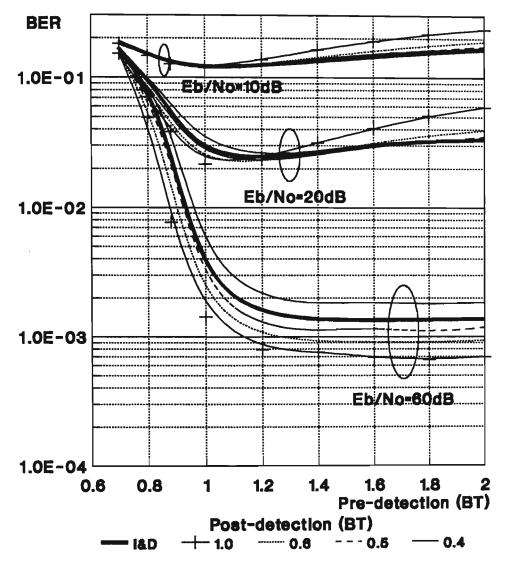


Figure 5.17 Pre/Post detection filtering effects for a conventional detector ($f_d T=0.00625$)

 $E_b/N_o=60$ dB). This clearly shows that for a low SNR ($E_b/N_o=10$ dB) the I&D filter and 2nd order LPF with BT<0.5 produce the best BER for all pre-detection BTs. As E_b/N_o is increased the AWGN no longer dominates the impairments, and non-gaussian noise from the fading process govern the performance. When $E_b/N_o=60$ dB, the I&D filter no longer performs best, and it is found that a large Post-detection BT which introduces minimum amount of ISI is desirable for decreasing the irreducible error rate.

For an $E_b/N_o=20dB$ (Figure 5.17) the curves for a post filter with BT=0.4 and BT=1.0 show a cross over effect for producing the optimum BER when the pre-detection filter BT≈1.25. For a pre-detection BT>1.25, a large amount of noise passes into the system. Hence a post BT=0.4 produces an equivalent BER to that of an I&D filter. However, for predetection BT<1.25, a post BT=1.0 is best as it introduces a minimum amount of ISI into the signal. A post filter with BT≈0.5⁴ introduces approximately the same amount of ISI and reduces the AWGN to the same level as the I&D post filter. Hence a 2nd order Butterworth post filter with BT≈0.5 is equivalent to an I&D Post-detection filter for a conventional detector.

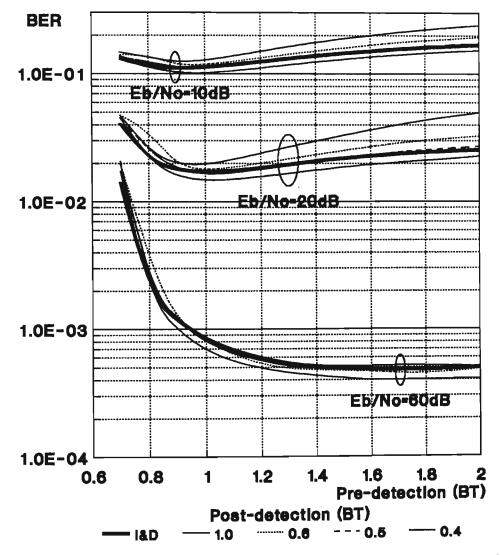


Figure 5.18 Pre/Post detection filtering effects for the New detector ($f_dT=0.00625$)

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⁴ Though the curves suggest a BT slightly less than BT=0.5

In the high E_b/N_o region of Figure 5.15 the FEDFE scheme always gave the best error floor. In terms of complexity, the FEDFE scheme is much easier to implement than MLSE and will be chosen for optimising the pre/post detection filters. Figure 5.17 shows that the optimum BER for low E_b/N_o is obtainable by a pre-detection BT of $0.9\rightarrow 1.0$.

The irreducible error rate for the FEDFE scheme is very insensitive to post detection BT product (see Figure 5.18) as compared to conventional detection since the inherent ISI caused by the GMSK modulation is removed. With this ISI removed, the BER performance is improved. This is apparent when comparing Figure 5.17 with Figure 5.18, for all pre-filtering BT products. Figure 5.18 still shows significant ISI and group delay distortions when pre-filtering BT < 1.0. This ISI could be minimised at the cost of high complexity but this would only improve the irreducible error rate, beyond an already acceptable BER value.

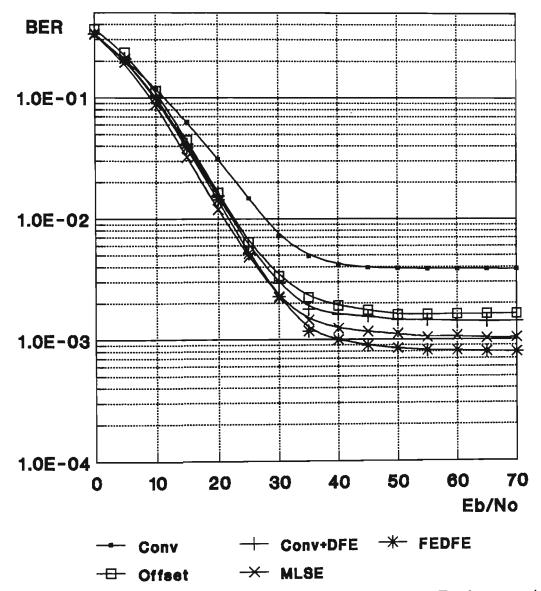


Figure 5.19 Simulated BER for the best receiver structure, FEDFE scheme optimised. GMSK4 BT=0.25, pre BT=1.0, post BT=0.4, f_d T=0.00625

5.5 Conclusion

This chapter considered five different frequency discriminator schemes and determined the best under a mobile radio channel. The simulation model presented was based on hardware implementation using existing transmitter/receiver sets designed for the present analog system, and using the minimum amount of modification in adapting them for data transmission. The results in both the AWGN and fading channels obtained by the model were similar to those from the published literature. However, the slight discrepancies in the results were due to the lack of information regarding the type of models used in the published literature.

MLSE proved to have the best performance. However for a 0.8dB loss in E_b/N_o the FEDFE scheme would result in reduced complexity and irreducible error rate. The pre and post detection filter BT products were selected for minimum BER for low E_b/N_o , giving the final performance shown in Figure 5.19.

The performance of the five schemes were evaluated under the same AWGN and Rayleigh fading. Hence selection of the best scheme was made competently rather than selecting the best scheme from published material. The simulated IF filter modelled the practical system closely, because group delay was considered. The only factor which can alter the practical performance when compared to the simulated performance presented, would be due to the transmitting configuration (GMSK BT product, Bit rate and deviation). The transmitting configuration depends on the application, which determines the ACI requirement of the system. To reduce the ACI, the GMSK BT product must be reduced and/or the bit rate reduced. E_v/N_o performance will therefore be effected. The next chapter describes a practical GMSK implementation.

6.0 Hardware Implementation

In this chapter, the implementation of a possible system will be presented which can co-exist with the existing PMR analog system. Measurements will be presented in section 6.1, which will highlight limitations of the data modulation required to meet the ACI specification of the current analog PMR system. The design of the hardware test system, both demodulator and simple coding, will be described in section 6.2.1 and 6.2.2 respectively. The practicalities of modifying analog radio sets will be examined in section 6.2.1.1. Finally, the performance will be considered with comparison to simulated results, in section 6.3.

6.1 Limitations on Bit Rate

The main driving force behind this project is to develop a digital system which can co-exist with the existing analog PMR system. Hence, the ACI requirements must satisfy existing analog specifications, covered in section 2.4 of R.B. 234 [53]. Applying this specification a set of curves will be developed from measurements which will determine the required Bit Rate, pre-modulation BT product and Deviation. Summary of this procedure and results obtained will be presented here with further detail in Appendix B (extract from [54]).

The standard analog ACI measurements were performed for verification of the measurement technique. These results are shown in Table 6.1. The test signal was injected across the microphone terminals in the handset to ensure correct conditioning of the transmitted signal. This test signal used three different modulating frequencies with varying amplitudes, which were relative to the level required to produce 60% of the maximum deviation at a frequency of 1500Hz. The SINAD measurements were taken from the unloaded speaker output, with the volume control set to give 0.9 Vrms (RF level -40 dBm). The specification requires < 12 μ W adjacent channel power, which was clearly satisfied by the Philips PRM-80 transceiver and, as expected, performed significantly better due to the improved IF filtering when compared to the standard receiver.

The sensitivity of an analog signal to an adjacent digital channel was then measured. The GMSK modulator (as described in section 2.6.1) was fed into a gain/offset stage which performed deviation and DC coupling respectively. These measurements simply used a reference analog channel where -12dB SINAD was reduced to -9dB SINAD by adjusting the bit rate of an adjacent digital channel with fixed deviation and modulation BT product. A diagram showing the hardware layout and measurement procedure are presented in Appendix

Β.

Table 6.1	Analog ACI	test on	a PRM-80	transceiver	to R.B.	234 [1].
Adjacent cl	hannel power	must be	< 12µW.			

Frequency of test modulating signal	level, rel. 60% 1500Hz	Adjacent Channel leak through, from a 50W transmitter
1500	10 dB	6.9 μW
300	15 dB	4.4 μW
3000	0 dB	7.8 μW

Once the maximum bit rate was obtained, measurements of the received digital signal were made relating to eye-openings and allowable timing jitter for both the conventional and half bit delayed eyes. Eye-opening gives a measure of BER performance, while timing jitter indicates sensitivity to synchronisation. Figure 6.1 shows a combination of three typical graphs which relate to conventional detection. The first graph shows the bit rate versus eye opening, where eye opening is in mVolts. This curve allows a Gaussian filter BT to be selected which achieves maximum eye opening for a given bit rate. An important point to note is that the eye opening may be negative. Under these conditions it would be pointless using a single threshold detection scheme. Improved schemes capable of removing ISI must be adopted. This curve also shows that as the bit rate is increased for a given Gaussian filter BT the eye opening drops. This can be attributed to the IF filtering stages introducing ISI into the signal.

6.1.1 Use of Graphs

After a given bit rate has been selected, a line can be traced to the bit rate versus jitter time graph in Figure 6.1. This shows absolute time. The jitter time for negative conventional eyes is undefined. Hence the reason for the reduced number of points. Figure 6.1 shows an example where the bit rate was selected as 16kb/s indicating a Gaussian filter BT=0.3 which gives the best eye opening (38.4mV) and a timing jitter of 28.3 μ S. Tracing the 38.4mV eye opening to the deviation versus eye opening curve in Figure 6.1, indicates a required deviation of $\leq \pm 2.0$ kHz.

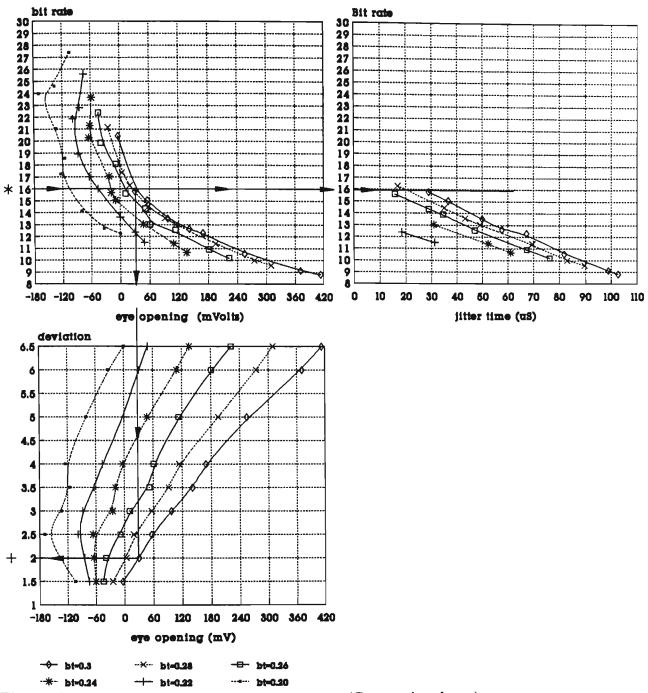


Figure 6.1 Selection of modulation parameters (Conventional eye)

The equivalent graphs for half bit offset detection are shown in Figure 6.2. An important observation is that the bit rate versus eye opening shows relative insensitivity to the Gaussian filtered Frequency Shift Keying (GFSK) BT product, when compared to the conventional eye. For a fixed bit rate of 16kb/s the eye opening for conventional sampling instance varies by 120mV, whereas the eye opening only varies by $\approx 30 \text{mV}$ for half bit offset detection under the same conditions (i.e. same range of GFSK BTs from $0.2 \rightarrow 0.3$).

In this example, half bit offset detection will be considered for a bit rate of 16kb/s. The top left hand graph in Figure 6.2 indicates that a GFSK BT $\approx 0.22 \rightarrow 0.26$ will provide the

maximum half bit offset eye. However the jitter curves suggest GFSK BT=0.26. Tracing the 146mV opening down to the deviation curves shows that the deviation should be set to ± 2.9 kHz to meet the analog ACI specification.

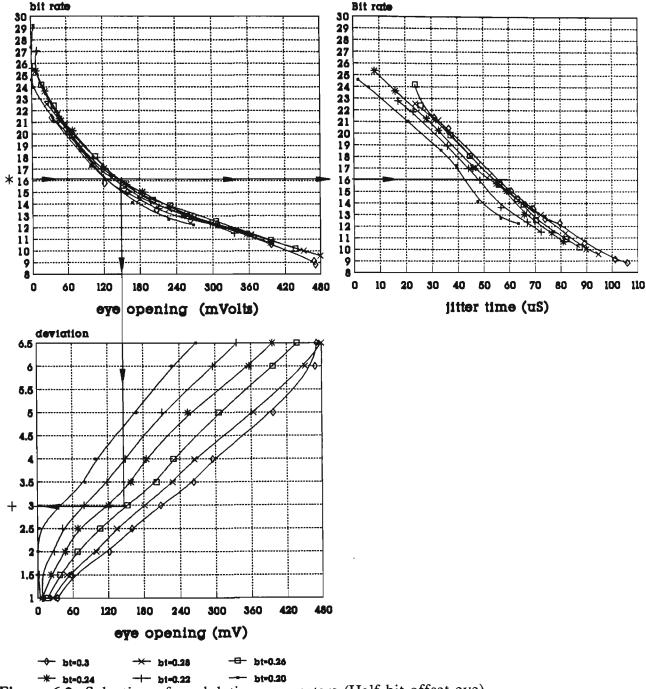


Figure 6.2 Selection of modulation parameters (Half bit offset eye)

These sample selections of modulation parameters for both the conventional and half bit offset sampling positions have been summarised in Table 6.2. Although the eye opening for the half bit offset position is 3.8 times wider with simple single symbol decisions, the conventional eye can be opened with more complex detection algorithms.

Detection	Modulation Parameters			Performance Indexes	
Position	Bit Rate	BT	Deviation	eye (mV)	jitter (µS)
Convent.	16kb/s	0.30	±2.0kHz	38	28.3
Half	16kb/s	0.26	±2.9kHz	146	54.0

Table 6.2 Possible modulation selections satisfying existing analog PMRACI requirements.

6.2 Test system implementation

The test system shown in Figure 6.3 can be sub-divided into two main sections. Specifically, the uncoded data stream, which includes GFSK filtering, FM Transmitter/ Receiver and GFSK demodulator and the Packeting system, which includes Packet encoding/decoding with error correction.

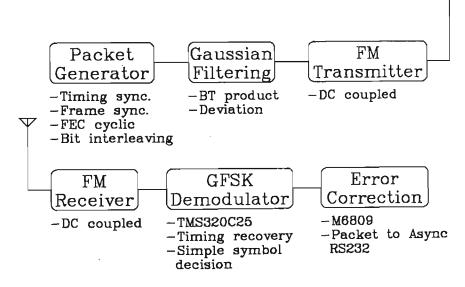


Figure 6.3 Test system

6.2.1 Uncoded data stream

The GMSK filtering was previously discussed in section 2.6 and thus will not be presented in this section. This sections primary concern is the modifications of existing analog radios for data transmission and the implementation of some of the algorithms presented in Chapter 5. A simple timing recovery implementation will also be considered.

6.2.1.1 Baseband Hardware

The major problem associated with adapting analog voice radio sets for data transmission is that of maintaining DC. The microphone input and speaker output are generally AC coupled. Transmitting a GMSK signal would result in loss of DC causing a DC wandering problem. The pre-emphasis and de-emphasis circuits must also be considered. There are two possible solutions to this problem; i) The data can be coded for DC removal along with pre-distortion. This reduces the maximum throughput and spectral efficiency of the system. ii) The data signal is injected/extracted where the system is DC coupled. This has the disadvantage of modifications to the radio sets.

Another problem is associated with the Phase Locked Loop (PLL) synthesiser which generally has the modulating signal injected at the VCO input. Any DC in the data signal would be considered as long term phase error. Hence it would be removed by the inherent nature of the PLL. However, this was not a major problem as the Philips PRM-80 transceiver, used for this work, had a double feed PLL, with a modulating signal to the main VCO (conventional PLL operation) and the other modulating feed signal went via a LPF, to a variable reference oscillator of 10Mhz. This enabled operating the signal down to DC.

The next problem was related to determining of an adequate interface (bulk DC offset removal and Gain circuit) between the output of the discriminator of the receiving radio and the input to the DSP development system. The objective was to maximise the dynamic range of the DSP for the purpose of improving timing recovery and to ensure that the threshold level obtained was close to optimum. Before any calculations could be performed, the characteristics of the discriminator must be known so that the deviation settings at the transmitter may be converted to received voltage limits. The characteristic of the 455kHz discriminator is shown in Figure 6.4.

The Volts/kHz characteristic of the discriminator was found to be 0.1151 Volts/kHz, from Figure 6.4. The received signal limits, shown in Figure 6.4 take in to account the worst case mobile offset of ± 3 kHz (c.f. section 4.6 in [53]) and assumes that the deviation is set to ± 3 kHz. Maximum dynamic range was achieved by forcing the signal limits shown in Figure 6.4 to occupy the ± 5 Volt ADC input range used with the DSP system.

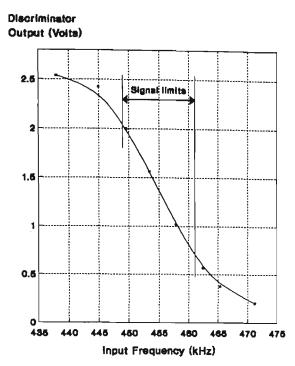


Figure 6.4 455kHz IF discriminator characteristics

Once DC coupling is achieved data can be passed through the system, however the frequency offset between the transmitted and receiver center frequencies would result in a DC offset which would effect the threshold levels used for bit decisions. This DC due to carrier offset must be removed without effecting the signal, which is achieved by obtaining the maximum and minimum extremes of the data signal then obtaining the average which is the carrier and discriminator circuit offsets. These maximum and minimum extremes are also used to calculate half bit offset thresholds and decision feedback coefficients which are again transmitter dependant (Hz/Volt of the VCO) and receiver dependant (Volt/Hz of the discriminator). This is illustrated by the switch and find limits box in Figure 6.5.

6.2.1.2 Timing Recovery

Since PMR networks are based on SCPC configurations, there are only two possible ways to implement timing recovery; i) Transmitting a separate synchronising signal (pilot clock), which would greatly increase the complexity of the GMSK generation. This is not feasible since the main criteria is to implement the system using existing Analog radio sets with minimum modifications, ii) Self-synchronisation, which uses a non-linearity to extract timing information from the received data signal. The latter will be adopted as the transmitter/receiver complexity is reduced and no RF power is wasted by transmitting a pilot clock. Figure 6.5 illustrates the timing recovery within the GMSK Demodulator functional diagram.

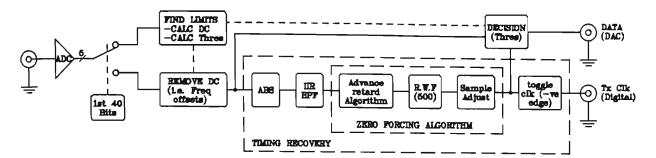


Figure 6.5 GMSK/GFSK demodulator

Clock Extraction

Figure 6.6 shows the clock extraction performance both simulated and practical, of two different non-linear elements, absolute value and square law. Measurements were performed in the frequency domain after the appropriate non-linear processing. The level of the timing spectral component above the modulation noise floor was obtained, hence the relative performance could not be improved by simple gain insertion. The simulated results clearly show that Absoluting has up to a 8dB improvement over Squaring of the signal for small GMSK BT products. Since the final implementation will use a GMSK BT < 0.3 these gains will have significant effects on the timing recovery performance, especially when noise is considered.

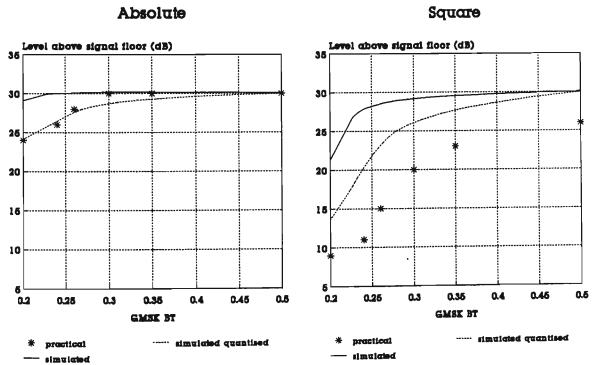


Figure 6.6 Extraction of symbol timing tone. Level of the tone above the modulation noise floor for different GFSK BT products.

The overall performance of the practical extraction with 32 level quantisation showed severe degradation when compared to the unquantised simulated performance. This indicates that squaring is more sensitive to the number of quantised levels used, which agrees as expected that if X represents a number between 0 and 1, X^2 will always be less than X.

The simulated 4 bit quantised values verified these discrepancies were due to the effects of quantisation. The practical Absoluting and quantised simulated Absoluting agreed well. However there was a larger difference between the practical Squaring and the quantised simulated Squaring.

BPF implementation

A sampling rate of four times the baud rate was selected as it simplified the BPF design and allowed a simple zero forcing algorithm to be implemented. Figure 6.7 shows the Z-domain unit circle for a simple BPF with conjugate poles and zeros. A general BPF design program was written to place conjugate poles and zeros in the Z-domain for a given sampling frequency, centre frequency and attenuation with upper/lower cutoff frequencies. The required attenuation specification was met by placing the pole a given distance from the unit circle. The purpose of the zero was to control the ringing (impulse response length of the filter) by placing it as close as possible to the pole but still achieving the attenuation specification.

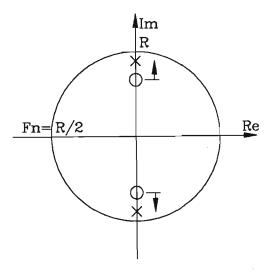


Figure 6.7 BPF representation in the Z-domain

Ringing is a major problem which may cause the BPF to simply oscillate at the centre frequency. This is a direct function of the Q of the BPF. A high Q would be advantageous as the BPF could free wheel the timing clock between packets (if a packet system is adopted)

and very deep fades. However, if the Q is too high, the timing recovery may never achieve phase lock as the received clock spectral component may be outside the BPF. On the other hand, if the Q is too low, the tolerance to noise is diminished which also causes a non-locking scheme.

The specifications of the IIR BPF used are shown below:

 $f_s = 40000 \text{Hz} \quad f_{cent} = 10000 \text{Hz}$

Atten = -20dB with

 $f_{iower} = 8000Hz$ $f_{upper} = 12000Hz$

The following pole/zero locations were found:

POLEs= $0.968426\Delta \pm 90^{\circ}$ ZEROs= $0.526016\Delta \pm 90^{\circ}$ (6.1) This gives the following difference equation:

O(n) = I(n) + I(n-2)0.2767 - O(n-2)0.9378(6.2)

with a series gain of 0.078253 (-22.13dB) to achieve 0dB passband gain.

Hence, selecting the sampling frequency as four times the bit rate simplifies the difference equation as the poles and zeros both have angular positions of $\pm 90^{\circ}$.

Zero Forcing Algorithm

Full timing recovery requires phase lock with the transmitting clock so that the slippage of the optimum eye across the signal, which would cause poor BER performance, does not occur. Assuming there is a frequency offset between the transmitter and receiver reference crystals which is the practical case, the sampling must be advanced or retarded so that the optimum sample point always occurs at the zero crossing of the recovered timing wave at the BPF output. This forces the receiver to be in phase lock with the transmitter, hence eliminating slippage of the eye. This work will use a modified version of the zero forcing algorithm presented in [55].

The top sinewave in Figure 6.8 shows the aim of the zero forcing algorithm, which is to force the 3^{rd} sample to the +ve going part of the sinewave. Initially the four sample numbers are assigned to consecutive samples and are remembered over the baud. After the 4^{th} sample one of four states are possible (a1,a2,b1 & b2 in Figure 6.8). The 'a' states are within $\pm 90^{\circ}$ of the required position only requiring fine tuning (small sampling phase adjustments are performed). Advancement and retardation of the sampling phase for the 'a1' and 'a2' cases are shown in Figure 6.8 respectively.

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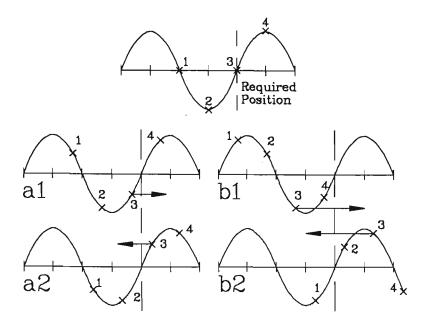


Figure 6.8 Zero forcing method

For the 'b' cases in Figure 6.8 the error is greater than $\pm 90^{\circ}$. Using the proportional control for 'a' would result in poor initial locking delay which is important in a system using a packet structure. For the 'b1' case the next sample is assigned a '4' which causes the 'a1' case in the next baud. For the 'b2' case, the next sample is assigned a '2' which will force an 'a2' case in the next baud. In this way a 90° step correction is obtained when the phase error is greater than 90°. Therefore, by considering the 'b' cases, rapid zero forcing can be achieved thereby reducing the length of packet timing preambles. Hence increasing overall data throughput.

The sampling phase advancement and retardation was implemented using the timer interrupt on the TMS320C25. The two main registers used for timer period control are the 16 bit timer (TIM) and period (PRD). The TIM register is decremented once every instruction period, which is 100nS on the TMS320C25. Once zero is reached, the TIM register is reloaded with the PRD register.

Calculations for mean value which should be loaded into the PRD register is shown below:

Design for a bit rate of 10kb/s (actual 10M/1024=9.765kb/s)

- i) Bit period $(1/R) = 102.4\mu S$
- ii) Sampling period with $4*R = 25.6\mu S$
- iii) With 100nS cycles \Rightarrow a count value of 256 cycles

The advancement/retardation of the sampling phase for a bit rate of 10kb/s was

achieved by decrementing/incrementing the PRD register. This adjustment occurred after the 4^{th} sample and then held for a whole baud. This was adequate at this bit rate. However doubling the bit rate (19.531kb/s) resulted in no phase lock since the timing adjustments were too course. The problem was overcome by direct adjustment of the TIM register of the current sample rather than adjusting for all samples of a baud. This adjustment was still relatively coarse. However phase lock was achieved by slight movement of the POLE in the BPF away from the unit circle (i.e. reducing the BPF Q).

Once noise was introduced into the system, the output of the BPF would not be a pure sinewave. Hence the above algorithm would be sensitive to added noise. A Random Walk Filter (RWF) was included to increase the noise tolerance of the zero forcing algorithm and also to allow finer control over the sampling phase. The RWF allowed the retardation/advancement of the phase once over many bauds as opposed to a correction per baud. The RWF is fed with the raw advance/retard pulses from the zero forcing algorithm. If the total count number of advance or retard pulses¹ exceeds a given threshold then the actual sampling phase is appropriately adjusted, and the counter reset to zero.

Optimum eye position

Once phase lock with the transmitter clock is obtained, good BER's can only be achieved if one of the four samples of the baud coincide with the optimum sampling instants. Generally the delay between the timing recovery system and the decision is unknown, with the required optimum sampling point located between the real samples. In these cases a polyphase interpolation filter or a change in f_{cent} of the BPF would be required to compensate for these sub sample delays. However, the practical implementation adopted here required no such additional processing as the conventional (and half bit offset) sampling points were very close to existing samples.

¹ These advance and retard pulses can cancel each other out.

6.2.1.3 Detectors

The first four schemes outlined in section 5.3 were implemented on the TMS. The complexity versus performance based on the simulation programs written in 'C' and simulated performances, did not warrant the practical implementation of MLSE (processing power was also a concern). Some of the schemes require feedback coefficients based on modulation dependant parameters, specifically Conventional with DFE and the proposed new scheme (FEDFE). Since the gain stage was adjusted to always achieve $\pm 2.5V$ signal limits into the DSP hardware, it was a simple matter to scale this 2.5V limit by the appropriate g(T) for a given GMSK BT.

After implementing the four schemes in the TMS assembler the number of instructions for each scheme was found (excluding timing recovery), see Table 6.3.

SCHEME	# instructions	
Conventional	16	
Convent+DFE	21	
Half bit offset	23	
New (FEDFE)	32	
MLSE ⁺	73	

 Table 6.3 Number of instructions per scheme

NOTE: ⁺ estimate only

6.2.2 Packeting System

The previous section examined the uncoded data stream implementation which implies a continuous stream of bits. This section will look at structuring the data in an organised way so that error recovery can be more logically performed. Decomposing the data stream into isolated entities (packets) would allow rapid retransmission of any received bit error streams. In this section the design of a possible packet structure will be presented. However the packet controlling protocol will not be investigated. The purpose of the Packeting system is not to produce the most optimum throughput but to demonstrate that a packet system, with appropriate coding, can combat the deep fades in a mobile radio environment with a relatively strong received signal.

6.2.2.1 Packet Length

The criteria used here to determine the packet size will be based on obtaining one deep fade per packet. An assumption of reasonable received signal strength is made, so that the system is running very close to the irreducible error rate (i.e. $E_b/N_o \approx 40$ dB). The time between deep fades can be calculated if the carrier frequency and maximum vehicle speed are known:

$$V_{\text{speed}} = 100 \text{ km/hr}$$
 fc= 480 MHz
 $f_d = \frac{100/3.6}{3e8/480e6} = 44.4Hz$ (6.3)

The absolute worst time between deep fades is 11.3mS $(1/2f_d)$ and due to the nature of the fading process this would be a very low probability event (i.e. Pr(level<-40dB)=0.01). If a raw bit rate of 20kb/s is assumed, then this implies a packet length (R/f_d) of 225 bits with a maximum one deep fade per packet. This would be adequate for commercial PMR users and the majority of emergency services.

6.2.2.2 Packet Structure

The packet can be divided into 3 groups: i) Timing recovery preamble, ii) Frame synchronisation code, and iii) Error Coding. The length of the timing preamble is dependent on several factors namely, the longest time delay between two packets, the Q of the BPF in the timing recovery and the locking delay of the zero forcing algorithm also part of the timing

recovery. As the delay between two packets is unknown it can be assumed the system is operating at maximum throughput.

The timing preamble length was based on the longest locking delay of the zero forcing algorithm² at a bit rate of 20kb/s with the BPF excited. The longest zero forcing delay occurs when the 3rd sample of the 'b' cases in Figure 6.8, where the 3rd sample is greater than 90° from the required position. This would require one whole bit plus a 12.5 μ S time correction, which decodes to 125 sample phase corrections. This implies a minimum of 33 timing preamble bits (RWF not included). Designing for 64 preamble bits will allow for cold synchronisation. Generally, the synchronisation system is warm, thereby guaranteeing timing lock.

Frame synchronisation is required for correct decoding of the data and as a separator from the timing preamble. This was implemented by passing the incoming bit stream through a 16 bits shift register, where after each bit received the Hamming distance between the register and the frame word was calculated (see Figure 6.9). Under no fading conditions, this 16 bit frame synchronisation code (sync-code) should be selected to maximise the Hamming distance between the sync-code selected and all possible versions of the shifted sync-code. A computer program generated a 16 bit synch-code of 149Dh, giving a distance of 9 (assuming timing recovery for 1/2 bit offset GMSK detection, constant 1's).

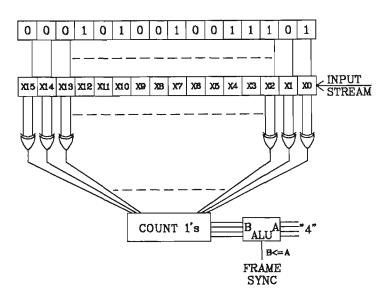


Figure 6.9 Frame synchronisation technique

² The zero forcing algorithm which was based on an update every sampling instant, through the use of the 'PRD' register.

Under fading conditions a frame sync may be corrupted (in a burst nature), hence an ideal Hamming distance of zero will not be possible in many cases. Therefore, a threshold must be found between 0 and 8, inclusive. This was found by observing the Hamming distance of all possible received sync shifts corrupted by a burst of 6 bits (all combinations of the 6 bit burst were used, 0 to 31). A simulation program showed that the distance of 9 was reduced to 5, hence the threshold should be set so that frame synchronisation is achieved once the distance is ≤ 4 . A 6 bit burst was used, since approximately 6 bits were observed to be corrupted at a bit rate 20kb/s (see Figure 6.10) when a test carrier with no modulation was passed through a RF Rayleigh Fader.

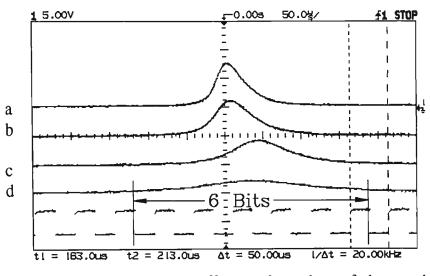


Figure 6.10 Typical effects of a deep fade at the discriminator output of an unmodulated carrier (four examples a-d)

Using the same criteria as above the data section of the packet, based on the tolerance of a 6 bit burst error, can be designed. The number of bits actually available for data per packet is (225-64-16)=145 but this will be significantly reduced once coding is adopted. Reed-Solomon (RS) coding would be the best to apply here as this is designed for burst errors. To achieve a 6 bit burst error capability would require an RS with G(31,19) [56]. Work has been done on block error rates and burst lengths [44] which showed that sequence detection (Conventional+DFE, MLSE and FEDFE) with bit-interleaving (to disperse burst errors) and FEC, out performs symbol-by-symbol detection (Conventional and Half bit offset) with FEC, at least in an AWGN channel. Due to the ease in implementation and understanding a simple block code (7,4) [56] with bit interleaving, to minimise the effect of burst errors, will be adopted.

The (7,4) block code fits very well with 140 available coded bits and can have various configurations as shown in Figure 6.11. Figure 6.11a shows a 7 bit wide coded nibble which implies a depth of 20 (burst capability of 20) to achieve the 140 bits. Using the two block structure (b) there is a burst error capability of 10 (6 is required), but a fade in each block is acceptable. Hence the maximum tolerable fading rate is doubled by using this option. The former structure is suitable for slower fading rate situations (low carrier frequencies) where the fade duration can be long. The latter is more suitable for the fast fading situation and is used in this work.

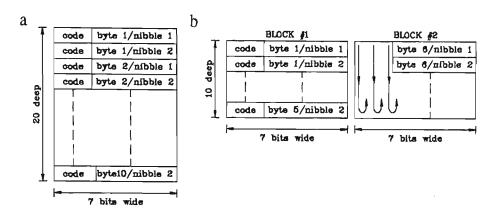


Figure 6.11 Coded data structure

Block#2 in Figure 6.11b illustrates the bit interleaving. The block code works horizontally, while the actual transmitted bit stream reads top to bottom then left to right. So, while the burst errors are less than 10 bits, there is no overlapping of errors within a 7 bit coded nibble. Hence the single error correcting ability of a (7,4) code is not exceeded. This is adequate for high received signal strengths in that the irreducible error floor of the system is removed. However, for signals with low $E_{\rm v}/N_{\rm o}$ the system performance would be inadequate. Hence it would be the function of the protocol (using for example CRCs) to improve the system. An alternative to detection and correction for very deep fades would be the use of erasure information which could be generated from the demodulator by checking for received signal exceeding known deviation limits.

64bits (all 1's)	16bit 1s	t block	of 7	'O bits	2nd	block	of	70	bits
Timing Recovery	Frame Sync.	Forv	vard	Error	Corr	ected	Dati	a	

Figure 6.12 Structure of packet

The final packet structure is shown in Figure 6.12. After considering the packet overheads and the coding of data, the throughput was only 36.4% (80 bits real data/220 bit packet) with reference to the un-coded data rate through the radio channel.

The timing recovery preamble within a packet had two different forms depending on the detection scheme used; i) Constant 1's for the half bit offset technique with an external differential encoder, ii) Alternative 1's and 0's for conventional and all other schemes. The frame sync and coded data were the same for both techniques.

6.2.2.3 Implementation of packet system

Assuming that a transparent RS232 link is a main criteria, this would require a packet assembler/disassembler (PAD) at both the transmitter and the receiver. For a half duplex implementation some form of memory base is required. A full duplex system would require two channels hence two frequency synthesisers resulting in poor utilisation of spectrum allocation and also the need for the transceivers to be completely redesigned. To achieve effective two way communications a protocol would have to be developed for synchronisation of Rx/Tx transceiver modes at the near and far ends, which would have to be optimised to take into account change-over delays.

Although this full system would be useful in demonstrating the potential of digital PMR, time was a major constraint. The implementation will only consider a one way link with packets generated from a ROM look up table, and a 6809 μ Processor used for packet disassembly.

Packet Disassembly

A standard 6809 development board was used for packet disassembly at a bit rate of 20kb/s. The implementation included frame synchronisation, bit de-interleaving, forward error correction and cyclic buffering for the asynchronous output. These functions and processing stages are shown in Figure 6.13.

The search SYNC process would first decide whether timing recovery bits have been received through the use of a Random Walk Filter (RWF) with a threshold set at 10. Once this RWF was triggered, the system shown in Figure 6.9 is initiated. The whole process of shifting, XORing, counting the number of bits in error then deciding for correct synchronisation would require the majority of the power of a CMOS 6809 running at 2MHz

with a bit rate of only 10kb/s. Therefore rates greater than 10kb/s would not be possible. The alternative implementation required two 256 byte tables which had pre-calculated Hamming distances for the frame sync codes. Once the new bit was shifted, the sum of the indexed data given by the LSB and MSB of the shift register produced the required Hamming calculation. This approach significantly increased the maximum bit rate at which frame synchronisation could be achieved at the expense of cheap memory.

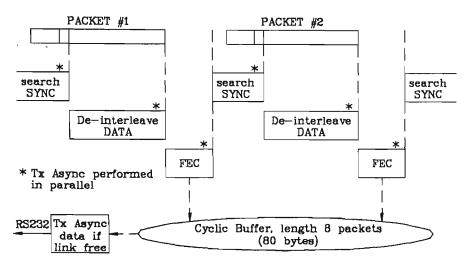


Figure 6.13 Packet disassembly functions

The de-interleaving was performed with nested loops-the inner performed 10 times and the outer 7 times. This implementation had a minimum effect on the maximum bit rate. The FEC, as indicated in Figure 6.13, is very critical as the FEC may finish after the 16 bit frame sync word of the next packet which would result in a lost packet. Therefore all efforts must be made to reduce the FEC processing. The same concept used for frame synchronisation can be adopted here. This time using a 128 byte table with 4 bit data (7 bit coded data to 4 bit actual translation). Once the 2 blocks of coded data were converted to 10 bytes of actual data, they were stored in a cyclic buffer of 80 bytes length to allow for instantaneous input/output rate inconsistencies caused by RS232 handshaking or program operation.

I/O considerations

The highest priority of the 6809 software is to receive a bit from the GMSK demodulator subsystem, since any lost bits from the demodulator would render the packet useless. The transmission of an asynchronous RS232 byte is a secondary priority (any minor delays would be taken up by the output cyclic buffer). A standard 6809 board supported a VIA which could have been utilised for packet detection. However as this could not give an

indication of packet bit overruns, the VIA was replaced with a simple bit capture and an overrun detect circuit, which could be read or reset by addressing the existing VIA port addresses (see Appendix E). This was an indispensable asset in error control for determining the state of the packet disassembler during development.

Choices had to be made to whether interrupts or polling techniques where adopted for the packet receive data and asynchronous transmit data. Polling for the packet data was a must due to processing load at a bit rate of 20kb/s caused by the overhead in using interrupt processing. An analysis of polling and interrupt driven ACIA (see Appendix C) also showed polling to have a higher limit on the maximum Packet Bit rate (PBR). The possible limitations to maximum PBR are shown in Table 6.4.

Limitation Cause	PBR _{max} (kb/s)		
Cyclic buffer overrun	21.1		
Polled ACIA	22.1		
INT ACIA	18.7		

Table 6.4 Sources of limitation to PBR_{max}

Table 6.4 shows that using the Polled ACIA technique the maximum PBR=21.1kb/s due to cyclic buffer overrun, whereas the interrupt ACIA technique the maximum PBR=18.7kb/s due to interrupt overheads.

6.3 Performance Measurements

The performance of a digital transmission system is presented as BER versus E_b/N_o . However in the mobile radio environment, the fading rate is another parameter. The performance will first be considered in an AWGN only channel for comparison to published material (to verify measurement technique) and to the simulations performed in Chapter 5. Measurements will then be presented for a channel with a one path Rayleigh fader with AWGN, using various modulation configurations to observe the BER performance. The implemented packeting system was evaluated for its deep fade (burst) error correction capability.

6.3.1 Uncoded data stream performance

To obtain consistent and stable measurements the equipment setup is of critical concern. The setup used (Figure 6.14) minimises leakage from the transmitter to receiver which is critical when the RF input to the receiver is small as when operating close to the receiver noise floor. Also, the receiver had to be within the RF shielded room to minimise exterior noises. Signals radiated and received from/to the transceivers were further minimised with the shielded cases of the transceivers. The transmitter was set to a carrier of 147.325Mhz ensuring that there were no local amateur repeaters. The output power of the transmitter was set to 1 Watt (30dBm), which was totally shielded and attenuated down to \approx -53dBm on entry to the RF shielded room.

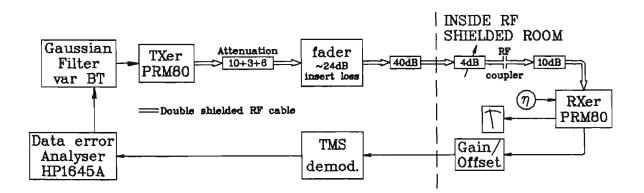


Figure 6.14 Equipment setup for BER measurements

An initial problem was a 50Hz loop which caused the received signal to be superimposed on a very large 50Hz signal due to separate mains circuits used inside/outside the RF shielded room, (In actual situations this never becomes a problem as the transceivers are electrically isolated with battery operation.) This was minimised significantly by installing a GPO on the same circuit as the shielded room. However there was still enough 50Hz to introduce a bit error floor even without noise injected into the system. This problem was overcome by building an RF coupler based on a small capacitance, with double shielding to reduce leakage.

White noise with a bandwidth of 50MHz was AC coupled into the radio before the 21.3MHz IF filter (injection of noise at 455kHz IF produced poor performance due to the poor spurious out of band rejection of ceramic filters). After the IF filters an RMS voltmeter (HP3400A) was required to measure the signal+noise (S+N) and noise (N) levels. These are shown in Figure 6.15. The performance of the system from the 21.3MHz IF stage to the final bit stream at the DSP is compared to published material and simulations performed in Chapter 5. When the fading performance is measured it will be later shown that the method in Figure 6.15 has a limitation due to the 60dB gain between the GMSK faded signal and the point to where the white noise is injected.

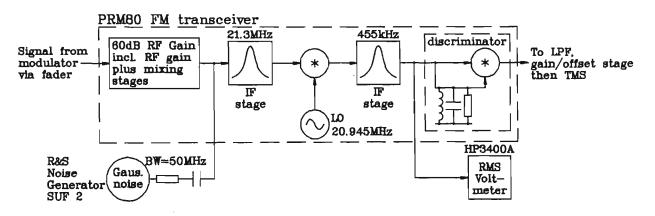


Figure 6.15 Signal to Noise ratio measurements

The bit error rates (PN maximal length= 2^{16} -1) as a function of SNR [(S+N)/N-1] was measured. The SNR was converted to E_b/N_o which is a standard comparison used in digital communications systems. The method for obtaining N_o is different to that shown in section 5.4 as we can not directly determine the Watts/Hz of the noise. However, knowing the noise power at the output of the IF filter and the equivalent noise bandwidth (B_N) of the IF filter, N_o can be obtained. The equations for the SNR to the E_b/N_o translation are shown below:

knowing, $\left(\frac{S}{N}\right)_{R} = \frac{S+N}{N} - 1$ (6.4)

$$E_b = \frac{S}{R} \tag{6.5}$$

$$N_o = \frac{N}{gB_N} \tag{6.6}$$

$$\frac{E_b}{N_o} = \frac{S}{R} * \frac{gB_N}{N} \equiv \left(\frac{S+N}{N} - 1\right) * \frac{gB_N}{R}$$
(6.7)

There are two unknowns in Equation 6.7, the passband gain (g, insertion loss) of the IF filter, which can easily be measured ensuring correct input and output matching impedance for the crystal filter. B_N is the bandwidth of an ideal filter which would allow the same noise power to pass as the practical IF crystal filter. The B_N was found using the frequency characteristics of the filter obtained from a Network Analyser and numerical integration (see Appendix F).

The final BER values were obtained by averaging six runs. Equation 6.7 was used to obtain the appropriate scaling required to find $E_{\rm b}/N_{\rm o}$. Once the curves were plotted, any points which deviated from the general trend would be measured again. Carrier drift was significant at high SNR as error rates in the order of 1e-5 require at least 1e6 transmitted bits which could take 100 seconds at a bit rate of 10kb/s. So periodic re-running (to calibrate the maximum/minimum limits) was required to ensure acceptable threshold levels and DC removal. In an actual situation this calibration could be synchronised with the start of a packet.

6.3.1.1 Timing Recovery Limits

Timing recovery is satisfactory with a received RF power of -110dBm. This is equivalent to a voltage of 0.707μ V but this also assumes that there no RF noise received (only self noise of the receiver is introduced). As the fading performance results will indicate, the timing recovery was adequate for an $E_b/N_o\approx$ 4-5dB at R=9.765kb/s while an $E_b/N_o\approx$ 1dB was obtainable at 15.625kb/s, with the latter including a RWF. Fading was not a major problem in affecting timing recovery performance provided the timing loop has a very large time

constant, and still allows lock within the timing preamble of a single packet.

Much work could have been performed in optimising the timing for high noise conditions through modification of the following timing recovery dependant parameters: i) BPF design, both gain and pole/zero positions; ii) RWF limits and phase correction increments. It was shown in both simulated and practical conditions that absoluting the signal is superior to squaring the signal, in achieving clock extraction from the signal.

6.3.1.2 AWGN performance

The BER curves in Figure 6.16 show the AWGN performance for the system with an input RF level of -60dBm (causing no saturation to the signal at the output of the 455kHz IF filter). The system parameters were GMSK BT=0.26, R=10kb/s, deviation of ± 2.5 kHz, predetection BT=2.0 and a post-detection filter BT=0.4. This configuration was selected to minimise the ISI interference introduced by the IF stage. Only the simplest detection schemes for both the conventional and half bit offset eyes are compared against the equivalent simulated results (showing all schemes reduces the graphs' clarity).

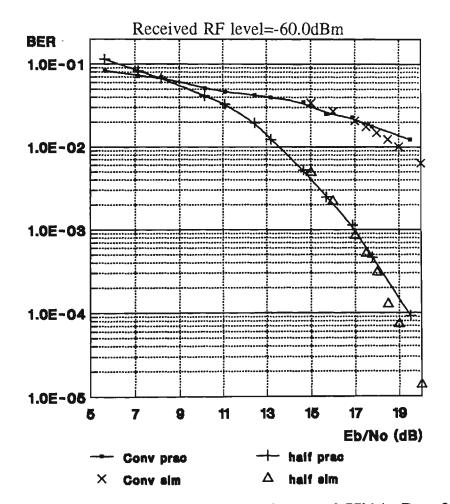


Figure 6.16 Performance of GMSK BT=0.26, R=9.77kb/s, Dev=2.5kHz

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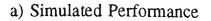
The AWGN measurements were repeated by reducing the received signal (noise no longer added) until the required E_p/N_o was obtained, this effectively uses the self noise of the receiver (assumed to be gaussian) as the distortion to received signal. The purpose of these measurements is to further verify the independence of the E_p/N_o performance to received signal strength, and to estimate the noise floor of the receiver which will be used for fading measurements. The results obtained here showed the approximate noise floor (N_{floor}) of the receiver to be -120dBm.

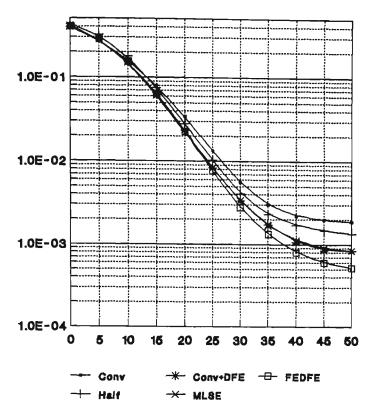
6.3.1.3 Fading Performance

Fading is introduced to the system at RF (147.325MHz) using a single path Rayleigh fading model (see Appendix G). Figure 6.17 shows the simulated and measured performance of a 10kb/s system with wide pre-detection filter to minimise the effect of the IF group delay. Both show similar characteristics in the static fading region ($15dB < E_b/N_o < 35dB$), and similar irreducible error rates across all schemes. The order of preference for selection takes FEDFE, Conventional+DFE, half bit offset then Conventional for both simulated results and practical measurements.

Figure 6.18 shows the simulated and measured performance of a 15.6kb/s system with modulation parameters set to co-exist with the current analog system (satisfies analog ACI requirements). As the GMSK BT is reduced to allow for the higher bit rate performance is slightly worse. While the additional ISI introduced by the modulator and the IF filter degrades the conventional detection scheme to a near useless level (observed in both the simulated and measured results). The New scheme (FEDFE) is shown to have a 1.7dB improvement at BER=1e-2 and approximately half the irreducible error compared to the closest rival, the conventional+DFE scheme. This results is reflected in both the simulated and measured performances.

Both Figures 6.17 and 6.18 show the practical results to have an improved performance over the simulated results, for low E_b/N_o . This discrepancy may be due to offset errors in the I/Q Rayleigh fader which would cause carrier leak (ie. Rician fading).





b) Practical Performance

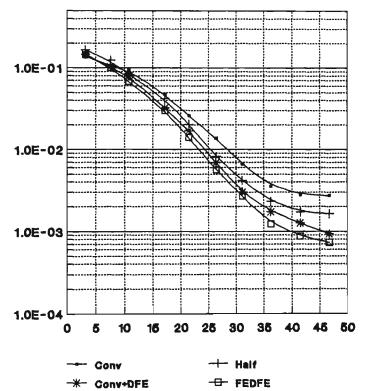
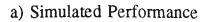
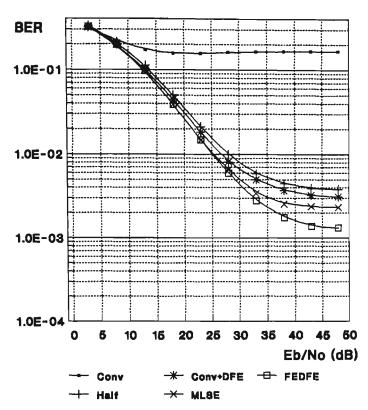


Figure 6.17 Performance with Gaussian filter BT=0.26, R=9.765kB/s, Dev= ± 2.4 kHz, f_dT=0.0064, PreBT=2.0 & PostBT=0.4





b) Practical Performance

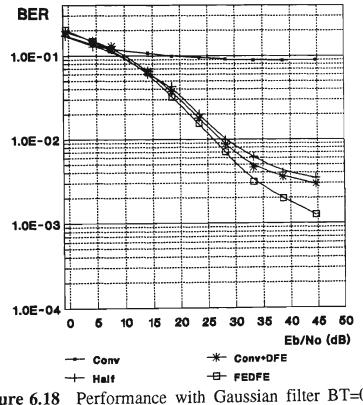


Figure 6.18 Performance with Gaussian filter BT=0.22, R=15.6kB/s, Dev= ± 3.9 kHz, f_dT=0.0064, PreBT=1.1 & PostBT=0.6

6.3.2 Packeting System Evaluation

By observing the errors at the RS232 output (displayed ASCII on a terminal), the performance of the proposed packeting system was evaluated. Although subjective, this will highlight the effectiveness of the coding mechanism in combating deep fades. The performance will be considered at two levels; i) Digital level fading, where the packet generator is connected directly to the 6809 (the transceivers, GMSK generator and TMS are omitted) via a burst error generator, ii) RF fading, whereby the whole system is connected, with an RF fader connected between the transmitting and receiving sets. A full evaluation of the packeting system is not possible as packets are only generated with a lookup table approach which does not allow the BER to be measured.

6.3.2.1 Digital level fading

The packet disassembler was tested using 'bit level fading' - that is, connecting the packet generator to the 6809 via a XOR gate with the other input connected to burst '1' generator (see Appendix E). The test assumed that the signal received would be strong and that every fade is deep, which rarely occurs in practical systems. The bit rate and fading rate could be controlled independently with the measurements made, shown in Figure 6.19. This shows that as the bit rate is increased the maximum fading rate can be increased proportionally. This is expected because the period of the packet decreases and each packet can tolerate up to two deep fades. One effect which is not shown in Figure 6.20 is that the deep fades depth is approximately fixed so for higher bit rates the burst error length would increase. This test looked at a 4 bit error burst for a bit rate of 10kb/s, so at 20kb/s a burst error of 8 bits should have been used.

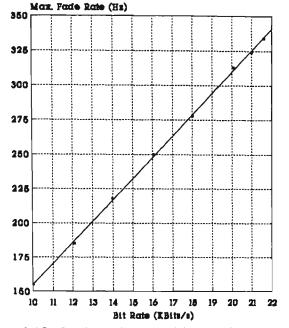


Figure 6.19 Packet disassembler performance with a 4 bit burst error.

6.3.2.2 RF fading

The coding was considered to be adequate when only a few errors per received screen were observed (80*24 characters \Rightarrow 15360 bits \approx 2 seconds of data when coding is considered @ R=15.625kb/s). Modulation with the following parameters was used: GFSK BT=0.22, R=15.625kb/s with a deviation ±3.9kHz (Raw bit rate performance as shown in Figure 6.19). With no noise added the fading rate was increased for each scheme (except Conventional which was too poor), until significant errors occurred. These results are shown in Table 6.5.

SCHEME	Maximum Fading Rate (Hz)		
Half Bit Offset	140		
Convent+DFE	150		
NEW (FEDFE)	180		

Table 6.5Maximum fading rate "noAWGN"

More realistic results are shown in Table 6.6, where the fading rate was set at f_d =40Hz (f_d T=0.00256) and the gaussian noise was increased until decoding errors were observed. Comparing the Eb/No values in Table 6.6 with the measured performance, the system operates with a BER≈1e-2. The performance improvement of Conventional + DFE over Half Bit Offset is $\Delta E_b/N_o$ =0.6dB, while the FEDFE scheme has a 1.2dB gain in E_b/N_o over Conventional+DFE.

SCHEME	Noise (Vrms)	E _b /N _o (dB)
Half Bit Offset	0.00065	26.1
Conv+DFE	0.0007	25.5
NEW (FEDFE)	0.0008	24.3

Table 6.6Coding performance with $f_d T=0.00256$,BER=1e-2.

6.3.3 Conclusion

The new FEDFE scheme gives overall system performance gains of 1.2dB when Conventional+DFE, or 1.8dB when the Half Bit Offset schemes are adopted as the data detector in the system.

Figures 6.17a and 6.18a shows the MLSE simulated performance follows the FEDFE curve for $E_b/N_o \leq 25$ dB. For $E_b/N_o \geq 25$ dB the performance gradually improves for the FEDFE scheme until the irreducible error floor is reached, where the improvement is constant. In both cases the MLSE floor was found to be approximately 1.9 times worse than the new FEDFE. Considering these observations, if MLSE had been implemented the E_b/N_o in Table 6.6 would have been approximately the same as FEDFE (i.e. 24.3dB). Since MLSE is twice the complexity of FEDFE, in terms of number of instructions, see Table 6.3. It can be concluded that the new FEDFE scheme gives the best performance versus complexity tradeoff.

7.0 Conclusion

This work has shown the feasibility of medium/high speed data transmission on narrowband radio channels. The selection of Gaussian filtered FSK modulations such as GFSK and GMSK allowed the use of existing analog PMR radio equipment with minimal modification. This was a requirement of the project.

Chapter 2 discussed GMSK modulation. The modulation was simulated in both the frequency and phase domains. Eye diagrams were produced for various GMSK BT products to compare with published material. Once GMSK generation was fully understood and confirmed satisfactorily through simulations, hardware was developed for both frequency and phase domain generation. Practical spectrums, both at Baseband and RF, confirmed the successful generation of GMSK through comparisons with theoretically derived GMSK spectrums.

Testing the various discriminator based detection schemes, required adequate modelling of the channel distortions (eg. multipath propagation effects). Chapter 3 covered the implementation of GSM's channel model, which is a comprehensive model that considers a variety of terrains and was developed using channel sounding techniques of actual measurements. The time dispersion, introduced at the bit rates achievable in narrowband systems, only produces flat fading effects. This was verified by comparing the complex GSM model with a simple and faster operating Rayleigh fader, this showed only small discrepancies in the BER performance of the various discriminator schemes.

Simulations of the various discriminator schemes (Chapter 5) suggest the best scheme to be the FEDFE. This gives the best performance with minimum implementation effort. Explanations are given for sources of the discrepancies between these simulated results and published material (Chapter 4). Simulations of the five different schemes in fading were then performed for balanced comparison. Each of the five schemes experienced exactly the same AWGN, fading and pre-discriminator processing. This extensive comparison is currently unavailable in published papers. Generally, only an AWGN channel and phase equalised predetection filter are considered when presenting a new scheme.

One of the main requirements of this research is to allow the Digital transmission to co-exist with the present Analog PMR. Extensive measurements were performed to obtain suitable modulator configurations to conform with the existing Australian Analog PMR

specifications. These measurements showed that there are virtually an endless number of solutions using the inverse relationship between the GMSK BT product and the deviation of the FM signal for a given bit rate. However the number of possible solutions are reduced once performance indicators, such as eye opening and timing jitter tolerance, are considered.

Chapter 6 examined the implementation/design of the GMSK detector based on the TMS320C25, and presented considerations in developing a simple packeting system. The packeting system minimised the effect of fading, and was based on a 6809 for the packet disassembling. The Bit Error Rates at the output of the TMS320C25 verified that the FEDFE scheme had significant increase in E_v/N_o performance with very little increase in complexity when compared to the Conventional, Conventional+DFE and Half Bit Offset techniques (5dB, 0.9dB and 2dB respectively at a BER=1e⁻², see Figure 6.17b). The packeting system implemented was shown to overcome, at high E_v/N_o , the effect of the very deep fades in a fading channel. However actual improvement at low E_v/N_o was not obtained as time constraints prohibited the implementation of a real time packet generator.

7.1 Performance

The performance of the various schemes in an AWGN channel for both the simulated and practical results show close agreement, see Figure 6.16.

The comparison between the simulated and measured performance in a fading environment is shown in Figures 6.17 and 6.18. The best scheme is clearly evident in all results, that is the new scheme, FEDFE, which gives the best performance followed by Conventional+DFE, Half Bit offset and finally the Conventional detector. The practical performance for $E_b/N_o \le 15$ dB was better than the simulated performance, this was due to carrier leak problems in the hardware fading simulator. Section 6.3.3 concluded that the new FEDFE scheme gives the best performance versus complexity tradeoff.

At high bit rates (≥ 20 kb/s) the conventional scheme was found to have one TMS 'C25 instruction cycle spare. This was inadequate to implement the complex schemes at high bit rates, hence poor performance would be achieved due to the lack of processing power. Possible solutions to allow complex schemes at high bit rates, include:

- i) Using 2 sample per baud timing recovery technique
- ii) Using TMS320C50 with existing timing recovery

Due to the 'C25 processing limitations and the unsuitable internal architecture (when

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Chapter 7

compared to a standard μ P, given the same task) for the packet disassembling process, the final system utilised a multi-processing architecture. A separate 6809 μ P was used for packet disassembly. This system implementation was tested at a bit rate of 15.6kb/s with processing loadings of 78% (for conventional, or 80% for FEDFE) and 74% for the 'C25 and 6809 respectively.

7.2 Novelty

This research has presented some previously unpublished material, these are itemised below:

- Extensive comparison of five detection schemes, in a mobile fading channel, based on a discriminator detector transceiver. With <u>real</u> IF filter modelling, i.e. including the phase and group delay effects.
- A new discriminator detector, the FEDFE, was developed with equal MLSE performance and reduced complexity (hence allowing faster bit rates to be achieved when compared to MLSE).
- Optimisation of the Pre/Post discriminator filtering for both AWGN and fading channels. This shows that in a fading environment, the I&D used in published material (to simply analysis) does not optimise the BER in a fading environment.
- A methodology was developed to design GFSK specific parameters to meet the current Analog PMR ACI requirements. These parameters included selection of deviation, the GFSK BT product and bit rate, to maximise the eye-opening and timing jitter tolerance but still satisfying ACI requirements.
- Modified timing recovery algorithm [55] to improve timing acquisition for a packeting system (allows reduced timing preambles, hence improved system throughput)

7.3 Future Work

a) Related to the uncoded data stream

- Apply coefficient adjustments for removal of ISI due to the IF filtering stages, applicable for the Conventional and FEDFE schemes. In the AWGN case improvements in the BER for a given E_b/N_o were observed by using BT=0.2 feedback coefficients for a Transmitter with GMSK BT=0.26 at an R=15.625kb/s and large deviation. The ISI introduced by the IF stages caused

the received signal to appear as GMSK with a BT=0.2.

- During some BER measurements there were carrier drifts which caused significant BER degradation. In the laboratory test system, the TMS would be self calibrating with an ideal signal (only once when the program is first run). Systems used in practice would required a more adaptive maximum/minimum finder which can tolerate noise and fading would be required. One possible solution would be to generate a trigger signal from the packet disassember which would activate the find limits algorithm. This would incorporate filtering for both limits to minimise the noise effects. The find limits algorithm would be held once the packet disassembler achieved frame synchronisation.
- Use of erasure information improves the power of coding schemes as a bit can be guaranteed to be in error. Implementation using DSP can be achieved by checking absolute signal limits and generating a pulse to the packet disassembler. However, care should be taken when considering very low E_v/N_o conditions.
- The VCO [54] and discriminator (Figure 6.4) characteristics appeared to be linear. Problems of non-symmetrical eyes (vertical) were noticed. This was due to simultaneous poor frequency offsets between the transmitter and receiver, with modulations of high deviation, pushing the discriminator into the non-linear region. This effect can be minimised for half bit offset using two thresholds found during the timing recovery bits of the packet.
- Development of a ASIC.
- A thorough investigation of 4 level FSK modulation.

b) Related to the Packeting system

- The packet system implemented here, although simple, highlights major issues of concern burst nature of very deep fades for the selection of an appropriate coding scheme, selection of packet length and frame synchronisation code. Evaluation of the statistical behaviour of the burst errors for the various schemes can lead to an objective type solution to the packet design.
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Appendix A

CPM Generator schematics

- CPM generator schematics
- DC coupling/gain schematic
- Reconstruction filter schematic

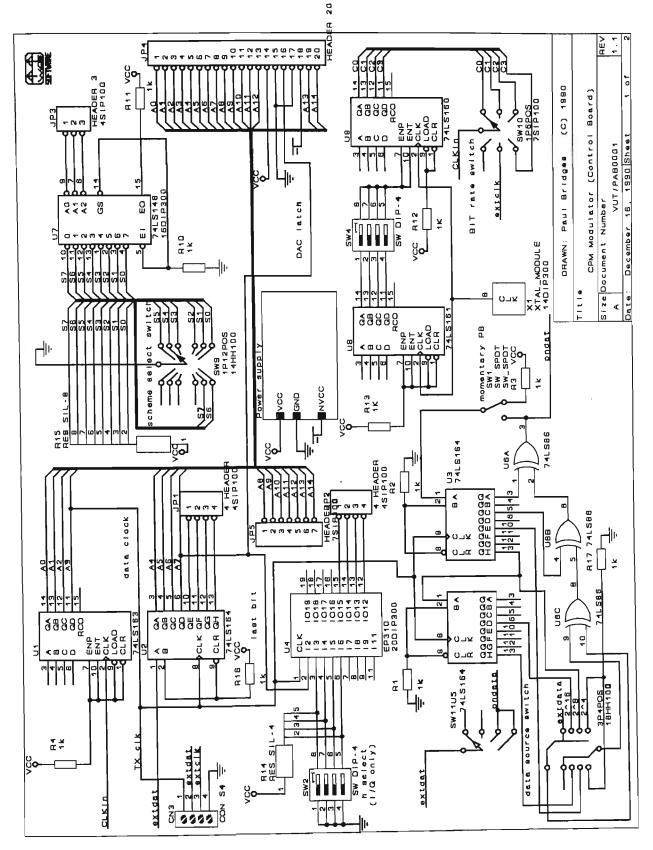


Figure A-1 Main Board (General CPM generator)

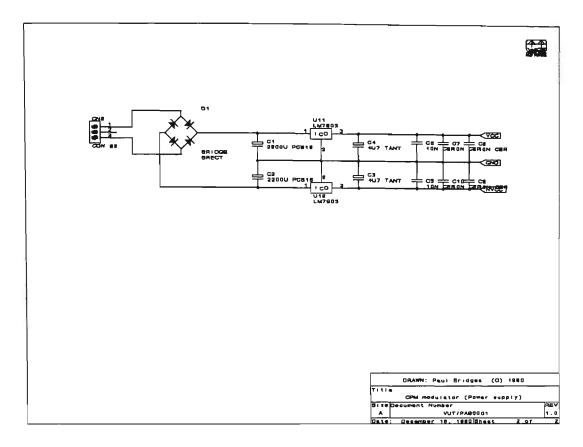


Figure A-2 Main Board (Power supply)

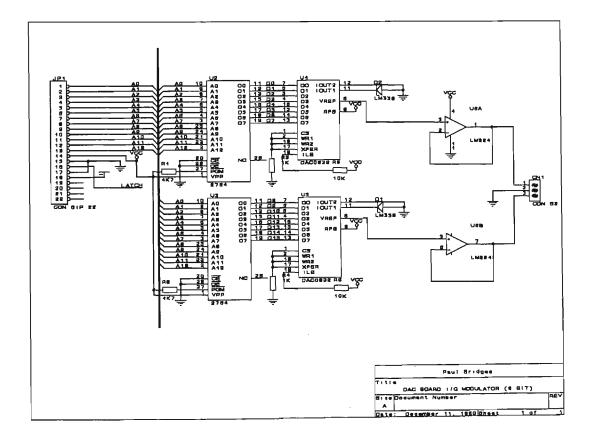


Figure A-3 Two channel 8 bit DAC board (I&Q generation)

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Appendix A

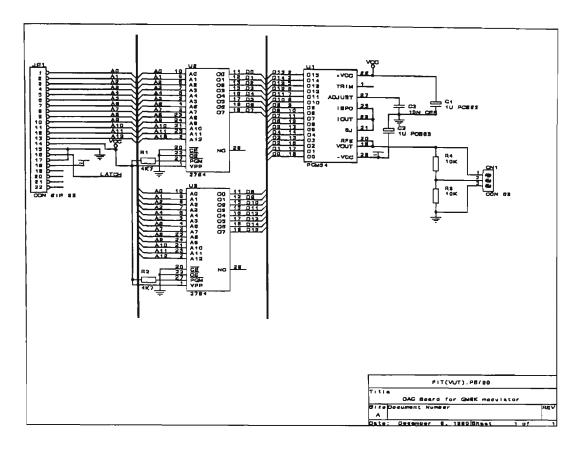


Figure A-4 One channel 16 bit DAC

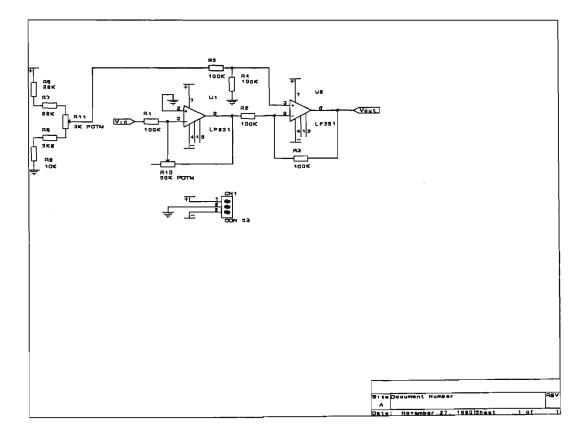


Figure A-5 DC shifter gain circuit

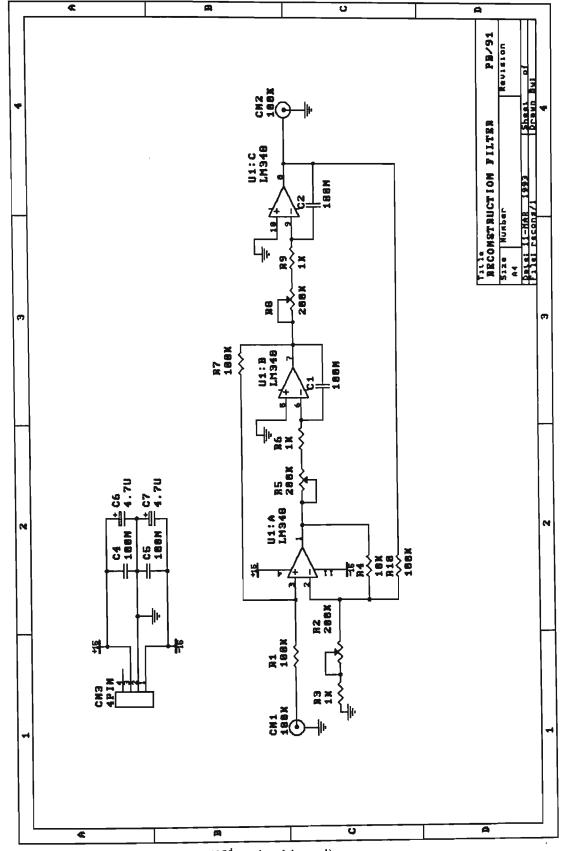


Figure A-6 Reconstruction filter (2nd order biquad)

Appendix B Digital ACI measurements

This appendix will present the measurement procedure used to obtain feasible filtered FSK to co-exist with present analog PMR systems. This is an extract of a report on "Adjacent channel measurements" for the Fast Data Project dated January 1991 (VUT Footscray) [54].

Procedure

i) The equipment was set up as shown in Figure B-1.

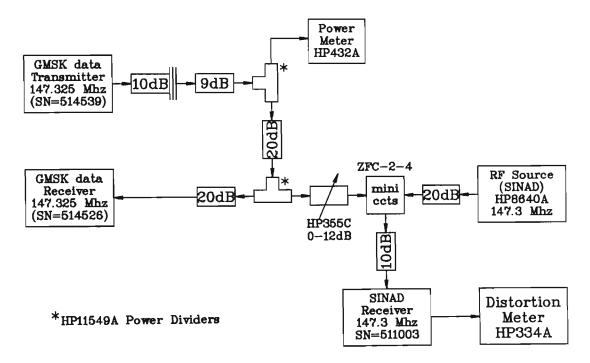


Figure B-1 Equipment set-up used for the Digital ACI measurements.

- The RF source is first connected to a frequency counter and adjusted to give 147.3000Mhz center frequency.
- iii) The RF source was then connected back to the coupler and set to generate a 1000Hz FM signal. The RF level was reduced to -40dBm, and the receiver volume set to give 0.9 Vrms. (reading \approx -37dB SINAD)
- iv) The RF signal level was reduced until a SINAD of -12dB was obtained. (generally -86.0 dBm)
- v) Assuming a 50W base station and we require $10\mu W$ (safety margin), the

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Appendix B

required adjacent channel rejection is -67dB. The power meter measurement was -5.2dBm.

-85.17-20-(level) = $-67 \implies -38.17$ dBm required adjacent power

-4.8-20-6-atten = $-38.17 \implies 7.37$ switched (7dB used)

{-4.8dBm power meter, 20dB fixed, 6dB power splitter}

The levels are now set such that 10μ W adjacent channel leakage occurs when an additional 3dB SINAD is measured (i.e. -9dB signal and noise distortion, of 1kHz test signal).

- vi) The deviation¹ in the data channel is set to 4kHz, GMSK BT products of 0.20,0.22,0.24,0.26,0.28 and 0.30 were selected, the bit rate for each was increased until -9dB SINAD was measured. The bit rate, eye openings and jitter were all noted.
- v) Steps ii) \rightarrow vi) were repeated for deviations of 3.5,3.0,2.5,2.0,1.5 and 1.0kHz.

Important notes

- The center frequency of the 1000Hz test signal. (Absolute accuracy of the PM6668 frequency counter was in error by +500Hz)
- ii) RF source/Receiver drifts during measurements (Source may have drifted by up to -1kHz from 147.3Mhz during step vi), in section 4.1)
- iii) Reference set were not used:

Receiver for adjacent tests	-	PRM 80 V B0
		SN=511003
GMSK Transmitter	-	PRM 80 V A9
		SN=514539
GMSK Receiver	-	PRM 80 V A9
		SN=514526

- v) Warm up period for all equipment ≈ 4 hours.
- vi) Readings of SINAD distortion are not very objective at such small received signal levels.

¹ The deviation was set while transmitting, symmetry about center frequency was checked by transmitting continuous streams of 1's and 0's.

Plotted results

There are three graphs for both conventional and half bit offset eyes (see Figures B-4 to B-11):

a) 'bit rate' VS 'eye opening'

- 'eye opening' is the eve opening in absolute mVolts, for comparison of tolerance to static fading. Figure B-2 shows the sections measured for both conventional eye and half offset eye opening.
 - A bit rate can be selected, the curve crossing furthest to the right gives the largest eye opening, a corresponding BT product can be obtained.

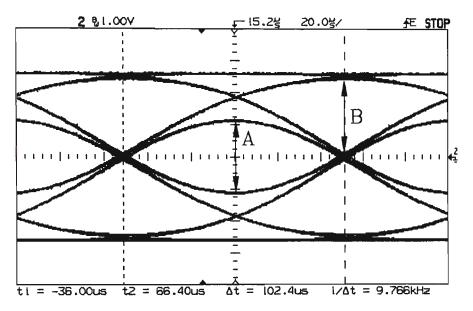


Figure B-2 Eye opening measurements

- b) 'deviation' VS 'eye opening'
 - Using the eye opening and BT product obtained from a), the required deviation can be obtained.
- c) 'bit rate' VS '% jitter'
 - '% jitter' is with reference to the bit interval, gives measure of parameters for timing recovery. Figure B-3 shows the sections measured for both conventional eye and half bit offset jitter measurements. Note that the half bit offset results are based on a non-symmetrical eye, for ease of measurements.
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- Using the required bit rate and BT product from a), the amount of timing jitter tolerable is found. (NOTE: There are not many points on the jitter graph for the conventional eye, as negative eyes are not open, and even perfect timing recovery would not help the BER, if a single symbol decision is made.)

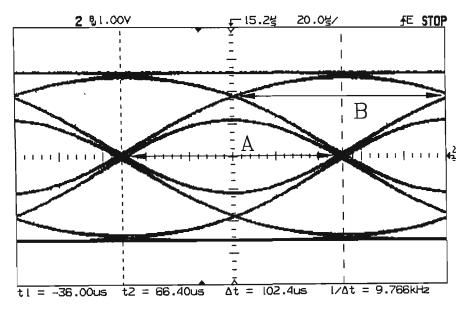


Figure B-3 Timing jitter measurements

conventional

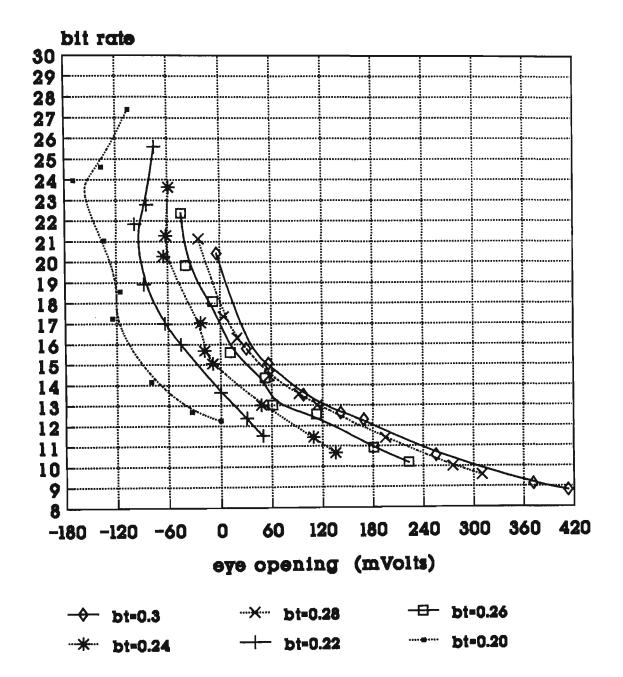


Figure B-4 Bit rate VS eye opening (Conventional)

deviation 6.5 6 5.5 5 4.5 4 3.5 3 2.5 2 1.5 1 -180 -120 -60 180 240 300 360 420 0 60 120

conventional

eye opening (mV)

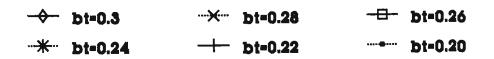


Figure B-5 Deviation VS eye opening (Conventional)

conventional (jitter)

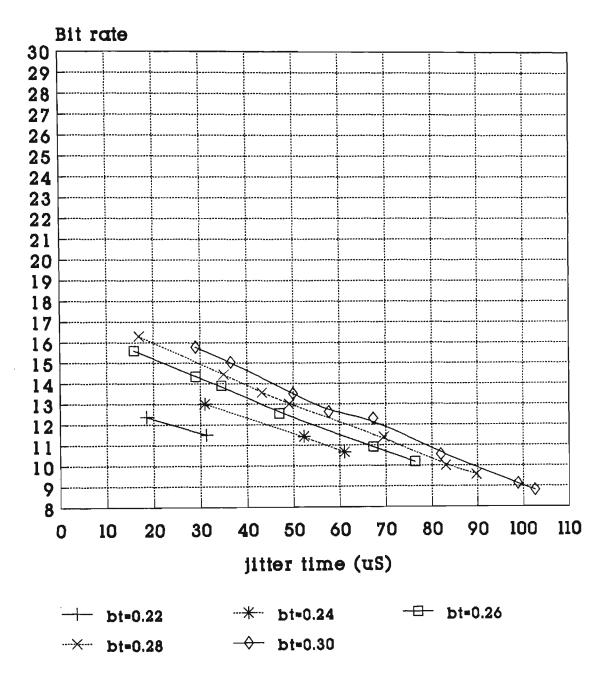


Figure B-6 Bit rate VS Absolute jitter (Conventional)

conventional (jitter)

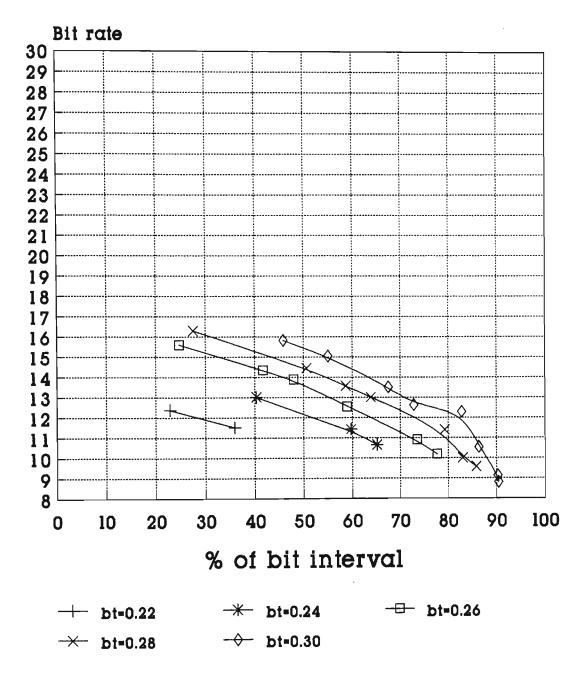
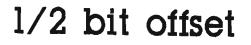


Figure B-7 Bit rate VS % jitter (Conventional)



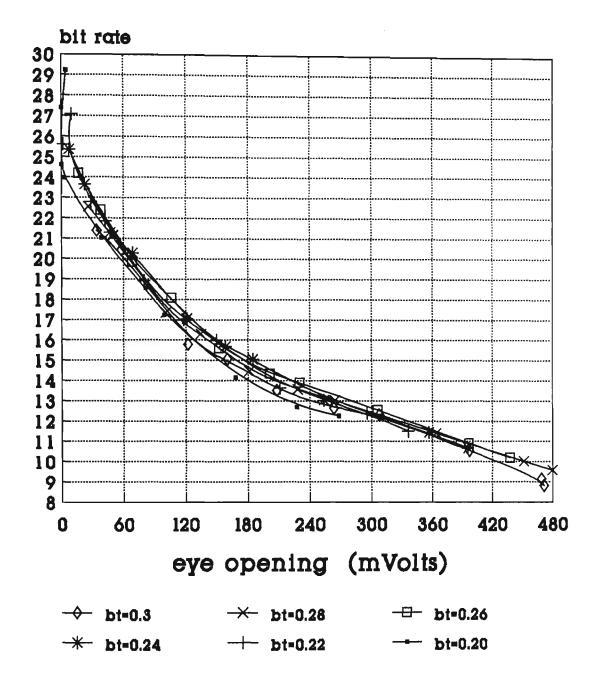


Figure B-8 Bit rate VS eye opening (1/2 bit offset)



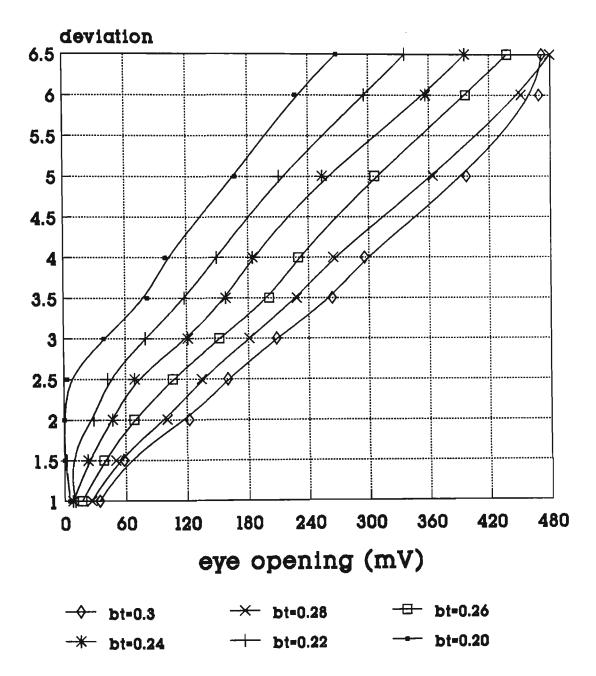


Figure B-9 Deviation VS eye opening (1/2 bit offset)

1/2 bit offset (jitter)

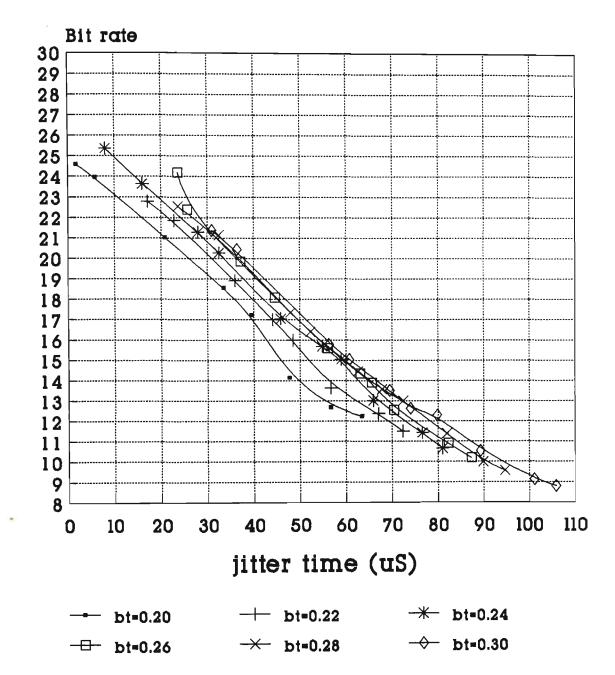


Figure B-10 Bit rate VS Absolute jitter (1/2 bit offset)

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1/2 bit offset (jitter)

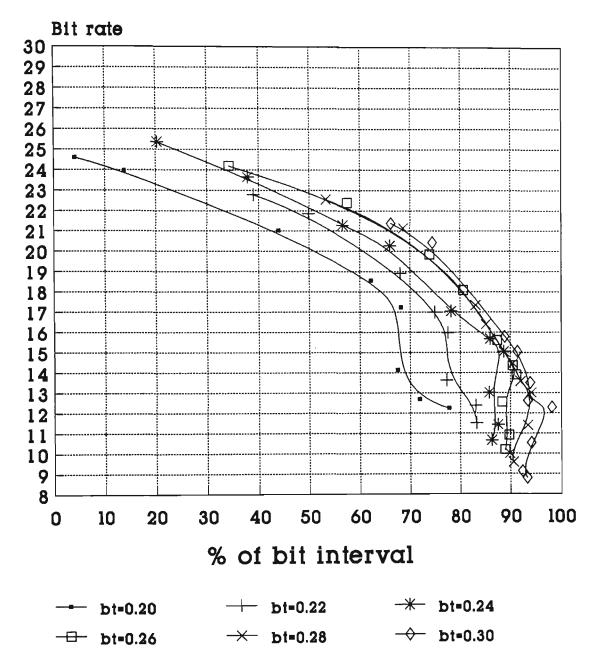


Figure B-11 Bit rate VS % jitter (1/2 bit offset)

Appendix C

Analysis of Packet Disassembler Limitations

Interrupts could only be employed for the RS232 output, as asynchronous data is transmitted over ten times less often as packet bits are received. Some preliminary investigations showed that a bit rate of 20kb/s (2Mhz μ P clock) would only allow 43 cycles free for processing when interrupts are used, as opposed to 78 cycles free with a polling technique (based on packet bit data received with a VIA). When the ACIA was free to transmit new data it would generate an interrupt. If the cyclic buffer was empty and dummy data was not transmitted, this would cause the ACIA to generate continuous interrupts, which wasted time, resulting in received packet bits overrunning. Transmitting dummy data is not a feasible solution as the RS232 would not be transparent. Hence, transmission of RS232 data was re-designed utilising a polling technique.

The blocks labelled with a "*" in Figure 6.13 signify that as packet bits are received the ACIA is checked for availability to transmit data. The algorithm first checks if the ACIA is free to transmit the next byte in the cyclic buffer. Whether this occurs or not the algorithm sits waiting for a bit received flag (D1 of VIA1 @ \$E100). A bit overrun is checked through D2 of VIA1 ("1"=>overrun occurred). If an overrun occurred then the letter 'B' would be transmitted to the serial port, the error flag address would be marked appropriately and the program would halt. The data would be read from D0 of VIA1 and then reset by writing to the same address.

Packet Disassembler limitations

The performance and limitations of the proposed packet disassembler will now be reviewed. The packet bit rate limits can occur due to any of the following;

A cyclic buffer overrun. To ensure this does not occur the RS232 rate ≥ modem rate (assuming a zero wait time between packets).
 Assuming RS232 set for 9600,7,e,1+1 bit start, 7+1+1+1=10
 ⇒ 960 char/sec = 7680 b/s (8*960)

Hence, the maximum packet bit rate = $7680/0.364^{1} = 21.1 \text{ kb/s}$

ii) The FEC decode and copy to cyclic buffer processing overlaps the frame synchronisation of the next packet.

Time (FEC decode) + Time (Copy Buffer) $\leq (64-20)^2 * 1/(\text{packet bit rate [PBR]})$ (560 cycles + 213 cycles)/2.5e6 $\geq 44 * 1/\text{PBR}$

 $PBR*309.2\mu S \le 44 \implies \underline{PBR}_{max} = 142 kb/s$

iii) Frame synchronisation search must be performed once per received bit interval.

 $1/PBR \ge (cycles for frame sync)/2.5e6$

The Cycles for frame sync depended upon whether polling/INTs were used for the ACIA.

a) Polled ACIA required 60 (frame sync search) plus 53 (get bit) cycles.

PBF_{max}=2.5e6/113=<u>22.1kb/s</u>

b) Interrupt driven ACIA required an additional 52 cycles for the interrupt overheads.

PBF_{max}=2.5e6/165=<u>15.1kb/s</u>

Measurements showed that the bit rate for iii b) could be much higher than the 15.1kb/s calculated but still slower than the polled ACIA technique of iii a). This occurs because; i) The time between interrupts is 1/960 (with ACIA 9600 baud). During this time several packet bits would have been received, ii) The software can sample the bit at any time during the interval as external latching exists. Both these effects allow the instantaneous processing for ACIA interrupt to be averaged out over several bits. As long as all of these delays are absorbed (see Figure C-1) before the next interrupt, there will never be a bit overrun. Hence, it can be said, the interrupt ACIA can never work at the bit rate possible by the polled ACIA method. A correct calculation for iii b) will be shown below:

¹ Throughput of packet system, see section 6.2.2.2.

 $^{^{2}}$ 64 bits timing - 10 bits RWF - 10 bit burst error, with no delay between packets.

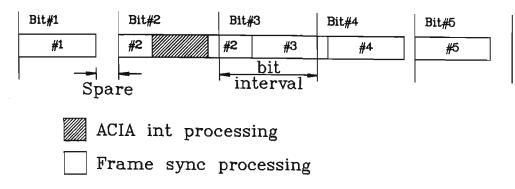


Figure C-1 Frame synchronisation processing

'Spare' processing per packet=(1/PBR - 131/2.5e6)

Time between ACIA interrupts = 1/960 (assuming 9600 baud)

Total additional processing time available for processing (PBR/960)*'Spare'

The following inequality ensures no cumulative effect will result in received bit overruns:

$$\left(\frac{PBR}{960}\right)\left(\frac{1}{PBR} - \frac{131}{2.5e6}\right) \geq \frac{52}{2.5e6}$$

Solving for PBR gives $PBR_{max}=18.7$ kb/s which agreed closely with experimental results, and as expected is less than the polled ACIA technique (22.1kb/s).

Appendix D

Frame Synchronisation Word

The packeting system adopts bit interleaving to combat burst errors caused by fading. Bit interleaving requires synchronisation which is achieved by detection of a frame synchronisation word with a sliding correlator. The frame synchronisation word is selected to maximise the Hamming distance between itself and all possible shifted versions of itself, as described in section 6.2.2.2. Possible frame synchronisation words found through simulation are shown below:

Optimim packet sync sequences

-											
Possible packet sync. seq. for a 10 bit sync, giving dis=5:											
	16	1 A	22	25	26	29	2C	2D	2E	32	34
	36	3A	48	4A	4B	4D	4E	52	53	56	59
	5B	5D	64	65	69	6A	6D	72	85	86	8B
	8E	95	98	9D	A3	A6	CB	D0	106	10C	10D
	116	118	11B	11C	123	131	185	216	21A	225	229
	232	286									
Possib	le pack	et sync.	seq. fo	r a 11	bit sync	, giving	g dis=6	•			
	53	59	6B	97	9A	A4	A7	C9	11A	219	247
Possib	le pack	et sync.	seq. fo	r a 12	bit sync	, giving	g dis=7	:			
	A6										
Possible packet sync. seq. for a 13 bit sync, giving dis=7:											
	A6	CĂ	D6	116	12E	135	13A	14C	14D	159	166
	19A	1B5	22D	234	24E	25D	26B	293	29D	325	42E
	48E	4A3	51 B	865	8CB	10A6					
Possible packet sync. seq. for a 14 bit sync, giving dis=8:											
	299	2B3	32B	335	527						
Possible packet sync. seq. for a 15 bit sync, giving dis=8:											
	299	2B3	329	32B	335	353	359	4B9	4C5	4D1	4D4
	4EB	513	519	527	532	533	537	54C	564	566	567
	599	59A	62B	645	64A	654	656	657	66A	66B	675
	6B3	735	859	8B4	8D3	8DA	8E9	939	947	959	967
	A13	A1B	A4C	A4E	A4F	A93	C95	C97	10D1	10EB	1143
	1161	123A	1287	128F	12A3	144F	2167	2173	218B	2197	22C6
	4299	42B3	432B	4335	4527						
Possible packet sync. seq. for a 16 bit sync, giving dis=9:											
149D											

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Possible packet sync. seq. for a 17 bit sync, giving dis=9: 946 9CA 9D6 A32 A36 A46 A62 A65 A6E A72 A76 ACD ACE B1A B3A B46 B4E C56 C6A CA5 CA6 149E 14CB 14CD 14DD 1531 1536 1593 1596 1**59B** 15A6 15B3 166A 18AC 192B 1956 195**B** 196A 19AB 19B5 1A66 4A1D 4A3B 4C2B 50DD 513D 522E 82CE 834E 8396 5076 8586 865C 8872 8963 911E 9171 1149D Possible packet sync. seq. for a 18 bit sync, giving dis=10: 19A9 3257 45A7 474B Possible packet sync. seq. for a 19 bit sync, giving dis=10: 19A9 1A99 1AB3 2353 1953 2359 2519 254C 2567 2573 2635 26A7 26AC 26B1 26B9 272B 2735 2753 2759 28C9 2967 4E5D 5139 519A 51B4 51C9 51DB 5247 5267 5279 5317 5593 5626 58EB 594E 599A 5A67 5A99 622D 625D 8A5C 8AC3 8AD3 564F 8B43 8B47 8B4E 8B4F 8B96 8D0B 8D2E 141B1 1464F 14C1D 190F5 20B39 20CAC 20D19 20D39 20D73 243A3 24717 28363 2864F 28793 289C3 419A9 43257 445A7 4474B Possible packet sync. seq. for a 20 bit sync, giving dis=11: 4D4E 52E6 5316 62B6 64AE 962E 1169D 1172D 128E9

Performance of frame synchroniser

The interleaving and coding combination used in this packet system was implemented to overcome the deep fades that exist in a mobile radio environment. Figure 6.10 showed typical burst error lengths of 6 bits. The synchronisation word and data coding were both designed to eliminate this burst error. A 16 bit frame synchronisation word was selected (149D) giving a Hamming distance of 9. The decision that frame sync is achieved when the calculated Hamming distance ≤ 4 gives the following synchroniser performance, for the given BERs:

Prob of mis-detection and false-alarm for frame syncronisation sync word length n=16 allowing for r=4 bit errors

BER	Pr(mis-detect)	Pr(false-alarm)
5.000e-01	9.616e-01	3.841e-02
2.000e-01	2.018e-01	3.841e-02
1.000e-01	1.700e-02	3.841e-02
5.000e-02	8.573e-04	3.841e-02
2.000e-02	1.162e-05	3.841e-02
1.000e-02	3.984e-07	3.841e-02
5.000e-03	1.304e-08	3.841e-02
2.000e-03	1.372e-10	3.841e-02
1.000e-03	4.328e-12	3.841e-02

Appendix E

Packet related schematics

a) Packet generator

The schematic of the packet generator used in this work is shown in Figure E-1. The packets are pre-calculated (incl. timing preamble, frame sync word, data interleaved and FEC using block codes) stored in EPROM, then read out from one of the eight streams available (D0-D7). Each stream consists of a message using 8 packets with 10 characters per packet.

b) Burst error generator

To evaluate the performance of the packeting system against burst errors due to fading the burst error generator shown in Figure E-2 was constructed. This circuit is capable of generating a burst error of length between 1 and 15 bits. The burst errors can be single shot or at a repetitive rate (eg. fading rate) independent of the data rate.

c) Packet disassembler hardware interface

This circuit was designed to be plug-in compatible with the SY6522 VIA. This interface sets a status flag (D1 at \$E100) when a bit has been received. If the packet disassembler does not service this bit before the next demodulated bit arrives, the bit overrun flag is set (D2 at \$E100). A received bit is serviced by reading D0 at \$E100, then a write to \$E100 which resets the hardware interface.

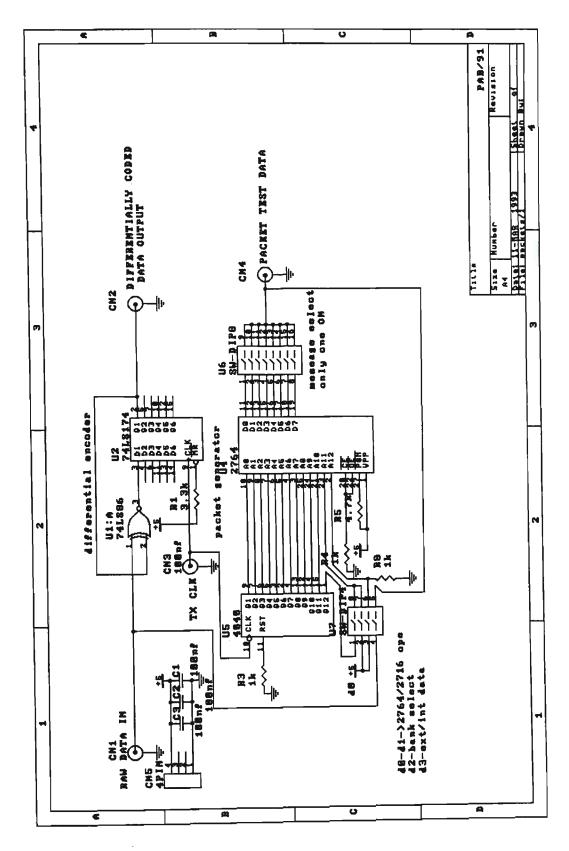


Figure E-1 Packet generator & differential encoder

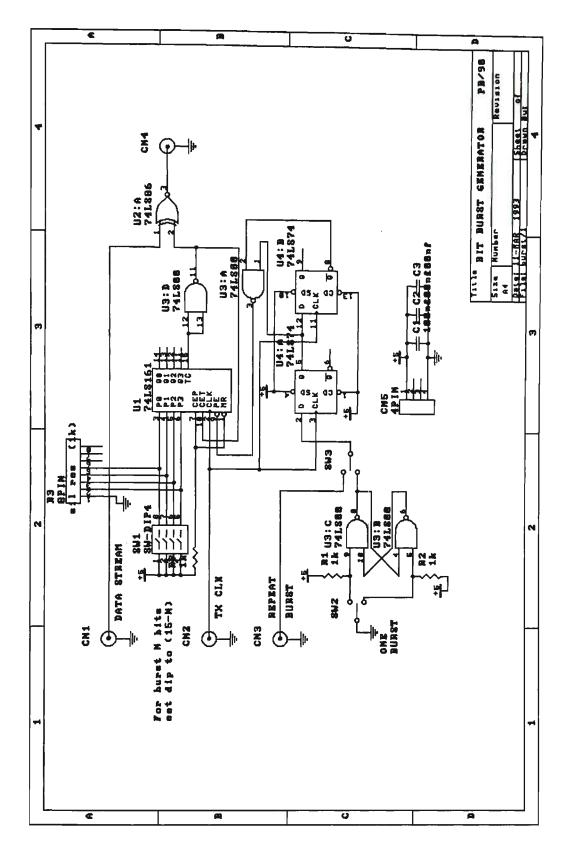


Figure E-2 Bit burst error generator

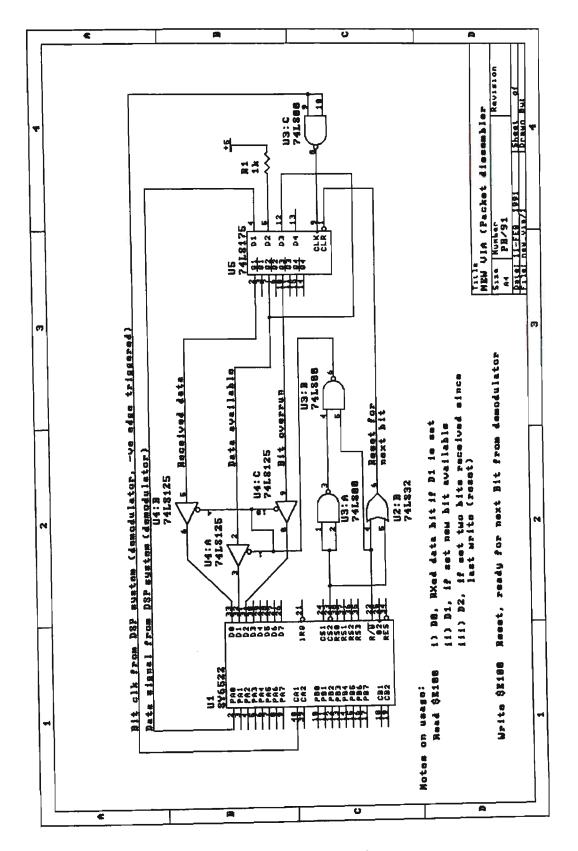


Figure E-3 Packet disassembler hardware interface

Appendix F

IF Noise Bandwidth measurements

To obtain correct scaling of the SNR to E_b/N_o as given by equation 6.7, the equivalent noise bandwidth (B_N) of the IF stages needs to be found. The B_N was found using a GPIB controlled Network Analyser (HP 8753C) to obtain a frequency sweep of the filter under test. These swept points were squared then numerically integrated to obtain B_N . This automated testing to determine B_N was verified using the following procedure for a ceramic filter:

A) A R&S Noise Generator was connected to a 50 Ω power meter, Figure F-1. The voltage source and 75 Ω resistor represent the noise source, with the 50 Ω resistor representing the power meter input impedance. The frequency bandwidth of the power meter was > the noise generator bandwidth. The power delivered to the 50 Ω resistor was -0.5dBm (891.25 μ W).

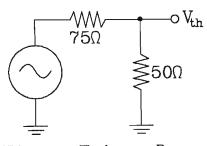


Figure F-1 Power measurement of R&S noise generator (SUF 2)

B) The equivalent circuit in Figure F-1 is now converted to its Thevenin's equivalent circuit.

$$V_{th} = V_{o/c} = \sqrt{891.25 \,\mu * 50} = 211.098 V$$
$$R_{th} = 75 \| 50 = 30 \Omega$$

C) The R&S noise source with a 50Ω resistor to ground, was then connected to a ceramic filter with an input impedance of 1500Ω. The equivalent circuit is shown in Figure F-2 with the additional resistors for the input and output. The input power to the ceramic

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filter is calculated as shown below:

$$Vin = \frac{211.098mV * 1500}{30 + 3000} = 104.504mV$$
$$Pin = \frac{V^2}{R} = 7.2807 \mu W$$

The input noise power spectral density can now be found:

$$\eta = \frac{Pin}{R\&S BW} = \frac{7.2807 \mu W}{6.1e^6} = 1.1936e^{-12} \frac{W}{Hz}$$

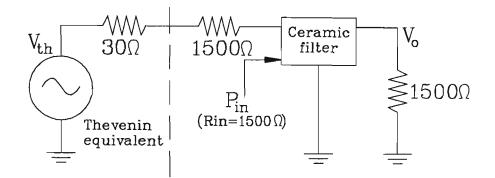


Figure F-2 B_N verification set-up

D) From measurements the value of Vo in Figure F-2 was found to be 0.00575 using a HP3400A RMS Voltmeter. B_N was found to equal 18484.1Hz using the automated process described earlier. The power delivered to the 1500 Ω resistor is:

$$\eta * B_N = 18484.1 * 1.19356e^{-12} = 22.0619nW$$

This would give a voltage across the resistor of:

$$V = \sqrt{P \cdot R} = 0.0057526 V rms \ across \ 1500 \Omega$$

This compares favourably with the measured value of 0.00575Vrms.

numbe SPAN (kHz)		gration points G H(f)^2	G = 401 over Gain (Lin)		Hz)	PBG (dB)	Bn (Hz)	
CFW4	55B M ⁺ ((+/- 6dB BW	V = +/-15 kHz					
50			8.7258301000)E-01 2.8558	524538E+04	-1.184dB	28558	5
60			8.7331542999					-
CFW4	55B P+ (·	+/- 6dB BW	=+/-15kHz)					
50	2.17584	75887E+04 8	8.6933592999	E-01 2.8790	765486E+04	-1.216dB	28790	.8
60	2.18517	02667E+04 8	8.7010193000)E-01 2.8863	235877E+04	-1.209dB	28863	.2
~~~~								
		+/- 6dB BW	,					
50			8.5249634999				28823	.5
60	2.09715	43368E+04 8	8.5314025000	)E-01 2.8813	069656E+04	-1.380dB	28813	.1
CEWA	155C N+ (	′⊥/- 6dB BW	/=+/-12.5kHz	)				
50			8.8609007999		805047E+04	1.0504P	24366	0
50			8.8660583999					
50 60			8.8551634999				24378	
00	1.71200	000000000000	0.0001004777	/L 01 2.4000	505050104	-1.0500D	24500	
CFW455D (+/- 6dB BW=+/-10kHz)								
	•	INTG H(f)	,	ı (Lin)	Bn (Hz)		PBG	Bn
	nt (kHz)	.,		. ,	, , ,		(dB)	(Hz)
1 20		1.318540268	8E+04 8.4824	4828000E-01	1.832514511	6E+04 -1	.430 183	. ,
2 40	1 50 1	.321839627	5E+04 8.478	L494999E-01	1.838978393	0E+04 -1	.434 183	89.8
3 40	1 50 1	1.314668546	5E+04 8.433	5326000E-01	1.848405348	2E+04 -1	.480 184	84.1
4 40	1 50 1	1.341263408	9E+04 8.5268	8860000E-01	1.844731498	3E+04 -1	.384 184	47.3
5 40	1 50 1	.5188991470	0E+01 2.8664	4207000E-02	1.848626078	5E+04 -30	0.853 184	86.3
6 40	1 40 1	1.316804550	5E+04 8.4633	3482999E-01	1.838386788	6E+04 -1	.449 183	83.9
7 40	1 30 1	1.315918021	6E+04 8.4624	4021999E-01	1.837559919	3E+04 -1	.450 183	75.6
8 40	1 60 1	1.3168444234	4E+04 8.456	5428999E-01	1.841402617	'5E+04 -1	.456 184	14.0
9 40	1 1 50 1	1.316597524	8E+04 8.4693	3603999E-01	1.835489085	5E+04 -1	.443 183	54.9
		1.318458365	0E+04 8.4620	0971000E-01	1.841240042	2E+04 -1	.450 184	12.4

NOTEs: * Input/Output of filter swapped to observe effect on Bn (NO EFFECT)
* These characters represent the batch of a specific class of IF ceramic filter [ Notice minimal effect of Bn and Int H(f)²]

#### ii) Typical $B_N$ automated measurements for a crystal filter pair (IF=21.4MHz)

Noise Bandwidth measurements for Crystal Filter 21.4MHz (21F15B) Center Frequency used 21398kHz

Ref	# pnts	Span (kHz)	Bn (Hz)
3	401	40	16081.7
1	401	50	17069.3
2	401	70	16680.9
4	801	50	16537.8
5	801	70	16711.2
6	1601	50	16286.7
7	1601	70	16658.8
9	1601	75	16724.7
8	1601	80	16753.4

Examination of the  $B_N$  for the filters at both the 455kHz and 21.4MHz stages, show that the 21.4MHz IF stage dominates the overall system  $B_N$ .

### Appendix G

### Rayleigh Fading Hardware Implementation

Final system testing was performed utilising a one channel Rayleigh fader based on the concept outlined in section 3.1.2. The hardware implementation of this Rayleigh fader is shown in Figure G-1.

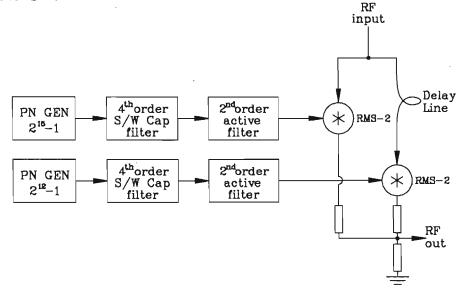


Figure G-1 Hardware implementation of the fader.

This hardware implementation uses two different maximum length PN sequences, to produce two independent uniformly distributed random sources. These random sources are then filtered with 4th order switched capacitor filters (MF-10) with Q $\approx$ 7.3, and a clocked frequency of 200 times the break point frequency. The Q of this filter gives the peaks of a classical Rayleigh fading channel, setting Q too high will cause this filter to ring (i.e. become an oscillator) no longer exhibiting correct Rayleigh statistics. The switched capacitor filter integrates the input signal, this effectively performs the central limit theory producing a gaussian distributed signal. The spectral output of one channel is shown in Figure G-2.

The output of the switched capacitor filter is then passed through a reconstruction filter, which is a  $2^{nd}$  order active filter (based on the LM348) with a -3dB point of 500Hz. Gain and DC offset circuitry is also provided for RF interfacing. The frequency response of the reconstruction filter is shown in Figure G-3.

The outputs from the reconstruction filters are fed to the RF circuitry which performs mixing (with RMS-2 ring modulators) with the RF signal and a 90° phase shifted version of

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the RF signal. As ring modulators are used this method is only suitable for constant envelope modulations. The 90° phase shift was implemented with a length of rigid coax, which length was determined by the carrier frequency (147.325Mhz) and measurements with a time domain reflectometer.

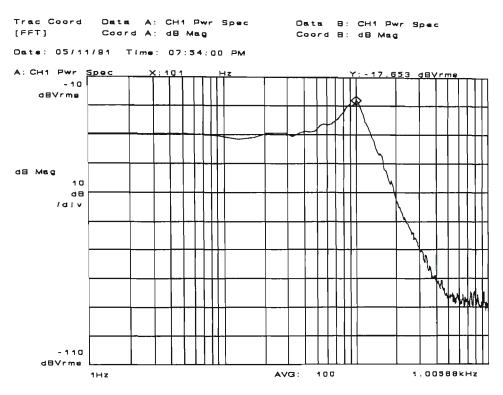


Figure G-2 Baseband spectral characteristics of one channel of the Rayleigh fader, with  $F_d=100Hz$ .

Format

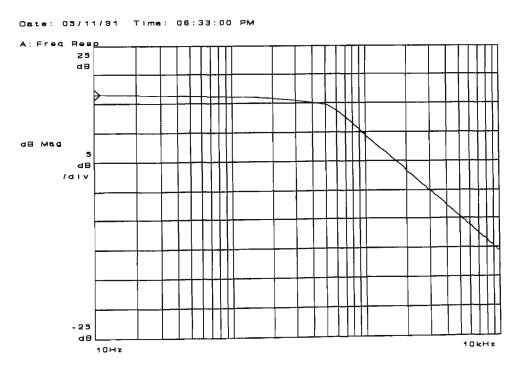


Figure G-3 Frequency characteristics of the reconstruction filter.