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Digital Power Line Communication on EHV Power Lines

A Thesis submitted for fulfilling the requirement of the Degree of Master of Engineering (Electrical)

By:

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Declaration

This thesis contains no material which has been accepted for the award of any other degree or diploma in any university. To the best of my knowledge and belief, it contains no material previously published or written by another person, except where due reference is made in the text of the thesis.

Aleksandar Cosic

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Table of Contents

SYNOPSIS

Digital modulation can be used on PLC communication links to increase system capacity. The improved noise and interference capability of digital modulation can lead to reduced guard distances between co-channel users and can more than offset the additional bandwidth requirements of digital modulation. QAM-16 is proposed as a suitable modulation scheme. In the example given this modulation leads to a modest capacity improvement of 10% when ADPCM is used for voice coding. This improves dramatically with the use of more advanced voice coders. Simulations are performed on a 500 KV line to determine the effect of reflections and modal propagation on the equalization requirements of the modem. The major distortions are caused by the applied filtering within the modem, and the reflections on the transmission path, the later are particularly evident at low carrier frequencies, and when the line lengths are short.

A PLC bandlimited modem, whose frequency is user selectable within the PLC spectrum has been designed and tested. Particular emphasis is placed on the adaptive equalisation algorithm, that is selected in the modem design to combat distortions due to the imperfections of the modem and reflections on the power line. Most of the modem functions were implemented using DSP techniques.

1 Introduction

1.0 Introduction

The rapid development of electrical power networks has increased the necessity to control and monitor the various parts of the interconnected power network. A communication system that is reliable and cost effective is therefore required. A number of systems are used and these include the public telephone network, radio communication systems, fibre optic lines and power line carrier (PLC) communications systems. To maintain an order of reliability at least equal to that of the power system, it is not sufficient to rely completely on one communication system, and in addition, communication system must be maintained, even in the event of a power system collapse. The public telephone system has the advantage of being the least expensive, proven system for voice and data transmission. It exists universally, but has a number of disadvantages namely the electric utility does not have complete control of the system, it is insufficiently secure, and it is unavailable at remotely scattered substations.

Power authorities across Australia, as in most places throughout the world, have found it necessary to install their own private communication networks (although they are reinforced with public telecom networks). Separate networks may be established for different purposes: speech transmission, data transmission, telemetering etc. Power line carrier systems can provide a transmission path for all these systems. Power line carrier communication (PLC) provides [1]:

- fast and reliable communication for both interoffice business and for load dispatching.
- high speed relaying for fast detection of faults, fault locations, rapid clearance of

faults, isolation of faults with the least possible loss of load.

- efficient means for the supervision and control of the interconnected power network.

The major advantages of PLC systems are [2]:

- power lines are good conductors at high frequencies.
- power lines already link the power stations and substations which require the communication facilities.
- the high voltage PLC coupling equipments are still less costly than other means of communications. Economically the cost of PLC communications is reasonable since its shelter and power supply are easily available.
- power lines are highly reliable. High voltage transmission lines are very strong, using large conductors, thus provide a very reliable path for carrier signals. Furthermore, the power line is more reliable for carrier transmission than for power transmission, because in the events of power failure, it is usually possible to maintain a reliable communication operation. Also power lines could withstand such natural hazards as sleet, windstorms, floods etc.

1.1 Existing PLC systems

The principal disadvantage of PLC communications encountered in practice are [3]:

- limitation in the number of the carrier frequencies leading to low system capacity. Yet, there are growing requirements for more digital services; for example telex, telemetry, fax and so forth.
- presence of random and impulse noise, will cause severe interference to the communications equipments. For the protection signalling systems, signalling is required to operate during noisy periods on the line, however, it is equally important that noise does not cause a maloperation. Protection signalling and remote contol circuitry must therefore be very complex.
- need for special expensive protection equipments to prevent hazardous voltages between communication lines and ground. Furthermore the coupling and line trap equipments are very expensive making PLC communications over lines less than

80 Km in length uncompetitive.

- presence of signal reflections and losses due the multipath transmission. Hence PLC is usually used on lines over 110 KV.
- growing incompatibility between modern communications systems which are digital in nature and the analog modulation systems used for PLC communications

We define the power line carrier channel to include the signal path from the transmitting electronic equipment at one terminal, through to the tuning equipment at receiving end, and into the electronic equipment at receiving terminal.

PLC systems use frequencies between 40 KHz and 500 KHz for communications, signalling and protection. Much of this spectrum is available on a shared non-interference basis. The lower frequency is determined by the coupling circuits and line traps, while the upper frequency is set by line attenuation and the need to avoid interference with other users in this part of the spectrum, notably medium wave broadcasting services (navigation radio facilities, radio broadcast services, railway authorities etc). Higher frequencies are used (even beyond 1000 KHz), but only for fault location applications [1].

Frequency Division Multiplexing (FDM) is a technique for simultaneous transmission of many narrow-bandwidth signals over a wideband channel, and it is currently used in PLC applications. Most PLC systems are based on SSB (Single Side Band) analog modulation with a 4 KHz bandwidth. Telemetering, supervision and control signalling generally require a smaller bandwidth of 1 KHz or 2 KHz [3,4]. The terminal equipments are usually single channel units, however 2, 3 and 4 channel multiplexing is sometimes used.

The nominal channel bandwidth is 4 KHz and this baseband is shared between speech and various types of signalling systems (e.g. supervisory control, telemetering and protection signalling). Although the exact baseband frequency allocation varies from manufacturer to manufacturer and application to application, it could be expressed as [3]:

300 Hz - 2400 Hz for speech transmission
2580 Hz - 2700 Hz for telephone signalling

2700 Hz - 3780 Hz for general purpose signalling channels each with a bandwidth of 120 Hz.

When part of the channel is used for signalling in this way, the speech signal is passed through a low pass filter to prevent interference with data channels when they are all combined for the modulation process. The limiting of the speech band in this way reduces the quality of the transmitted speech signal, but the intelligibility is not severely affected and is considered adequate by most users. The 120 Hz signalling channels are not partitioned in the communication terminal equipment, and any number of channels may be combined together as required by the signalling speeds of the various applications.

After the various signals are combined, modulation is performed in two stages and a reduced level of the IF carrier is inserted at the second modulation stage to enable synchronous demodulation at the receiver end. This technique eliminates the need for high accuracy in the IF or RF carrier oscillators and thereby reducing overall costs.

Line traps attenuate the RF signal, and cause that sufficiently large portion of the signal coupled to the line flow in the desired direction. However, it is not sufficient to prevent interference to a carrier signal operating on the same frequency on other lines into the substation [3]. Frequency reuse of the same channel on the different power lines from the same substation is therefore not possible due to this cross-talk coupling (the worst case could be nearly -35 dB). Thus a minimum separation of at least one span (for voice communications) or two spans (for protection signalling) between equipments operating at the same frequency is necessary to minimize the problem of cross-talk interference. Unfortunately this further limits the use of power line carrier, but it is essential for reliable communications. Furhermore, the rapid development of the electrical network has increased the requirement for new communications, control and monitoring facilities, yet the available spectrum is limited. Capacity can only be increased by more efficient use of the spectrum, and any gain in system capacity will reduce the requirement for major capital investments in alternative communication systems.

1.2 Digital PLC System

Digital modulation can provide an improvement in signal to interference ratio which can eliminate many of the cross-talk separation requirements. Unfortunately, there is an increase in channel bandwidth required for digital modulation. Even so, the overall system spectral capacity is still expected to be increased especially with the advent of a low bit rate voice coders now appearing on the market. As a consequence it will be possible to have all the branches into a given substation to receive on the same frequency channel. The same channel could be then used again on any section of the network.

Digital PLC communication has not been developed completely yet, although digital bearers on main communication trunks are established practice. Several projects have investigated the problem [6,7], but until now digital PLC voice communication has not been feasible [1]. However, the recent availability of powerful digital signal processing (DSP) microprocessors should make the implementation of a digital PLC possible.

The objective of the project is to research and develop an efficient means of transmitting digital information through existing wideband analog PLC channels. The first stage of the project involved the investigation and design of a method to encode and transmit voice and data information in a narrow band channel. The second stage of the project involved the development of algorithms to implement the necessary data modulation and demodulation functions. Finally the construction of the limited bandwidth PLC modem was undertaken. The carrier frequency was made user selectable within the PLC range to permit a flexible installation.

One of the main problems of analog PLC system is its sensitivity to various type of interferences which in turn limits its capacity. This is described in further detail in chapter 3, and the benefits of employing digital modulation techniques on PL C channels are investigated in chapter 4. The channel characteristics play an important part in a

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[1] Mr. J. Hayden, Acting Planning Engineer, State Electricity Commission of Victoria (SECV) Communication Section, Transmission Development Department, confirmed that no such commercial digital PLC communication has been developed.

digital PLC communication design. Simulated frequency response data for a typical channel is presented in chapter 4, and is further analyzed in the same chaptrer with a view of estimating the equalization requirements for a proposed PLC modem. The study includes a frequency and impulse response analysis.

The modem design description is included in chapter 5 and in chapter 6. The specification suggested for the project stipulates that the bit rate of integrated voice\data bit stream be 34.4 kbs; that is a bit rate of 32 kbps of ADPCM (standard G 721 - voice information) merged with a data bit stream of 2.4 kbps (control and supervisory signals). Quadrature Amplitude Modulation with 16 points in a rectangular grid constellation (QAM-16) is found to be the the most suitable modulation scheme to satisfy the capacity and signal to interference requirements. The Texas Instruments TMS 320C25 DSP microprocessor was chosen for modem implementation.

2 Literature Survey

Modern Literature on PLC communication is relatively rare, perhaps because the area of application is relatively small and the commercial interest in research and development in this area is limited. One of the traditional references is a book by Podzeck [1], which provides much of the necessary information to PLC users emphasizing international PLC practices. However, substantional changes in available equipment and techniques have occurred, and the book does not address the modern aspects.

Another basic reference is the General Electric PLC Guide [3], which provides general guidance covering the use of power line carrier systems in North America. The reference provides a number of graphs, tables and formulae, so that accurate computations are possible. Some complex formulae have been avoided to free the user from extensive and complicated calculations. Detailed equipment design information is not provided as it varies from manufacturer to manufacturer. The guide provides a detailed analysis of the various causes of interference, and proposes methods by which it can be reduced. Some differences appear in application techniques and philosophies, between North America and Australia, although the basic principles remain the same. These differences plus the related national and international standards give rise to variations in equipments and techniques compared to North American practice. Furthermore, this reference is not an up-to-date PLC guide, and a new revision is still to come.

Sherif and Zahir in their paper [6] examine various communication techniques, discuss advantages and disadvantages of each with a special emphasis on PLC system, and also present recommendations and suggest areas for further research as:

- The effect of loading conditions of the lines on carrier attenuations.
- Comparison of intrabundle communication systems with PLC system performance, and the integrity of intrabundle communication during the faults involving adjacent lines or the other phases of the same line.
- Possibility of utilising a two-way full duplex transmission system to minimize message delay.
- Security problems in communication systems over power lines.

Faulkner [8] provided field measurements of attenuation and group delay on a 41.5 Km 220 KV power line. The reported measurements show the presence of large ripples in the frequency response, which confirm the results obtained from the simulation program used in this project. In addition the author showed the major interfering sources, with their typical levels. This work is strongly related to this project.

Unintentional propagation of PLC signal through and around a power sub-station (cross-talk) has been examined by Morgan in [9]. Morgan describes a new technique for adaptive interference cancellation that has the potential of providing cost-effective interference suppressions. The cancellation is accomplished by an active filtering techniques, making use of existing and in-place PLC components (transmitters, receivers, line tuners, coupling capacitors and line trap), and requires only the addition of the relatively simple RF circuit. A portion of the transmitted (or received) signal is adjusted in phase and amplitude and fed into the external side of the link in order to cancel a relatively small amount of signal that leaks through the line trap. The basic functional block is the adaptive correlation cancellation loop. The method was verified in laboratory, and it seems to be a very promising technique to reduce interference using inexpensive circuitry. However, there are several other practical problems that tend to increase the complexity of the technique such as cancellation bandwidth limitations and reliable sensing techniques. In addition it may be necessary to null out the signals that are coupled onto the other two phases of the three phase lines This techniques has the potential to improve the system performance substationally, if these problems can be successfully overcome.

Signal transmission on PLC channels has been developing through the use of analog SSB modulation techniques. Telemetering, supervision and control signalling generally uses FSK (frequency shift keying) modulation techniques. An excellent

description of currently used techniques in Australia are shown by Rietz [10] who also presented noise measurements for high voltage power line.

The basic theoretical investigations into the propagation of alternating current waves along telephone wires took place at the beginning of this century, and it was regarded as a general aspect of communications. During the same period, the first practical experience with the transmission of the information by means of power lines was gained, even though the fundamental understanding of the transmission mechanism was lacking. The existing analysis could not explain many of the propagation phenomena produced with power lines consisting of several conductors. There are many complicated mutual couplings in a polyphase line.

Transient analysis of a general lossless two wire transmission line as well as a distributed parameter transmission line is described in a number of textbooks of power system analysis, for example, Gross [11].

In the early sixties the requisite mathematical method which permitted more reliable and accurate calculation of the propagation of carrier frequency signals in power lines was developed by Wedepohl [12]. He introduced matrix algebra and fundamental concept of modal analysis to reduce the original n-conductor problem to n individual, decoupled single conductor problems.

Pertz [13] at the same time applied modal analysis to the solution of some PLC problems on a horizontal 3-phase extra high voltage lines (EHV) transmission line, by calculating high frequency modal impedances and current and voltage components on the line. Exact, problem oriented calculation and evaluation was not possible at that time since mainframe computers were not generally available.

A power transmission line is not normally homogeneous throughout its length. The system may be transposed, or the conductor configuration may change at certain points. Also serious problems occur due to tapped lines (tee configuration). Each of the above mentioned problems generally cause additional attenuation due to mode conversions and standing wave effects. Such systems are analyzed in terms of the modal parameters as a number of homogeneous sections as was developed in [14] by Wedepohl.

A graphical method was proposed by Sen [15] to study different coupling arrangements, and it has proved to be effective in assessing PLC channel performance,

especially for non homogeneous lines.

Neredo et al. [16] gave an approximated modal analysis method for PLC system design, which is suitable for implementation on mini and microcomputers. With the advent of powerful mainframe computers, modal analysis became an important design tool in a broad spectrum of PLC applications [17,18]. The simulation model used in this project is mainly based on the distributed parameters of Wedepohl.

Data communication plays a more and more significant role in the efficient running of the power distribution network [19]. Low speed data transmissiong has been investigated and analyzed in several studies [10,20,21,22]. A 300 bit/s convolutionally coded QPSK data telemetry modem is described [23] for EHV power lines (for application precise in Australia for its specific electric network.

Digital signal voice transmission on PLC channels has not been realized yet, although a preliminary study (Burrascano et al. [7]) concerning its feasibility has been underway for some years. In the study a computer aided procedure was presented to evaluate channel response to any input digital signal sequence. The possibility of digital transmission was verified by analysis of the eye diagram. An application which considered a 400 KV three-phase line, gave a valuable result which confirms the effectiveness of the proposed method. However, the use of two level digital modulation involved occupation of a frequency band much wider than the minimum required by an analog modulation. For a fixed line length, the carrier channel frequency response is almost independent of the matching condition beyond a minimal frequency value f_{min}; therefore, the digital transmission must use frequencies higher than f_{min} in order to avoid reflection problems. Since the transmission was carried in baseband, a high pass filter with a cut-off frequency f_{min} had to be included in the system, and proper transmission code had to be used in order to move the maximum power spectral density of the input signal to a frequency higher than f_{min}.

Ramirez et al. [24] gave an accurate qualitative and quantitative definition of the corona noise, and described its undesirable effects on the PLC communication channels. A noise measurement technique, which uses magnetic and electric field sensors placed in the induction field is also described. Burrascano et al. [25] in a later work included a new procedure in a digital simulator, which generate a random time sequence having the statistical characteristic of the corona noise that occurs on transmission line carrier

channels. The method involves the synthesis of an autoregressive filter excited by a white noise generator. A systematic study of the transient responses caused by corona noise allowed evaluation of the bit error rate under operational conditions. The analysis of the corona noise is not considered in this project due to time limitation.

3 PLC Description

3.0 Introduction

This chapter describes the main features of the PLC system. Section 3.1 considers coupling to the power line, and describes the major circuits involved. Section 3.2 describes the spectrum allocation and the frequency division multiplexing used for the PLC channels. The final four sections describe the major problems that influence the performance of the system. Discussed also are the noise level present at the receiver (section 3.3), the attenuation of the line (section 3.4), modal effects (section 3.5) and interference (section 3.6).

3.1 Coupling the power line

In Australia power lines generally operate on 22 KV, 33 KV, 66 KV, 132 KV, 220 KV, 330 KV and 500 KV (EHV lines). The most used constructions are:

- Vertical: three phases above the other.
- Flat construction: three phases horizontal side by side.
- Triangular construction: two phases above the other on one side of tower with the third phase on the other side usually vertically in the middle of the other two phases.

There are several ways for feeding one or more conductors of a 3-phase power line so that signal will propagate down the line, and they are [1,2]:

1. Phase-to-ground coupling
2. Two-phase coupling
3. Phase-to-phase coupling
4. Intercircuit

The difference between two-phase and phase-to-phase couplings is that two coupling capacitors are connected in parallel to the same coupling filter in the former coupling method, whereas they are connected to the separated coupling filters in the latter coupling method. Two phase coupling had been used in early days of PLC

communication, but abandoned because of the excessive loss. Intercircuit is the case where one conductor each of two three phase systems suspended from a common tower is used. Phase-to-phase coupling and intercircuit are more reliable in the event of broken conductors, because carrier signals continue over the other coupled conductors. Phase to ground has been prefered for economical reason, but has a higher loss. Because of the lower attenuation, phase to phase and intercircuit coupling is used where large distances have to be spanned, where a high interference level is encountered. Furthermore phase-to-phase coupling reduces radiation, since the effectiveness of the transmission lines as an antenna decrease as the spacing between the outgoing and return part gets smaller [1,3]. In Australia phase to phase or intercircuit configurations are used (Figure 3.1.1).

Coupling equipment is required to inject the carrier frequency signal onto the line without undue loss, while at same time, protect the communication equipment from the hazards of the normal line voltage and switching surges [1,2].

1) Coupling Capacitors

Firstly there are capacitive voltage transformers (CVT) which can double as coupling capacitors for carrier systems and voltage transformers for protection purposes and secondly there are coupling capacitors dedicated to the coupling of RF signals to the power line. CVTs are normally more expensive than coupling capacitors, hovewer, when CVT can be used instead of the combined purchase of magnetic voltage transformers and coupling capacitors, there is a cost saving. Thus, for the installation on new line, CVTs are more commonly used. The main functions of the coupling capacitors is to block the power current and pass only the communication signal.

The SECV commonly uses capacitors (or CVTs) of the value 6400 pF. Connection to each capacitor from the carrier set is via an unbalanced to balanced transformer network described next.

2) *Line tuning unit*

The line matching unit with the 3 mH inductors (Figure 3.1.2) acts as drains coils for the CVT capacitors. The line tuning unit (coupling filter) unit provides an inductance that can be adjusted such that its reactance cancels the reactance of the coupling capacitors at the carrier frequency, for the maximum transfer of the carrier energy. The tuning elements match the characteristic impedance of the power line (300 Ω to that of the transmitting equipment (75 Ω at the carrier frequency. This unit also splits the signal for coupling phase to phase if required. Connection to carrier terminal equipment, usually indoors, is made with a coaxial cable.

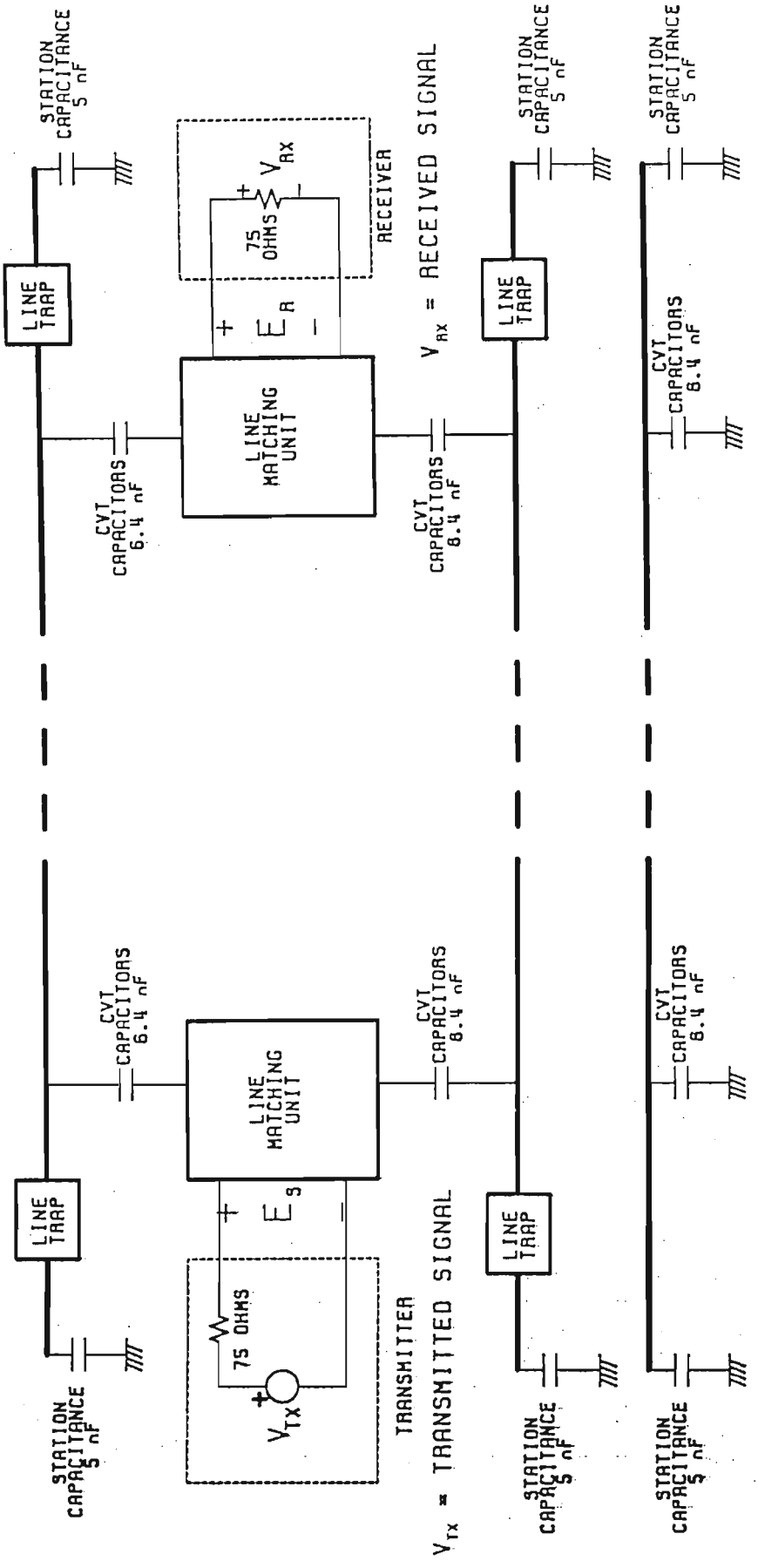

Figure 3.1.1 PLC communications network

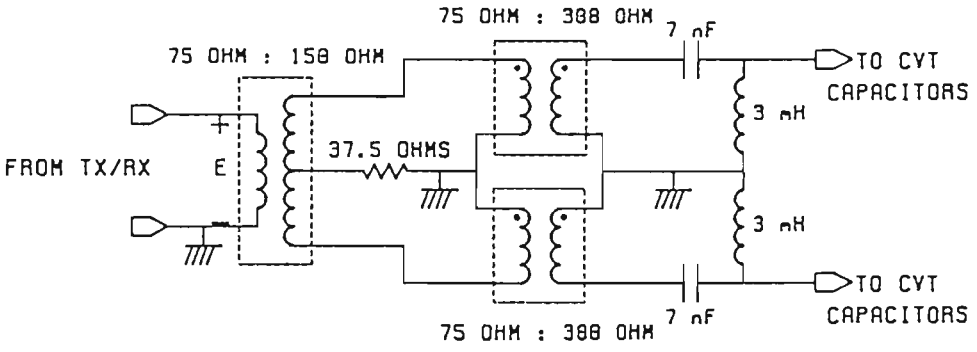

Figure 3.1.2 Line matching unit

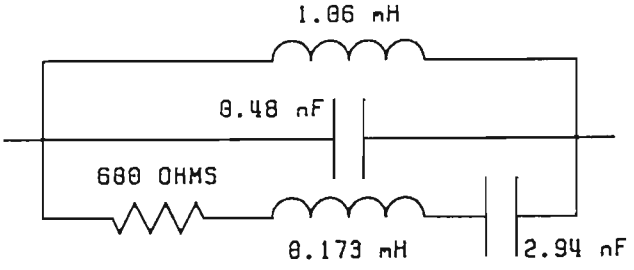

Figure 3.1.3 Line trap

3) Line trap

The function of the line trap is to present a high impedance at the carrier frequency and negligibly small impedance at power frequency, thereby preventing the carrier signal from being dissipated in the station equipment and being grounded in the event of a fault outside the carrier transmission path, as well as isolating the carrier channels from one to another to prevent interference. They are installed in series with the power line conductors. Resonant single, double-frequency, and wideband line traps are used. The purpose of line traps is to minimize carrier losses by confining energy to the desired path as much as possible. Line traps are huge equipments, which can range up to six feet in diameter, because of the large amount of 50 Hz current that must be carried, and they involve very high manufacturing costs [1,3]. Figure 3.1.3 shows a typical PLC line trap commonly used by SECV.

4) RF hybrids and Separation filter

When the wideband coupling method is used, several communication equipments are connected to the power line via a single communication cable. Therefore some sort of external separation circuits are included in the communication system to prevent desirable interactions, such as analog filters (simple L/C units) and carrier frequency hybrid units.

3.2 Frequency allocation

The PLC band of frequencies ranges from 40 KHz to 500 KHz (or beyond). The lower frequency is determined by the coupling circuits and line traps, while the upper frequency is set by the need to avoid interference with other users in this part of the spectrum, notably medium wave broadcasting services. There is also an increased attenuation at high frequencies. In some cases higher frequencies are used (even beyond 1000 KHz), but only in fault location systems [1,2]. Power authorities throughout the world have set aside a number of bands for PLC services, some exclusively and some on a shared non-interference basis.

The Department of Transport and Communication, who are the licensing authority in Australia, have set aside a number of bands for PLC services:

Frequencies exclusively set aside for continuous PLC transmission:

(a) 140 KHz to 200 KHz
(b) 405 KHz to 448 KHz
(c) 460 KHz to 484 KHz

Frequencies available for continuous PLC transmission provided there is no interference with other services:

80 KHz to 148 KHz

Frequencies available for intermittent (maximum transmission time 10 sec) PLC transmission:

200 KHz to 380 KHz

For continuous services, the frequency bands are subdivided into 4 KHz slots and normally one slot is allocated for the "go" direction and an adjacent slot for the "return" direction.

With the rapid development of the electric power network the necessity to control and monitor its various distant parts has become very important. Therefore, there is an increasing requirement for more channels, yet the available bandwidth is limited. This necessitates the efficient use of the existing channels.

Frequency division multiplexing (FDM) is a technique for the simultaneous transmission of many narrow-bandwidth signals over a wideband channel. Each narrow-band signal is separated in the frequency domain spectrum by modulation on a separate carrier [28]. The frequency separation has to be at least equal to the signal bandwidth to prevent the spectra overlap. This assumes SSB (single side band) modulation.

3.3 Noise

The noise comes from a variety of sources. These include noise inherent in high voltages lines, noise generated in PLC equipment itself, and the environmental noise around the lines. The different types of noise present in a particular line contribute in different ways and to different degrees to each of the communication functions of the PLC system. The two major types of noise effecting PLC communications are random noise and impulse noise.

Random noise has a continuous frequency spectrum within the PLC frequency range. Therefore, it can be considered as a "white noise". Among the factors that originate random noise are the thermal agitation of the molecules which constitute the high voltage conductors, the types of load on the system (such as electric ovens, power rectifiers, rotary machines etc) and corona effect. Corona noise (due to corona effect) occurs when the voltage gradient at any point in the vicinity of the conductor surface exceeds a critical value, which is a function of atmospheric conditions, diameter and geometry of the line. There are two different effects of corona noise on the PLC channel: one is the additive noise which is superimposed onto

the carrier wave, and the other is the intermodulation noise produced partly by nonlinearities. The variations of the line impedance due to corona itself, in fact modulate the carrier producing intermodulation noise. Thermal or resistive white noise are normally insignificant when compared with the corona noise level [1,7].

Impulse noise is of high importances in PLC communications, because it is characterized by string of sharp and sporadic impulses with variable repetition frequency. The amplitude of impulse noise is very high above the average level of random noise. Usually, it is caused by line faults, flashovers, atmospherics discharges, circuit breakers and isolator switching due to line faults or normal operation. While corona noise is uniformly distributed along the line, impulse noise has a well localized source. If these pulses are regular then the spectrum is discrete with spectral lines occuring at the repetition rate. Impulses with definite repetition rate are attributable to the rotating machines and rectifiers close to the power line; otherwise, the spectrum is continuous. PLC noise is predominantly of the impulse type and it is considered as a limiting factor in reliable communications and it consists of the pulse peaks being well above the general level, but the space between them is occupied by random noise [1,3].

Bad weather increases the line impulse noise level. Thunderstorms produce discharges which result in increased line impulse noise, sometimes as large as ten times that under fair weather conditions. Also light rain falling on dust and salt polluted insulators, will produce a sustained noise level, due to leakage currents. The operating voltage of the transmission line influences directly the noise level present in the line. As line voltage decreases, line noise increases. Large conductor diameter lower the noise level. Noise is substantially reduced in bundled conductor lines, where the effective diameter of the phase conductors is virtually increased. Bundled conductor lines are composed of two or more individual conductors in parallel to form one line. This increases the effective diameter of the line [2].

Tests [1] show that peak and average value of noise tends to decrease as the carrier frequency increases. The noise vs. frequency data shows definite peaks and valleys superimposed on the general decreasing trend. This is very similar to the line attenuation vs. frequency characteristic. Noise is actually subject to the same absorption and mismatches as the signal [2]. The actual range within which noise varies must be obtained by a series of measurements taken in all weather condition. According to measurements taken in Australia [18] corona noise is usually less than -5 dBm. Noise due to light rain falling towards the end of the dry season produces sustained noise levels as high as +8 dBm, (measured in the 4 KHz bandwidth of PLC channel). Impulse noise due to isolator operations is of the order of +10 dBm to 20

dBm with a maximum of up to +25 dBm in a burst of typically of 500 ms duration. A 4 KHz bandwidth was used for all measurementss.

More signal power (or less attenuation) does help to reduce the effect of additive noise produced by the corona. Therefore PLC systems must use large transmit powers to counter the noise problem. However, too high a transmit power can cause interference to users of the same channel in other parts of the system. A compromise is therefore required and most practical systems operate with transmit powers in the range of 10 to 100 watts.

3.4 Total signal attenuation

The total PLC attenuation is composed of [5]:

1. losses in coaxial cable
2. tuning, coupling and shunt losses
3. losses due to transmission line itself etc.

The coupling losses are the losses due to resistance of high voltage capacitors. The tuning losses are the losses due to resistance of tuning circuits. These losses vary as a function of the frequency, design, line impedance etc. The shunt losses originate from all leakage paths to ground [1,3].

Line attenuation is a function of the frequency, type of line, geometric construction, line voltage, conductor size, presence of ground wire, method of coupling, weather conditions, transpositions etc. Choice of which two phases to be coupled together depends on the loss between two stations, station layout requirements and the line design requirements. Line attenuation varies with the type of construction, and it is influenced by the ratio of the distance between the conductors and the height above ground. The greater the height of the conductors above the ground, and the smaller the distances between them, the lower the loss.

3.5 Modal analysis-practical concept

A signal applied on on a n multiphase transmission line effectively breaks up into n idependent signals which are called modes. Accordingly any arbitrary voltage applied to three phase line will be broken into three modal voltages; each of which has a different propagation constant, and each will propagate in manner similar to the single phase signal on a single line. The resultant voltage is the sum of theses natural voltage waves on the line [1,2]. For example, a power line can have a large peak in its attenuation characteristic if the amplitudes and phases of the 3 modes all sum

to zero. This condition can be avoided by changing the channel frequency, which changes the phase relationship between the modes.

Modal propagation also has implications for data transmission. The three modes travel at differrent speeds, and it is therefore possible for the fast mode of one bit to catch up the slower mode of the previous bit causing intersymbol interference at the receiver. Modal analysis is further explained in the next few paragraphs.

The modal theory is founded on the principle that there will be as many modes of propagation as there are conductors in a system. Therefore, a simple, untransposed threee-phase power circuit will have three natural modes of propagation. In Figure 3.5.1 three basic modes are illustrated.

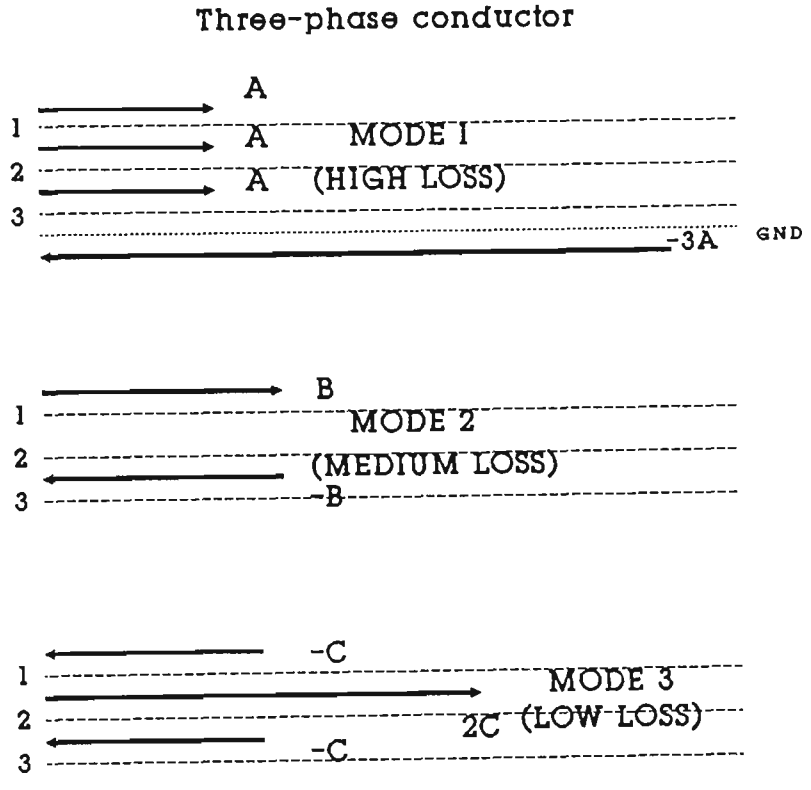

Figure 3.5.1 Basic modes

In mode 1 currents are simultaneously flowing in the same direction with equal magnitudes in each of the three phases. The return path is through the ground. The ground path is lossy. Therefore, this mode has high attenuation and is usually neglected. In mode 2 opposite currents flow in the outside phases, and this mode is medium loss mode. Mode 3 is a low loss mode; a currents flows in one direction in the center phase, and return equally split between the two outside phases.

In the following Figure 3.5.2 the method for determining the modal content of a specific current distribution on the line is illustrated. The composite currents in the three phases are denoted as Ir, Iy and Ib.

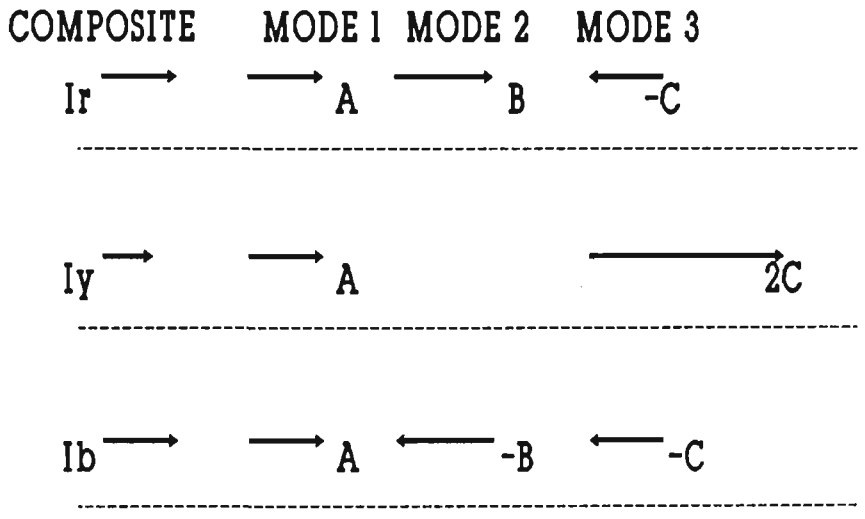

Figure 3.5.2 Modal content

From the Figure 3.5.2 (composite = mode1 + mode2 + mode3) it ensues:

$Ir = A + B - C;$ (3.5.1)

$Iy = A + 2C;$ (3.5.2)

$Ib = A - B - C;$ (3.5.3)

The mode currents are therefore:

$A = 1/3\ (Ir + Iy + Ib);$ (3.5.4)

$B = 1/2\ (Ir - Ib);$ (3.5.5)

$C = 1/6\ (2Iy - Ir - Ib\ );$ (3.5.6)

The conversion losses are illustrated in Figure 3.5.3 for three coupling methods employing modal analysis.

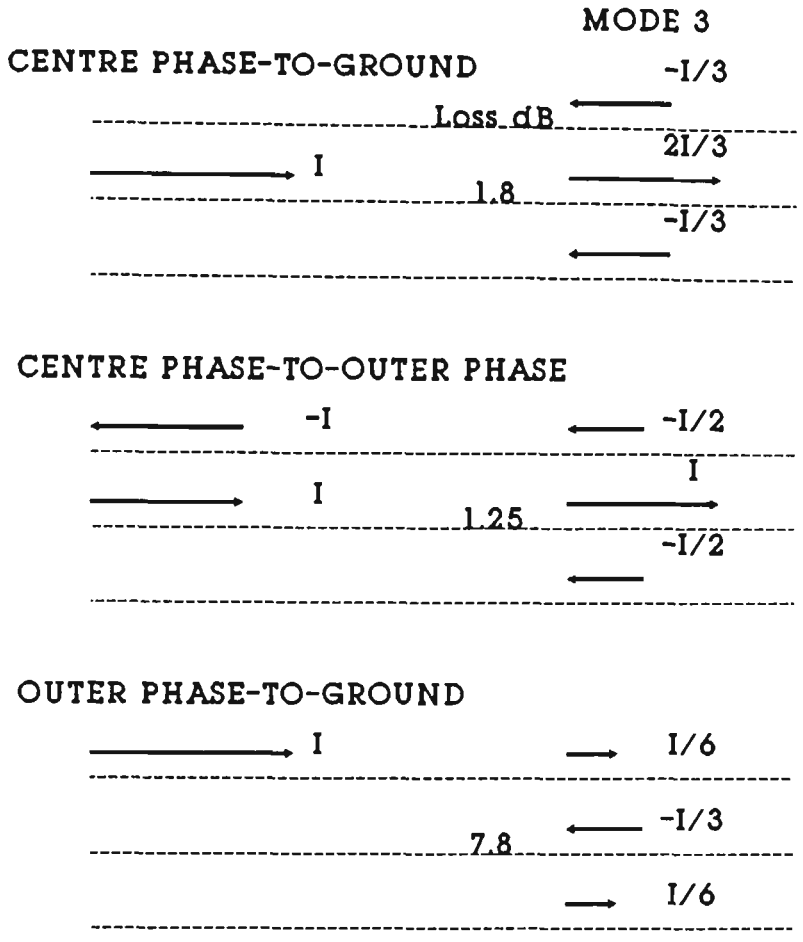

Figure 3.5.3 Conversion losses

The mode 1 and mode 2 have been neglected, since it is assumed that they will not contribute to the output at the end of the line. And from these examples it ensues:

Table 3.5.1 Conversion losses

coupling method	conversion loss [dB]
center phase-to-group	3.6
center phase-to-outer phase	2.5
outer phase-to-ground	15.6

Also the effect of transposition losses could be analyzed by modal analysis (Figure 3.5.4). Unsymmetrical spacing causes the flux linkages and therefore the inductance of each phase to be different resulting in unbalanced receiving-end voltages even when sending-end voltages and line currents are balanced. Also voltages will be induced in adjacent communication lines even when line currents are balnced. This problem is tackled by exchanging the positions of the conductors at the regular intervals along the line such that each conductors occupies the original position of every other conductor over an equal distance. Such an exchange of conductor positions is called transposition. Mode 3 currents enters a transposition from the left and emerges on the right with the changed current distribution. Then the resulting composite signal is expessed in its modes (mode 1 is zero). The transposition loss is calculated on the assumption that mode 2 current can be neglected. Conversion loss is 6 dB, but that is only a theoretical estimation. In most practical applications, the losses are much less than 6 dB, because it is assumed that only the mode 3 signal arrives at the transposition [2].

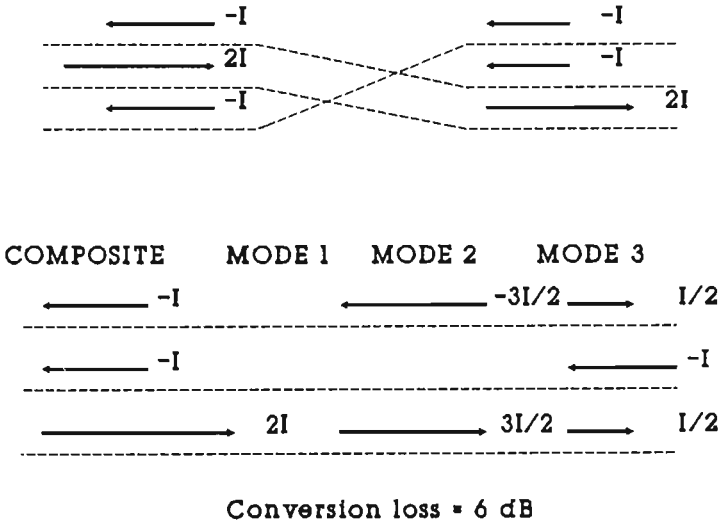

Figure 3.5.4 Transposition losses

Basically, the transposition of a transmission line causes a change in the energy content of the different modes, and it will behave as follows: the line attenuation is increased by a certain amount over a wide band, or the line attenuation varies significantly with frequency (pronounced attenuation maxima and minima occur). Regardless of how a carrier circuit is coupled to a transmission line, the signals ultimately adjust themselves to a combination of the mode 2 and mode 3. In a transposed line the natural modes are disturbed at each transposition and are constantly readjusting themselves. A similar situation happens at a discontinuity, or at a line trap.

3.6 Interference

When the signals share the same bandwidth, there are many potential interferers, but the main interfering signals usually originate from within the same substation, caused by unintentional propagation of PLC signals through and around the substation. Line traps are often used to control this problem, but they are difficult to manufacture (expensive) and not completely effective in preventing the small RF signal from passing through the substation to another line. Perfect isolation between signals operating at the same frequency is difficult to maintain and cross-talk interference occurs between signals of the same frequency from lines sharing the same substation.

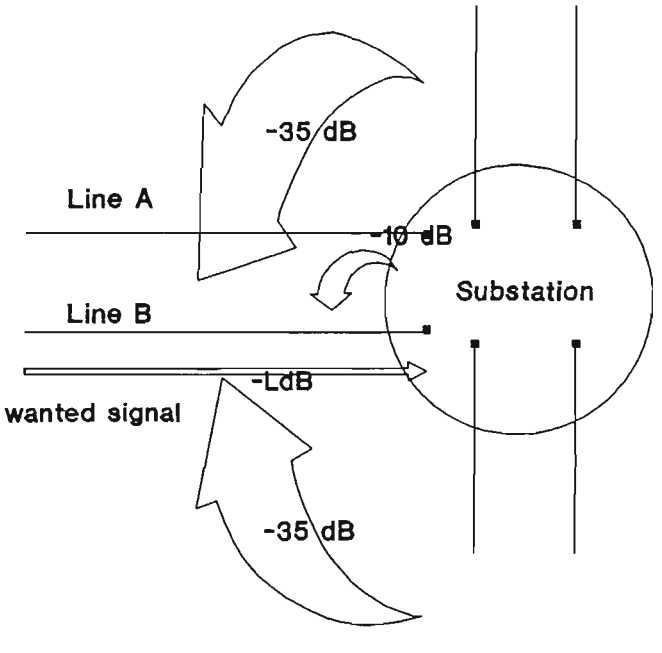

Figure 3.6.1 PLC interference sources into the receiver on the line B

Figure 3.6.1 shows the major interfering sources and their expected levels [5]. The attenuation levels shown are near the worst case obtained from practical field measurements performed by the SECV (State Electrical Commission of Victoria). Some of the results are shown in Appendix 1. In particular near-end interference from an adjacent line sharing the same tower could be nearly -10 dB (the worst case but typically about -25 dB). This interference could be appreciably larger than the desired signal, because the latter is subject to line attenuation. There is also a cross-talk interference between any two lines sharing the same substation. This interference is less than -35 dB, but typically around -50 dB. For acceptable good quality voice transmission using analog SSB modulation techniques, the interference to signal ratio has to be less than -55 dB. As a consequence frequency reuse of the same channel on two different power lines from the same substation is generally not possible due to the cross-talk interference. This reduces the spectrum utilisation.

In the design of PLC communications systems, the planner seeks to reduce the problem of co-channel interference between equipment operating on the same channel, by keeping a minimum separation of at least one trapped line (one clear span) for voice transmission or two trapped lines (two clear spans) for protection signalling. Thus system capacity is considerably reduced. Figure 3.6.2 shows a cascaded full duplex structure with two channels for the "GO" signal (f1 and f2) and also two channels for the "RETURN" signal (f3 and f4). Half duplex voice transmission requires at least two channels (each channel is 4 KHz) to provide a single voice circuit on each branch, or four channels for full duplex.

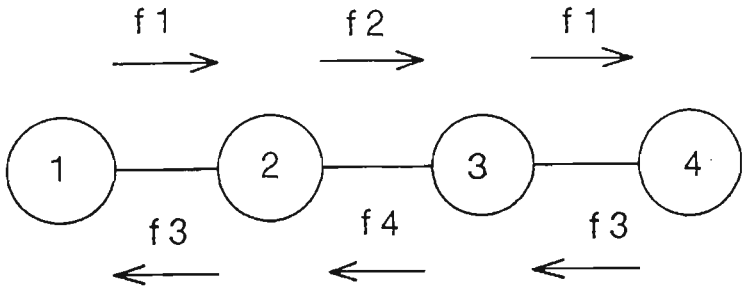

Figure 3.6.2 Cascaded full duplex structure
for analog SSB modulation

The reduction in capacity is greater for modern grid networks, particularly if substations have a large number of branches. Figure 3.6.3 shows a grid network based on that used by the SECV to supply western Victoria. The branch label f3/f8 indicates that the "GO" signal uses a channel f3, and the "RETURN" signal uses a channel f8. Substation 1 has five branches and determines the minimum number of frequency channels necessary to provide one full duplex transmission on each branch. In this case 2 x 5 = 10 separate frequency channel are required, and this will occupy a total of 40 KHz (4 KHz x 10) of spectrum. In general the more complex the network the less effective is the spectrum utilisation, and this resuls in a lower system capacity.

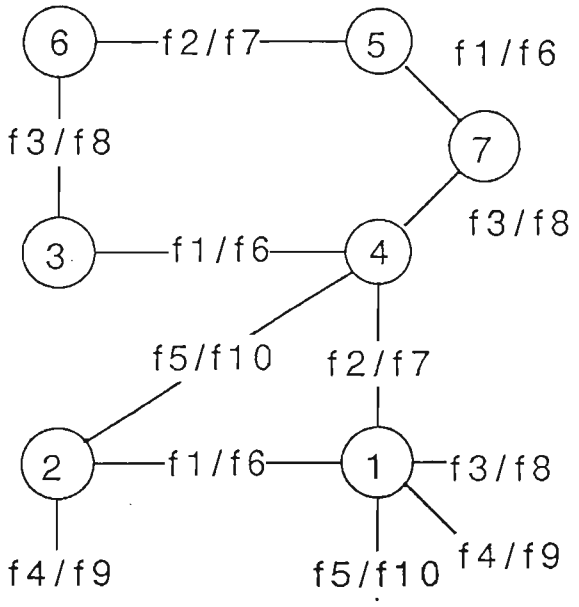

Figure 3.6.3 Grid network - spectrum allocation
for analog SSB system

4 Digital PLC Communication

4.0 Introduction

Digital PLC communication system can operate in a much higher interference environment compared to the existing SSB links. This can lead to a modest increase in capacity. This chapter seeks to investigate the benifits and disandvantages of digital modulation in PLC applications. It is shown that equalisation is needed to overcome dispersion problems caused by the PLC channel.

4.1 Proposed solution

To increase capacity, digital PLC modulation in conjunction with avoidance and power control is proposed. Avoidance is obtained by introducing a small amount of frequency division multiplexing, in this case the "GO" and "RETURN" signals on the same branch have to operate on different channels.

The transmitted power has to be set at its lowest level to obtain a given signal to noise performance at the receiver and to keep the level of interference as small as possible. A simple design policy for transmitter power control is to adjust the transmitted power so that the receiving power is the same for each line. Cross-talk interference around the receiver substation is minimised. This receiving power should be adequate for the worst (noisiest) link. Digital modulation can provide improvement in signal to interference ratio which can eliminate any separation requirements with a correct choice of modulation. This will allow immediate channel reuse on the branches from the same sub-station. As a consequence all the branches into a given substation receive on the same frequency channel.

It is possible to work backwards and calculate the carrier to interference tolerance required to reduce the separation for a typical network to zero spans. Consider the receiver in the substation 1 on branch B4 (Figure 4.1.1). The major interferences comes from branches B1, B2, B3 and B5 of substation 1. Other

sources of interference occur from substation 2 where output power from branch B6, B7, B8 and B9 is cross-coupled into branch 4. These branches are likely to have different output powers to compensate the different attenuations.

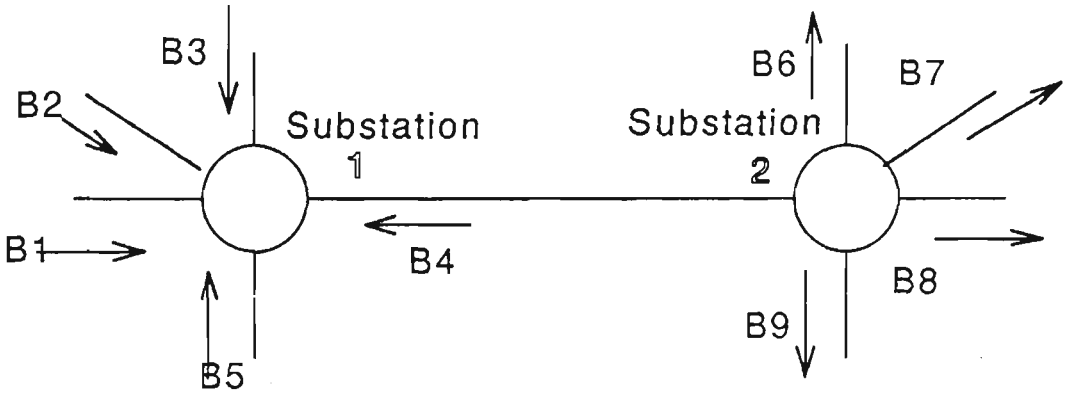

Figure 4.1.1 Interference analysis. Arrows indicate channels using the same frequency. The wanted signal is B4. The others are possible cochannel interferers

If the receiving power p_r is same on all branches then the transmitting power is $p_{ti} = p_r \cdot L_i$, where L_i is the line attenuation, if α_{i4} is the cross coupling coefficient from branch Bi (= B6, B7, B8 and B9) to the branch B4, then:

total interference $= \alpha_{14}.p_r + \alpha_{24}.p_r + \alpha_{34}.p_r + \alpha_{54}.p_r$

$$+ (\alpha_{64}.p_{t6} + \alpha_{74}.p_{t7} + \alpha_{84}.p_{t8} + \alpha_{94}.p_{t4})/L4 \qquad (4.1.1)$$

this gives:

total interference $= (\alpha_{14} + \alpha_{24} + \alpha_{34} + \alpha_{54}).p_r$

$$+ (\alpha_{64}.p_r.L_6 + \alpha_{74}.p_r.L_7 + \alpha_{84}.p_r.L_8 + \alpha_{94}.p_r.L_9)/L_4 \qquad (4.1.2)$$

and:

total interference/signal (I/S) $= \alpha_{14} + \alpha_{24} + \alpha_{34} + \alpha_{54}$

$$+ (\alpha_{64}.L_6 + \alpha_{74}.L_7 + \alpha_{84}.L_8 + \alpha_{94}.L_9)/L_4 \qquad (4.1.3)$$

If all the α_i are same and equal to the worst case -35 dB, then:

$$I/S = \alpha\{4 + (L_6 + L_7 + L_8 + L_9)/L_4\} \qquad (4.1.4)$$

or [in dB]:

$$I/S = -35\ dB + 10 \log_{10}\{4 + (L_6 + L_7 + L_8 + L_9)/L_4\} \quad (4.1.5)$$

If the line attenuations are all equal then:

$$I/S = -35\ dB + 9\ dB = -26\ dB \quad (4.1.6)$$

but this is not normally the case, because of different branch lengths. In particular, when L_4 is much smaller compared to $(L_6 + L_7 + L_8 + L_9)$ then the cross talk interference will be high. To allow for this the modulation should be able to handle cross-talk interference at a higher level than the -26 dB value shown in equation 4.1.6.

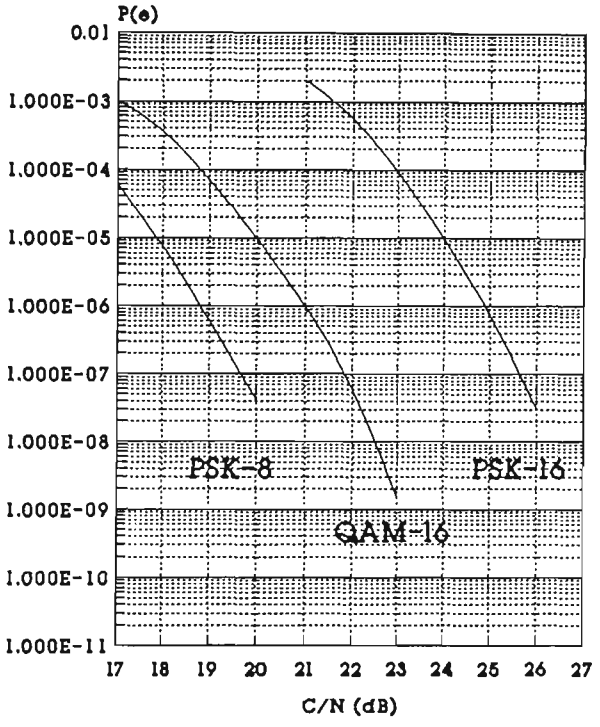

Figure 4.1.2 BER performance of QAM-16 for double-sided Nyquist bandwidth

To satisfy these requirements, it is proposed that quadrature amplitude modulation QAM-16 is the most suitable compromise between channel capacity (bit/Hz) and interference immunity. QAM-16 has a two dimensional signal constellation, with 16 points in a rectangular grid [25,26]. QAM-16 yields better spectral efficiency than phase shift keying PSK-8, since in QAM-16 each symbol represents four bits of information. On the other hand, QAM-16 is less sensitive to noise and interference than PSK-16. This is obvious because the spacing between symbols is larger than they would be if they were on a single circle. From Figure 4.1.2 it has been found that for a S/N ratio of 20 dB, QAM 16 gives a bit error rate of

10^{-5}, which is more than sufficient for digital voice applications. A similar performance can be expected in the presence of a number of a cochannel interferers, which approximate a noise signal (central limit theorem). QAM-16, therefore, gives 35 dB (55 dB - 20 dB) more tolerance to cochannel interference than analog SSB modulation.

A small margin of 6 dB (-26 dB is the value for cross talk interference) caters for different line losses. This may appear little, but in most practical cases it will be much larger due to the cross-coupling coefficients not being at their worst case values. For example, if the average value is taken for the cross-coupling coefficients α then the margin increases to 21 dB.

In most practical situations the system designer can get optimum performance by applying the general case expression derived from equation 4.1.3 to each receiver.

$$I/S = \sum_{i \neq d}^{all\ i\ at\ Rx} \alpha_{id} + L_d^{-1} \cdot \sum_{i \neq d}^{all\ i\ at\ Tx} \alpha_{id} \cdot L_i \qquad (4.1.7)$$

The number of major interferers is likely to be limited to one or two dominant sources. This and some flexibility in choosing the channel frequencies should enable most systems to operate with a considerable reduction in the number of channels.

Of course digital modulations which are more robust to interference than QAM-16 do exist. QPSK (quadrature phase shift key) for example, would give a further improvement of about 6 dB but this would require doubling the bandwidth to obtain the same data rate. This trade-off is unlikely to lead to an improvement in system capacity.

The bandwidth requirement of the digital modulation is set by the data rate and applied pulse shaping. For this analysis a data rate of 32 Kbits/sec has been selected because of its simplicity for voice transmission using the ADPCM G 721 standard. Pulse shaping is performed by squared root raised cosine filters which use a 50 % excess bandwidth ($\beta = 0.5$). This choice of β is a design trade-off between bandwidth, and complexity in both the filters and timing recovery circuits incorporated in digital design. The ADPCM 32 Kbit/sec data bit stream with before mentioned pulse shaping filtering requires double sided bandwidth of 12 KHz.

Figure 4.1.4 shows a cascaded full duplex structure with one channel for the "GO" signal (f1 or f2) and one channel for the "RETURN" signal (f2 or f1). Half duplex or full duplex transmission requires two channels (each channel is 12 KHz).

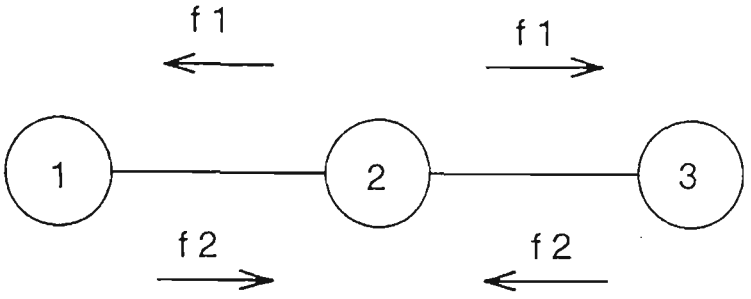

Figure 4.1.3 Cascaded full duplex structure - Dig. modulation

Figure 4.1.3 shows a grid network (same as the one in Figure 3.6.3), where voice transmission requires 3 channels (All branches into a given substation receive on the same channel frequency: F1 or F2 or F3.); in this case 12 KHz x 3 = 36 KHz of spectrum compared with 40 KHz for the analog SSB case. Accordingly, spectral efficiency is marginally improved. The improvement is expected to increase as the networks get more complex. Furthermore, there is a potential for a much greater capacity increase when low bit rate voice coding algorithms such as such as VSELP (Vector-Sum Excited Linear Prediction) become commercially available. VSELP compresses speech down to an 8 Kbps rate, and would provide an additional four times gain in spectral efficiency. CELP (Code Excited Linear Prediction) even compresses speech into a 4.8 Kbit/s data stream for transmission to provide good communication quality, which is expected to be released in the market in near future.

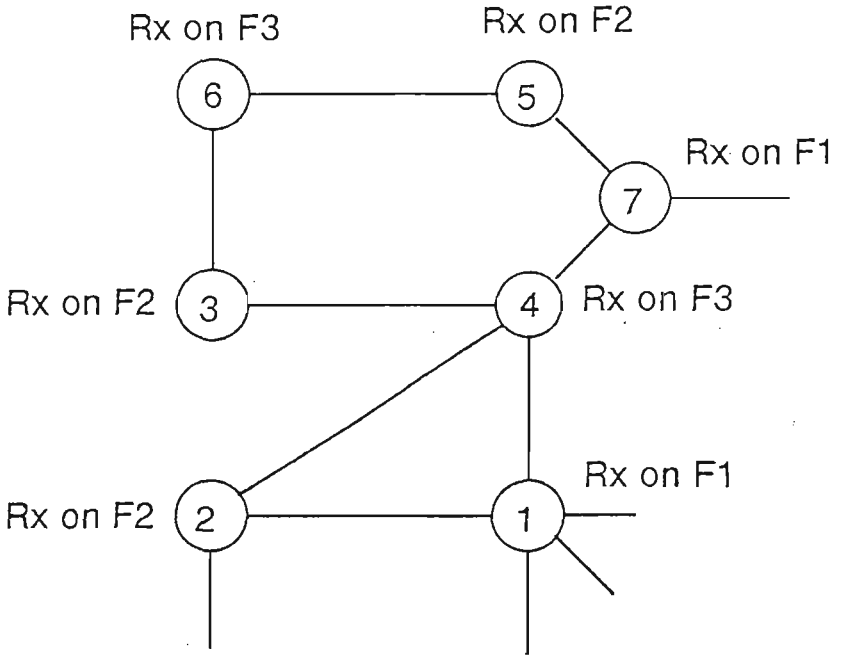

Figure 4.1.4 Grid network - Dig. Modulation

4.2 PLC characteristic measurements

Frequency characteristics of PLC power line are affected by several factors, such as conductivity of the wires, its spacing, its distances from the ground wires configuration, the distance of ground wire from the earth etc. Therefore, unlike telephone lines a PLC line are not standardized to any appreciable extent [1,2]. Group delay measurement on power lines are not normally available since narrow band modulations have been used in PLC communication.

In conjuction with the SECV, a set of measurements of amplitude and delay frequency characteristic have been obtained on a 220 KV power line over the frequency band from 210 KHz to 390 KHz for a 41.5 Km long power line (East Rowsvile to JLA) [8]. Both frequency characteristics show definite peaks and valleys superimposed on the general trend, which suggests of a standing wave on the line. These ripples are in the range of 1 to 2 dB peak to peak. A further set of measurement was attempted on a longer power line (Moorabool, Geelong to ALCOA, Portland), but was abandoned because noise level was to high for the measuring equipment to function properly. The measurement were taken co-ax to co-ax, and therefore effected by the performance of the line traps, line matching units and separation filters. Assuming simple reflection model and measuring the period between the ripples (3.75 KHz) the time delay for the reflected wave is 0.28 ms suggesting a phase velocity of 0.99 x C with reflection occurring at the line ends. This leads to the conclusion that the line traps and coupling units don't work perfectly.

Further examination of the results shows a number of other anomalies such as the amplitude change of the ripples, the presence of apparent beats in the ripples and superimposition of a slow periodic change. These are probably caused by different propagation modes, reflection from the line transposition, changes in impedance of the line matching units with applied frequency and the expected increase in attenuation at higher frequencies.

4.3 Signal dispersion

Transmission quality is deteriorated due to the presence of the reflected waves and other distortion of the channel frequency response. Reflected waves are generally produced by a terminal mismatch of the line. The forward traveling (initial incident) wave is reflected, and creates a reverse traveling reflection wave at the same speed and velocity as the incident wave. This may occur again producing

further reflections. Owing to this phenomenon, each pulse is likely to occur more than once at the receiving end. In the case of considerable attenuation (long lines or higher frequency) the reflection is not so large, because the reflected wave has to travel at least twice the line length further than the main wave [1]. For short lines, reflection in the PLC channel is a major cause of distortion.

Reflections can be caused by joining of the transmission lines of different impedances, branching of lines, line discontinuities, imperfectly matched terminal loads, transpositions, serial impedances, each of which generate reflected waves. Minor reflections occur continuously along any transmission line, because of the unavoidable fluctuation of transmission line characteristic (such as variable conductors heights above uneven terrain). These deteriorations can be reduced considerably by proper application of the line traps, and careful matching of the line impedances, and in the case of digital PLC modulation appropriate equalisation techniques can be added to the receiver. Equalisation can correct for linear distortions in the channel and certain impairments caused by the modem itself.

This section seeks to predict the channel distortion using a transmission line model. The interaction between the line conductors in the three phase configuration is accounted for, as is the effect of the earth and termination impedance. The impedance presented by a power sub-stations is made up of the impedance of bus bars and switches (all capacitive) as well of the impedance of the measuring and power transformers (also capacitive in most cases). The bus bar capacitance could be obtained either by calculation or by measurements. The values found range between 0.5 nF and 10 nF depending on the size of the substation. The transformer impedance depends on the size of the transformer and it is a function of the frequency. The impedance ranges between 1 nF and 5 nF, but in some cases could be inductive [1]. As previously discussed in section 3.5 signals applied to a single circuit three phase line break up into three independent modes; each of which has a different propagation constant; each travels through a power line with different speed and attenuation, and could be considered as single phase signal on a single phase line. The resultant voltage is the sum of these voltages on each line separately.

The powerful method of modal analysis provides an efficient means to analyse the PLC channel. Its calculation depends on the specific parameters of the PLC channel. The simulation studies presented here are derived from an existing in-house program based on the distributed parameter modal analysis of Wedepohl [14,18]. The program can model any arbitrary waveform propagation down a three phase transmission power line, and includes the effects of line geometry, line conductivity, line traps, line matching units, coupling capacitors, transposition, earth resistivity,

conductor and earth wire resistivity. It operates in the frequency domain, calculating the gain and phase shift for each spectral component of an applied waveform.

The study here involves a 500 KV line of 100 Km, with a horizontal three phase cross section, as shown in Figure 4.3.1. Coupling is outer phase to centre phase. A sub-station impedance of 5 nF was selected. CVT (capacitor voltage transformer) capacitors have a value of 6.4 nF.

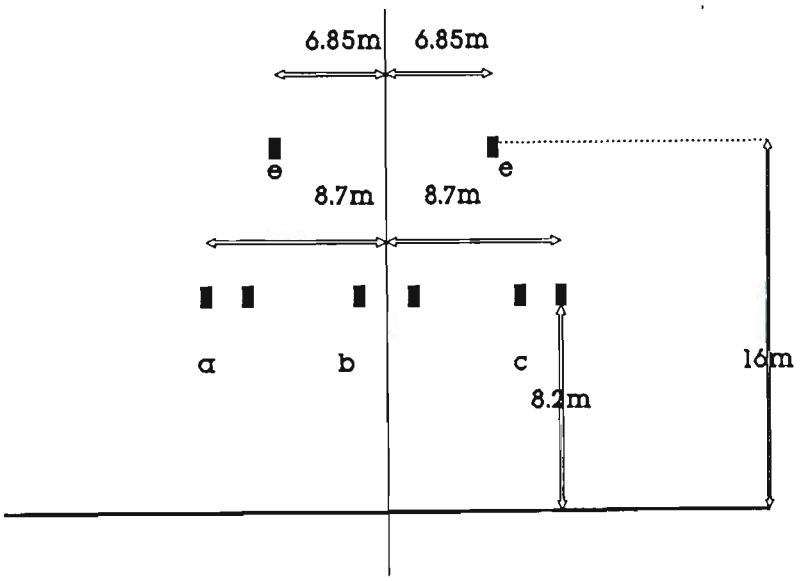

Figure 4.3.1 Line configuration e-earth wires
a, b and c main conductors

The data for this line are:

1. Number of the conductors = 3
2. Number of earth wires = 2
3. Line configuration (metres) =
(-8.7,8.2), (8.7,8.2), (0.,8.2), (6.85,16), (-6.85,16)
4. Conductor geometric mean radius GMR (metres) = 0.0905
5. Earth wire GMR (metres) = 0.018
6. Conductor resistivity (ohm-metres) = 3.21e-08
7. Earth wire resistivity (ohm-metres) = 3.21e-08
8. Radius of the outer layer conductor strands (metres) = 0.00125

9. Radius of the outer layer earth wire strands (metres) = 0.00175
10. Number of the strands in the outer layer of the conductors = 30
11. Number of the strands in the outer layer of the earth wire = 6
12. Number of conductors per bundle = 2
13. Earth resistivity 100 ohm-meters
14. Relative magnetic permeability of the conductor = 1
15. Relative magnetic permeability of the earth wire = 1
16. Homogeneous line section lengths (Km) =

33.333 33.333 33.333

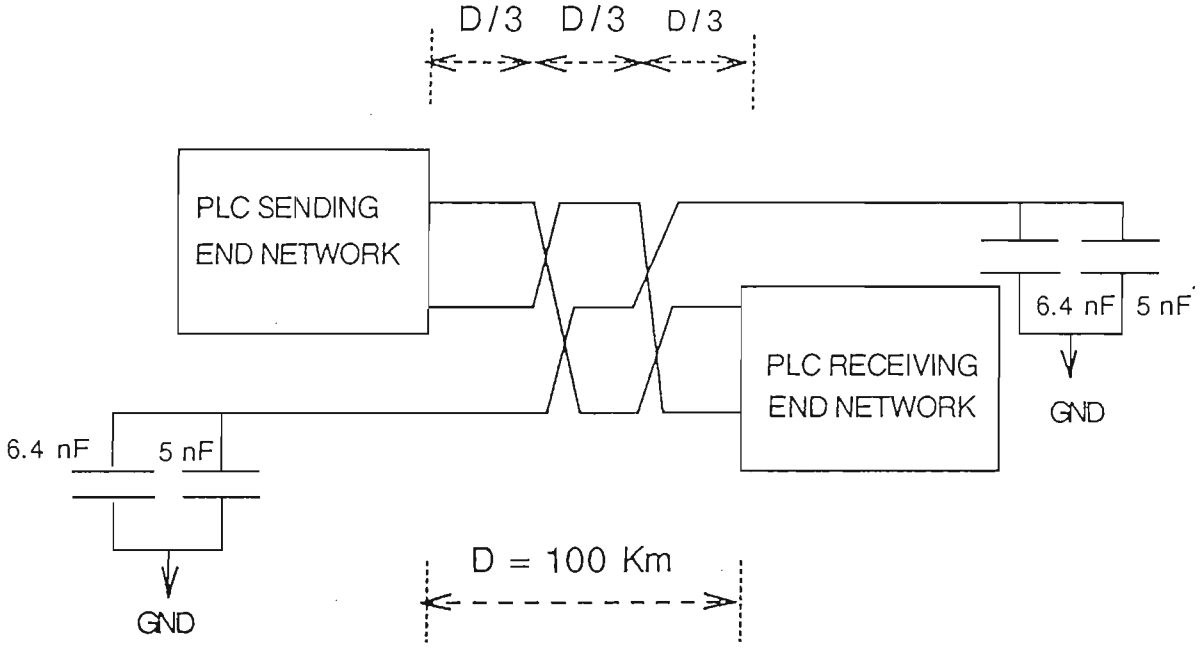

Figure 4.3.2 Line transposition and coupling

To analyse the distortion of the PLC channel, it is first necessary to determine its frequency response H(jw) [27]. This is done by passing a comb of unity amplitude tones through the simulation model and measuring their respective gain and phase shifts. For this simulation 2048 tones were used and these were equally spaced between 0 Hz and 500 KHz. The resulting graph of amplitude frequency characteristics of the simulated PLC line (Figure 4.3.3) shows the expected low frequency null of the coupling circuits, followed by a somewhat unexpected resonance at 26 KHz. Another null follows and about 80 KHz the response shows the expected gradual increase in attenuation with frequency. Superimposed on these slower variations is the presence of high frequency ripples which are particularly prevalent at lower frequencies. The channel amplitude response in log scale is shown in Figure 4.3.4. The channel phase response is shown in Figure 4.3.5, and is dominated by a large linear phase component which can be accounted for by end-to-end propagation delay of the line. Quantization effects on the frequency axis is responsible for the saw-tooth effect at the wrap-arround phase of π and $-\pi$. The channel group delay frequency characteristic is shown in Figure 4.3.6. The delay over most of the frequency band is close to the expected end-to-end propagation delay of 300 μsec.

Spice simulations were performed on the line matching networks to see what their contribution was to the overall amplitude response of Figure 4.3.3. The back to back overall frequency response of the line matching networks, when connected to the ideal lossless 300 Ω line is shown in Figure 4.3.7. The extremes in the frequency response at 26 KHz and 55 KHz correspond to the resonant frequencies of the drain coil and parallel and series combination of the CVT capacitors. Clearly much of the low frequency behavior in Figure 4.3.4 can be explained by the line matching networks. The high frequency ripples and gradual attenuation with frequency must therefore be caused by the power line. The ripples have a maximum value of 5 dB peak-to-peak at 45 KHz, which reduces with frequency. Above 300 KHz they are almost extinct. The period between the ripples, delta f, is approximately 1.5 KHz, which suggests they are caused by reflections off the end of the line. The wave velocity is given by v = delta f x 2 x l, where l is the line length (100 Km). The velocity is equal to the speed of light within the accuracy of measuring delta f.

The amplitude of the ripples is a good indication of the relative strength of the reflected wave. The result reported in [8], for measurements on 220 KV line, showed the presence of large ripples even at high frequencies (>300 KHz) and this was explained by the low attenuation of the reflected wave because of the short line length (40 Km). The reflected wave is strongest at lower frequencies and on shorter lines, when the end-to-end line attenuation is small.

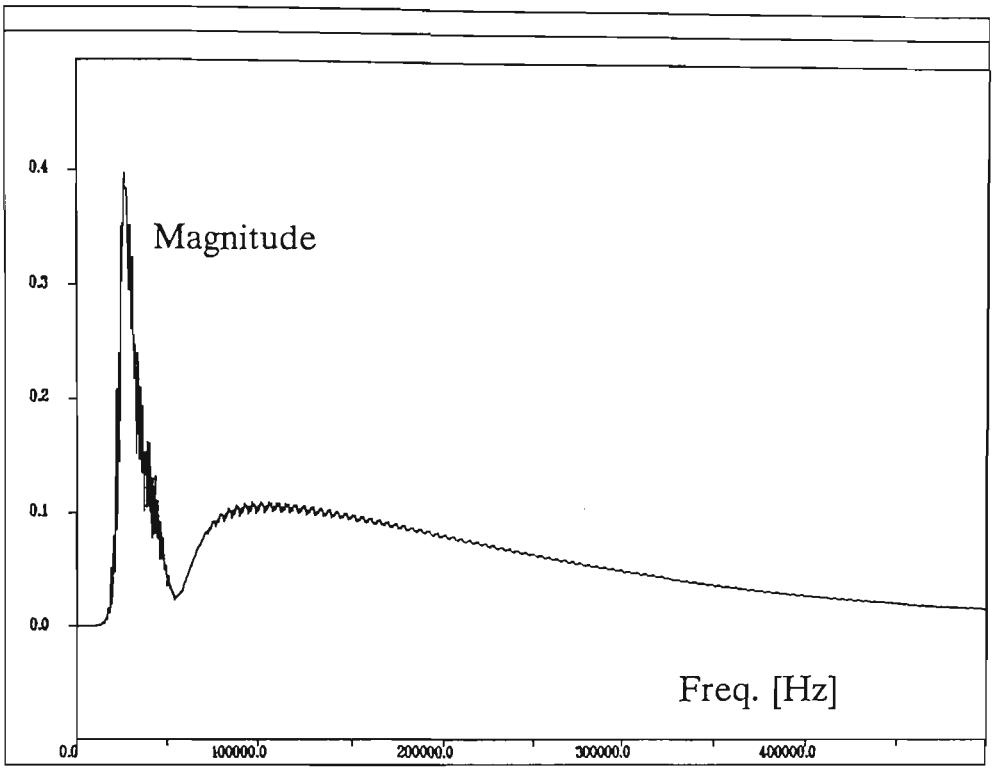

Figure 4.3.3 Channel frequency response (magnitude), R_k, obtained from simulation model

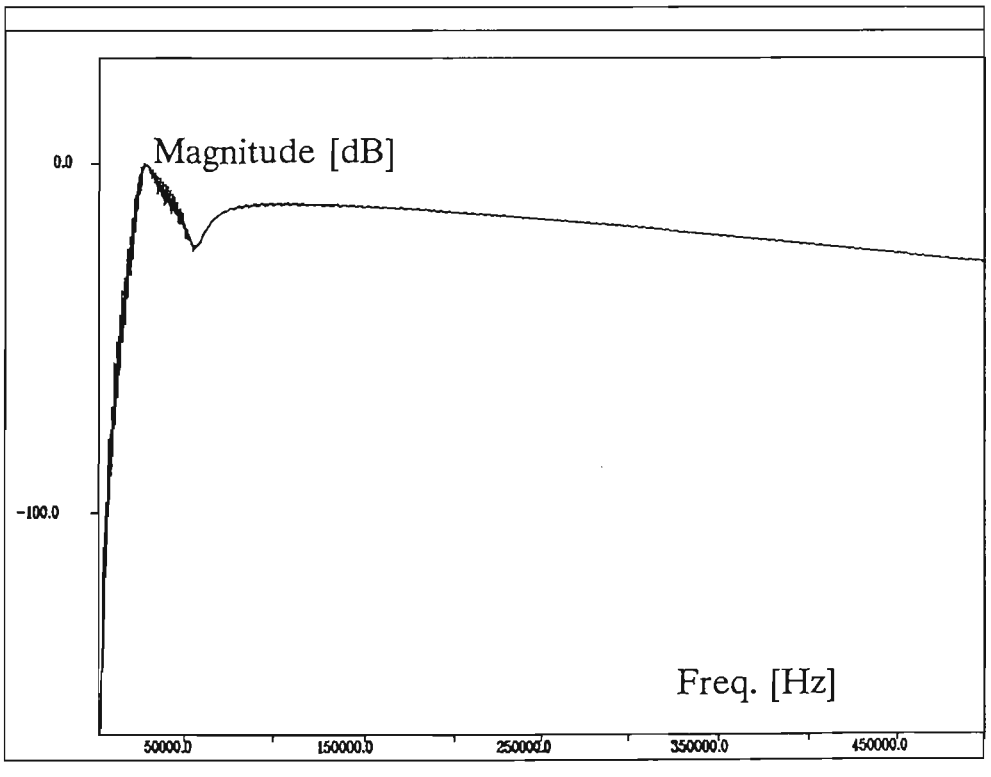

Figure 4.3.4 Channel frequency response (log magintude), R_k, obtained from simulation model

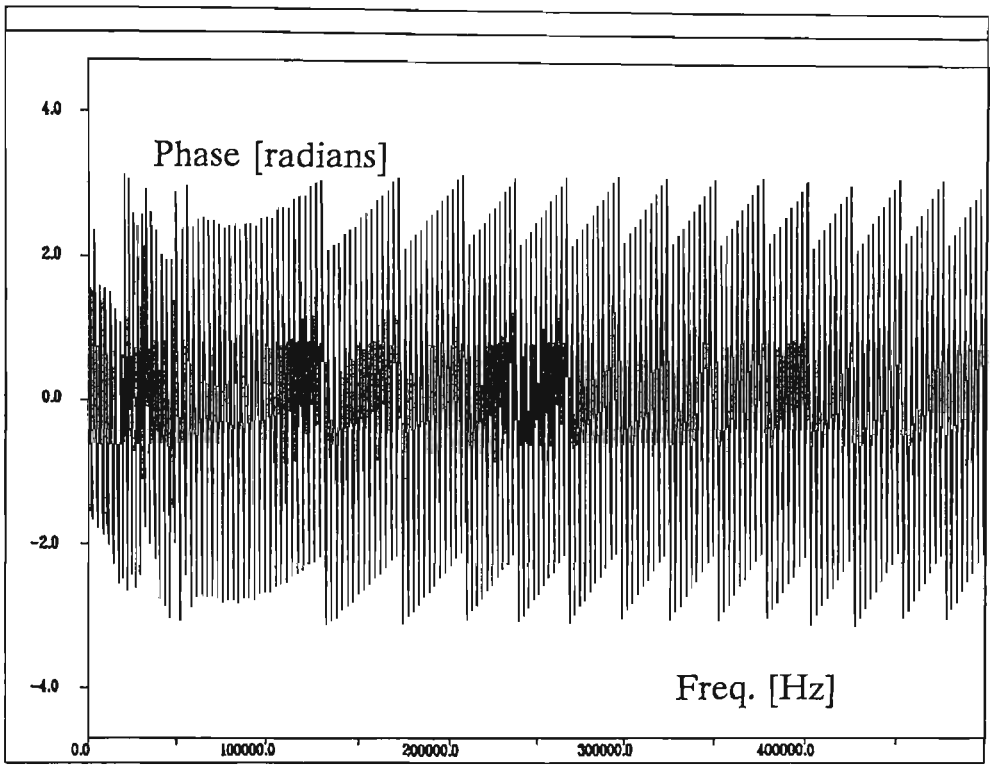

Figure 4.3.5 Channel frequency response (phase), θ_k, obtained from simulation model

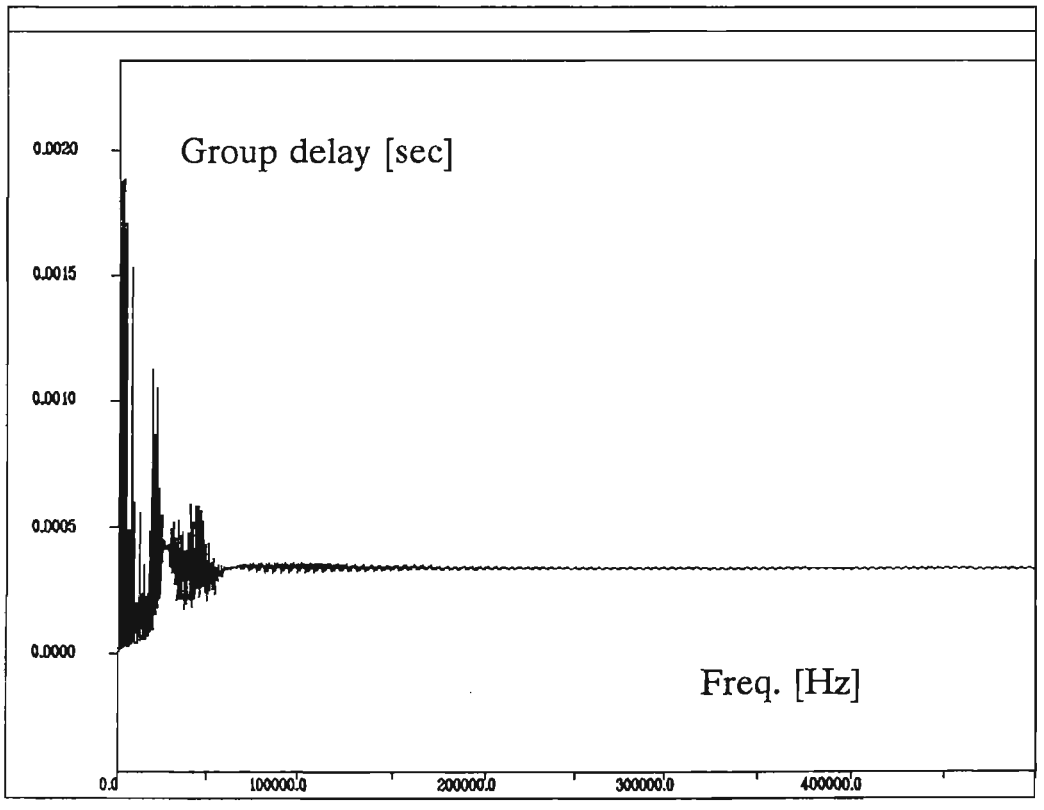

Figure 4.3.6 Channel group delay

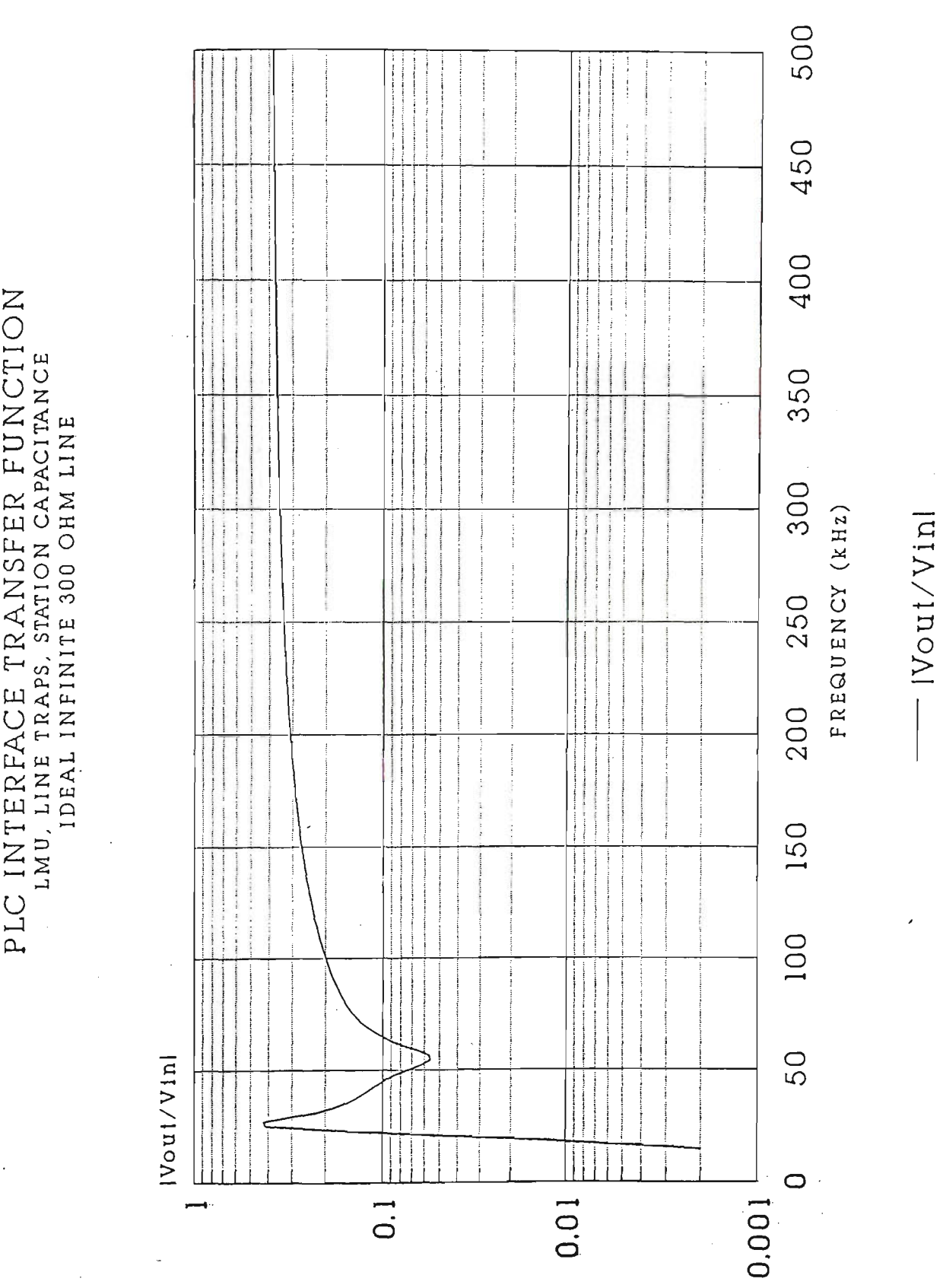

Figure 4.3.7 PLC interface transfer characteristics. Spice simulation.

4.4.0 Digital PLC Analysis

Digital modulation such as QAM-16 has a high tolerance to noise but is very sensitive to channel distortions which cause the signal to disperse, as is caused by modal propagation and reflections on the line. If the dispersion is longer than one symbol period, it produces intersymbol interference (ISI), which reduces the performance of the system, and in some cases makes it totally unworkable. Modems often use linear transversal equalisers to combat this problem. The following section seeks to investigate the dispersion on the line to see if equalisation is in fact necessary, and if so, how difficult it might be to achieve.

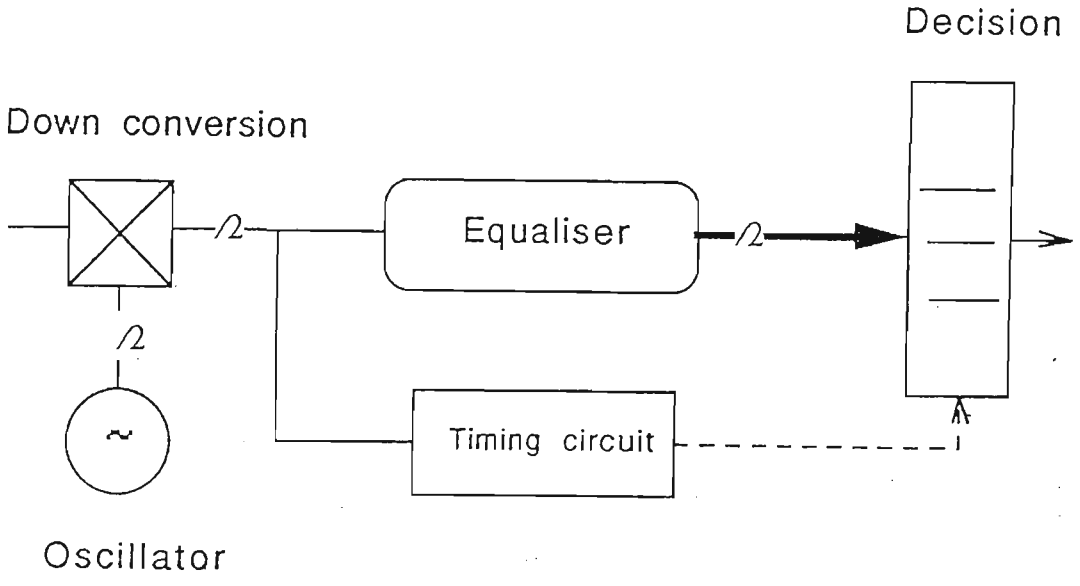

Figure 4.4.1.1 Receiver - simplified block diagram

4.4.1 Equaliser Design

Figure 4.4.1.1 shows a simplified block diagram of the PLC communication receiver, and Figure 4.4.1.2 gives the tapped delay line structure of the transversal equaliser. The receiver consist of a down conversion stage, which brings the modulated carrier

signal to baseband followed by an equaliser and decision block which reconstitute the transmitted data. The baseband signal is complex and consist of two signals, one inphase with the carrier, the other in phase quadrature with the carrier. More details on the modem design can be found in the following chapter. The equaliser takes the form of a finite impulse response filter and can operate on the modulated carrier signal or the complex baseband signal. The latter is the more usual approach, because it leads to a more compact design (reduced number of the taps). This is particularly important if a solution involving digital signal processing is being considered.

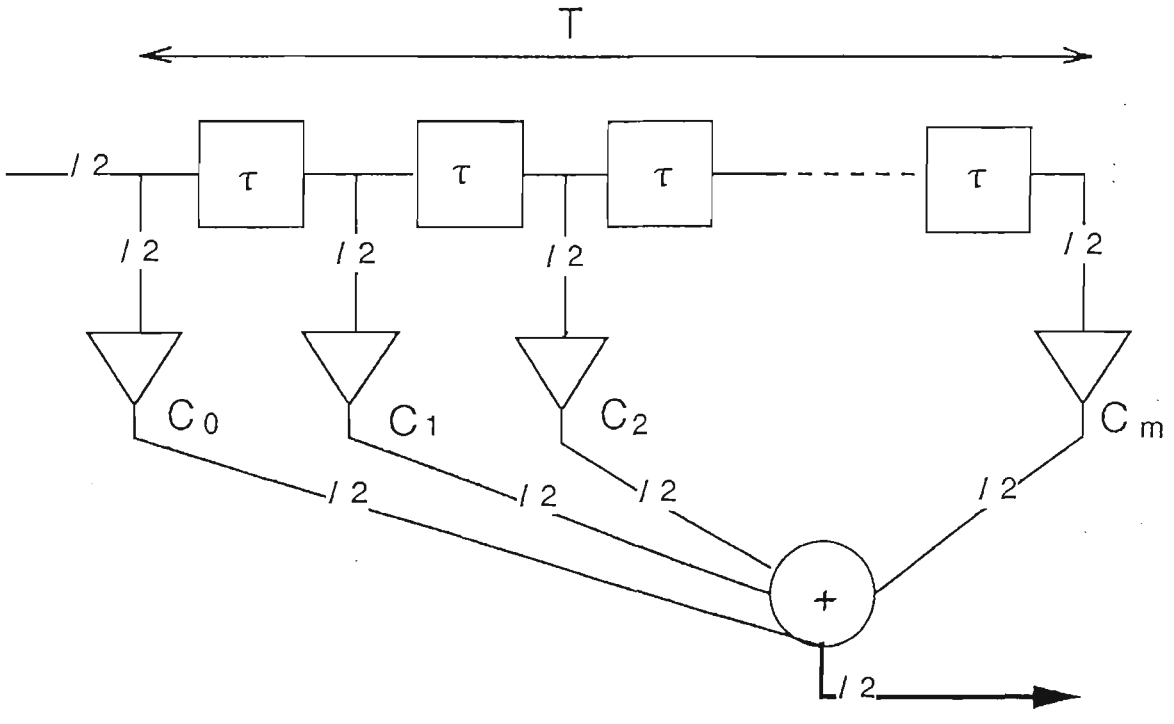

Figure 4.4.1.2 Transversal Filter - complex equaliser for baseband signals

The design information required for the equaliser includes the value of the complex tap coefficients, Cn, the delay period between each tap, and the total number of taps required. For a baseband equaliser the tap delay period, τ, is set at one symbol duration, or in some cases half a symbol duration $\tau/2$ is used. For a 32 Kbps QAM-16 modem the symbol rate is 8 Ksymbols/s (τ = 0.125ms), the tap coefficients can be adjusted in situ by making the equaliser adaptive, and only the number of the taps, (m+1), needs to be decided by the designer beforehand.

The number m is selected so that the equaliser can span all the parts of the signal that make a contribution to the output data sequences. This can be achieved by making the time length of the equaliser, T = m.τ, equal to the time duration of the channel impulse response.

4.4.2 Channel Impulse Response

The impulse response of the PLC Channel can be obtained by taking the inverse Fourier Transform (IFFT) of its frequency response H(jw), this involves treating aperiodic signals as periodic for the purpose of the numerical calculations [27]. First h_n is defined as a sampled version of the channel impulse response, and H_k is the sampled version of the channel frequency response $\tilde{H}(jw)$. Then H_k is generated which includes negative frequencies so that the resulting IFFT will produce an impulse response that is real (non-complex).

If

$H_k = R_k \exp(j\theta_k)$ of length N (k = 0 to N-1)

and

$\tilde{R}_k = \tilde{R}_k \exp(j\tilde{\theta}_k)$ of length 2N (k = 0 to 2N-1)

where R and θ are respective amplitude and phase responses; then the for a real impulse response, $\tilde{R}_k$ must have even symmetry and $\tilde{\theta}_k$ odd symmetry. These are obtained by concatenating the response of H_k with its reflection about the frequency sample k = N and then inverting the phase of the reflected portion. The only samples hat do not have a mirror image are the DC term H_0, and the sample H_N which doesn't have a value. The value is interpolated from its two neighbors. Mathematically:

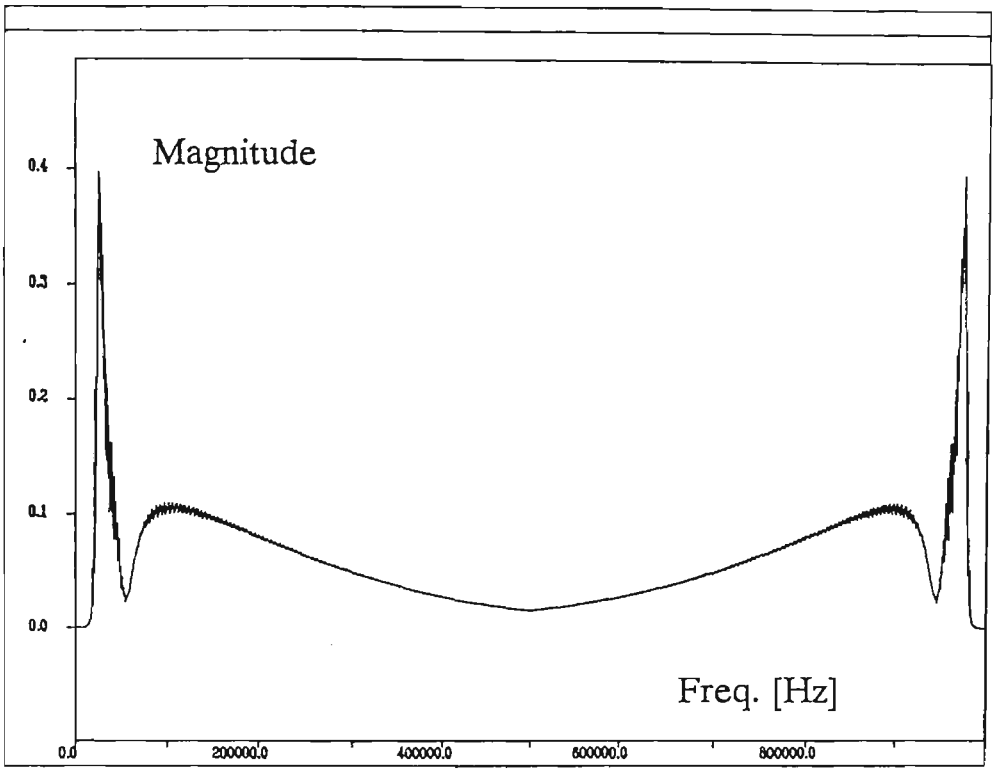

Figure 4.4.2.1 Concatenation - amplitude response, $\tilde{R}_k$

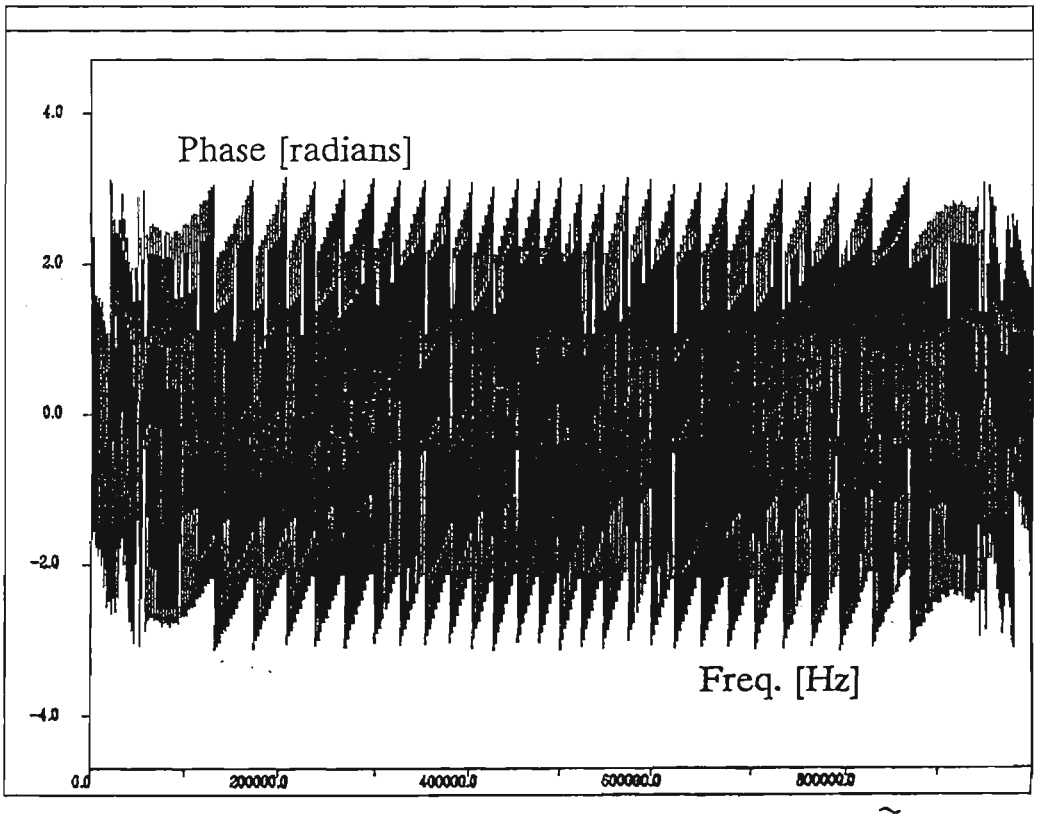

Figure 4.4.4.2 Concatenation - phase response, $\tilde{\theta}_k$

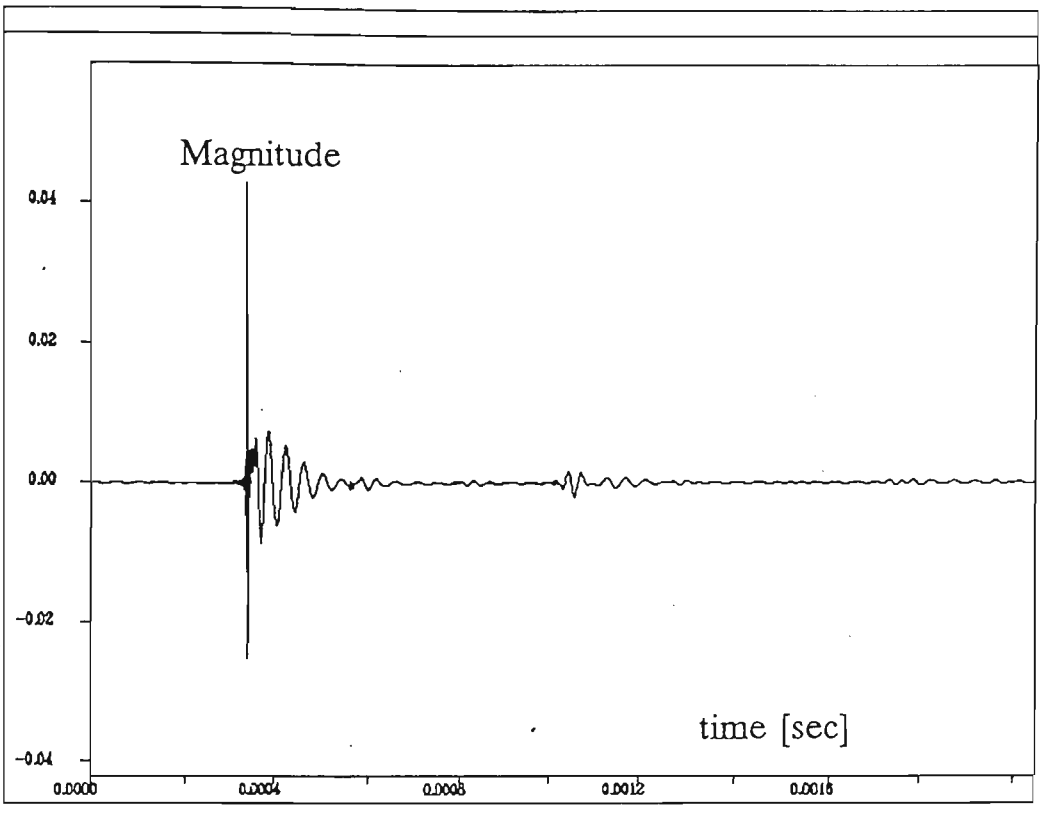

Figure 4.4.2.3 Channel impulse response

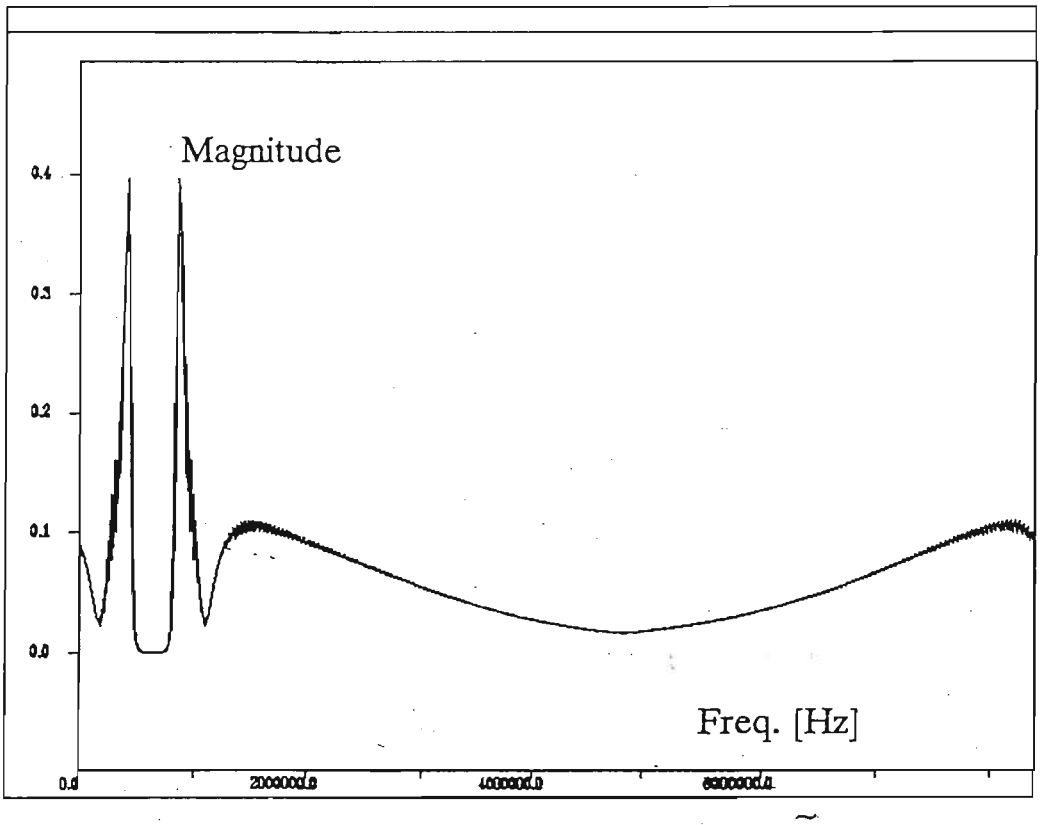

Figure 4.4.2.4 Circularly shifted - amplitude response $\tilde{R}_{(k+75\ KHz)mod\ 1000KHz}$

$$\tilde{R}_k = \begin{cases} R_k & k = 0 \text{ to } N-1 \\ R_{2N-k} & \text{for } k = N+1 \text{ to } 2N-1 \\ R_{N-1} & k = N \end{cases}$$

$$\tilde{\theta}_k = \begin{cases} \theta_k & k = 0 \text{ to } N-1 \\ -\theta_{2N-k} & \text{for } k = N+1 \text{ to } 2N-1 \\ 0 & k = N \end{cases} \qquad (4.4.2.1)$$

and the resulting amplitude and phase response $\tilde{R}_k$ and $\tilde{\theta}_k$ are shown in Figure 4.4.2.1 and Figure 4.4.2.2. After taking the IFFT of this waveform the impulse response (Figure 4.4.2.3) shows a pulse delayed by 0.34 ms, which is slightly longer than that expected from a pulse traveling at the speed of the light (0.33ms). There are two other smaller response delayed by the 1.02 ms and 1.72 ms which represent the first and second reflections. These travel the line length three and five times respectively, which explains their reduced amplitudes with respect to the main response of -12.4 dB and -25.7 dB respectively. The amplitudes are measure by the maximum peak to peak amplitude of the non-transient section. Furthermore, there are two small peaks in the response at 0.57 ms and 0.8 ms caused by reflection from the transpositions. It is difficult to measure the relative amplitude of the first of these, because it is overlapped by ringing from the main signal. However, the second is some 28 dB down on the main response.

All the reflections and other responses cause ISI, but whether it is significant depends on the particular modulation. For the modulation used, QAM-16, noise and interference has to be kept below -20 dB of the signal. The ISI should be kept at least 10 dB below this level (-30 dB), because there are many other sources of interference and noise. The transversal equaliser should cover all responses above this limit.

All the responses of the Figure 4.4.2.3 are accompanied by a significant amount of ringing, at a frequency of the about 26 KHz, the frequency of the resonance. This suggests that there is a significant amount of energy at this frequency, which might limit the applicability of the results. The lower band limit for PLC communications is in the region 40 KHz to 80 KHz and does not include the resonance around 26 KHz. A better approach is to consider the impulse response of a single bandlimited data channel, in which case only the frequencies of interest will be included.

The carrier frequency is selected to represent near worst case ISI condition and this occurs at low frequency of 75 KHz. The analysis proceeds as follows: first the 75 KHz response is mixed down to baseband and then bandlimited with a lowpass filter. This is equivalent to bandpass filtering the signal prior to down conversion. Secondly, IFFT is taken to get the impulse response of the bandlimited channel. The mix down procedure is performed in the frequency domain by a circular right shift operation on the concatenated frequency response of the figure 4.4.2.1 (Figure 4.4.2.4) and Figure 4.4.2.2 (Figure 4.4.2.5).

$$\tilde{H}_k(75) = \tilde{H}_{(k+75\ \mathrm{KHz})\mathrm{mod}[1000\ \mathrm{KHz}]} \qquad (4.2.2.1)$$

The resulting spectrum has a complex impulse response, because the required even and odd features of the real and imaginary parts of the spectrum no longer hold. Filtering is also performed in the frequency domain. The cut-off frequency of the low pass filters is selected to be 8 KHz and a second order Butterworth approximation ($\tilde{A}_k$) is used (Figure 4.4.2.6). In any practical modem design these filters would not only reject noise and other signals operating on different carrier frequencies, but also act as anti-aliasing filters for the analog to digital conversion process which normally follows.

The overall impulse response is obtained by using the IFFT

$$h_n(\text{narrow band}) = \mathrm{IFFT}(\tilde{H}_k(75) \times \tilde{A}_k) \qquad (4.4.2.3)$$

and the complex impulse response is shown in Figure 4.4.2.7 and Figure 4.4.2.8. The major feature of the response is the effect of the filtering. The first reflection at 1.02 ms can still be seen but significantly reduced (-31 dB) and is just below the threshold of -30 dB, where it can be neglected from the equalisation point of view. This will not be so for shorter lines because the relative reflection power will increase. A 100 Km line length appears to be close to the limit, where the reflected wave has to be accounted for in the modem design. It is therefore proposed that the equaliser on a QAM-16 digital PLC modem should cover the first reflection on a 100 Km line, that is the length of the transversal delay line should be at least 1.02 ms - 0.34 ms = 0.86 ms long. Shorter lines will give larger reflections, but these will be covered by the equaliser. Longer lines will give reflections not covered by the equaliser, but these will have negligible power. At the proposed symbol period τ = 0.125 ms the

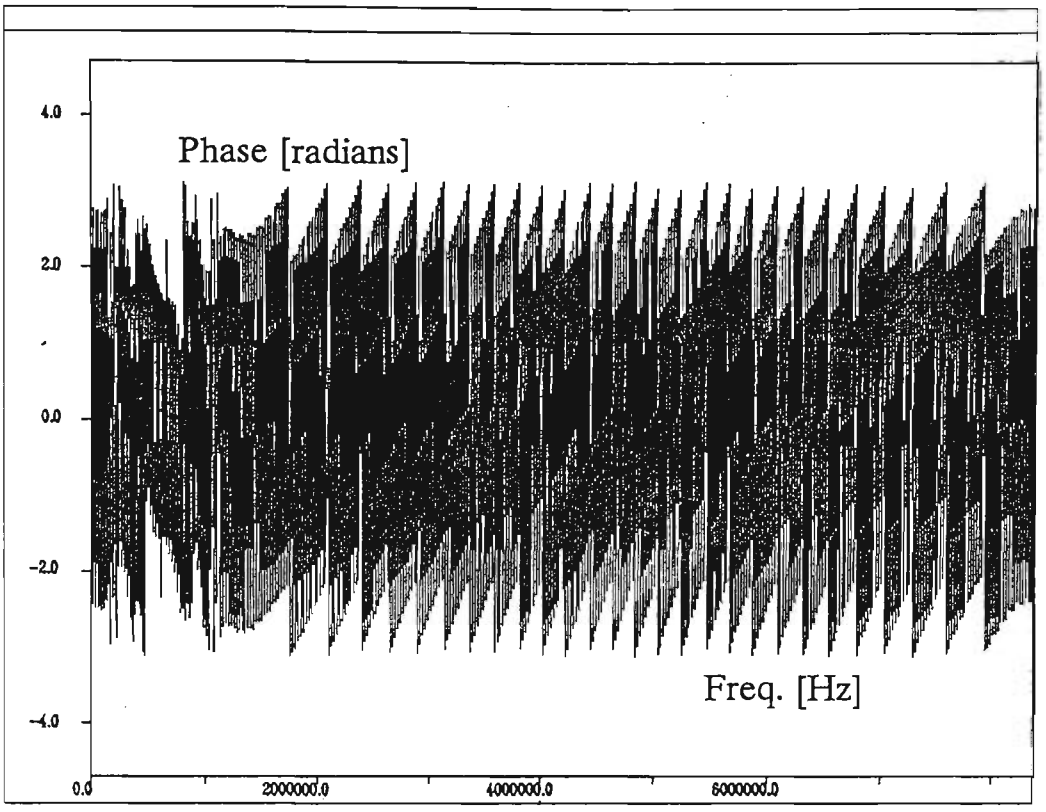

Figure 4.4.2.5 - Circularly shifted - phase response $\tilde{\theta}_{(k+75KHz) \bmod 1000KHz}$

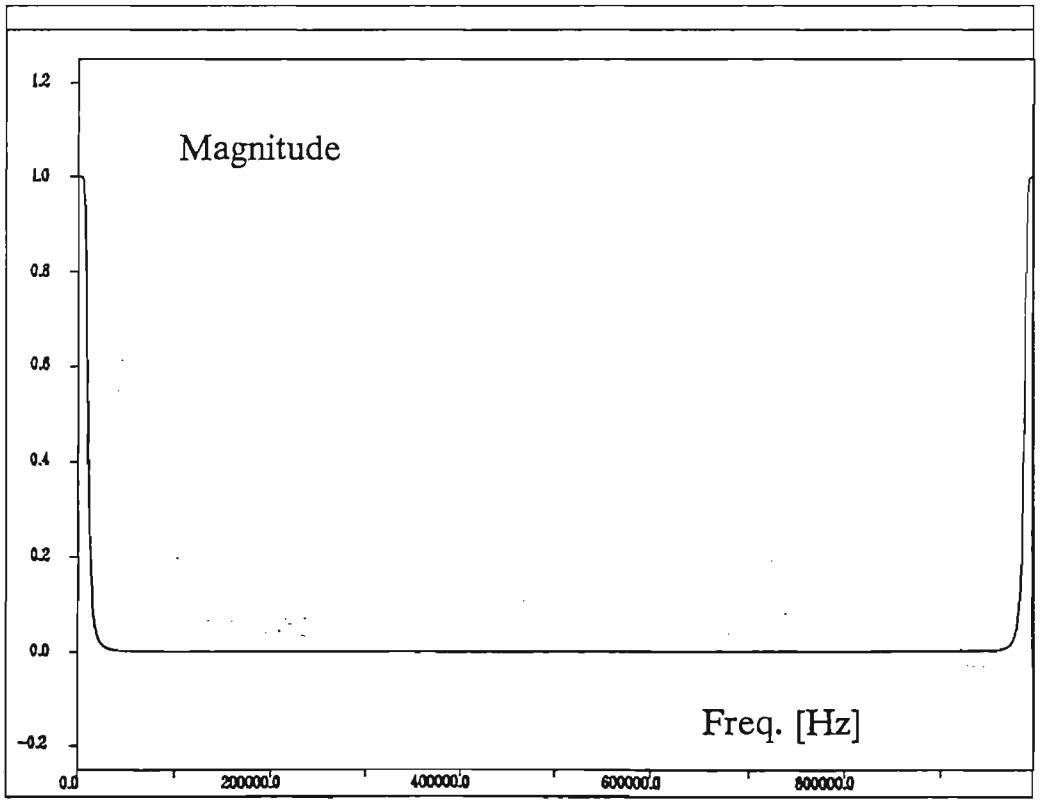

Figure 4.4.2.6 Concatenation - filter frequency response (magnitude) - $|\tilde{A}_k|$

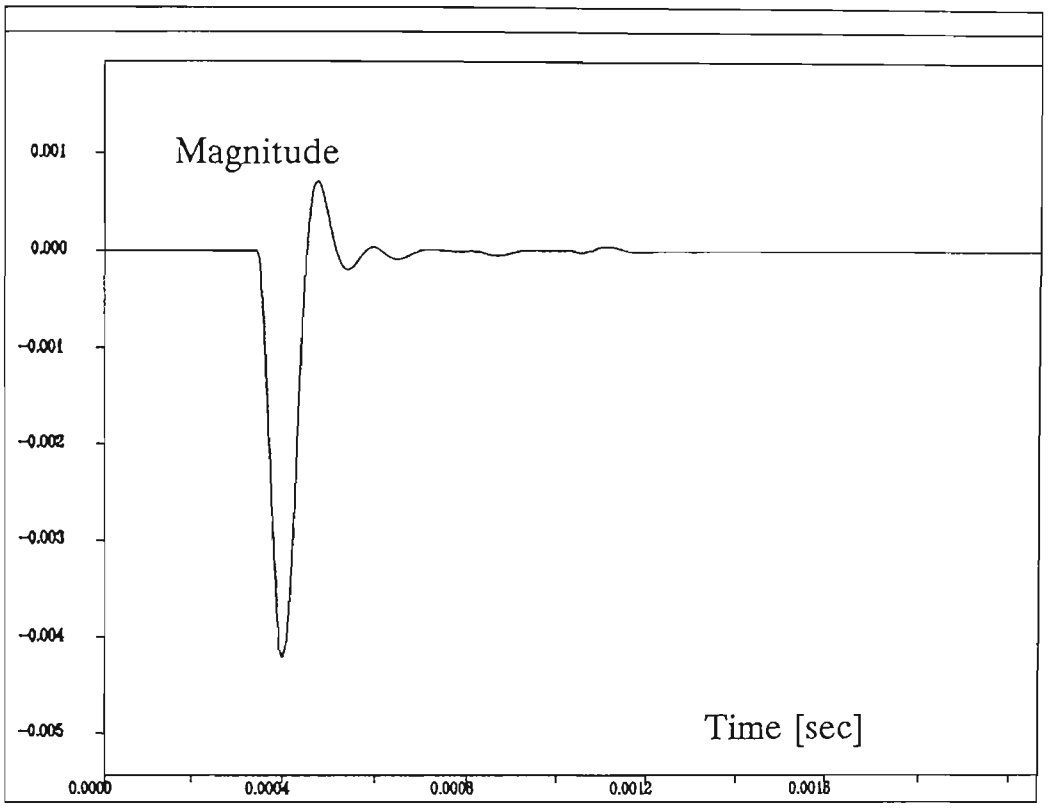

Figure 4.4.2.7 Baseband impulse response of bandlimited system - h_n (narrow band) - real part

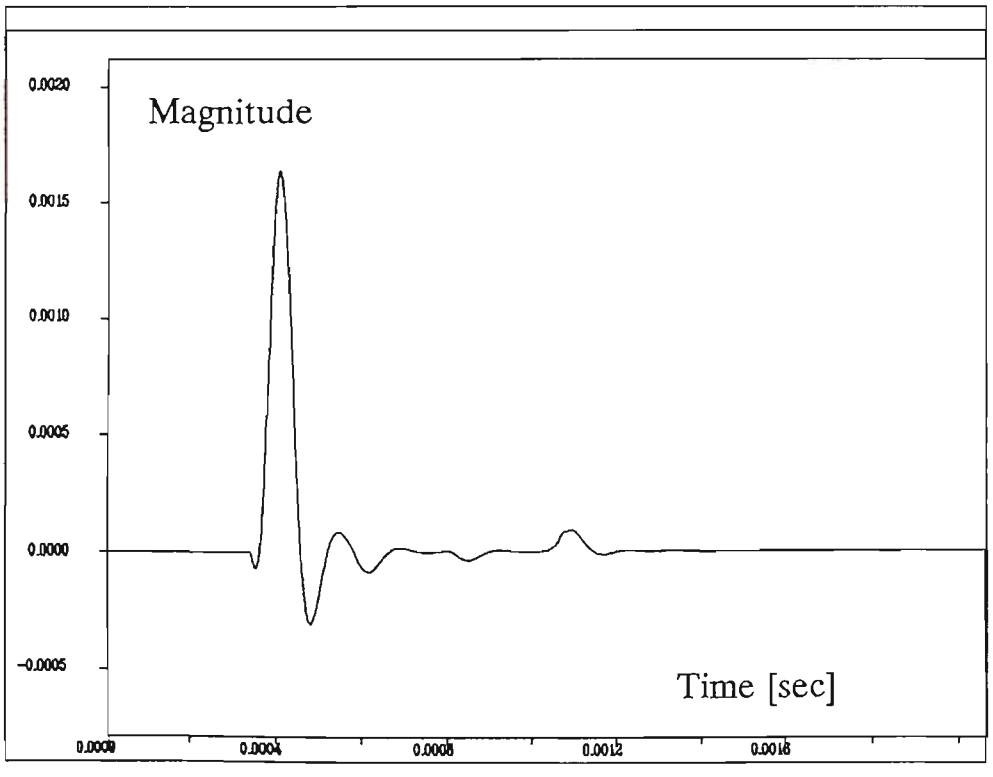

Figure 4.4.2.8 Baseband impulse response of bandlimited system - h_n (narrow band) - imaginary part

equaliser will require 8 taps (m = 7) to give a time length T = 0.875 ms, or 15 taps if a fractionally spaced ($\tau/2$) equaliser structure is chosen. Equalisers of this complexity are not hard to implement, and it should be possible to use current technology digital signal processor to perform this function.

5 Modem - part I

5.0 Introduction

This chapter begins by describing the major design features of a digital modem suitable for operation in a PLC environement (section 5.1). The section 5.2 gives details of a simulation program that was developed to aid in the evaluation of different design trade-offs. Details of the QAM-16 modulation are given in the section 5.3, and include coding, mapping and pulse shaping aspects. Section 5.5 describes hardware and implementation aspects of the data modulator including a small section 5.4 on multirate processing which is used extensively in the both the transmit and receive algorithms. The analog up-conversion circuits are described in the section 5.6, and because of the similarity of design, the receiver down conversion circuits are also covered in this section. The complex signal processing algorithms required to perform the demodulation in the receiver are left to chapter 6.

5.1 PLC modem

The major block of the PLC modem are illustrated in Figure 5.1.1. Opeations at the transmitter include differential encoding in the data (needed to remove carrier phase ambiguity), mapping the data four bits into symbols, pulse shaping to obtain the desired spectral characteristics and up-conversion to the selected PLC carrier frequency. The receive side processing is the reverse, but additional blocks are necessary for carrier recovery, synchronisation and equalisation.

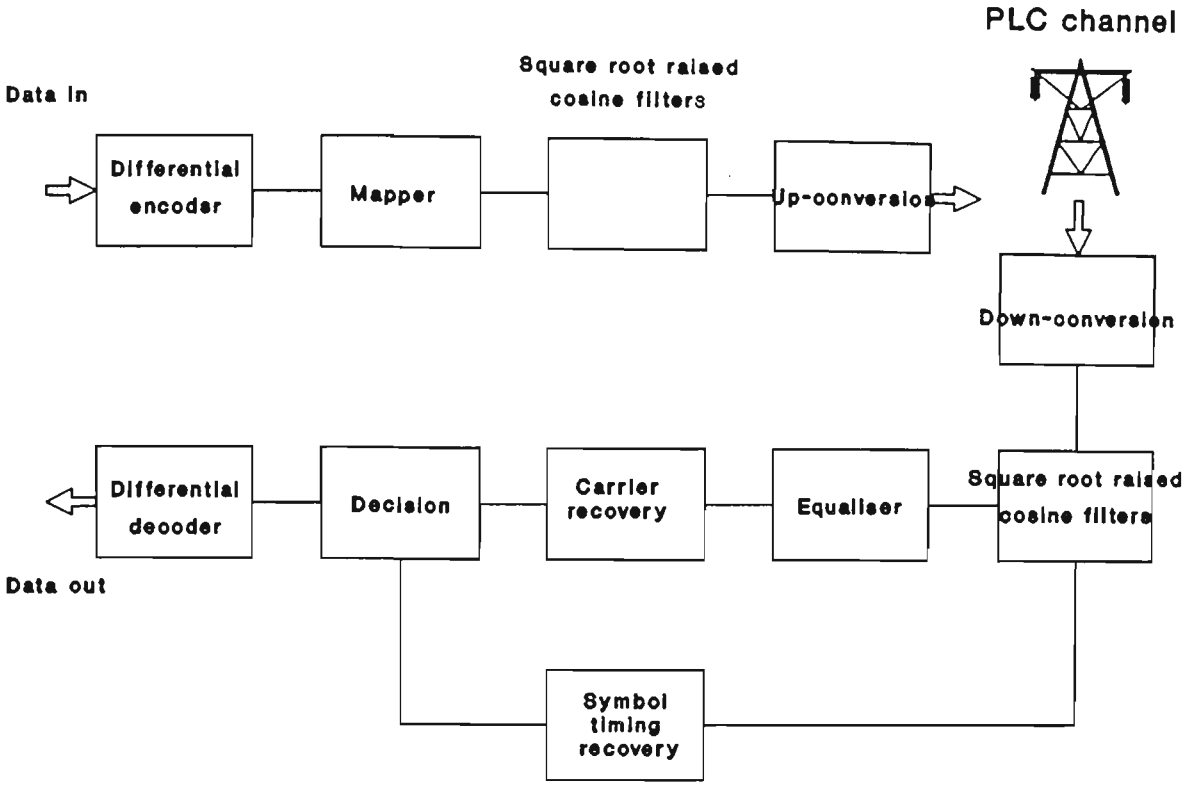

Figure 5.1.1 Modem block diagram

Traditional analog techniques have been used for low precision filtering and high frequency operations such as mixing etc. DSP (Digital Signal Processing) techniques have been used for the implementation of more complex tasks such as carrier recovery, bit timing recovery, equalization, pulse shaping and so forth. Furthermore DSP techniques facilitate the difficult process of algorithm implementation and development.

A more detailed block diagram of the modulator is shown in Figure 5.1.2. Bold lines represent DSP operation, while faint lines represent analog operation. This mapper combines four input bits to produce one complex symbol burst. The in-phase (real) and quadrature (imaginary) parts of the symbol are processed separately. They are shaped by square root raised cosine filters, converted to the analog signal (D to A conversion), passed through analog low pass filters (reconstruction filters), and finally modulated by a quadrature mixer and summed together. The digital section of the modulator is implemented on a Texas Instrument TMS 320C25 DSP microprocessor system.

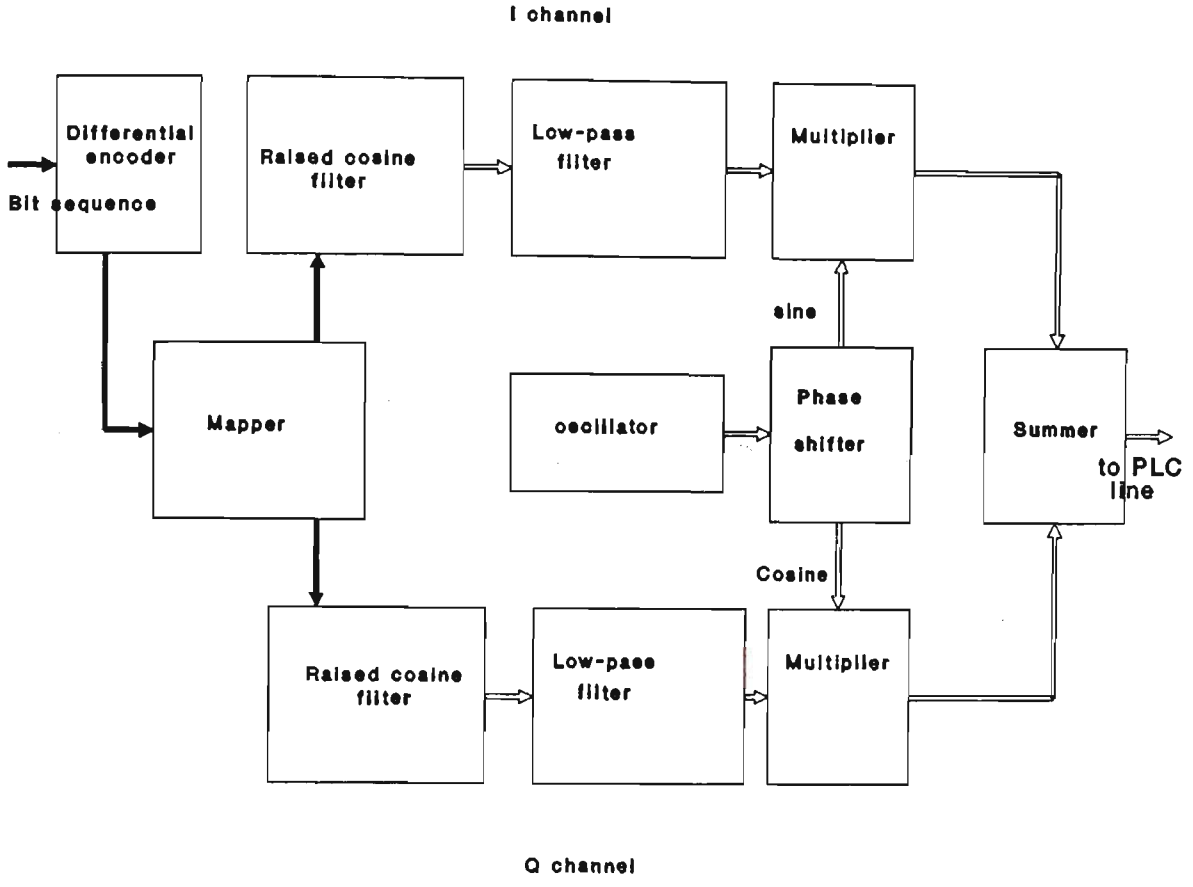

Figure 5.1.2 Modulator block diagram

The received signal is mixed down to baseband using a quadrature demodulator (Figure 5.1.3), low-pass filtered, sampled and then passed on to the DSP section for demodulation. The demodulated signal will, however, consist of the baseband signal plus the translated noise term. Even more, the detector requires a reconstructed carrier in order to operate. Before a receiver can begin to decide which of the various symbols it is receiving, it must establish symbol timing. Therefore, a function block for timing recovery is included, which synchronize the local clock with the timing of the received symbols. In addition the local oscillator must be synchronised to the transmit carrier oscillator. This is not possible without a separate synchronisation channel, so a phase rotator is needed to cancel out any phase error between the two oscillators. The equalizer attempts to undo the channel distortions. Functional blocks implemented by analog means are drawn by faint lines, while the digital ones are drawn by bold lines. The digital section of the demodulator was also implemented on a TMS320C25 system.

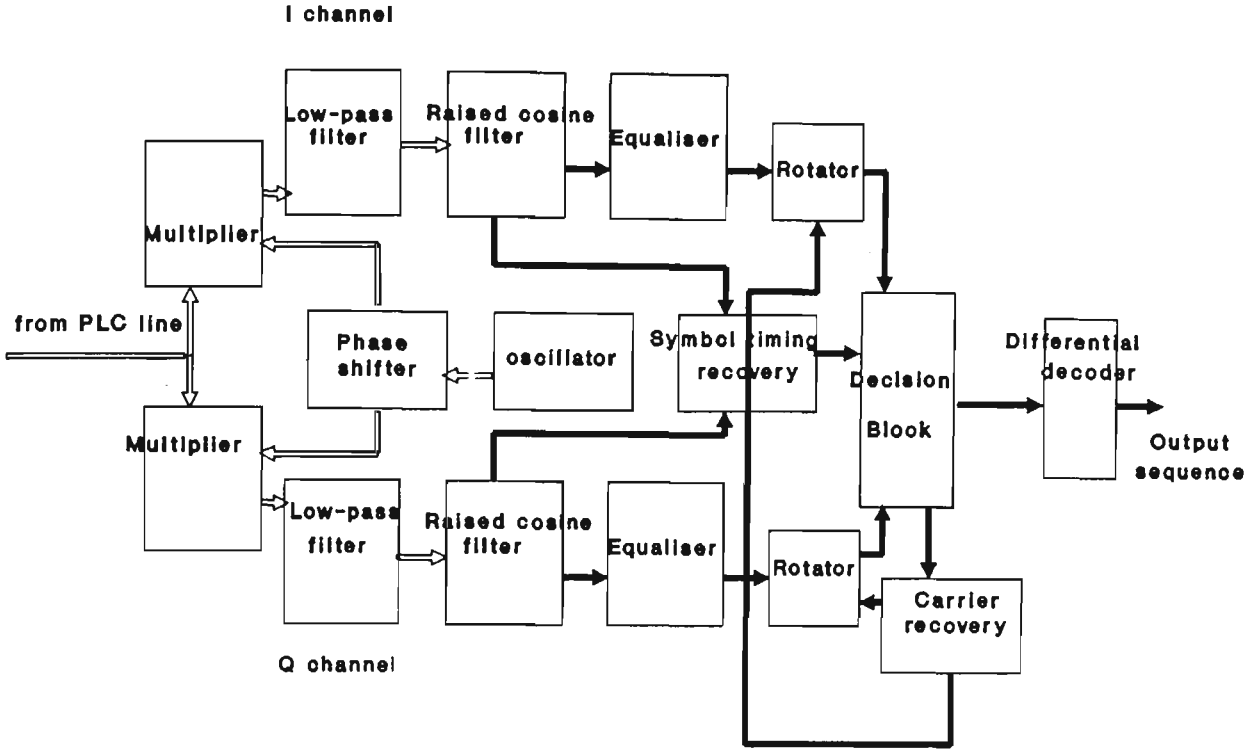

Figure 5.1.3 Demodulator block diagram

5.2 Simulation program of PLC modem

Simulation has become an increasingly common tool for the prediction of system performance. The simulation block diagram of the program developed in Turbo C on IBM PC compatible computer is shown in Figure 5.2.1. Special consideration was done in the noise algorithm design. It was necessary to design I and Q noise components, which are supposedly indenpendently normally distributed.

The software generally follows the transmitter and receiver structure of Figure 5.1.2 and 5.1.3 but with some simplifications. The signal is represented in complex baseband (I and Q representation) throughout and, as a concequence, there is no up-conversion and down-conversion to a carrier frequency. The channel blocks adds noise (a random signal - Box Muller method) to the I and Q signals and simulates a single complex reflection by adding to the signal an appropriately scaled and delayed version of itself. The two square root raised cosine pulse shaping filters (one on the

transmit side and one on the receive side) have been implemented as one reduced length (44 taps) raised cosine filter on the transmit side to minimise simulation time. on the transmit side to minimise simulation time. In simular way the two analog Butterworth filters have been cascaded into one block and, because they are continuous time filters, they are implemented at an increased sample rate (interpolation factor of 256). The pseudo random binary generator used a maximal length sequence algorithm. The differential encoder and decoder operations were not included in the program, and a different signal constellation was used (Gray coded), because at the stage of simulation of the PLC modem, the phase ambiguity problem was not detected. Other blocks which are included in the software but not shown are for the error rate counting and signal analysis.

5.3 Digital modulation

A transmission of the baseband sequence {a(n),b(n)} can be accomplished by using two separate modulation carriers, a sine wave and a cosine wave. These waves are orthogonal. The information in the direction of the one wave is independent of the information in direction of the other wave, and therefore this information is recoverable. The possible realization of the pair {a(n),b(n)} can be represented as points in two dimensional signal space. QAM-16 (quadrature amplitude modulation) has such 16 points. The baseband sequence that modulates the cosine wave is called the in-phase sequence, while the baseband sequence that modulates the sine wave is called the quadrature-phase sequence. The part of the transmitter/receiver that processes the in-phase is commonly referred as to as I channel, while the other part is referred to as the Q channel.

The class of two-dimensional signal constellation includes phase modulation, quadrature amplitude modulation (QAM, in which the points form a rectangular grid) and more general patterns corresponding to combined amplitude and phase modulation. Several signal constellations were analyzed.

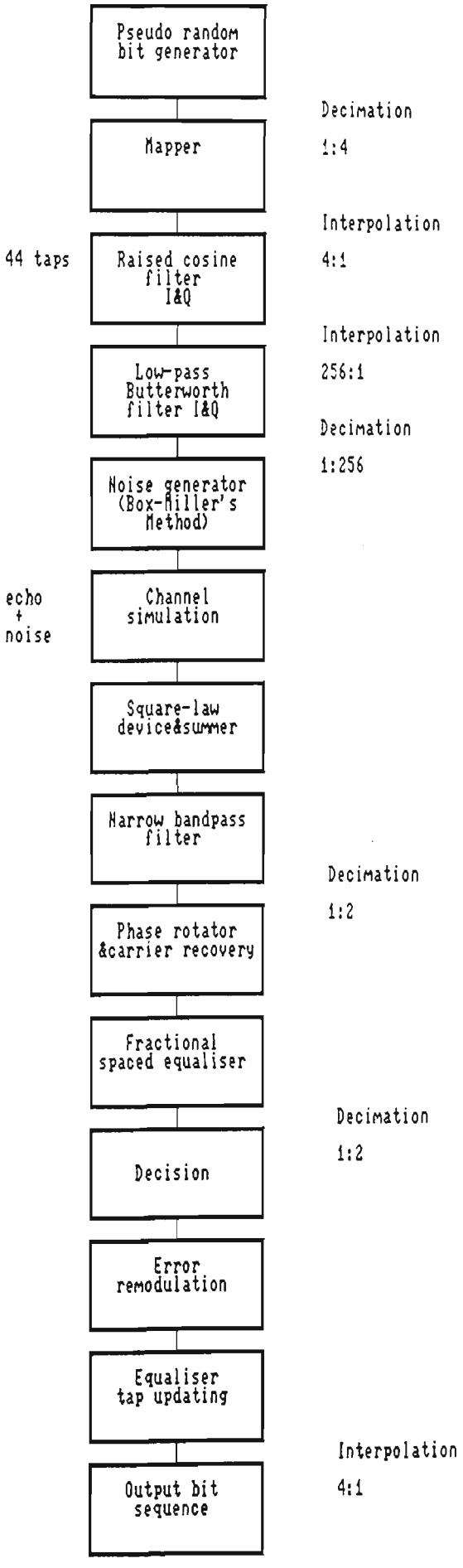

Figure 5.2.1 Simulation program - flow diagram

For example an "optimal" signal constellation (provides the best possible resistance to additive noise under an average power constraint despite its unsymmetrical appearance) offers a small advantage in the terms of the signal to noise ratio over the rectangular constellation (less than 0.5 dB in the 16-point example), but its implementation is considerably more difficult and complex [30,31].

The "V.29" signal constellation (adopted as a CCITT standard for 9600 bps private-line voiceband telephone modems) provides a better performance in terms of fluctuations of carrier phase. Unfortunately, it is more sensitive to additive noise than the rectangular signal constellation, since for the same average power it has a smaller distance between the closest pair of signal points. The 16-point rectangular constellation is also very popular, and it is appealing for its simplicity and relatively good resistance to noise, and that was the main reason why this structure was selected for the PLC modem application in the specific noisy environment.

QAM is a combined amplitude and phase modulation scheme. QAM-16 is a modulation scheme with 16 transmitter states, and can be represented by:

$$V_{mod} = a(n)\cos wt + b(n)\sin wt \qquad (5.3.1)$$

where $0 \leq t \leq T$. T is the symbol interval (four times the bit interval T_b), and a(n) and b(n) are four-level PAM (pulse amplitude modulation) baseband sequences. QAM-16, the modulated carrier, can be viewed as having two vector components: the in-phase I, and the quadrature Q, each of which may take one of four possible values (Figure 5.3.1).

The carrier recovery used in coherent detection usually suffers from a problem known as phase ambiguity. QAM-16 is two-dimensional signal; owing to the symmetry of the constellation, there is a fourfold phase ambiguity in data recovery. This means that the carrier may shift the phase of the received signal vector by 90°, 180° or 270°. The problem of phase ambiguity is overcome by the use differential encoding, although it increases the probability of symbol error compared to the uncoded case. Information is carried by the change in phase, rather than by the absolute phase. Proper operation of a differential decoder depends on the decision being correct in the receiver. If a single decision is incorrect, two symbol intervals will

be incorrectly decoded, so there is an error propagation, but the impact of this error propagation is usually minimal.

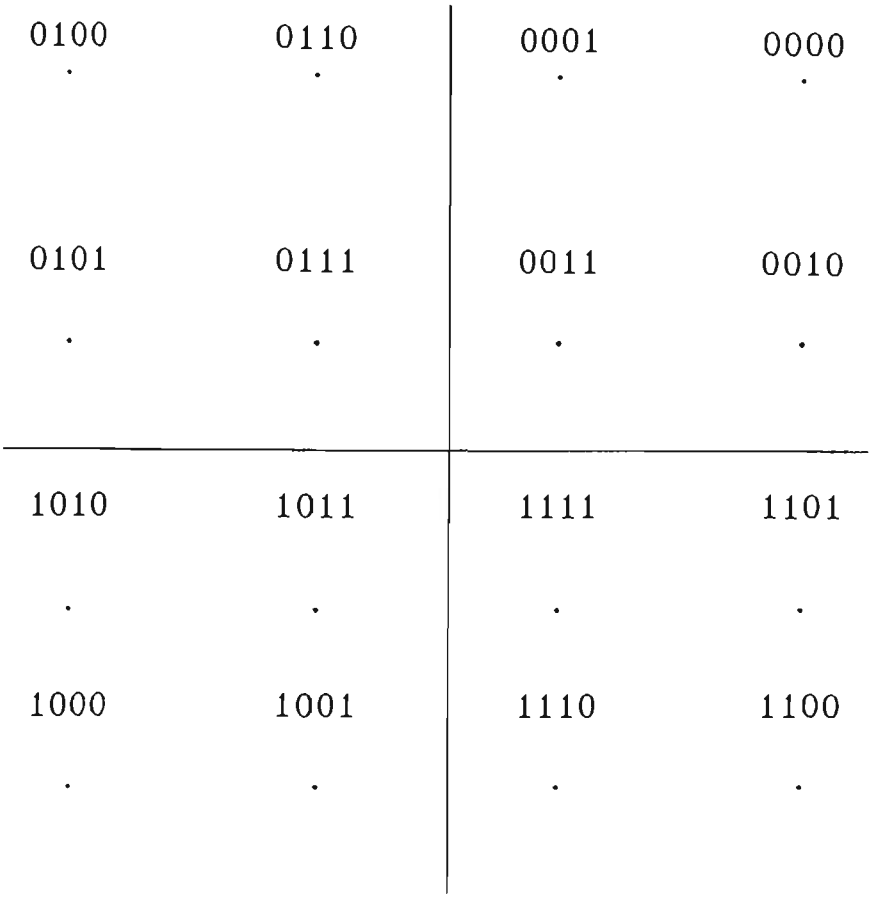

Figure 5.3.1 Rectangular signal Constellation

However, the probability of bit error can be minimized by the proper assignment of the bits to the symbols; i.e. the assignment of bits to the symbols can be made such that its nearest neighbors differ in as few bits as possible.

A signal constellation is illustrated in the Figure 5.3.1. The first two bits are differentially encoded and represent the change in quadrant; the second two bits represent the points within the quadrant (Figure 5.3.1). It can be seen that, with the use of the constellation, the second two bits remain unchanged, even if the phase shift of 90°, 180° or 270° occurs in the receiver vector, so they do not require differential encoding. Only the first two bits require differential encoding. The first two binary digits determine the quadrant, and remaining two determine the position in the quadrant. The latter digits in any quadrant are the same as those in the all-positive quadrant, if this is

rotated to coincide with given quadrant. Thus phase errors of multiples of 90° do not cause decision errors, although smaller phases might.

Gray coding is an example in which each adjacent symbol differs by only one bit. For QAM-16 signals, unfortunately, it is not possible to have Gray coding after differential encoding. Gray coding cannot be achieved here over the whole of the signal constellation, but it is satisfied over the four points in each quadrant. By using a differential encoding scheme, at low error rates, the probability of errors is about 1.67 times that of a 16-ary QAM system [34].

The information to be transmitted is carried by binary digits $\{b_i\}$, where $b_i=0$ or 1. When the encoder has received b_{4i}, b_{4i+1}, b_{4i+2} and b_{4i+3}, it encodes the higher two bits b_{4i} and b_{4i+1} into e_{4i} and e_{4i+1} according to the adder (modulo 4) algorithm (see Table 5.3.1). Then it converts e_{4i}, e_{4i+1}, b_{4i+2} and b_{4i+3} into the corresponding signaling elements I and Q according to the signal constellation given by the Figure 5.3.0.1. The decoder shown in Figure 5.3.2 performs reverse encoding.

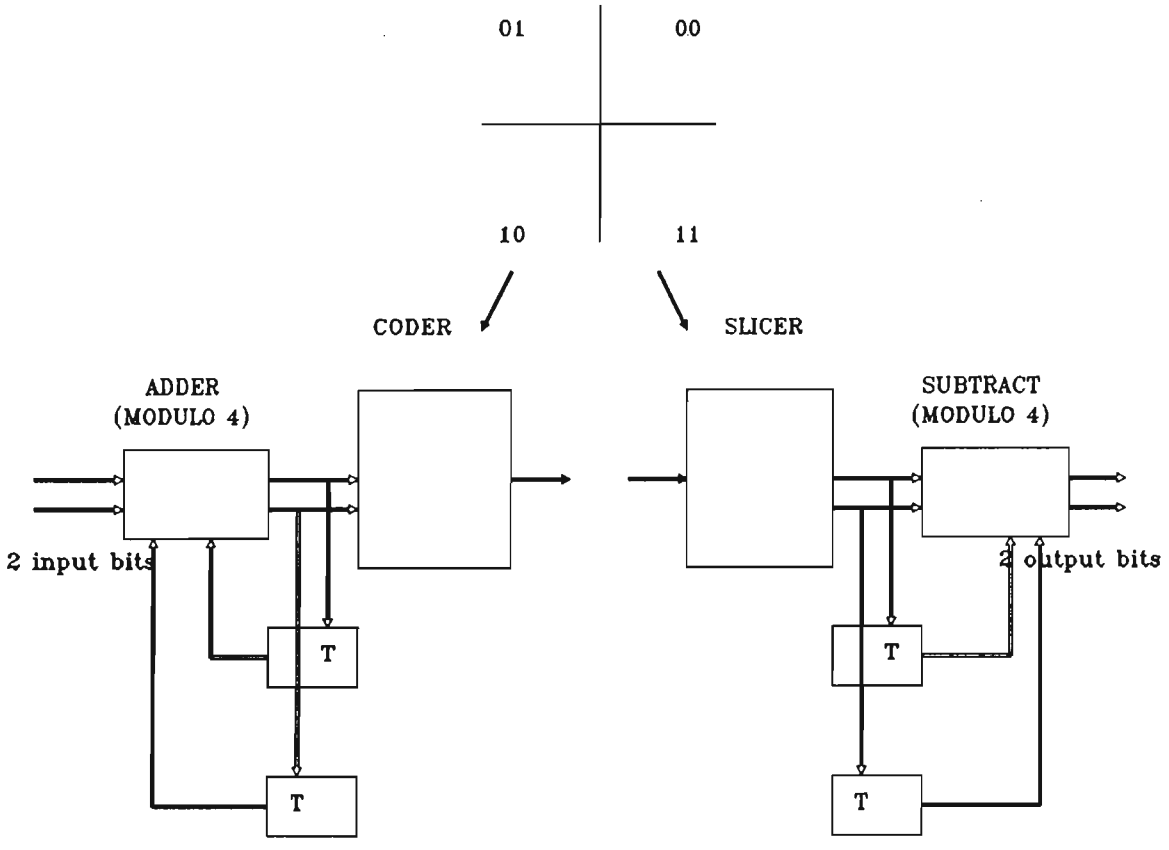

Figure 5.3.2 Differential encoding and decoding

current		previous		output	
b_{4i}	b_{4i+1}	$e_{4(i-1)}$	$e_{4(i-1)+1}$	e_{4i}	e_{4i+1}
0	0	0	0	0	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	1	1
0	1	0	0	0	1
0	1	0	1	1	0
0	1	1	0	1	1
0	1	1	1	0	1
1	0	0	0	1	0
1	0	0	1	1	1
1	0	1	0	0	0
1	0	1	1	0	1
1	1	0	0	1	1
1	1	0	1	0	1
1	1	1	0	0	1
1	1	1	1	1	0

Table 5.3.1 Differential Encoding

The bit stream e_{4i}, e_{4i+1}, b_{4i+2}, b_{4i+3} is the output bit stream.

Pulse shaping shaping is required to eliminate ISI (inter symbol interference) at the sampling instances while at the same time constracting the bandwidth of the transmitted signal. Nyquist demonstrated that ISI could be controlled by the use of a filter with a skew symmetric amplitude response and a linear phase response. The frequency at which response is skew symmetrical is known as the Nyquist frequency. The raised cosine family of filters has this property and its impulse response is defined by the following formula [36]:

$$p(t) = \frac{\sin(\pi t/T)}{\pi t/T} \cdot \frac{\cos(\pi \beta t/T)}{1-(2\beta t/T)^2} \qquad (5.3.2)$$

where $0 \leq \beta \leq 1$, and is called the rolloff factor. This pulse has its maximum at $t = 0$ and is zero at all other sampling instants $t = kT$, as desired.
The passband QAM signal is represented as:

$$V_{mod} = a(n)p(t-nT)\cos wt + b(n)p(t-nT)\sin wt \qquad (5.3.3)$$

Its Fourier transform, P(f), is T for all $|f| < (1 - \beta)/2T$; zero for all $|f| > (1 + \beta)/2T$; and, in between, falls from T to 0 as the decreasing half of a cosine-squared pulse. The cosine rolloff pulse is strictly bandlimited; when translated to the passband, it spans a bandwidth of $(1 + \beta)/T_b$ (β represents the % excess bandwidth).

The choice of the β involves considerations. For instance β near 1 compromises spectral efficiency, but choosing β near 0 makes implementation more difficult and costly; transmission is made more vulnerable to impairment. Accordingly, the usual choice of β is close to 0.5.

The requirement for zero ISI has to be applied to the complete PLC channel. In order to conform to both Nyquist and matched filter criteria, it is necessary to split the filter equally, with a square root raised cosine response in both modulator and demodulator.

For this application the ADPCM specification of 32 Kbits and the bandwidth limitation of 12 KHz suggests a β value for the QAM-16 modulation of 0.5. However, the SECV suggested that a 2.4 KBit data channel has to be added for the purpose of supervision and control signalling. This would give a total bit rate of 34.4 Kbits and require a reduced β of 0.395 to bit into the same bandwidth. Unfortunately the development system used on the project only allowed the selection of certain sample rates, the nearest being 31.125 KHz. Frequencies and bandwidths were therefore

scaled to this rate. The specification of the modulator raised cosine pulse shaping filter (square root) is shown below:

Finite impulse response (FIR)
Linear-phase
Parks-McClellan Algorithm
Filter length = 120
Sampliong frequency = 31.250 KHz
Centre frequency = 3.906 KHz
Rolloff = 39.500 %
16 bit quantized coefficients

The frequency response and the unit sample response are shown in Figure 5.3.4 and in Figure 5.3.5. The stop band attenuation is about 45 dB. Ripples in the passband are nearly negligible. The price is 120 taps; which is the maximum number of taps which could be implemented by the existing hardware without employing slow external data memory. Reducing the number oftaps would reduce stop band attenuations and increase passband ripple. This would introduce distortion to the signal and also influence adjacent channels.

The filters were designed using the DFDP package of Atlanta Signal Processors Incoporated.

5.4 Multirate processing

Multirate systems are used whenever changes in the system sampling rate can produce a more efficient performance, resulting in reduction in the computational rate [37,38]. The sampling rate for the modulator was chosen to be the same as the data bit rate of the input sequence. As each symbol represents 4 bits the sample rate at the output is 4 samples/symbol (the minimal sampling is two samples per symbol). The symbol rate at the output of the modulator is 31.250 Kbs/4 = 7.8125 Ksymbol/s.

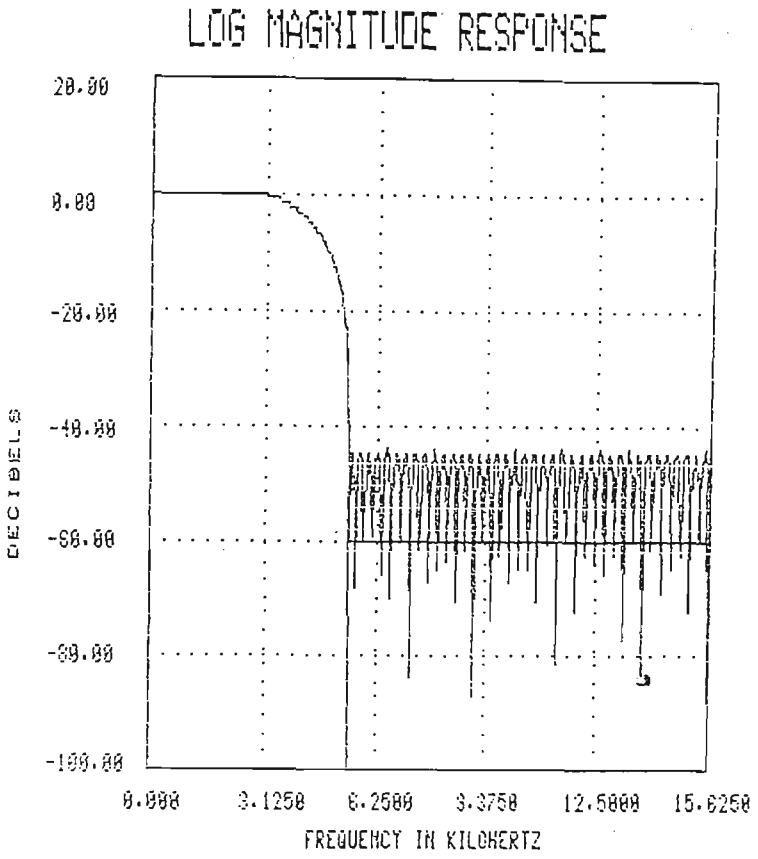

Figure 5.3.4 Log. magnitude response of square root raised cosine filter

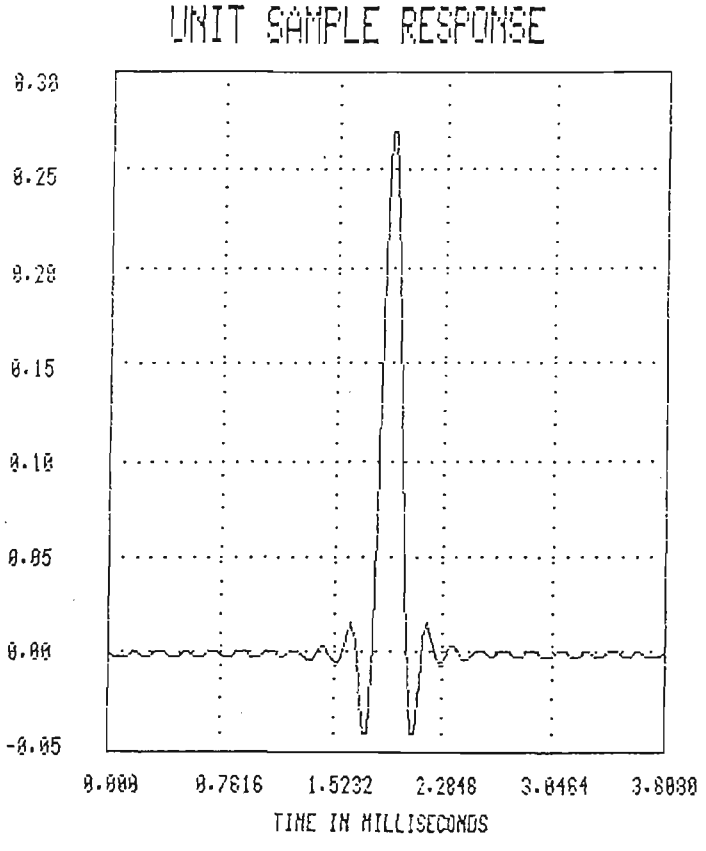

Figure 5.3.5 Unit impulse response of square root raised cosine filter

The number of taps of the square root raised cosine filter is 120 (for both I and Q branches). Considering that every fourth sample at the input of the filter is non-zero, some control logic can be provided to eliminate redundant computations. The sampling rate immediately before the modulator (at output points of D/A converters) is four times greater than the sampling rate at the input of the filters i.e. at the output of the mapper. Further efficiency in computation, as well as in terms of storage is gained by designing a polyphase network. The original filter was segmented into four sub-filters (each of 30 taps) to form a polyphase network. The filter coefficients are unchanged from the original, but reordered. The computations are executed not at the sample rate, but at the symbol rate; which is four times less than the sampling rate. The stored elements are now delayed by T, not by T_b, and storage requirements reduced by four. In Figure 6.3.1 the sample-rate expander is represented as a commutating switch at the filter output [52]. Sample rate down conversion (decimation) can be achieved using a similar techniques and is used in the receiver section.

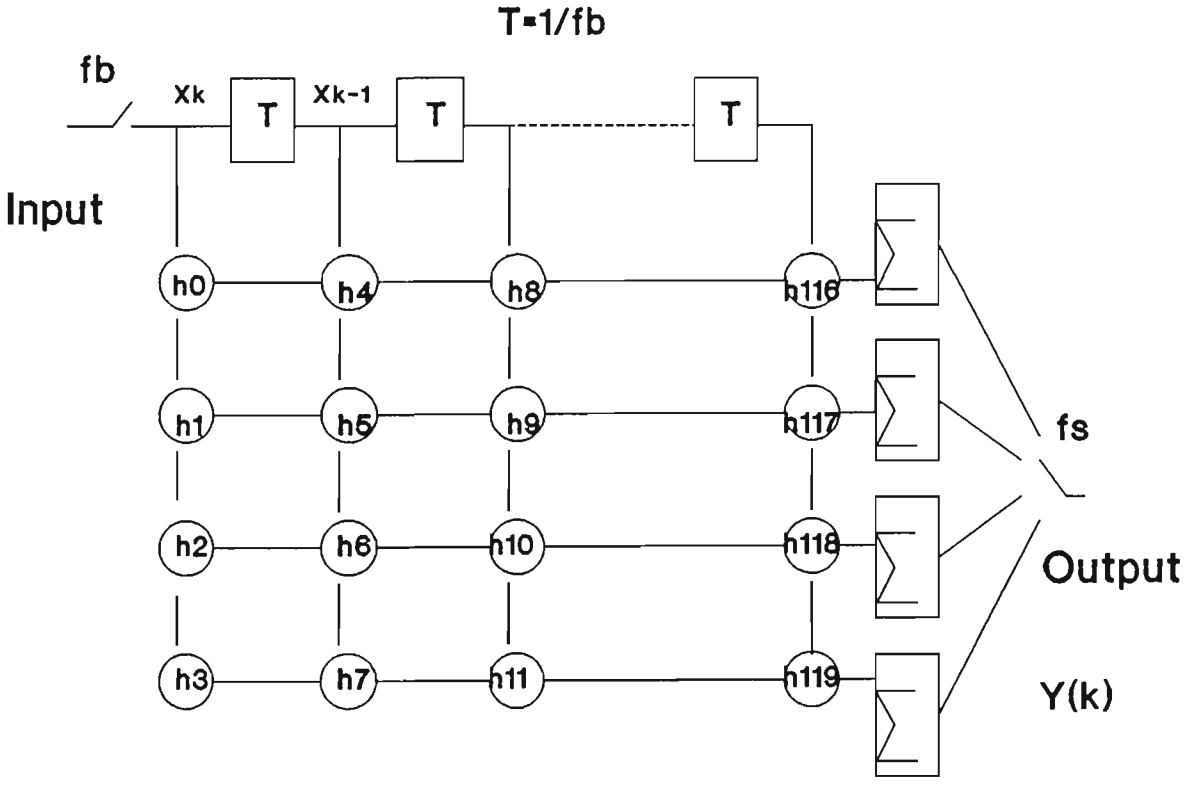

Figure 5.3.3.1 Polyphase interpolation filter

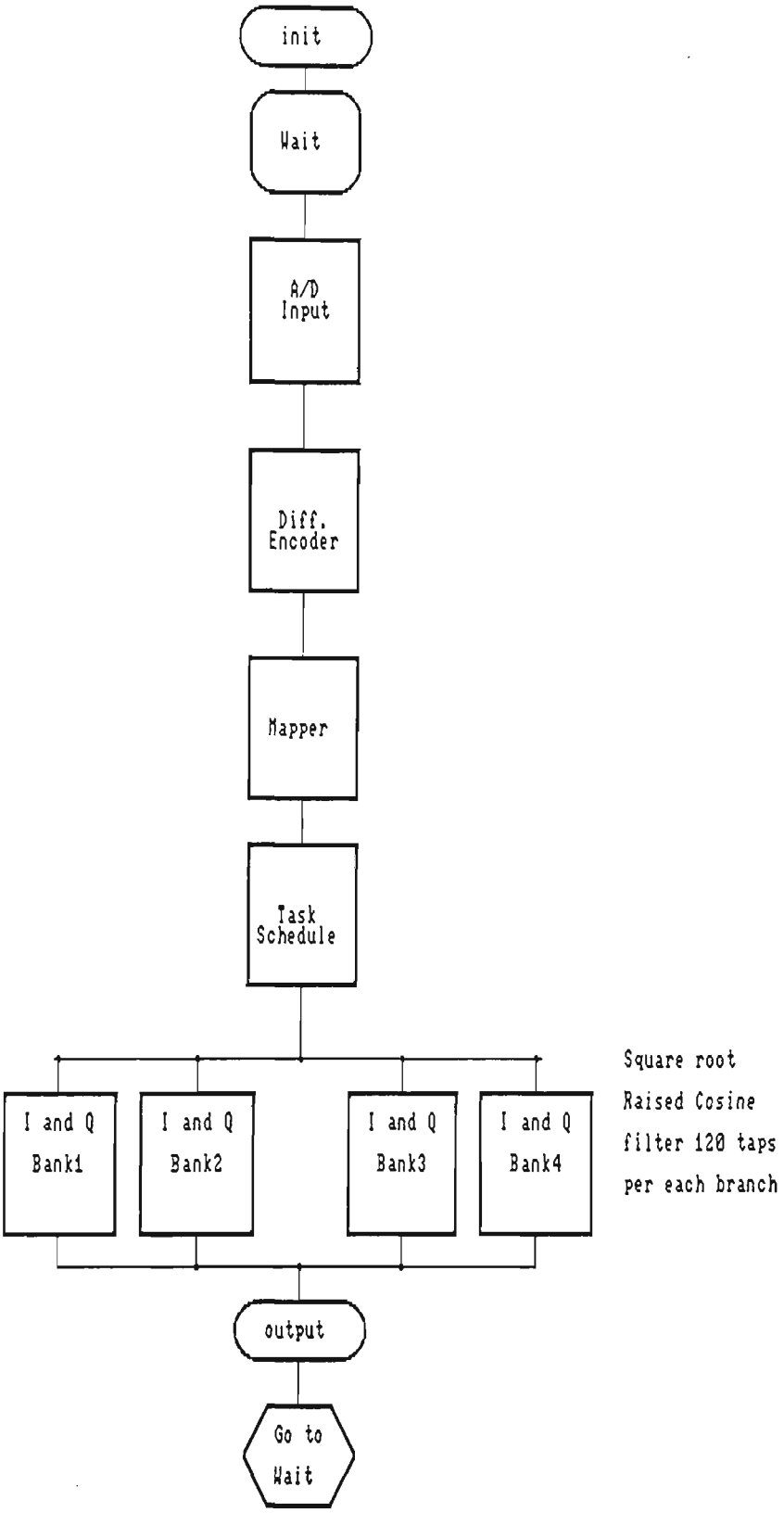

Figure 5.3.4.1 TMS 320C25 assembler modulator program modulator flow diagram

5.5 Modulator description

The digital part of modulator is based on an SPA-C25-1 general-purpose digital signal processing development card based on the Texas Instruments TMS320C25. A wide range of digital and analog I/O allows the user to develop a code for application in data communication, speech, frequency synthesis, spectral analysis etc. The card has two 12-bit D/A converters (National Semiconductor DAC1208LCN-1) and a 10 bit linear A/D converter (Analog Device AD7580JN) allowing sampling rates of 48 kHz.

Sampling frequency and switched capacitor filter cut-off frequency are programmable. A bidirectional DMA interface is also provided. Using a serial PC interface, the onboard monitor enables easy uploading and downloading of programmes or data, memory interrogation and modification, processor status display, breakpoints and single stepping. The processor used is Texas Instrument TMS320C25, 100ns DSP chip. The card was revised, modified and improved to meet requirements for the implementation of digital data modulation.

The following digital functions are performed on the card. Differential encoding, mapping and square root cosine filtering for both I and Q channels. The software flow diagram is shown in the Figure 5.3.4.1. Statistics are shown in the Table 5.3.4.1. The unit is fed by bits from a special pseudo random bit sequence (PRBS) generator (See Appendix 2). The generator was designed with a number of functions to aid in system debugging. These included variable lenfth sequences, a number of clock signals and a start of required pulse.

I and Q outputs are converted to analog signals via the on board DAC converters and then fed to the analog reconstruction filters which are described in the next section.

5.6 Analog section

This section describes the design of the analog section of this modem. Analog implementation is used for the design of active filters, frequency translators and so forth.

Table 5.3.5.1

Routine	Program memory	Data memory	Instr. cycles
Diff. Encoding	16	3	16
Mapping	35	2	9
Inter. filter	246	242	368
Overhead	120	35	76
Total	417	282	469

5.6.1 Analog modulator

After DSP processing, the I and Q signals move to the analog part of the modulator through D/A converters. Principal functional blocks of the analog section of the modulator are: low pass smoothing filters (one for each branch), a digital programmable crystal oscillator, 90° phase shift circuit, multipliers (one for each branch) and an analog summer. A block diagram of the demodulator is illustrated in Figure 5.6.1.1.

A continuous signal can be recovered without distortion from its ideally sampled version by a low-pass filtering. The ideal smoothing filter (reconstruction filter) has a flat gain response and linear characteristic in the passband, and an infinite attenuation in the stopband beyond. If the sampling rate is more than double the signal bandwidth, a finite transition region can be accommodated. In this case the baseband bandwidth of the signal is 5.448 KHz (3.906.(1+0.395)), and the first image occurs at 25.8 KHz (31.25 KHz-5.448 KHz), which gives a transition band of 20.4 KHz. The amount of attenuation required in the stopband depends on the usage of the nearby channels, but similar digital PLC systems would require any interference to them to be at least 30 dB below their receive signal level. For nearby channels travelling in the same "GO" direction 40 dB (30 dB + safety margin) attenuation should suffice, but for the signals in the opposite "RETURN" direction should be increased by the line attenuation. For this project, we chose a figure of 60

dB, which should cater for line losses to 30 dB. When the line losses are greater frequency planning must be used to avoid the contaminated channels in the "RETURN" direction.

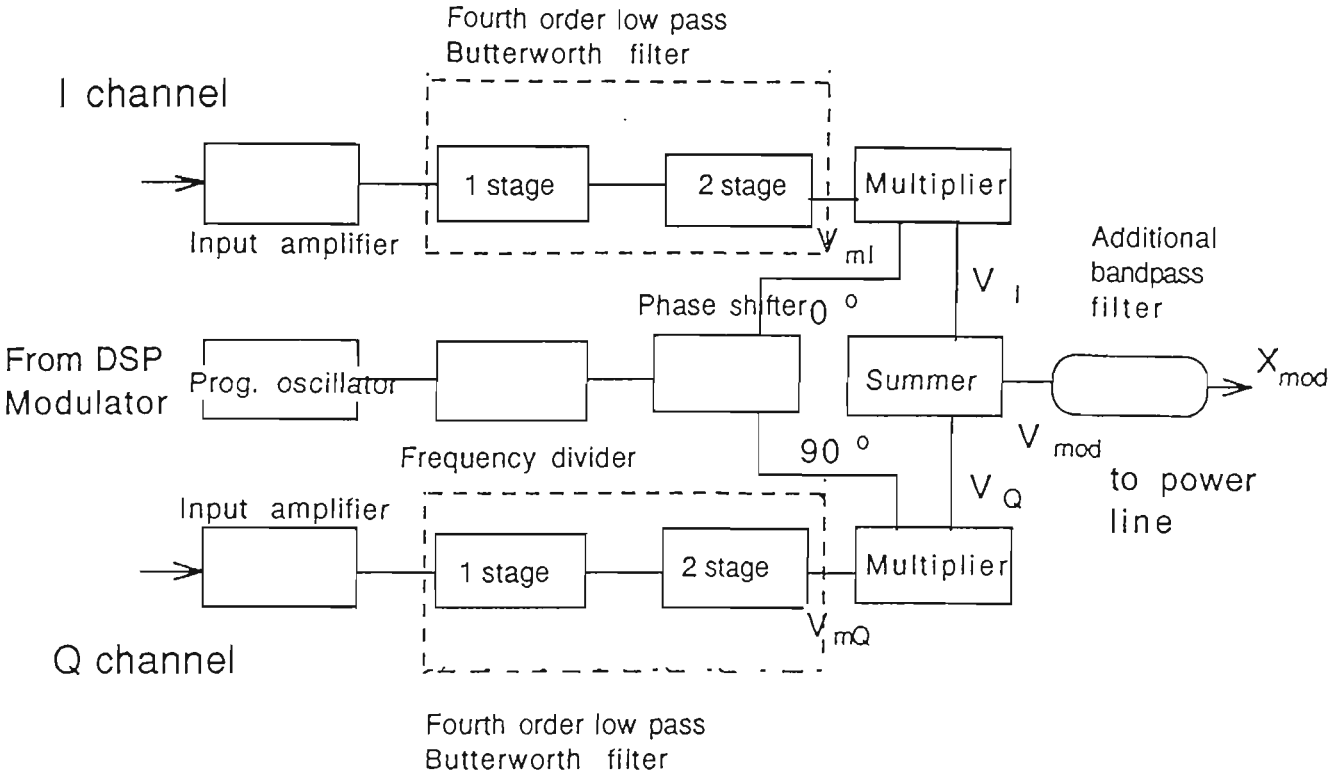

Figure 5.6.1.1 Block diagram - analog section of the modulator

Butterworth filters were selected for the both modulator reconstruction filters and demodulator anti-aliasing filters. Butterworth filters offer a compromise solution between steepness of roll-off in the transition band, and phase distortion in the passband. The alternative choices were Bessel filters which are linear phase (no phase distortion), but have a poor roll-off, and elliptic or Chebyshev which have a fast roll-off but poor phase response.

A fourth order Butterworth with cut-off frequency of 6 KHz will provide over 48 dB of attenuation at the first image. This improves to over 60 dB when the

$\text{sinc}(\pi f/f_s)$ responses of the the DAC's are included. Two cascaded 2nd order biquadratic stages implement the filter. Design equations for this type of filter are given in [33], and the resulting circuit is shown in Appendix 3.

In this case it is possible to use a square wave carrier waveform instead of a sinusoid waveform. By using the Fourier series the square wave carrier could be represented as follows:

$$v(t) = (2A/\pi)\sin\ 2\pi f_c + (2A/3\pi)\sin\ 2\pi(3f_c) + \ldots \qquad (5.6.1.1)$$

where f_c is the frequency, and A/2 is the amplitude of the square wave sequence. From the equation it is evident that third harmonics (and other odd harmonics beyond) could cause significant interference to the other channels. Filtering has to be included to cancel out the odd harmonics.

A programmable crystal oscillator ICO 1000 was used to generate the carrier waveform. It can generate 57 different output frequencies from one internal crystal oscillator. This signal feeds a digital 90° phase shifter which was implemented simply by two D latches and one inverter. The pulse waveforms at the output of the latches are in phase quadrature whatever the input frequency. The pulses have to have a duty cycle of 50 %. A circuit with the function "frequency division by two" has to be included immediately after the crystal oscillator, to guarantee a 50% duty cycle. The two quadrature carriers are used to frequency translate (multiply) the I and Q baseband signals to the desired channel frequency, in this case 75 KHz.
The frequency translation is performed by wideband four-quadrant multipliers (National Semiconductors MC 1495). They can operate as a balanced modulator\demodulator for frequency up to 3MHz. The multiplier's balanced modulator configuration is illustrated in Appendix 4. It simply multiplies the carrier - pulse waveform with the modulated signal immediately after the smoothing filter. Care has to be taken in order to minimize high-order intermodulation product and mixer feedthrough (leakage). The multiplier outputs are given by:

$$v_I = k\, v_{mI} v_c(t) \qquad (5.6.1.2)$$

and:

$$v_Q = k\, v_{mQ} v_c(t).\, e(j\pi/2) \qquad (5.6.1.3)$$

where k is a constant, v_I is the I channel signal at the output of a multiplier, v_Q is the Q channel signal at the output of a multiplier, v_{mi} is the I channel signal at the input of a multiplier, and v_{mq} is the Q channel signal at the input of a multiplier. The gain is externally adjustable by selecting appropriate values of resistors. It is necessary to adjust the squarewave carrier signal, from TTL to bipolar signal level for this circuit. It is also necessary to adjust by the potentiometers on the card to minimise carrier leak and signal leak in the output.

For the implementation of the analog summer a high speed operational amplifier LM 6361 was selected. It has a high slew rate of 300 V/μs, and a 50 MHz gain stability. It exhibits a high stability with a large capacitive load.

The output of the summer is the QAM-16 waveform, but it is still necessary to cancel out the odd harmonics from the carrier signal. A second-order multiple-feedback band-pass active filter was designed with centre frequency at the carrier frequency (75 KHz) and with Q-factor Q = 4 to remove unnecessary parts of the signal in the spectrum. The modulated signal is then coupled to the PLC channel using a coupling unit. The output signal, x_{mod}, is given by:

$$X_{mod} = 2AK/\pi\ (V_{mi} \cos 2\pi f_c + V_{mq} \sin 2\pi f_c) \qquad (5.6.1.4)$$

5.6.2 Analog demodulator

The input signal is derived from the PLC channel through the separation group filter. The analog part of the demodulator consists: the input amplifier, a digital programmable crystal oscillator, a 90° phase shift circuit, multipliers (one for each branch) and low pass filters (one for each branch). A block diagram of the demodulator is illustrated in Figure 5.4.2.1. The individual channels are extracted in the baseband using lowpass filters. The input amplifier is used for manually adjusting the signal

level. It is not necessary to include automatic gain control (AGC) circuitry in the design, because fluctuations of the PLC attenuation are very low. Further, some part of the AGC function can be done automatically by the adaptive equalizer. The quadrature multiplexed signal is demodulated by using quadrature carriers. For example, considering the in phase carrier cos ($w_c t + \theta$), where θ is the phase error between the transmit and receive local oscillators:

$$x_{mod}(t) \cos (w_c t + \theta) = \quad (5.6.2.1)$$

$$V'[V_{mi}(t) \cos \theta - V_{mq}(t) \sin \theta + V_{mi}(t) \cos (2w_c t + \theta) + V_{mq}(t) \sin (2w_2 + \theta)] \quad (5.6.2.2)$$

where V' combines all the various constants

The last two terms are removed by a low pass filter, and the signal at the output of the low pass filter is:

$$y_I = V'[V_{mi}(t) \cos \theta + V_{mq}(t) \sin \theta] \quad (5.6.2.3)$$

which is equivalent to V_{mi}, the desired output, for $\theta = 0$. The quadrature channel is demodulated by using a demodulating carrier of the form sin $w_c t$ to get the V_{mq} output. In fact, demodulation at the receiving side is accomplished by coherent demodulation with two reference sinusoids that are ideally phase and frequency coherent with the quadrature carriers. Thus, this modulation technique can be viewed as two separate digital modulation schemes operating in parallel. Coherent demodulation requires careful attention, for if the demodulation carriers are out of synchronism by even a small amount, serious distortion of the demodulated signal waveform can result. In this design no attempt is made to synchronise the carriers and so a phase correction block is required in the folowing digital signal processing sections.

The analog hardware was alomost identical to that used at the transmitter, the oscillator, phase shifter and filtering were identical and the MC 1495 mixer was also used for demodulation (Figure 5.6.2.2). An additional level shifter was required at the mixer outputs to remove the DC bias voltage.

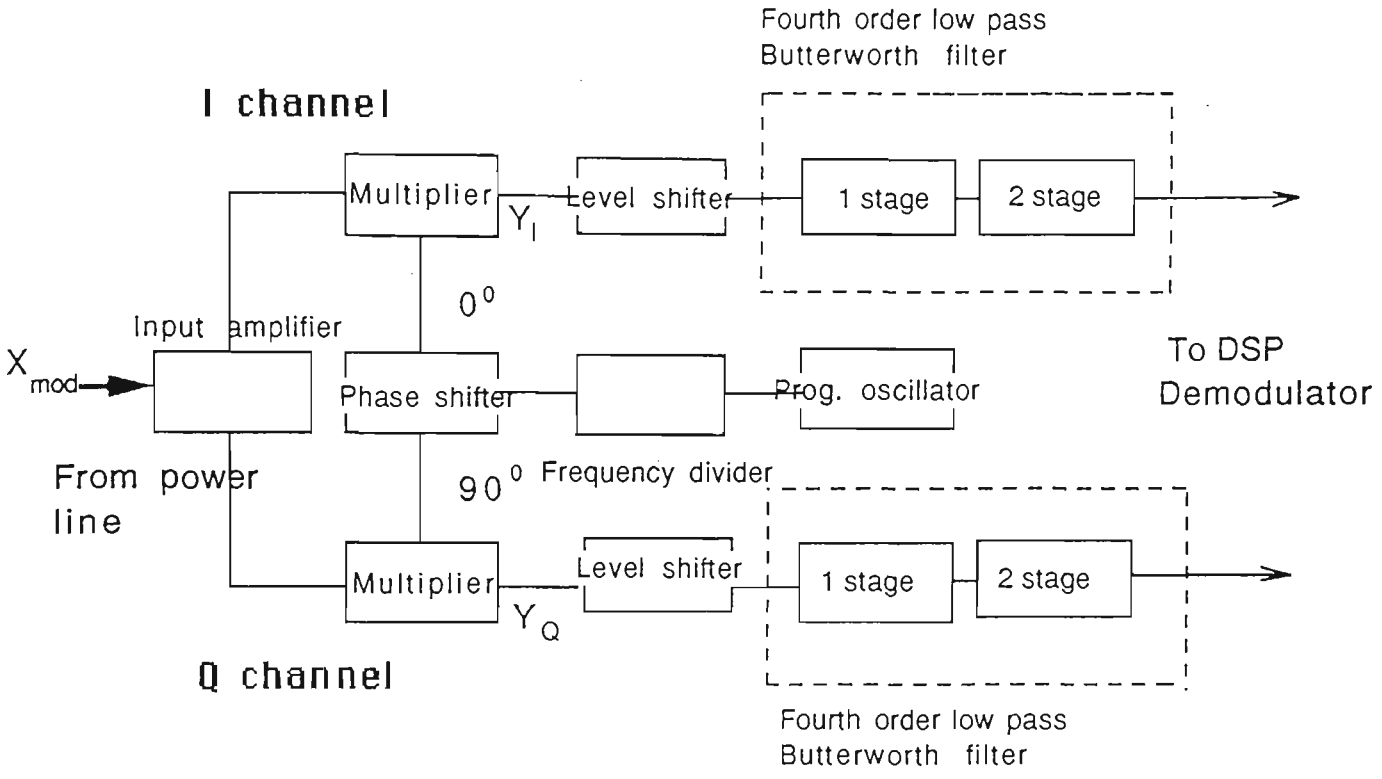

Figure 5.4.3.1 Block diagram - analog section of the demodulator

The purpose of the Butterworth low pass filters are different in the receiver section. They are required to remove second harmonic components of the carrierr frequency and to act as anti-aliasing filters for the following A to D converters.

To demonstrate how the analog system works, oscilloscope plots were taken. The first plot (Figure 5.6.2.2) shows the digital signal immediately after the D/A converter at the modulator. Figure 5.6.2.3 shows the same signal after the smoothing filter V_{mI}, while Figure 5.6.2.4 displays the same signal after the multiplier V_I (modulated with the pulse waveform of 75 KHz). The signal after the summer (QAM -16) v_{mod} is shown in Figure 5.6.2.5. Figure 5.6.2.6 shows the signal after the multipliers at the demodulator block (Y_I); the high frequency $2f_c$ component is clearly visible. Figure 5.6.2.7 illustrates the demodulated in-phase signal after the low-pass filter. This signal feeds into the digital signal processing section of the demodulator.

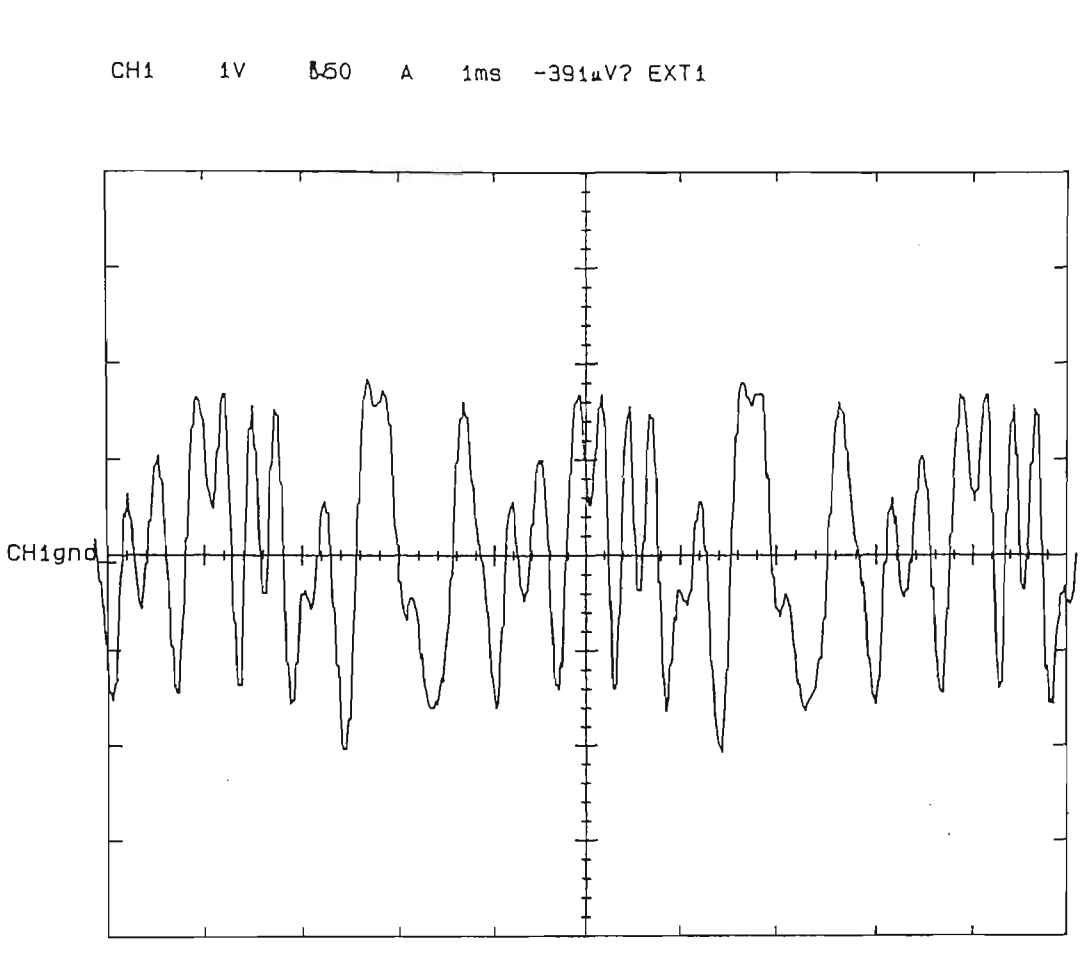

Figure 5.6.2.2 Signal after D/A converter - modulator side

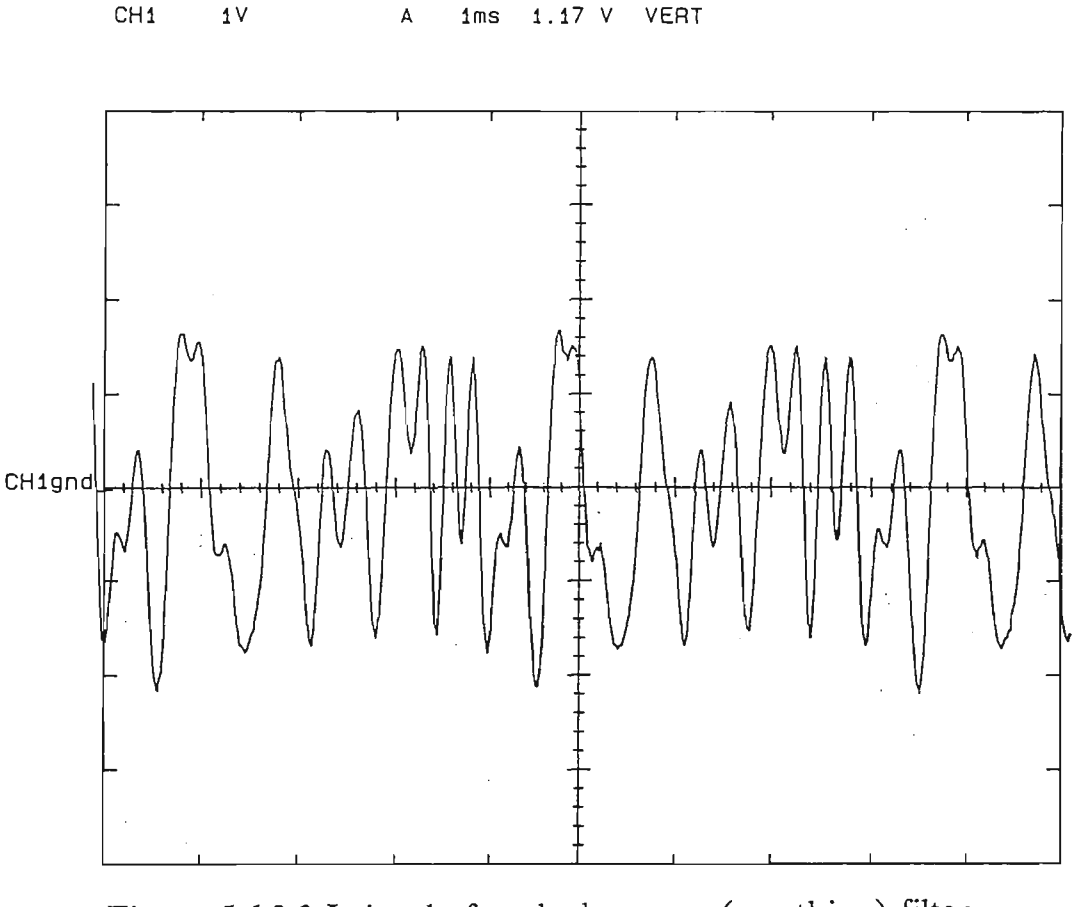

Figure 5.6.2.3 I signal after the low pass (smothing) filter demodulator side

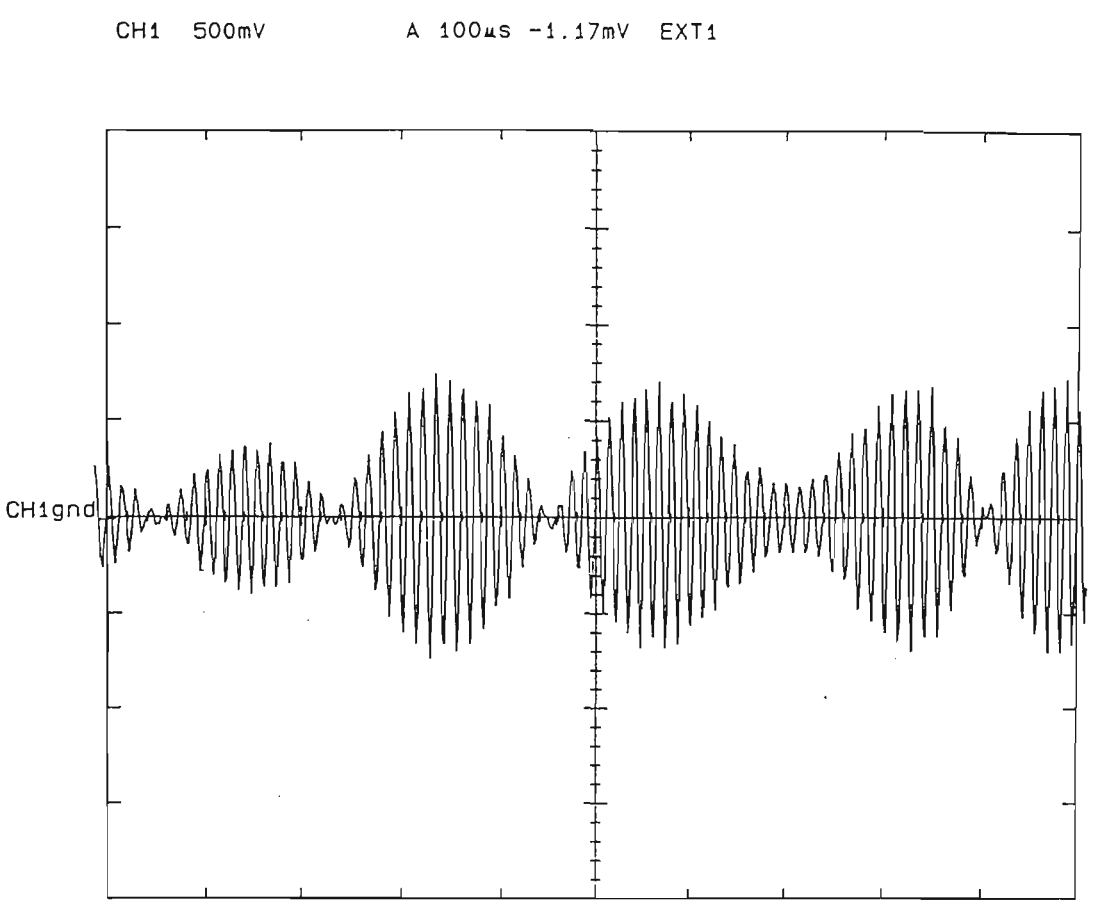

Figure 5.6.2.4 I signal multiplied with the carrier of 75 KHz - modulator side

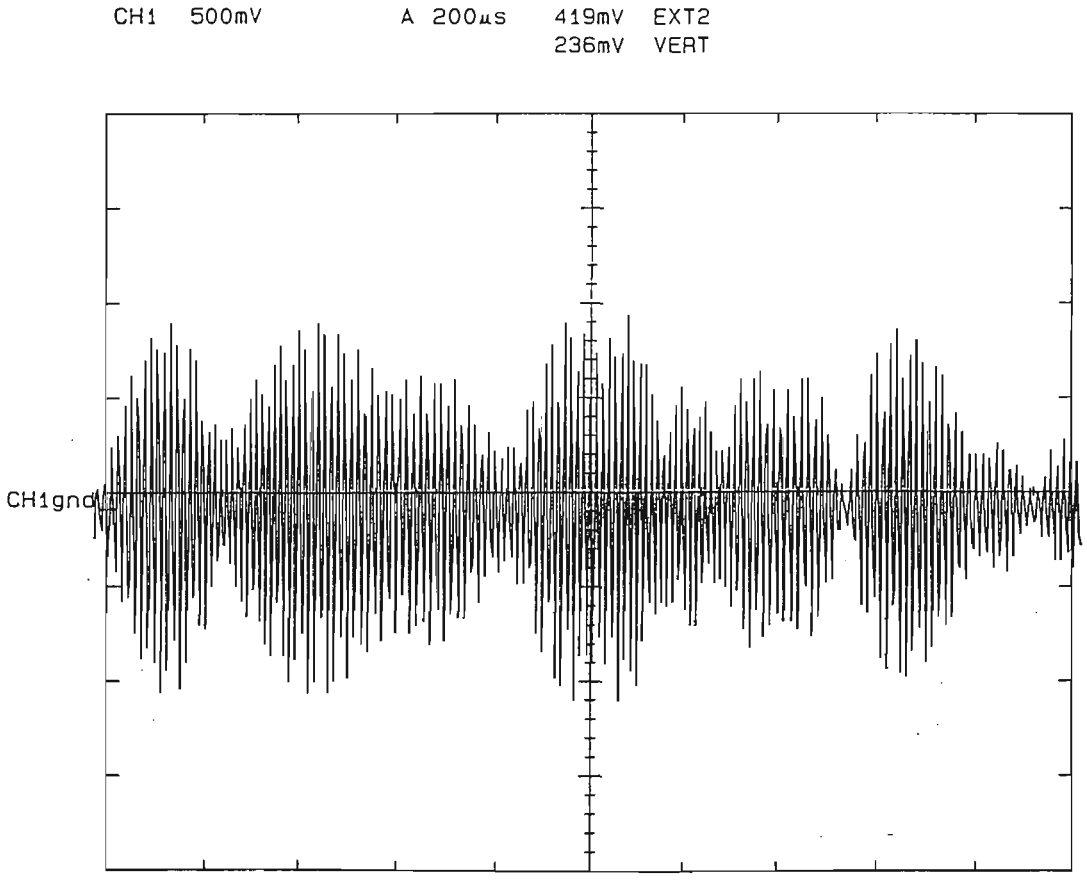

Figure 5.6.2.5 Signal after the summer - modulator side

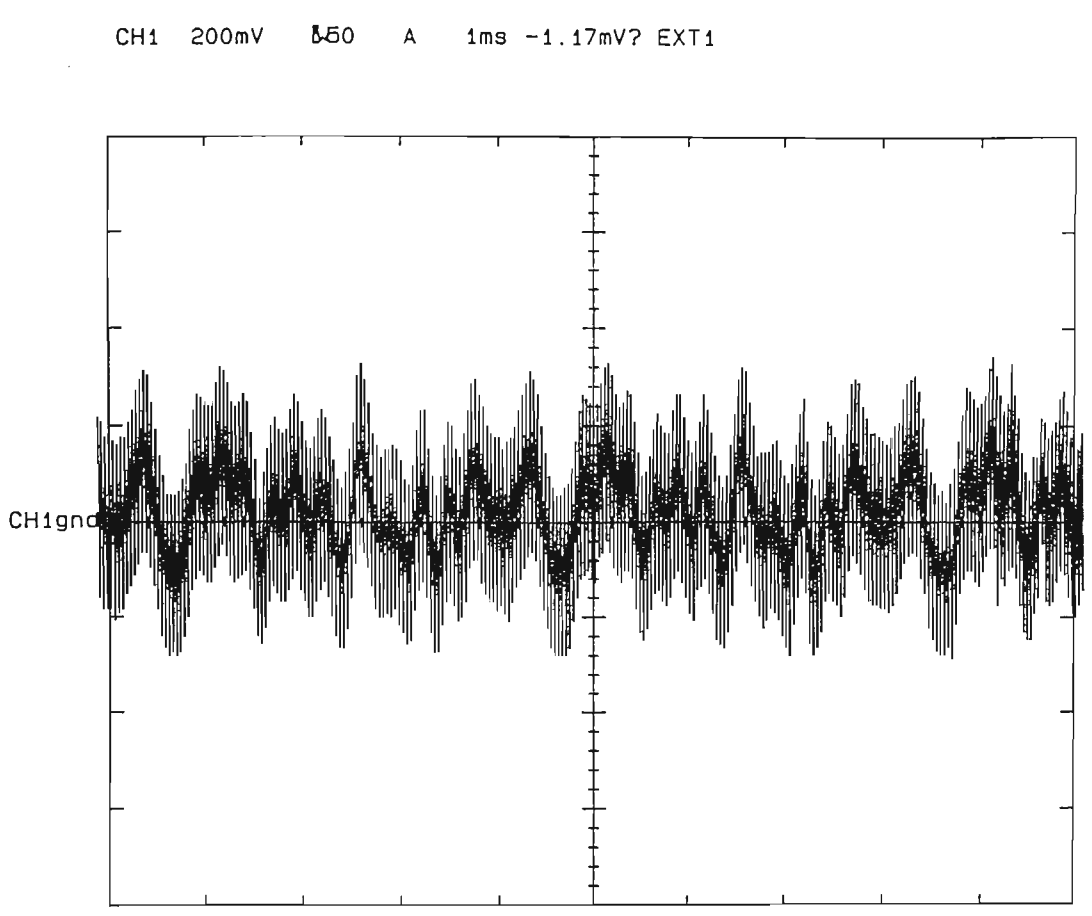

Figure 5.6.2.5 I signal after the multiplier demodulator side

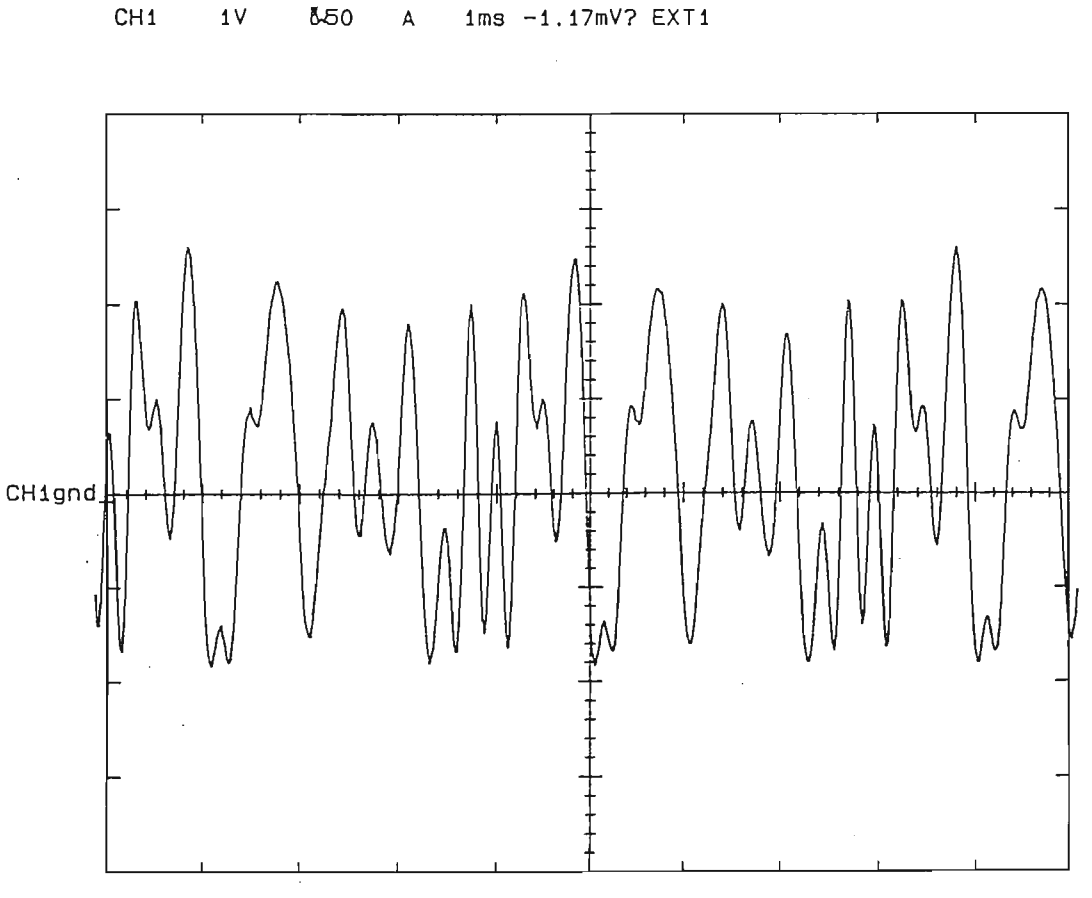

Figure 5.4.3.6 I signal after the low pass filter - demodulator side

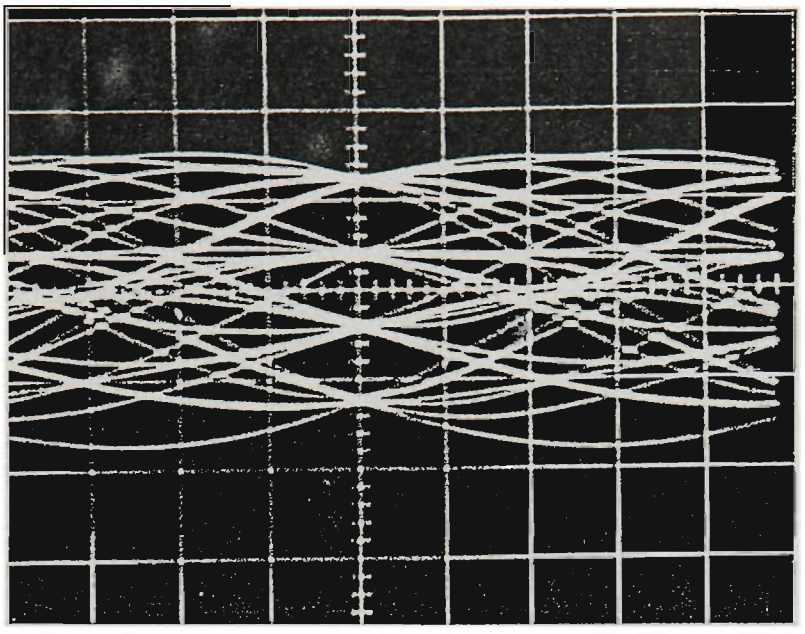

Figure 5.6.2.8 Eye diagram - raised cosine filter. Vertical scale 0.5 V/div - Horizontal scale 0.0128 msec/div

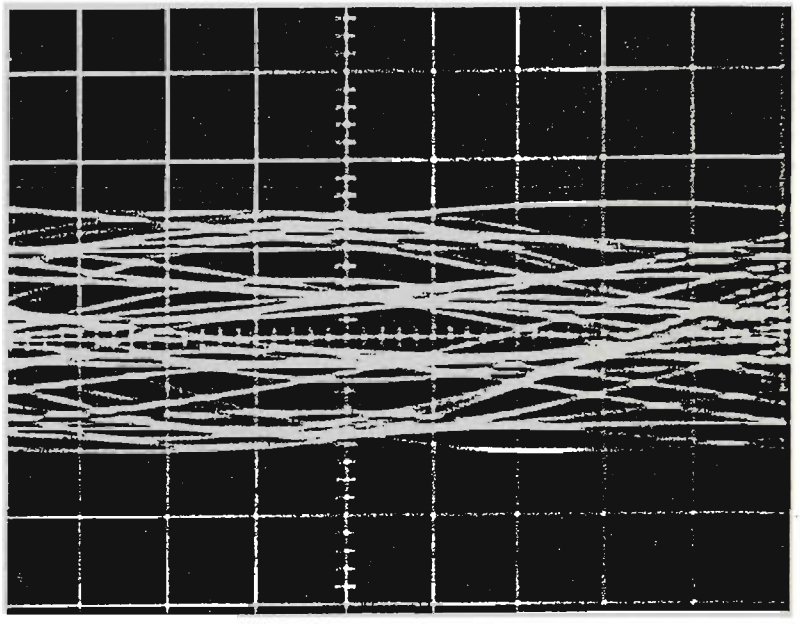

Figure 5.4.6.9 Eye diagram - square root raised cosine filter. Vertical scale 0.5 V/div - Horizontal scale 0.0128 msec/div

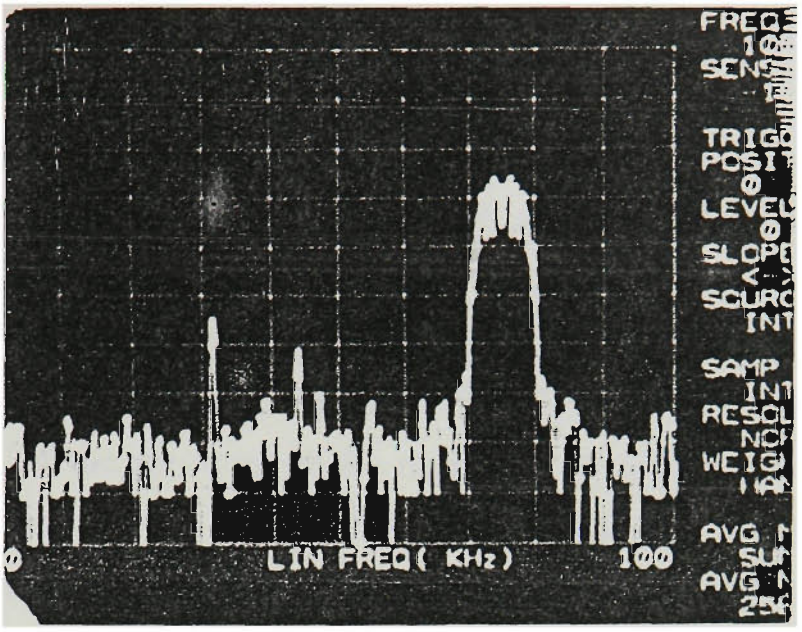

Figure 5.6.2.10 Spectrum of the modulated signal. Vertical scale 20 dB/div - Horizontal scale 10 KHz/div

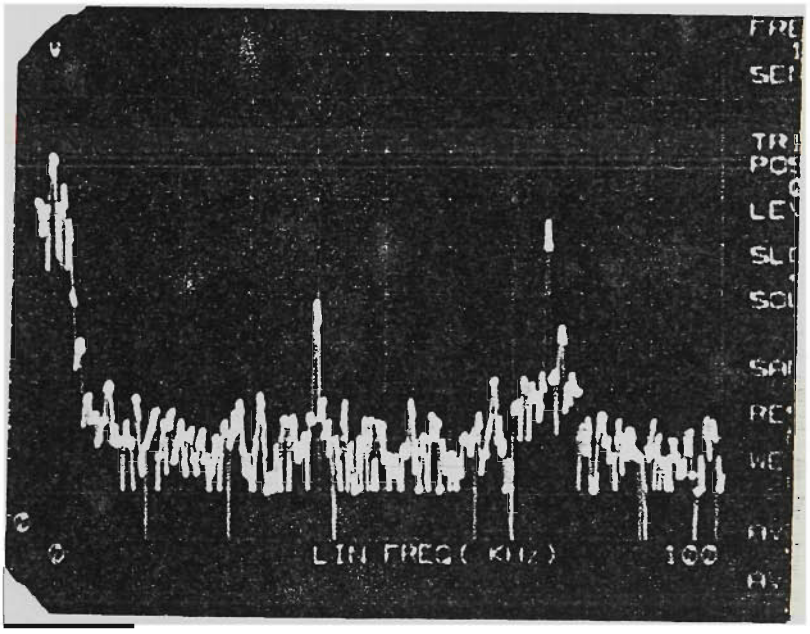

Figure 5.6.2.11 Spectrum of the demodulated signal. Vertical scale 20 dB/div - Horizontal scale 10 KHz/div

The photograph of the in-phase signal (eye diagram), before the modulation with the carrier pulse signal, is provided in Figure 5.6.2.8 with a raised cosine basic pulse shape (the rolloff factor is 0.395). There are three eye openings, because the QAM-16 has four signal levels. Also, the photographs of the signal with the square root raised cosine basic pulse shape (the rolloff factor is the same, 0.395) are provided in Figure 5.6.2.9. The eye opening is not as distinguishable as the signal with a raised cosine basic pulse shape, because the condition for zero ISI at the sampling points has not been fulfilled. This problem is corrected when the signal is feed through a second square root raised cosine filter in the receiver DSP section. The photographs of the spectrum of the modulated signal are shown in Figure 5.6.2.10. The carrier signal is 75 KHz. Also, the spectrum of the demodulated in-phase signal before the low pass filter is shown in Figure 5.6.2.11. From the figure it is obvious that there is a strong discrete component at the carrier frequency (75 KHz) carried by signal leak through the mixers. This and other spurious signals are filtered out by the low-pass filter situated immediately after the multiplier at the demodulator.

Modem - part 2

6.0 Introduction

This chapter describes the DSP section of the receiver. The preceding analog section down converts the signal from the carrier frequency f_c to a complex baseband representation with I and Q outputs. These are digitised and fed to the DSP section which is responsible for the important receiver functions of the symbol timing recovery, carrier phase correction, channel equalisation, detection and differential decoding. The first section 6.1 gives an overall description of the software, and this is followed by a detailed discussion of symbol timing recovery section 6.2, carrier phase correction in section 6.3, and equalisation techniques in the section 6.4.

6.1 DSP hardware system

This project used the Texas Instruments TI TMS 320C25 software development system (SWDS) on an IBM AT, to implement the DSP sections of the receiver. SWDS provides the system interface necessary to write, assemble/link, load and debug the TMS320C25 code on a PC workstation. The SWDS is capable of single stepping through the code or setting breakpoints for monitoring the registers and memory contents during execution.

The target hardware-digital signal processing unit was designed internally, and formed part of a common laboratory development system. It provided analog input and output facilities for the SWDS development system. Such an implementation is very cost effective, and provides flexibility and future growth potential at no additional

cost. The TMS320C25 provides the computational power to implement all significant demodulator's function without too many compromises.

There consist of an 8-bit high speed ADC with four multiplexed analog inputs, which uses a half-flash conversion technique to give a fast conversion rate of 2.5 μs, and a four channel 8-bit voltage output digital-to-analog converters with output buffer amplifiers. A block diagram of the target hardware is shown in Figure 6.1.1.

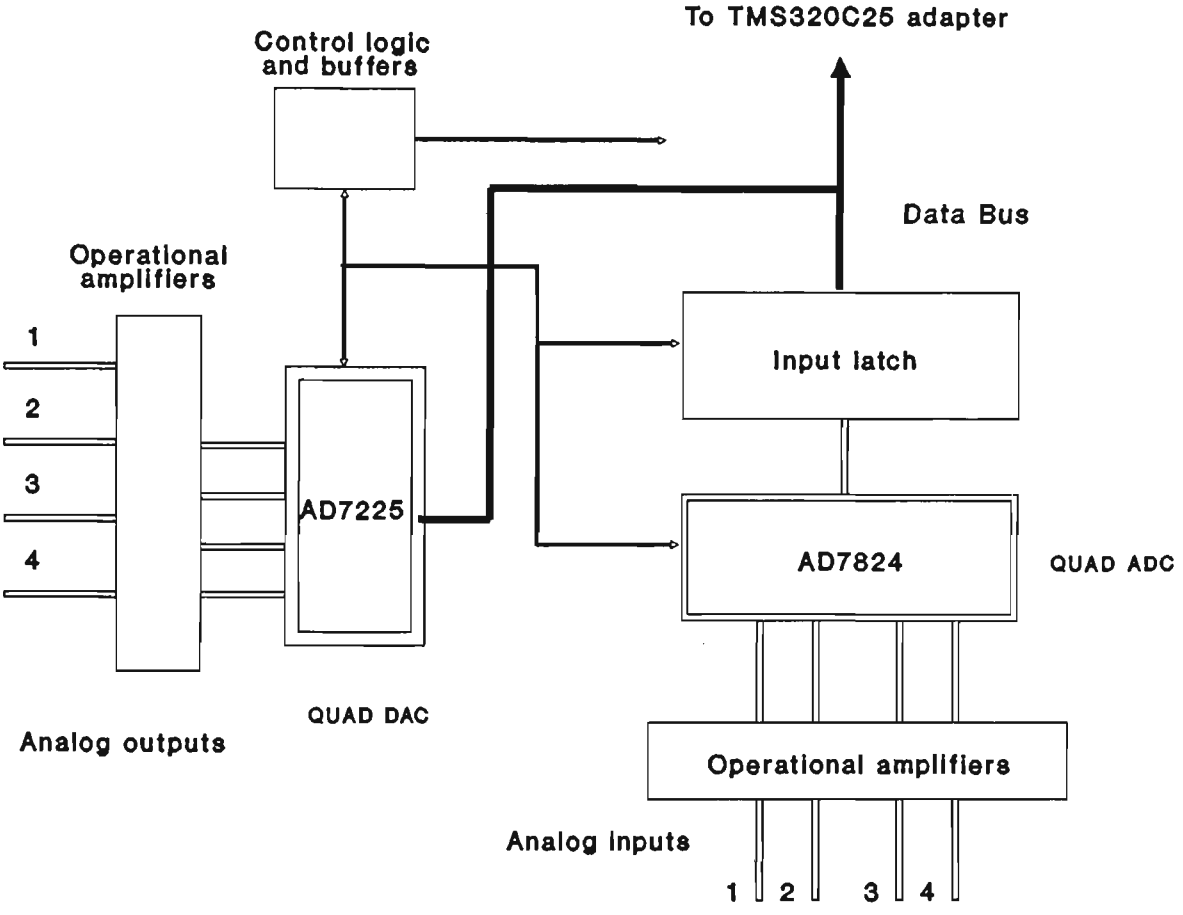

Figure 6.1.1 DSP TMS 320C25 target system - block diagram

The software routines were written in the TMS320C25 assembly language instead of C, because the main intention was to achieve a high computational efficiency for the given sampling rate. Furthermore, the earliest version of the C compiler for the C25 had few bugs, and showed poor results in performance and efficiency.

6.1.1 Demodulation algorithms

The software functions implemented in the DSP are shown in Figure 6.1.1.1. The computer flow diagram to implement this is shown in Figure 6.1.1.2. There are two square root raised cosine filters (one for each channel) in the modem design. There have 34 taps each. It is evident that with an increasing number of filter taps, the filter performance improves in terms of out of band noise and interference rejection. Unfortunately, there is not enough space to accommodate huge filters on the demodulator side, because other demodulator functions have to be included in the receiver's design. The square root raised cosine filter was designed as follows:

Finite impulse response
Linear-phase digital filter design
Parks-McClellan algorithm
Filter length = 44
Sampling frequency = 31.250 KHz
Center frequency = 3.906 KHz
Rolloff = 39.50 %
Ripple in dB = -34.8655
16-bit quantized coefficients

The log magnitude frequency response and unit sample response of the square square root raised cosine filter are illustrated in Figure 6.1.1.3. and Figure 6.1.1.4. The adjacent channel rejection (-35 dB) is clearly visible. A faster processor would allow more taps and greater rejection. The receiver filters are implemented in a somewhat more conventional manner than the transmitter filters. The receiver filters do not interpolate, nor they decimate. In this case, as for the modulator design, speed is more critical than program memory. Thus, it is beneficial to use the MACD instruction to perform convolution operations in the filters algorithms. The MACD instruction combines accumulate and multiply operations with the data move, and is very useful in the impementation of the square root raised cosine filter.

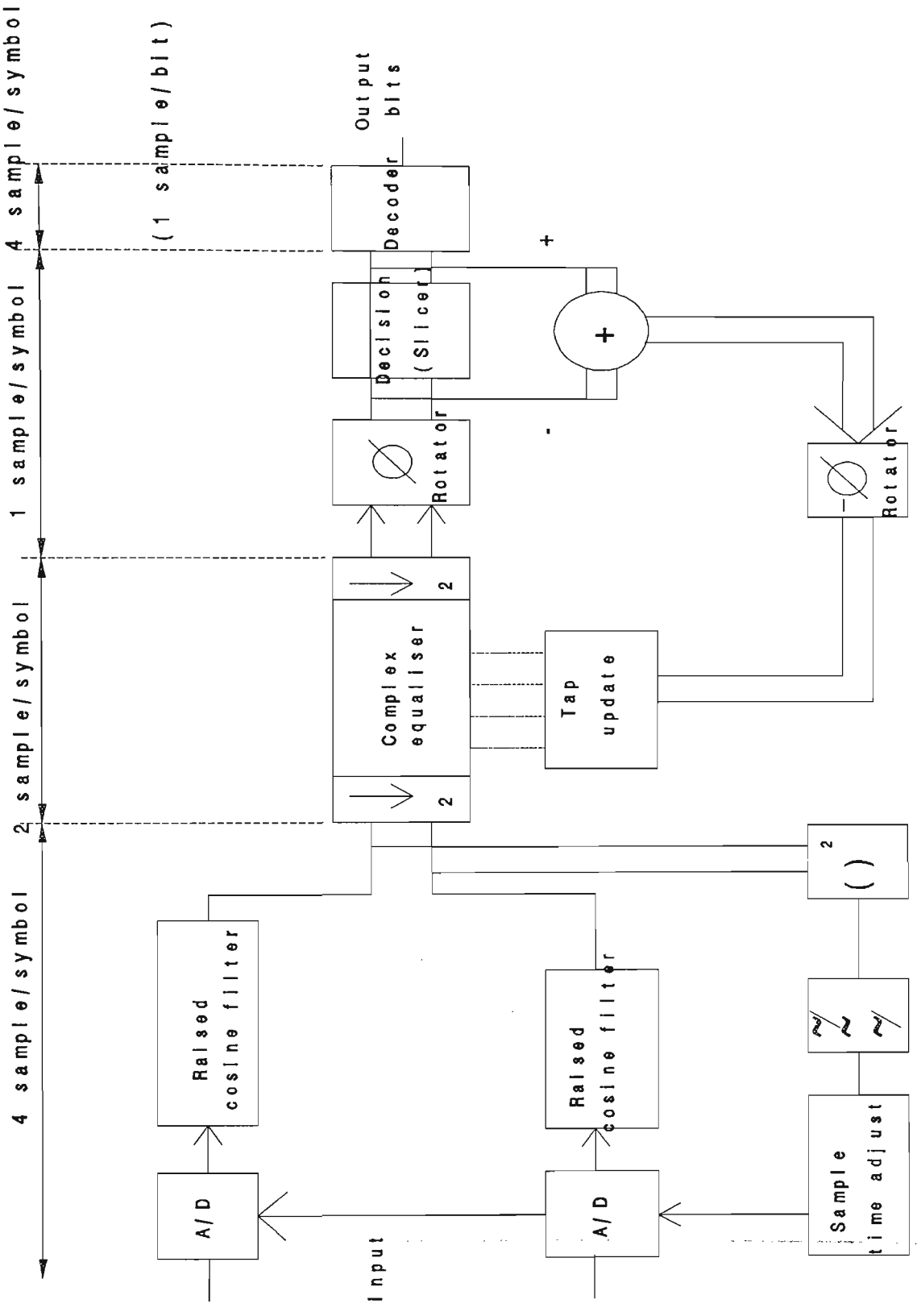

Figure 6.1.1.1 Block diagram of DSP receiver software functions

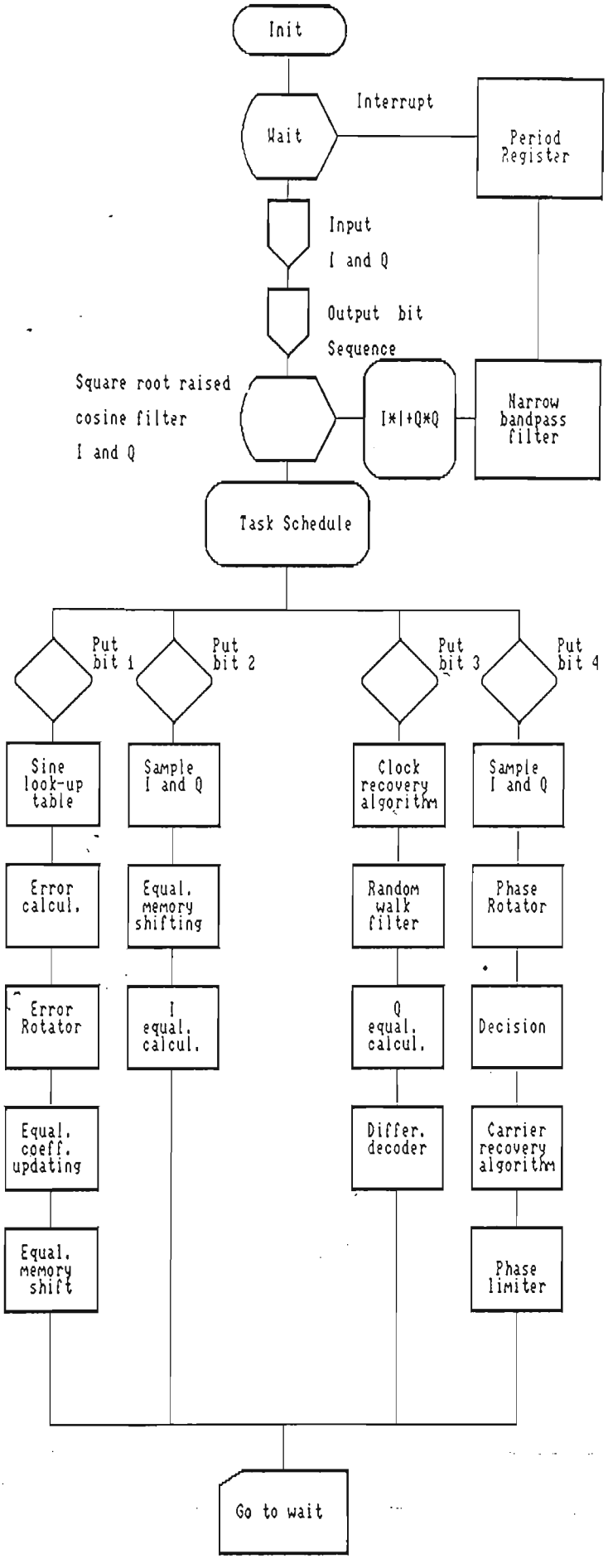

Figure 6.1.1.2 Demodulator block assembler diagram

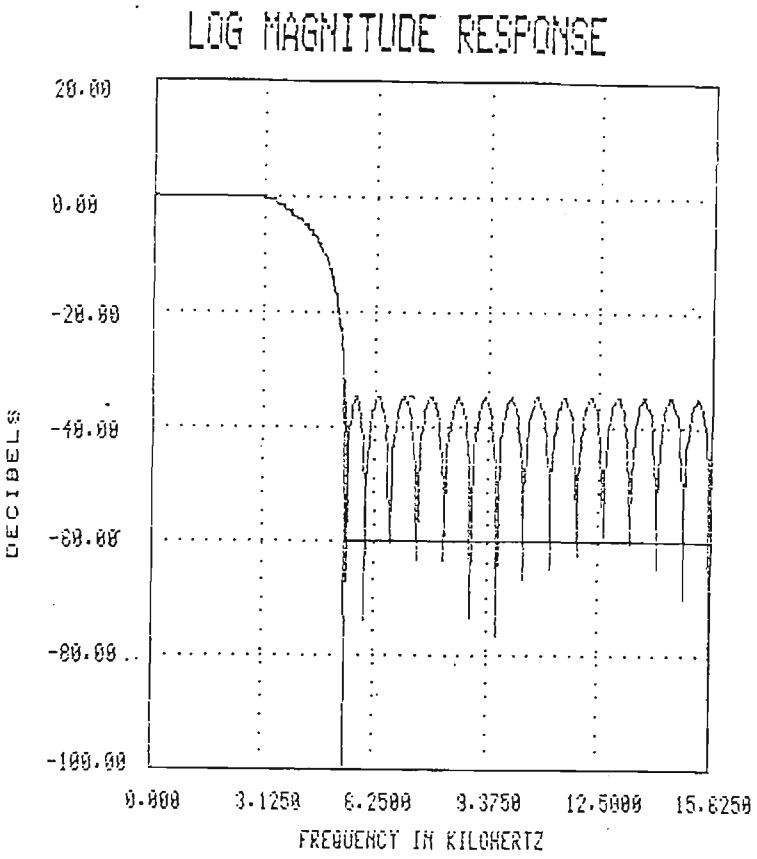

Figure 6.1.1.3 Square root raised cosine filter log magnitude response

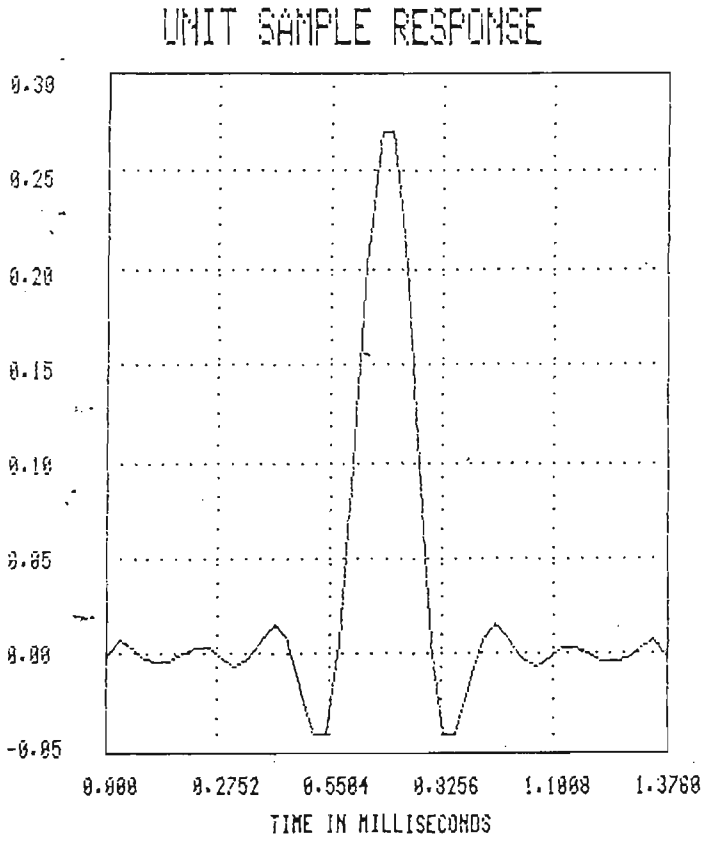

Figure 6.1.1.4 Square root raised cosine filter unit sample response

current		previous		output	
a_{4i}	a_{4i+1}	$a_{4(i-1)}$	$a_{4(i-1)+1}$	g_{4i}	g_{4i+1}
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	1	0
0	0	1	1	1	1
0	0	0	0	0	1
0	1	0	1	0	0
0	1	1	0	1	1
0	1	1	1	0	1
0	1	0	0	1	0
1	0	0	0	0	1
1	0	0	1	0	1
1	0	1	0	1	1
1	0	1	1	1	0
1	1	0	1	1	1
1	1	1	0	1	0
1	1	1	1	0	1
1	1	0	0	0	0

Table 6.1.2.1 Differential Decoding

The decision block is used to distinguish between the four demodulated baseband levels, three threshold comparators are required in each 4-to-2 level PAM converter. The algorithm estimates which of the four PAM levels is represented by each sample. Threshold levels are set at value which is at a half the distances between the nearest points in the signal constellation for each channel. The demodulator algorithm is implemented to perform 4-to-2 level conversion and simultaneous parallel-to-serial conversion. For the rectangular signal constellation, a simple slicer routines is all that is required, but for other more complex signal constellations, more difficult and complicated routines are required. This was the main reason why the rectangular signal constellation was selected.

The differential decoder is located immediately after the slicer. It has an opposite function to the function of the differential encoder; it actually reverses encoding [41,34]. The slicer, and the parallel-to-serial converter provide a detected bit stream a_i, a_{i+1}, a_{4i+2} and a_{4i+3}, which determines the corresponding signal point in the signal constellation. The first two bits a_{4i} and a_{4i+1}, are decoded by using a subtract (modulo 4) algorithm into bits e_i and e_{i+1}. It has been mentioned previously that the first two bits require differential encoding/decoding, the second two bits remains unchanged, and they do not require differential encoding/decoding. The decoder works as explained in Table 6.1.2.1, where $a_{4(i-1)}$ and $a_{4(i-1)+1}$ are delayed versions of the signals a_{4i} and a_{4i+1} (T is the symbol time), which are necessary for the implementation of an subtracting (modulo 4) algorithm. The bit stream g_{4i}, g_{4i+1}, a_{4i+2}, a_{4i+3} is the output bit stream.

6.2 Clock recovery

6.2.0 Introduction

Timing recovery circuits are employed to maintain receiver's clock equal in step with far end transmitter's clock to enable sampling at the best sampling instants.

There are two principal types of timing recovery techniques: deductive and inductive types. Deductive timing recovery directly extracts from the incoming signal a timing tone. Inductive timing recovery does not process the received signal to get a

timing tone. Inductive timing recovery does not process the received signal to get a timing tone, but rather uses a feedback loop. The inductive timing recovery uses a PLL (Phase Lock Loop) not as an added optimatisation to reduce timing jitter, but rather as an integral part of the method [41].

In analog techniques the signal is sampled after processing and conditioning, whereas in the digital receiver the unconditioned and probably distorted signal is sampled straight at the input. The timing recovery from the digitized signal must always be achieved with a feedback loop, in contrast to analog processing where non feedback schemes are possible [42].

It is well known that the performance of the transversal adaptive equalizer depends critically on the sampling phase. An improper instant may create a spectral null or deep depression in the sampled signal spectrum and thereby degrade the equalized system performance. In the case where the fractional type of adaptive equalizer is used sample phase becomes nearly irrelevant. This equalizer is relatively insensitive to timing errors, but it is still sensitive to the eye opening during training. Therefore it is necessary to achieve rapid baud timing acquisition [58]. This section investigate the most suitable clock recovery algorithm for the PLC modem.

6.2.1 All digital model

In this application timing phase is changed by advancing or retarding the sampling phase of the A/D converter at the digital receiver input. In order to vary the phase of the sampling clock, a controllable digital timer is necessary. The sampling clock is derived by dividing the microprocessor instruction cycle frequency with the number N x M, where N is the number of samples per baud required by the receiver, and M is the number of the instruction cycles per sample. It is counted down at the main clock rate and every time M cycles of that clock are counted, the A/D converter samples the received signal. When the counter reaches zero, a final sample is taken and a new baud period is started by loading the counter with N x M again.

There will always be a small frequency offset between the receiver and transmitter clock. Therefore, the receiver must repeatedly adjust the phase of the baud clock in order to track the baud timing of the incoming signal. If the transmitter clock

is slightly faster than the receiver clock, the receiver digital timing recovery scheme will detect the phase offset which will accumulate after several baud periods. In this case the receiver adjusts its baud clock by loading (N x M) - K into the divide counter for one baud period, where K is a positive or negative integer. This will change (shorten or broaden) the baud period, and in this manner the receiver clock will be realigned with the incoming clock of the transmitter. The minimum phase adjustment possible with this method is one period of an instruction cycle. This proposed timing recovery scheme is an all digital implementation or a DSP approach [43].

The control signal for the timing adjustment can generated using any of the standard approaches:

1. Wave difference method [41]
2. Mueller's decision directed method [41]
3. Spectral line method [45]

In wave difference method the transmitted symbol pulses are assumed to be symmetrical about their peak and the channel is assumed to be such that this symmetry is unaffected. In fact it works in the same principle as the early-late gate synchronizer. For example, there is a received pulse with three samples per baud: y(n-1), y(n) and y(n+1). If the pulse is symmetrical, then in the absence of noise and intersymbol interference, for y(n) at the peak of the pulse is:

$$|y(n-1)| = |y(n+1)| \qquad (6.1.1)$$

where | | denotes the amplitude of the timing waveform. If $|y(n-1)| > |y(n+1)|$ the sampling phase need to be advanced with respect to the received signal, and vice versa. Accordingly, computing of an average of differences between the two sampling points over several baud interval yields a timing function which will determine whether to advance or retard the sampling phase.

This method was simulated using the simulation model described in this chapter. It yields a good performance, but the assumption that pulses have to be symmetrical make this method not so amenable for PLC channel applications, because of the reflection phenomena and severe noise environment.

The second method is Mueller's decision directed method and also has a good performance. In this method a tracking error signal, given by:

$$err = \alpha.Re\{x_{n-1}.x_{n-1des} - x_{n-1}.x_{ndes}\} \qquad (6.1.2)$$

where α is a adaptation constant, small positive number; x_n is the input signal, and x_{ndes} is the signal from decision decoder at nth period is evaluated. The timing phase is driven in the discrete symbol period steps towards the optimal position, where the signal error err is equal to zero. Simulation proved that it is a fast converging algorithm. The adaptation loops for timing recovery, carrier phase control and adaptive equalization do not work independently of each other, and interaction must be carefully investigated, especially at start-up. Before sending the data stream on the channel, it is necessary to incorporate the preamble phase, in which the periodic sequence is transmitted. The choice of the sequence must meet certain requirements in order to remove the phase uncertainty. Unfortunately, this method could not be the best choice for the PLC noisy channel, especially when the bit error rate is of the error of 10^{-4} [42].

The third method is the nonlinear spectral line method implemented on the baseband signals, which was selected for the timing scheme applied in this design.

6.2.2 System model

The block diagram of the timing recovery for a baseband QAM signal is illustrated in Figure 6.2.2.1 Baseband signal obtained from the pulse shaping filter stage is given by:

$$r(t) = \sum_{n-0}^{n-N} a_n.h(t - nT) \qquad (6.2.2.1),$$

where (a_n) is the message sequence, which is assumed to be a zero-mean stationary discrete random process, and h(t) is an even Nyquist pulse. The function of the timing synchronization circuit is to extract from the r(t) a periodic wave with a period T and a proper phase indicating the sampling instant within each period. It is assumed that the

bandwidth does not exceed 1/T, or actually bandwidth occupancy approaches the Nyquist limit of 1/2T at baseband. The pulse h(t) therefore spreads over many symbol intervals, giving rise to intersymbol interference. In order to combat ISI at nominal sampling instants, the Nyquist shaping has been used.

If the data has a zero mean value, then E[r(t)] has no periodic components. (E [] denotes expectation). However, r(t) is a cyclostationary process and therefore:

$$E[r^2(t)] = E[a^2 \sum_{n-0}^{n-N} h^2(t - nT)] \qquad (6.2.2.2)$$

which hows that the square of r(t) does possess a periodic mean value, and by using the Poisson sum formula it ensues [68]:

$$E[r^2(t)] = E[a_n^2] \sum_{n} (A/T).e^{(j2\pi nt/T)} \qquad (6.2.2.3)$$

where:

$$A = \int_{-\infty}^{+\infty} H(n/T - f).H(f)df \qquad (6.2.2.4)$$

The bandwidth of H(f) is limited, and only the three terms in the previous equation with n = 0,+1,-1 are different from zero. The terms with n = 0 corresponds to a dc component, whereas the other two give a sinusoidal signal with frequency 1/T and amplitude A. This sinusoidal component vanishes when H(f) is completely bandlimited in the interval (-1/2T,1/2T). Therefore, if the data pulse has a bandwidth in excess of the minimum (Nyquist) bandwidth of 1/2T then $E\{r^2(t)\}$ has periodically varying components due to the n = +1 and -1 terms. And if the bandwidth does not exceed the 1/T, then $E\{r^2(t)\}$ contains sinusoidal components at a frequency of a 1/T with phase of (- 2π.t/T) [42].

The timing waveform is illustrated in Figure 6.2.2.2 together with the eye diagram, for the employed raised cosine filter obtained from the simulation program. The diagram shows the result of many traces on the screen. Each trace has a sample rate

of 64 samples/symbol. An efficient timing recovery circuit can be implemented by the nonlinearity (e.g. square-law device)/BPF (or PLL) arrangement, where the center frequency of the BPF is tuned to 1/T (PLL is tuned to track the restored timing wave at the same frequency). Alternate zero-crossings of the timing wave are used as the indication of the correct timing instants. For a real symmetric BPF transfer function there is an offset of an T/4 in the zero-crossing of the restored timing wave from the optimum sampling instants, which must be incorporated into the timing circuitry (see Figure 6.2.2) [46].

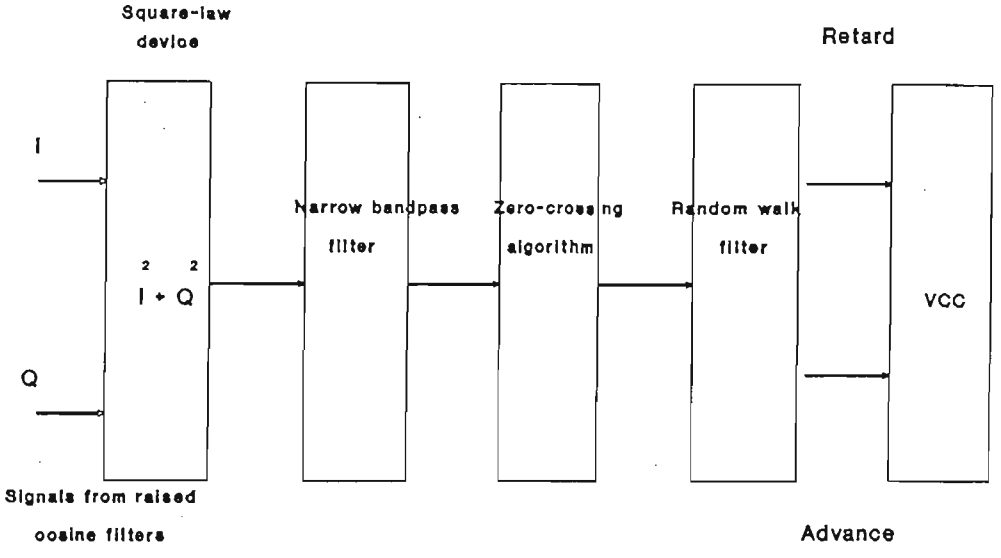

Figure 6.2.2.1 Timing recovery - block diagram
Nonlinear spectral line method - baseband domain

If instead of the BPF, a PLL is used, the same offset results because the VCO output locks in quadrature with the input. A typical realization of the process produces a nearly sinusoidal waveform with slowly varying amplitude and small fluctuation in the phase-shift. This is clealy seen in the Figure 6.2.2.2. Cyclostationarity of the timing

wave is the result of the fact that it is obtained by a time-invariant operation, which is itself a cyclostationary process. The spectrum of $r^2(t)$ presents a continuous part, besides the discrete one contributing to the desired spectral line. he continuous part acts as a noise source for the desired timing waveform (often called self noise or data noise). It is this that causes the amplitude and phase shift fluctuations (jitter).

For signals, with the small excess bandwidth, fourth-power nonlinearity outperforms the squre-law nonlinearity. It can even extract a timing wave from signals with the zero excess bandwidth. An absolute-value rectifier exhibits a better performance than a square-law rectifier for signals with a small excess bandwidth, and like the fourth-power nonlinearity, it can also extract a timing wave from signals with zero excess bandwidth. Simulations [46] demonstrate that absolute-value rectifiers outperform square-law rectifiers for signals with less than about 20 % excess bandwidth. But for the case of a rolloff factor β = 0.395 as used in PLC modem a square-law rectifier is best.

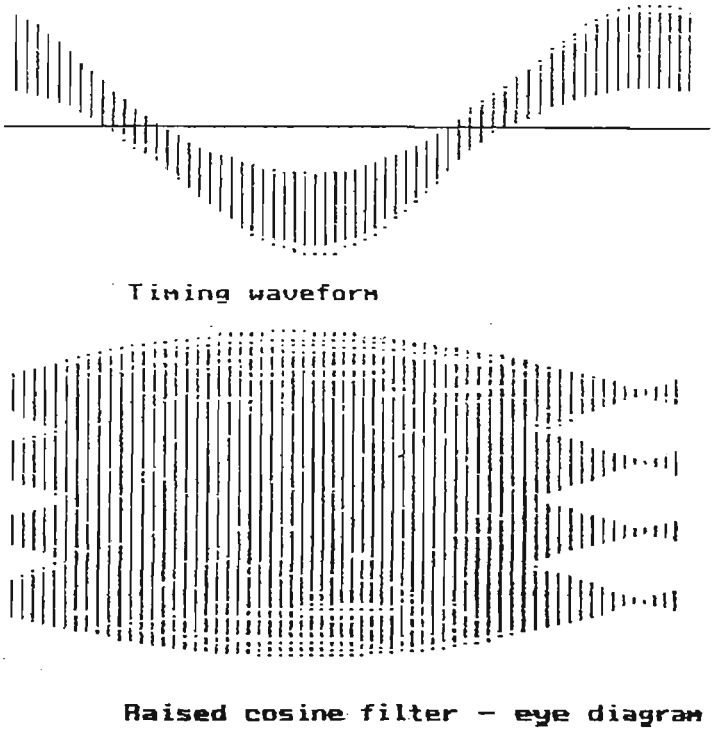

Figure 6.2.2.2 Timing waveform and the eye diagram
The way to select the optimal sampling point on the timing waveform

If timing recovery is implemented in DSP technique, aliasing must be considered in the choice of the nonlinearity. The nonlinear rectification process can create significant problems, with resulting high order harmonics giving rise to alias components folding back into the frequency band of interest, causing an additional timing jitter. Raising the signal to the fourth-power will quadruple its bandwidth, and for a full wave rectifier infinite even-order harmonics are generated in addition to the desired term. Accordingly, in DSP design a square-law rectifier offers a better performance than either absolute-value or fourth-power nonlinearity. The square law device is chosen for this application.

The output from the bandpass filter consists of a periodic sine wave, whose frequency is at the baud rate (symbol rate) and with four samples period. Simulation with 64 samples per symbol are shown in Figure 6.2.2.2. It shows clearly that the optimum eye opening occurs when the timing waveform is at its maximum.

The otput from the two filters feeds the symbol timing synchronisation circuit consisting of a squarer circuit, bandpass filter, and interrupt control circuit. These also operate at the input sample rate of four samples per symbol. The root raised cosine filters also feed a complex equaliser which operates at 2 samples per symbol, implyung a decimimation by 2. The equaliser feeds a phase rotator that corrects for phase error between the two local oscillators, and this in turn feeds a decision circuit. These circuits operate at the symbol rate, implying a further decimation by 2. Decimation is implemented in the software flow chart of Figure 6.1.1.2. by the "Task Schedule" block, which effectively selects each of the four parallel paths in turn. Each path operates at the symbol rate; blocks that are selected twice operate at twice the symbol rate, for example "Equaliser Memory Shift". Those selected once (most of the other blocks) operate at the symbol rate.

As a large amount of the signal spectrum doesn't contribute to the timing tone, the unnecessary part of the signal and some noise component could be removed. As a result the timing jitter could be reduced. In general a prefilter can reduce the timing jitter significantly, especially for low excess bandwidth, but it is not so efficient for signals with large excess bandwidth [41]. It is not used in this application.

The zero crossing $\{t'_k\}$ of the timing wave z(t) are not uniformly spaced in time and therefore do not coincide with zero crossing $\{t_k\}$ of the periodic component of

the r(t). The difference $dt_k = t'_k - t_k$ is termed the timing error or jitter and is approximately given by [73]:

$$dt_k = -z(t_0 + kT)/E[dz(t_0)/dt)] \qquad (6.2.2.5)$$

Where t_0 is zero-crossing of E[z(t)]. An expression for the expected slope E[dz(t)/dt] can be obtained from equation 6.2.2.3:

$$E[dz(t)/dt] = 4.E\{a_n^2\}.A/T^2 \qquad (6.2.2.6)$$

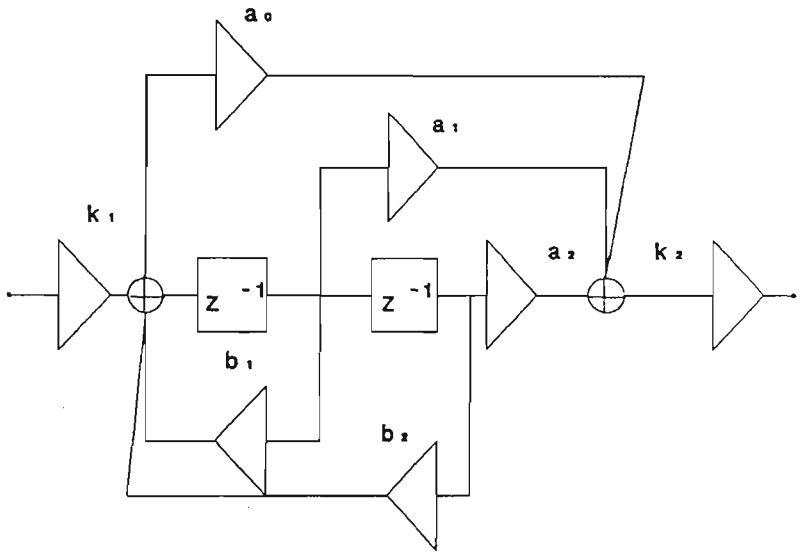

Figure 6.2.2.3 Second order narrow bandpass filter

The value of A depends directly on the amount of the excess bandwidth. Thus, for a very small excess bandwidth, A will be small too, and the timing recovery will be poor. The variation in amplitude of z[to + kT] at the sampling instances is primarily

caused by data noise. This noise can be reduced by using a narrow band-pass filter after the squarer. A second order IIR filter provide this function (Figure 6.2.2.3). The transfer function and coefficients are as follows:

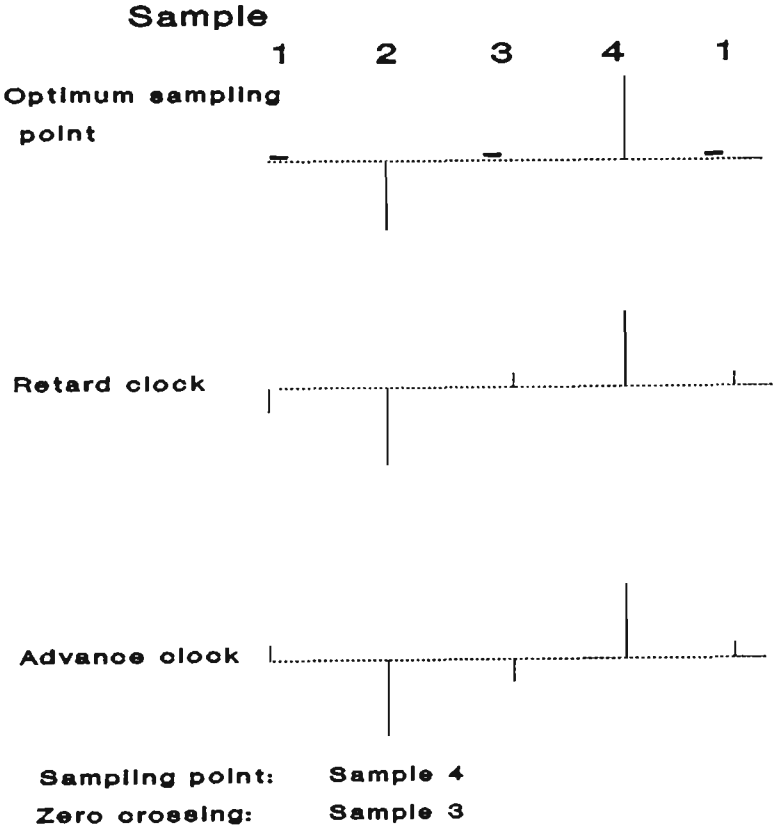

Figure 6.2.2.4 Optimal sampling point

$$H(z) = k_1(z^2 - 1)/(z^2 - b_1 z - b_2) \quad (6.2.2.8)$$

$$b_1 = 2\exp(-w_r Ts/2Q).\cos(w_d Ts) \quad (6.2.2.9)$$

$$b_2 = -\exp(-w_r Ts/Q) \quad (6.2.2.10)$$

$$k_1 = (1 + b2) \quad (6.2.2.11)$$

Where $w_r = 2.\pi.f_r$ = resonant frequency, symbol rate ($2\pi/T$), and:

$$w_d = \sqrt{(1 - 1/4Q^2)} \quad (6.2.12)$$

Simulations indicating what Q should be chosen are given in the next sub- section.

The best sampling point has a T/4 offset from the negative to positive zero crossing point. The algorithm for adjusting the timing assumes that the third sample is exactly at the zero crossing point, in which case the fourth sample is the optimal sampling point (Figure 6.2.2.4). The algoritm keeps the third sample at the zero crossing point by measuring its amplitude and adjusting the system sample period to drive this value to zero. The sign of the third sample produces a lag/lead signal. If the amplitude of the timing wave at the third sample is greater than zero, then the sampling phase has to be advanced with respect to the the received signal (the contents in the period register have to be decremented). Likewise if the amplitude is less than zero, then it has to be retarded (the content, in the period register have to be incrememented). Data noise causes the tracking algorithm to randomly move about the optimum point. Further lowpass filtering can reduce this problem. A random walk filter (RWF) is used for this purpose.

In the RWF (Figure 6.2.2.5) an up/down counter reacts to the lag/lead pulses by counting up or down. A phase step command is generated when either an upper or lower threshold is reached.

The threshold number denotes a minimum number of symbol intervals necessary to pass before the decision could be made. Then the counter is reinitialized and the procedure repeats. The RWF is a sequential filter which determines the rate of the phase corrections. The use of two different thresholds for acquiring and tracking the symbol rate could make the mechanism more effective and powerful, the

lower could be used for acquisition purposes and the latter for tracking purposes. The lower absolute value threshold gives more frequent adjustments, which is important for the acquisition, but for the tracking purposes a longer time between corrections is necessary. With judiciously chosen tracking threshold the loop will "flywheel" through long sequences of leads and lags caused by noise and timing jitter.

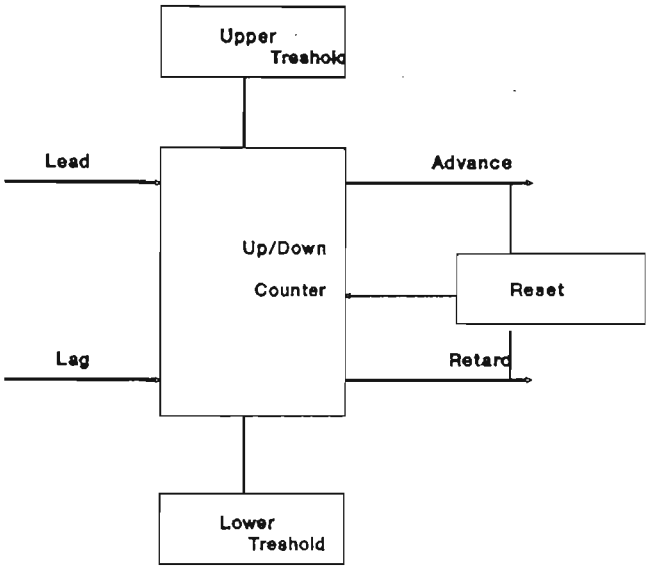

Figure 6.2.2.5 Random walk filter

6.2.3 Static jitter measurement

If the amplitude of the timing signal ("sinewave") at the output of the NBPF could be considered as constant during a one baud period (this is the case when NBPF has a large Q factor), then the following expressions :

$$A1 = -A.\sin((2\pi/T).0 + \theta) = -A.\sin(\theta) \qquad (6.2.3.1)$$

$$A2 = -A.\sin((2\pi/T).(T/4) + \theta) = -A.\sin((\pi/2) + \theta) \qquad (6.2.3.2)$$

$$A3 = -A.\sin((2\pi/T).(2T/4) + \theta) = -A.\sin(\pi + \theta) \qquad (6.2.3.3)$$

$$A4 = -A.\sin((2\pi/T).(3T/4) + \theta) = -A.\sin((\pi/4) + \theta) \qquad (6.2.3.4)$$

denotes amplitude of the timing signal A_i at the i-th sample. θ is a phase angle caused by jitter inherent to the timing waveform. Then it ensues:

$A1 = -A.\sin(\theta)$ (6.2.3.5)

$A2 = -A.\cos(\theta)$ (6.2.3.6)

$A3 = A.\sin(\theta)$ (6.2.3.7)

$A4 = A.\cos(\theta)$ (6.2.3.8)

And from the above equations:

$\theta = \text{atan}(A3/A4) = \text{atan}(A1/A2)$ (6.2.3.9)

By observing amplitudes of the timing wave at the certain sampling points, the static jitter could easily be estimated. Jitter variance Var is defined as the mean square value of t_k/T, or $\theta/2\pi$. Here static jitter is assumed to be jitter inherent to the timing waveform itself. The tracking jitter is assumed to be the jitter caused by variations in tracking of timing waveform, based on the zero crossing algorithm.

6.2.4 Simulation result

In the simulation program Figure 5.2.1 the analog sections, namely the lowpass Butterworth filters are run at a 256 times higher sampling rate to accurately model the continuous time environmemt (interpolation factor I = 256). When the signal is resampled at the receiver, only 1 of these 256 outputs are used. The timing recovery circuits determine which one. The timing phase can be adjusted in increments of 1/256 of a baud. This value is close to that obtained on the actual hardware, where 280 instruction cycles were used for every baud giving an adjustement increment of 1/280.

The first series of simulations to be performed considered the effect of NBPF bandwidth (or Q) on the timing jitter. This is shown diagrammatically in Figures 6.2.4.1, 6.2.4.2, 6.2.4.3 and 6.2.4.4 for Q factors 20, 50, 70 and 100 respectively. The diagrams show the position of the forth pulse relative to the eye opening. The forth pulse activates the slicer in the decision block of the modem. The width of the scatter plot determines the jiter and the height the amplitude variation.

It is obvious from the graphs that the maximal amplitude variation of the timing waveform at the fourth sample increases as the Q factor decreases. For the Q = 20 the amplitude sometimes takes negative values. These results are as expected, the reduced bandwidth reduces the noise that causes the amplitude varaition. There is a small difference between the fourth sample point of the timing waveform and the optimal

sampling point at the eye diagram. This is not a great problem because the adaptive equaliser (if fractionally tapped) will account for this small timing error. However, at start up this will not be the case, and the timing must be sufficiently accurate to give a good eye opening, which is the case here.

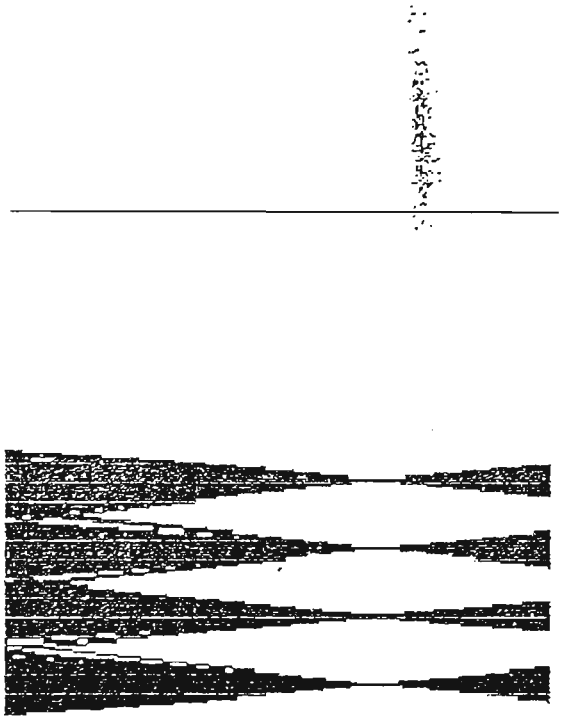

Figure 6.2.4.1 Q = 20, forth sample of the timing waveform
- eye diagram for a random sequence

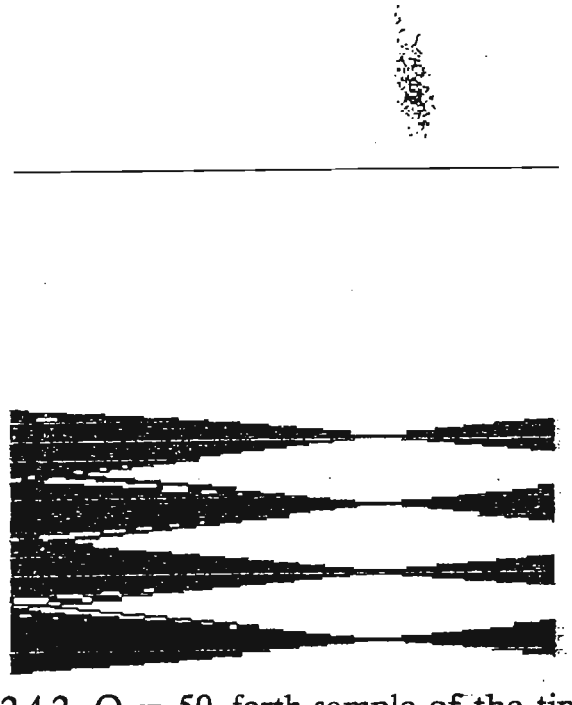

Figure 6.2.4.2 Q = 50, forth sample of the timing waveform
- eye diagram for a random sequence

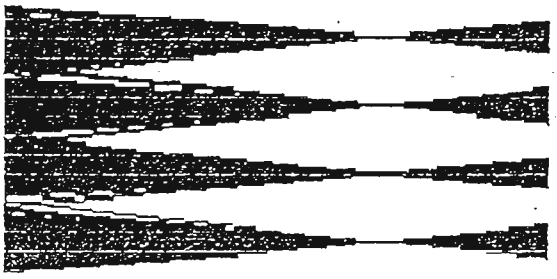

Figure 6.2.4.3 Q = 70, forth sample of the timing waveform
- eye diagram for a random sequence

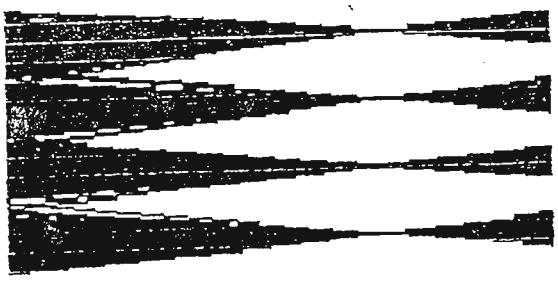

Figure 6.2.4.4 Q = 100, forth sample of the timing waveform
- eye diagram for a random sequence

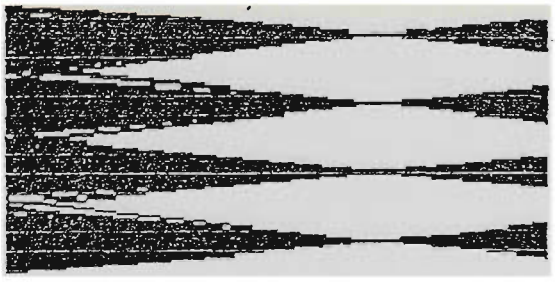

Figure 6.4.5 Q = 100, forth sample of the timing waveform - eye diagram for a random sequence; random walk filter threshold = 2

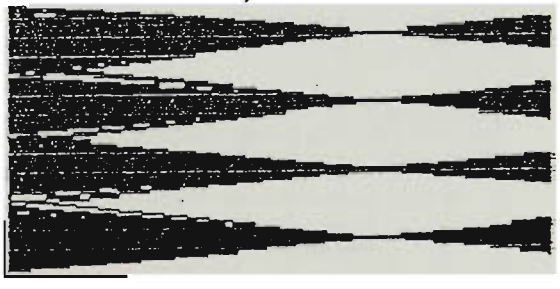

Figure 6.4.6 Q = 100, forth sample of the timing waveform - eye diagram for a random sequence; random walk filter threshold = 5

Figure 6.4.7 Q = 100, forth sample of the timing waveform - eye diagram for a random sequence; random walk filter threshold = 10

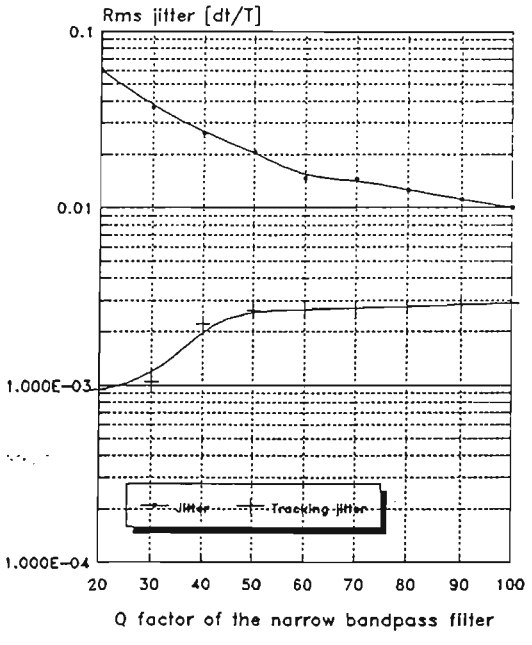

Figure 6.2.4.8 Jitter variance versus Q factor

The graphs for the system with Q = 100 and with a random walk filter incorporated in the system for different values of its thresholds: 2 (Figure 6.2.4.5), 5 (Figure 6.2.4.6) and 10 (Figure 6.2.4.7) are included. Analyzing the plots, it is evident from the graphs that random walk filter can greatly reduce the tracking jitter by an appreciable amount. A threshold of 10 was chosen.

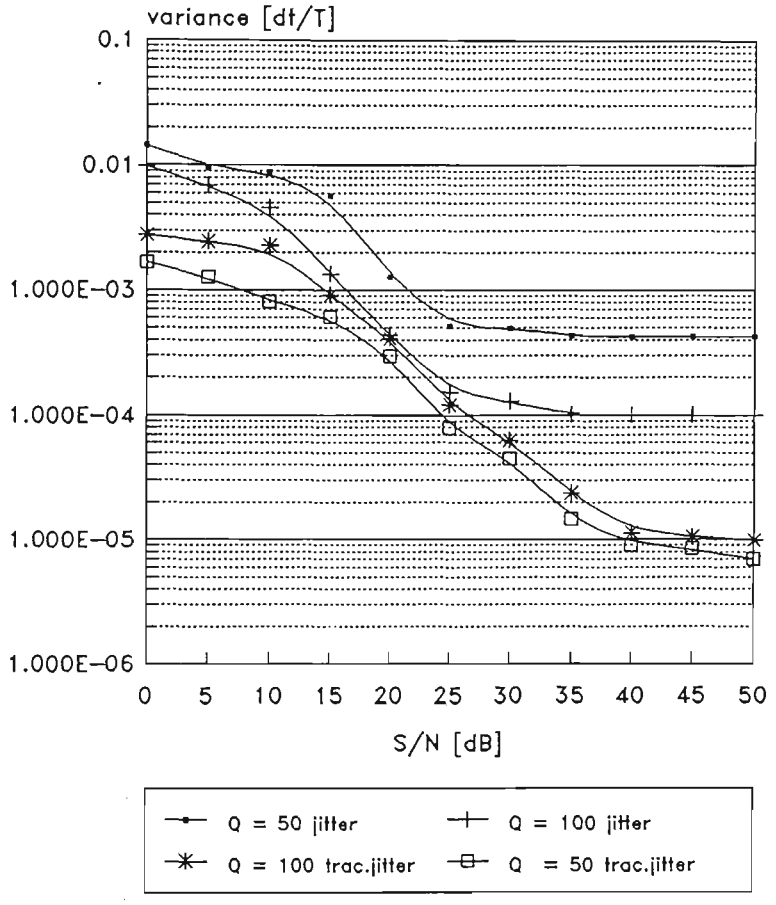

Figure 6.2.4.9 Jitter variance versus noise

Measurements of the static and tracking jitter are presented on the graphs (Figure 6.2.4.8 and Figure 6.2.4.9). The variances of the tracking jitter are much less than the variances of the static jitter. The reason is that the algorithm which tracks the static jitter (fluctuations of the timing waveform) induces some low pass filtering effects in its tracking mode. The algorithm operates in the same manner as a PLL loop. Actually, it constitutes a feedback loop, which in fact alleviates static jitter fluctuations.

Static jitter decreases as the Q factor increases, because the larger the Q factor, the smaller the bandwidth of the NBPF filter and the as a result lesser the amount of noise that could pass through the filter which could cause the phase fluctuations of the timing waveform. But the tracking jitter is decreasing with decreasing the Q factor. It seems unlogical, because it is not consistent with static jitter. It appears that the system with a filter of Q = 50 can more easily lock onto the timing waveform and more accurately the timing signal by filtering jitter and fluctuations caused by noise than the system with filter of Q = 100 (for example).

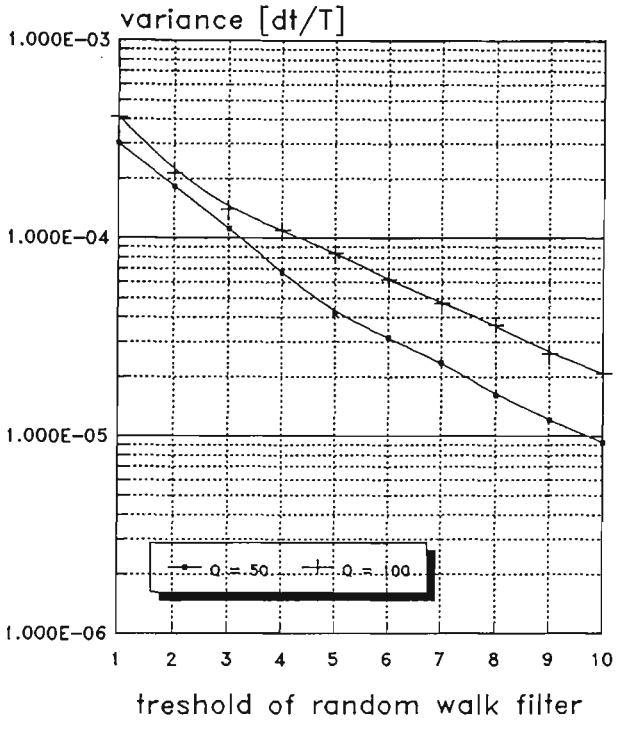

Figure 6.2.4.10 Jitter variance versus threshold

The results on the diagrams "Static jitter variance versus Q factor" (Figure 6.2.4.8) and "Static jitter versus noise" (Figure 6.2.4.9) are approximately the same as reported by Franks and Bubrovski (46), and N.A.D'Andrea and U. Mengali (47). There is a small difference (10 - 15 %) with the results of (47). The reason could be because of the fact that different pseudo-random sequence were used for each measurements.

Diagrams "Tracking jitter versus threshold" and "Convergence speed versus

threshold" are included (Figure 6.2.4.10) and (Figure 6.2.4.11). It is evident from the diagrams that with larger value of threshold of the employed random walk filter tracking jitter decreases, but unfortunately the convergence speed decreases too. The convergence speed is taken to be within 4% of optimum from an initial condition of the signal being half a baud period out of the phase synchronisation.

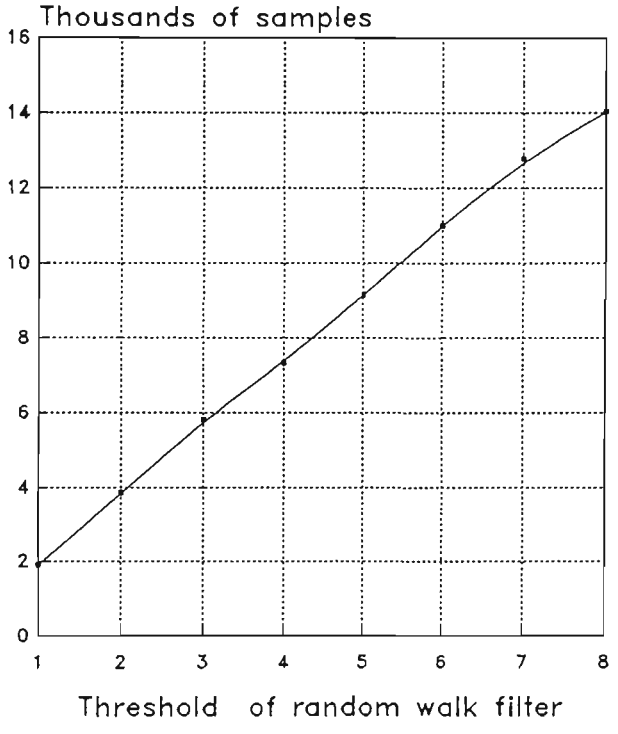

Figure 6.2.4.11 Convergence speed versus threshold

6.2.5 DSP microprocessor model

The TMS320C25 provides a 16-bit (TIM) on chip timer and its associated interrupt to perform various function at regular time intervals. It also provides 16-bit period (PRD) register [35]. The timer is a down counter that is continuously clocked by CLKOUT1, and counts (PRD + 1) cycles of CLKOUT1. The period register holds the starting count for the timer.

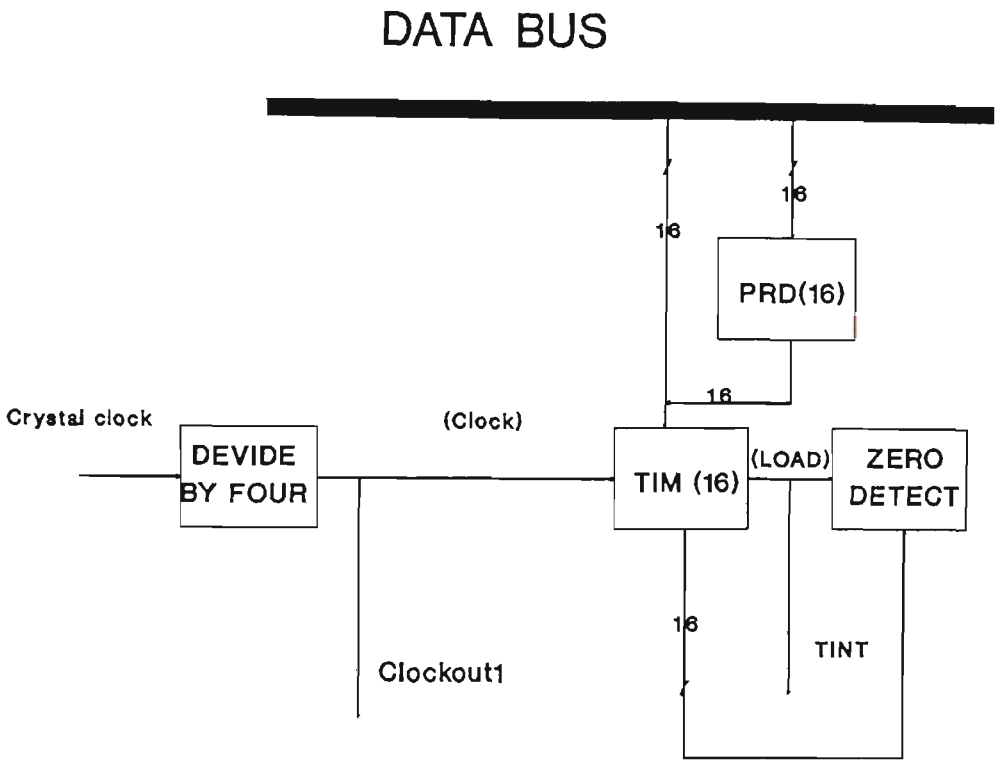

Figure 6.2.5.1 TMS320C25 timer block diagram

A timer interrupt is generated every time the timer decrements to zero, and then the timer register is reloaded with the value contained in the period register within the next cycles after it reaches zero. The timer and period register can be read from or written to on any cycle. The count can be monitored by reading the TIM register. The timer block diagram is shown on the Figure 6.2.3.1. The timer is a Numerical Controlled Oscillator (NCO), which is illustrated in Figure 6.2.2.1. This forms the Voltage Controlled Clock (VCC) in the DSP software.

6.3 Carrier recovery

This section explaines the carrier recovery algorithm applied for the construction of the PLC modem.

6.3.0 Introduction

Optimum demodulation requires a local carrier at the receiver side whose frequency and phase are in perfect alignment with that of the transmitted signal. In principle, two pairs of the identical signal oscillators could ensure the synchronization and coherence required for proper operation of the system, but this solution is usually too expensive. A phase and frequency offset therefore exists between the receiver and transmitter. Furthermore transmission of the modulated signal through the different media (in this case EHV power line) introduces not only signal distortions and noise, but also to some extent phase jitter. These must all be compensated for. In addition the convergence time should be small so as to minimise the modem start up time. Here differences between the two programmable crystal oscillators must be taken into account. Frequency stability is ±0.015%. The worst possible frequency offset is 150 Hz at the maximal carrier frequency of 500 KHz. The overall phase difference could be modeled as a fixed frequency offset (linear phase shift with time) and a random or quasi-periodic waveform that is a manifestation of the phase jitter.

Optimum techniques are based on the state variable formulation (ranging from the simple extended Kalman filters to the more sophisticated optimum nonlinear techniques to rotational process estimation techniques). Unfortunately, most of these approaches are associated with a very high computational complexity, and thus, are of no practical interest for this applications in spite of their optimality.

There are three main types of carrier synchronizers: the remodulator, the squaring loop (more generally: power of N), and the Costas loop (used in two-dimensional, suppressed-carrier, data communication systems). They differ in the positioning of the nonlinearity, which, in the squaring loop, is entirely separated from the

PLL, while in the case of remodulator and Costas loop it is included in the phase detector. In the remodulator synchronizer the received signal is demodulated, and the message is recovered, which is then used to remodulate the received signal so as to remove the modulation. If the baseband waveforms are time aligned, the output of the balanced modulator has pure carrier component that can be tracked by the PLL. The squaring loop is in fact a quadrupling loop for QAM-16. The Costas loop is actually a decision-directed synchronizer. Decision - directed techniques are used at the level of the baseband signal.

Decision directed synchronizers give excellent noise rejection, but unfortunately, they cannot acquire the carrier until a clock has been obtained. Thus, it is not recommended for applications requiring fast acquisition. This system does not require fast acquisition but if it did, some special predefined pretraining sequence would be necessary to quickly acquire the correct symbol timing and carrier phase. A stable lock can be achieved at any of the four different phases. There is an inherent fourfold ambiguity that must be resolved.

In this case the demodulation has been done at the analog part of the receiver, and the carrier recovery circuit is included to correct the signal phase only. A phase rotator in DSP performs this task.

6.3.1 Decision directed carrier recovery

The carrier recovery scheme used here are known as a decision directed technique. The slicer simply decides which constellation point A(n) is the closest to the equaliser output X(n). The phase discriminator supplies the loop filter with an estimate E(n) of the counterclockwise rotation that needs to be applied to A(n) to arrive at X(n). Mathematically:

$$\phi(n+1) = \phi(n) + E(n).K \qquad (6.3.1.1)$$

$$E(n) = \arcsin \frac{Im\{X(n) \; . \; A(n)^*\}}{|X(n)| \; . \; |A(n)|} \qquad (6.3.1.2)$$

where E(n) is the phase error, $\phi(n)$ isthe phase of the VCO at the interval n, $\phi(n+1)$ is the phase at the next interval (n + 1), X(n) is the complex signal at the input of the phase detector, and $A(n) = X_{des} + i.Y_{des}$ is the output from the slicer at the n-th interval. K is a small number ($0 < K <= 1$), and it is referred as a tracking coefficient (Figure 6.3.1.1). It is common to simplify still further equation 6.3.1.2 and omit denominator in the calculation, so as to avoid the division. Division as a mathematical operation is difficult to implement in the TMS 320C25. A careful design of loop filter can lead to carrier recovery loops that perfectly track frequency offset or phase jitter at selected frequencies.

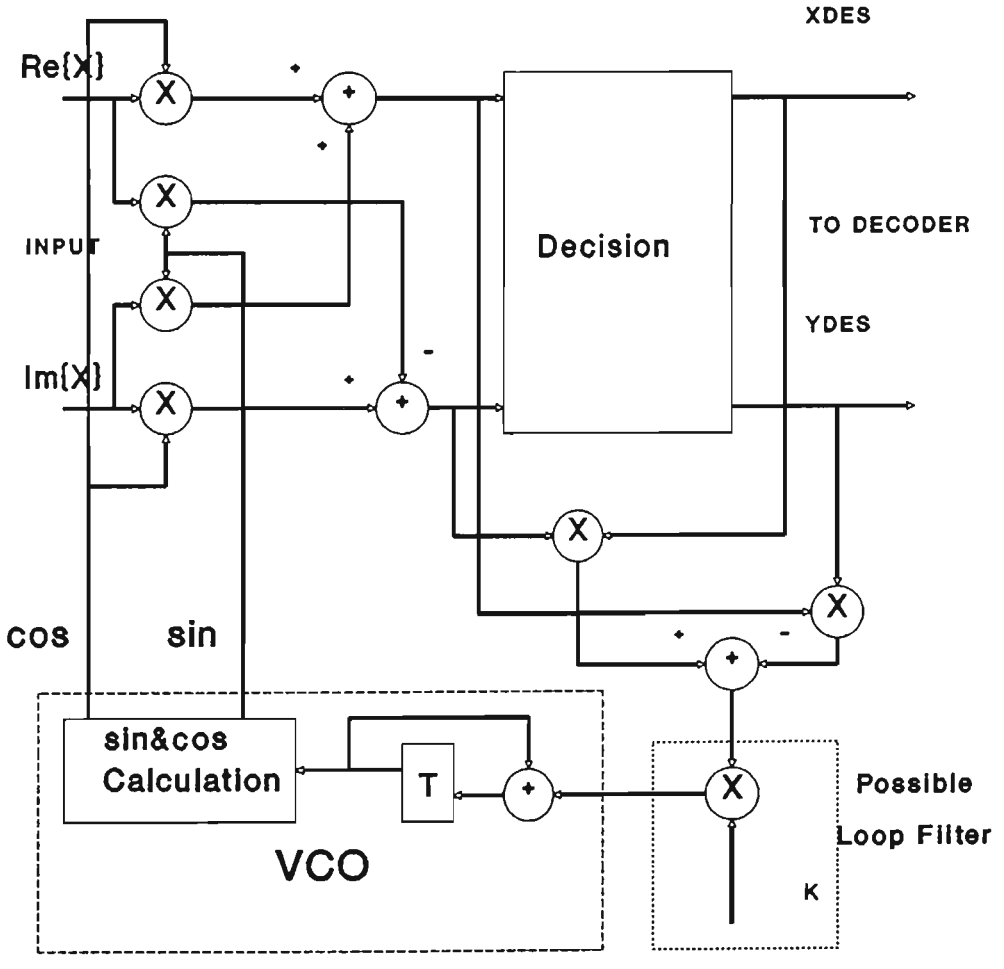

Figure 6.3.3.1 Decision-directed synchroniser

As an illustration of the receiver effectiveness in tracking and removing sinusoidal phase jitter the diagrams of the residual phase jitter are included for

channels with signal to noise ratio 20 dB and 30 dB versus tracking coefficient (Figure 6.3.1.2 and Figure 6.3.1.3). The jitter is 14-degrees peak to peak sinusoidal with frequencies of 50 Hz and 200 Hz. It is evident from the graphs that there are different optimal values of tracking coefficients for different values of frequency jitter. For the channel with S/N equal to 30 dB at 50 Hz jitter frequency, the optimal value for the tracking coefficients is about 0.3, whereas at 200 Hz, the optimal value is about 0.6. For the channel with S/N equal to 20 dB, the optimal value for both frequencies is about 0.3. The no jitter curves show the effect of noise only, in this case the smaller the value of K the better.

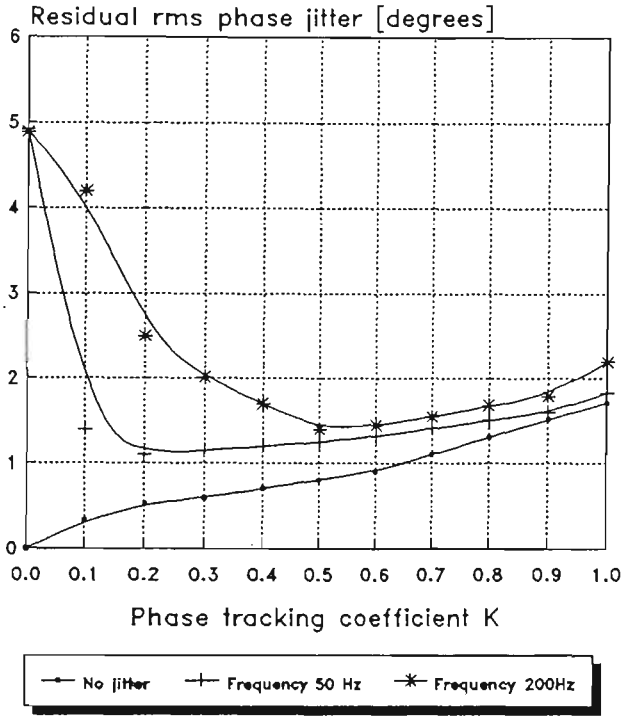

Figure 6.3.1.2 Residual rms phase jitter for channel with S/N = 20 dB

Also plots are included which show two-dimensional QAM-16 output constellations for the various values of the tracking coefficient K. Jitter is the sinusoidal phase jitter with frequency 50 Hz (Figure 6.3.1.4). There is no noise. It is obvious from the graphs that for K = 0.01 the first-order PLL loop could not perfectly track the phase jitter, resulting in banana-like shapes lying along the circumferences of the circles centered at the origin (Figure 6.3.1.5). K = 0.3 allows sinusoidal jitter to be

tracked, and almost completely canceled from the receiver (Figure 6.3.1.6). In Figure 6.3.1.7 K = 1, the system can perfectly track the phase jitter, but the residual RMS jitter is slightly larger.

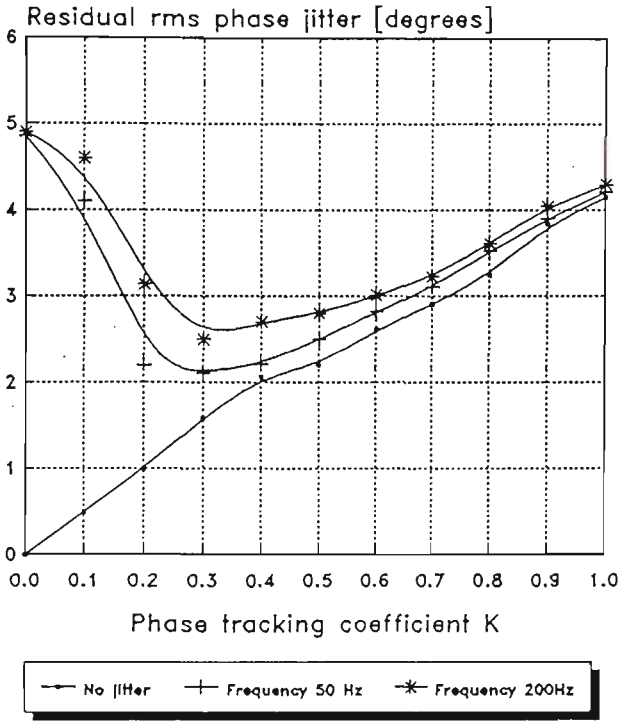

Figure 6.3.1,3 Residual rms phase jitter for the channel with S/N = 30 dB

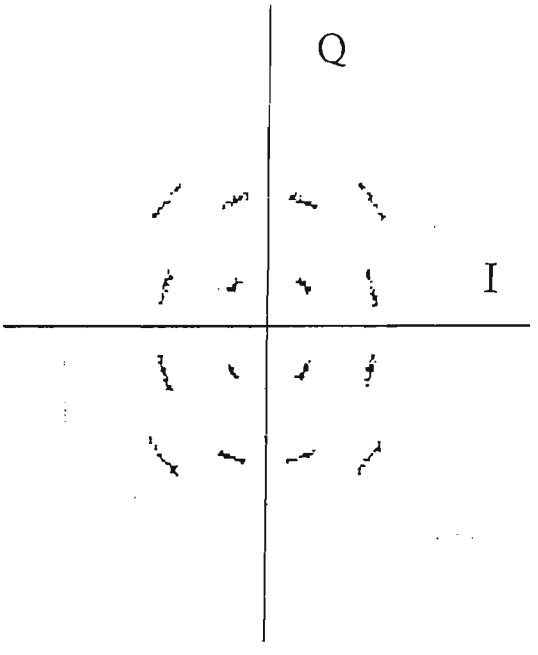

Figure 6.3.1.4 Signal constellation - sinusoidal phase jitter. 14 degree peak to peak - frequency 50 Hz.

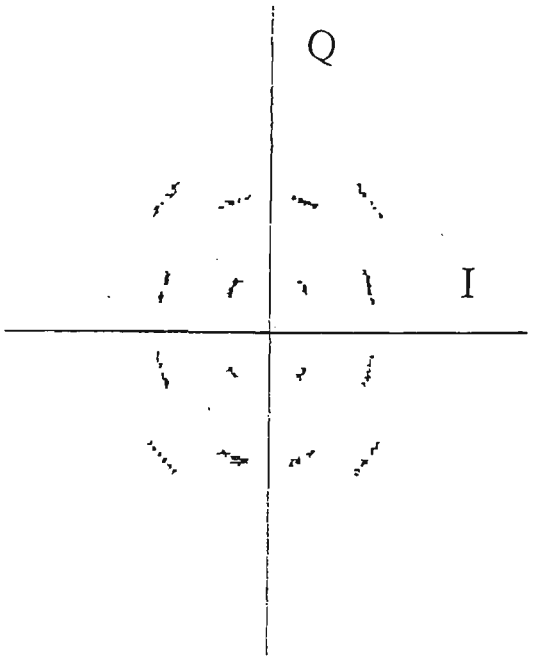

Figure 6.3.1.5 Signal constellation - sinusoidal phase jitter. 14 degree peak to peak - frequency offset 50 Hz. Receiver K = 0.01

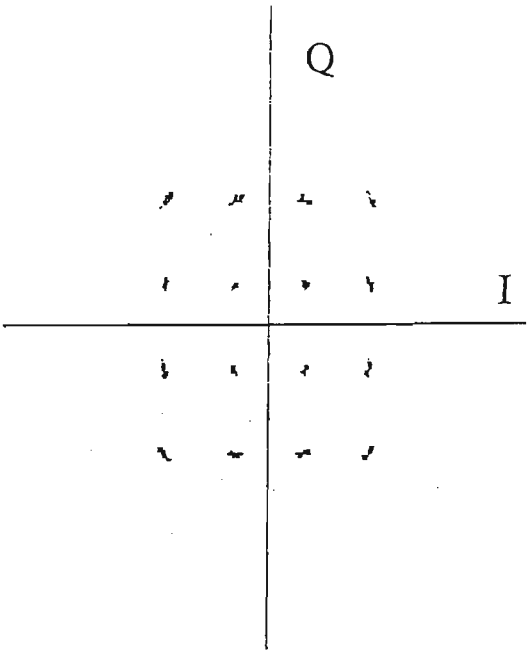

Figure 6.3.1.6 Signal constellation - sinusoidal phase jitter. 14 degree peak to peak - frequency 50 Hz. Receiver K = 0.3

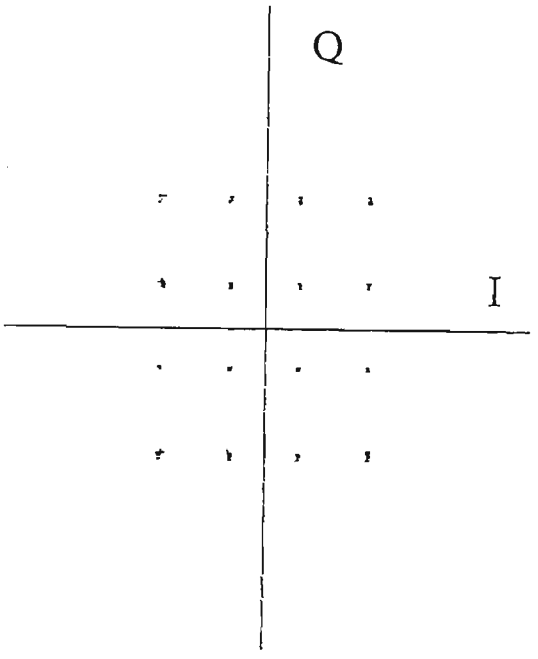

Figure 6.3.1.7 Signal constellation - sinusoidal phase jitter. 14 degree peak to peak - frequency 50 Hz. Receiver K = 1

The influence of the additive random noise is the scatter plot like circles centered at the decision points with radii proportional to the rms value of the noise. From diagrams (Figure 6.3.1.2 and 6.3.1.3) it is obvious that with decreasing K, the residual rms phase jitter is decreasing. So it is not recommended to use a greater K number than it is necessary to have to follow phase jitter. The optimum value of parameter K depends on the noise and phase jitter parameters, so a reasonable design compromise can be made [50].

The symetrical nature of the square QAM-16 constallation means there is a 90◦ phase ambiguity. Errors in decision will result in an incorrect phase detection. A phase ambiguity is solved by employing a differential encoder at transmitter and a differential decoder at the receiver. Then the information is carried by change in phase, rather than by the absolute phase. For the QAM-16 encoding only two bits are used to determine the quadrant.

6.3.2 Analysis

The carrier recovery scheme applied here are known as second order decision directed techniques. An additional loop filter is added to the feedback path (Figure 6.3.2.1) to improve the handling of frequency offsets. The loop filter takes the error signal E(n) and scales it down by a factor C_2 to get an estimate of the phase jitter, and further scale down by a factor C_1 to make any necessary correction to its estimate of frequency offset. DPLL (digital phase local loop) consist of three major functional units:

(a) phase detector (PD)

(b) digital loop filter

(c) voltage controlled oscillators (VCO)

This second order DPLL is equivalent to an analog PLL with a linear phase detector which has a first order active filter as a loop filter. The voltage controlled oscillator is based on a microprocessor implementation using a look-up table to generate sine and cosine waveforms. This DPLL provides an extremely wide frequency tracking range and completely linear behavior. Using z transform techniques the transfer function of the DPLL is:

$$H(z) = \frac{C_2(z-1) + C_1}{(z-1)^2 + C_2(z-1) + 1} \qquad (6.3.2.1)$$

Equivalent second order analog system transfer function is:

$$H(s) = \frac{\eta w_n + w_n}{s^2 + 2w_n s + w_n} \qquad (6.3.2.2)$$

Where η is the damping factor and w_n is natural frequency of analog counterpart PLL. When the sampling frequency is very high compared to the natural frequency of the loop ($w_nT << 1$) it could be written:

$$C_2 = 2nw_nT \qquad (6.3.2.3)$$

$$C_1 = C_2/4\eta \qquad (6.3.2.4)$$

Phase response of the DPLL is:

$$H_e(z) = \frac{(z-1)^2}{(z-1)^2 + C_2(z-1) + C_1} \qquad (6.3.2.5)$$

Using final value theorem it can be shown that the steady-state phase error is zero for both frequency (dw) and phase step (dθ) inputs. The transient can be found by taking the inverse Z-transform of the following equations:

$$H_e(z) = \frac{dw.T.z}{(z-1)^2 + C_2(z-1) + C_1} \qquad (6.3.2.6)$$

and:

$$H_e(z) = \frac{d\theta.z.(z-1)}{(z-1)^2 + C_2(z-1) + C_1} \qquad (6.3.2.7)$$

The DC loop gain is given by:

$$K_v = \lim_{z \to 1} \frac{C_1 + C_2(z - 1)}{(z - 1)^2} \to \infty \qquad (6.3.2.8)$$

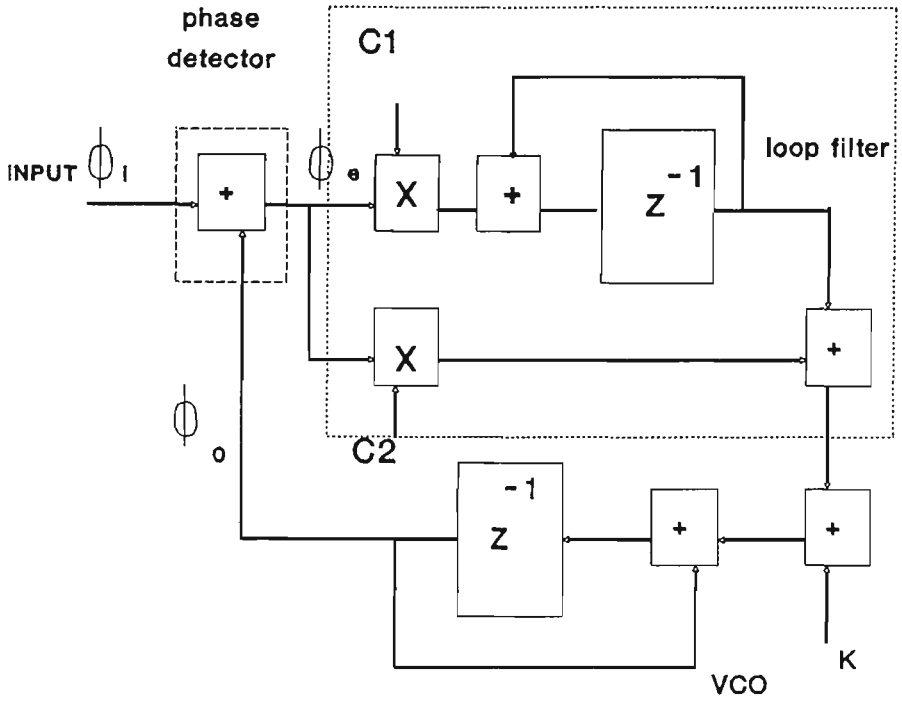

Figure 6.3.2.1 Loop filter incorporated in DPLL

The tracking range is proportional to the loop DC gain; so the DPLL has a very wide tracking range, which is only limited by half the sampling frequency. The condition for stability of the DPLL is:

$$\frac{2 - C_2 \pm \sqrt{[(C_2 - 2)^2 - 4(C_1 - C_2 + 1)]}}{2} < 1 \qquad (6.3.2.9)$$

Or it ensues:

$$2C_2 - 4 < C_1 < C_2, \quad (6.3.2.10)$$

$$C_1 > 0 \quad (6.3.2.11)$$

It is noted that due to the truncation errors, sometimes an oscillation can be seen at the output of a digital filter, even in the stable region of the coefficients of the filter.

The VCO is modeled as a perfect integrator. Also it is seen that it is better to limit the input phase that has to be corrected to half of the closest non zero angle between any two constellation points, in order to limit its sensitivity to noise (additive and adaption).

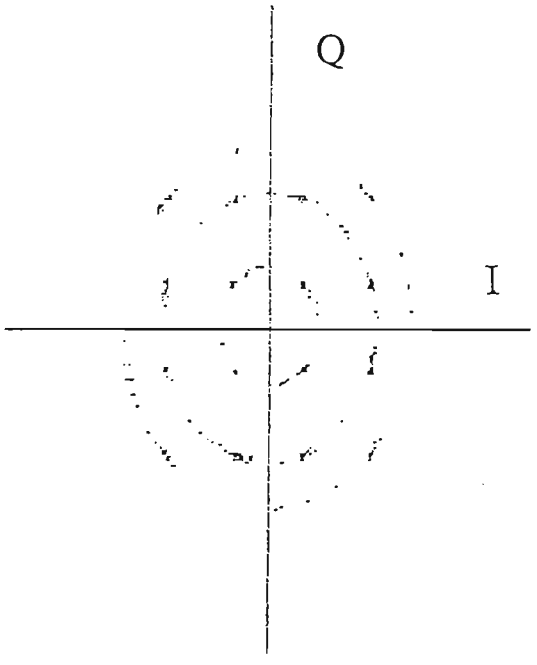

Figure 6.3.2.2 Signal constellation with frequency offset 250 Hz, Loop filter - natural frequency 50 Hz. After 700 symbols.

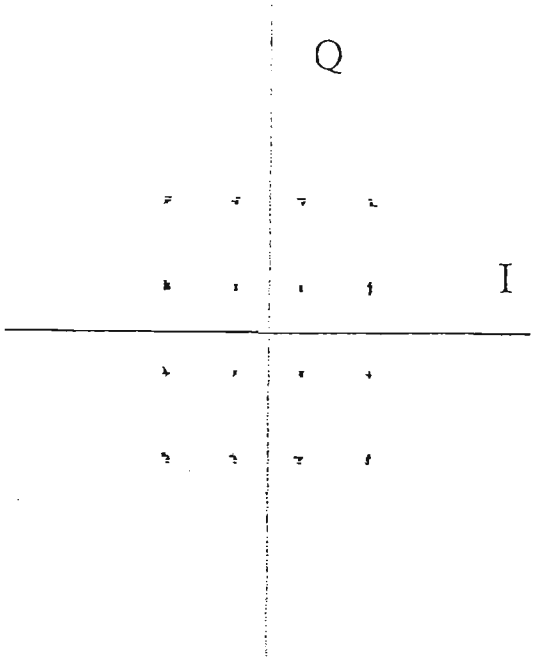

Figure 6.3.2.3 Signal constellation with frequency offset 250 Hz, Loop filter - natural frequency 100 Hz. After 700 symbols.

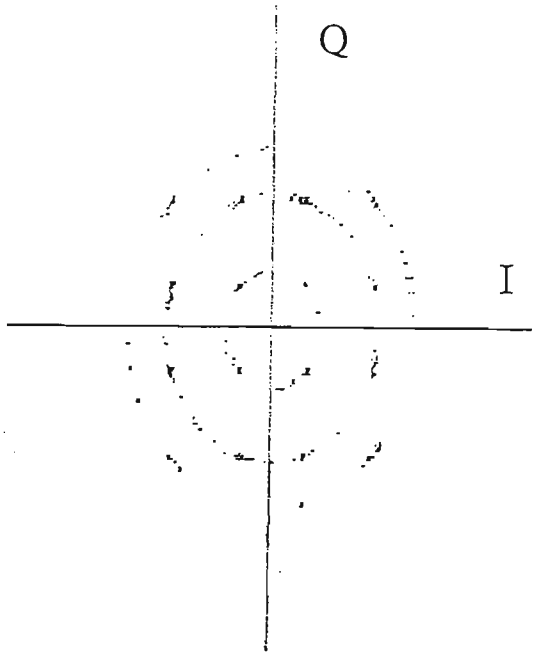

Figure 6.3.2.4 Signal constellation with frequency offset 500 Hz, Loop filter - natural frequency 50 Hz. After 2500 symbols.

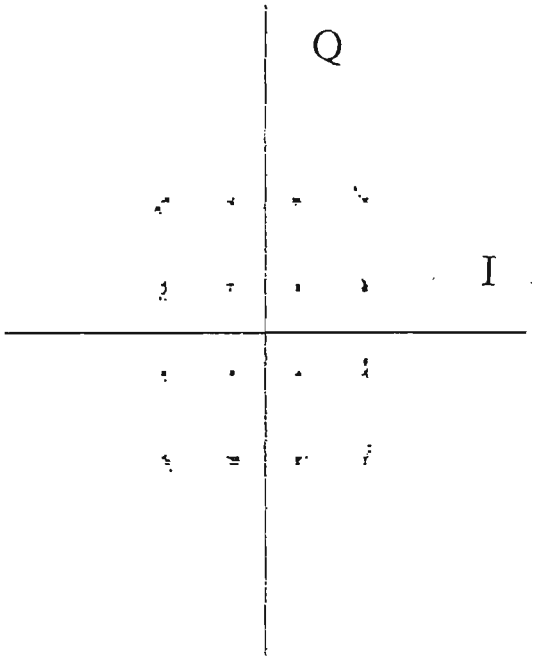

Figure 6.3.2.5 Signal constellatiom with frequency offset 500 Hz,
Loop filter - natural 50 Hz. After 3000 symbols.

The bandwidth of the loop filter plays a significant role in the design of the carrier recovery loop. The loop bandwidth must be greater than the expected frequency offset and its natural frequency must be also greater than the frequency offset. The larger the bandwidth, the faster is the settling time as it is evident from Figure 6.3.2.2 to Figure 6.3.2.5. But from the other point of view it is better to have a bandwidth as narrow as possible, because the amount of the noise which pass through the loop filter is proportional to the filter bandwidth. Residual RMS phase jitter is illustrated as the function of a natural frequency of a PLL for the channels with different S/N ratios (Figure 6.3.2.6). From this figure it is evident that the smaller the natural frequency, the smaller the bandwidth of the loop filter and accordingly the smaller the amount of the noise passed through the filter. Hence the jitter too is small.

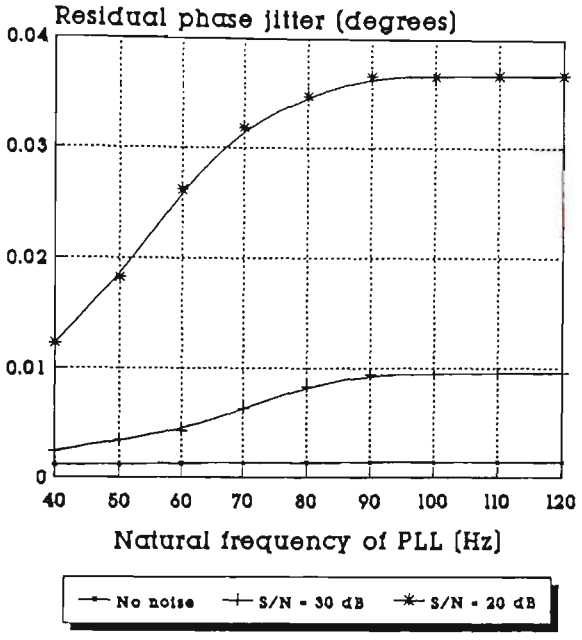

Figure 6.3.2.6 Residual rms phase jitter
Decision directed carrier recovery; Second order digital PLL

One of the more important part of clock recovery circuits is a sinewave generator. Here,in DSP design, it is simply the reading out of a series of stored data value representing discrete samples of the sine wave to be generated. The sine waveform is generated by repeatedly cycling through the data memory locations. These samples are represented in binary two's complement form in 16-bit format. The address counter is required in the form of a modulo counter providing wrap-around at the end of the data table to make algorithm efficient. By continuously varying the step size of the address counter any frequency can be generated within sampling constrains. The frequency of the oscillation is given by equation:

$$f = STEP/(T_s \times N) \qquad (6.3.2.12)$$

where STEP is the address counter increment and N is the number of stored samples. Memory reduction techniques could be employed in order to reduce memory requirements, and only a quarter of the memory needs to be stored requiring a more

complex algorithm, which keeps track of which quadrant of the waveform is to be generated and with what sign. The cosine waveform is generated by employing offset from the main pointer such that the data samples accessed are phase shifted by 90 degrees. Because memory reduction techniques take a large number of instructions, a simpler algorithm was chosen, with a look up table of 256 entries.

6.3.3 Circuit calculation

For the loop filter a natural frequency, w_n = 100 Hz, and damping factor η = 0.707 are chosen. Coefficients of the loop are calculated according to the before mentioned formulae, and they are: C_2 = 0.10330 and C_1 = 0.051653. The amplitude frequency response of this DPLL is illustarated in Figure 6.3.3.1. The configuration of the filter is slightly revised to account for the small value of coefficient C_1, because quantisation effects deteriorate the performance. To overcome this problem coefficient C_2 is placed before the filter algorithm implementation and the filter polynomial is divided at same time with C_2. In that way instead of the C_1, the filter calculation is performed on the C_1/C_2, which is not so small number as C_1 (Figure 6.3.3.2). In this case C_1/C_2 is 0.51665 (or in two's complement representation 1692) which is a quite acceptable value for DSP implementation.

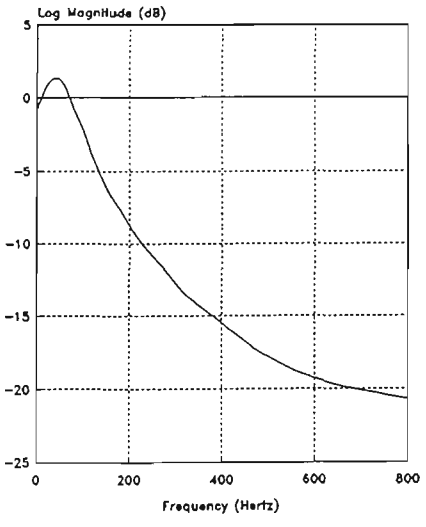

Figure 6.3.3.1 Transfer function of DPLL
log magnitude (dB) versus frequency

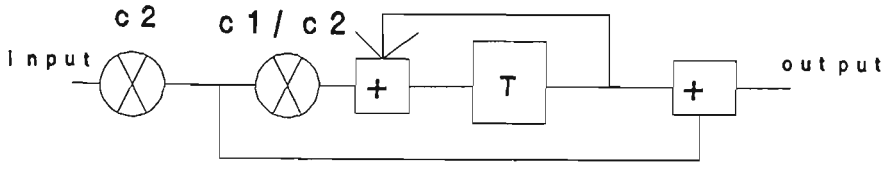

Figure 6.3.3.2. PLL filter configuration

6.4 Equaliser

6.4.0 Introduction

The amplitude and delay distortion encountered in the transmission of digital signals through PLC channels results in intersymbol interference at sampling instants. The purpose of equalization is to reduce the ISI to a point where the receiver has a high probability of making a correct decision in the presence of noise. Ideally, the equalizer should have the inverse frequency response of the channel. Accordingly, the overall system should have a flat amplitude and linear phase characteristics [60].

The simplest structure selected was the tapped delay line filter, known as a linear transversal equalizer (Figure 6.4.0.1). Tapped delay lines are at intervals of sampling

time T. This structure has no feedback. It is easily designed; extremely versatile, simple and straightforward to implement using DSP techniques and always stable. The transversal filter structure consist of a shift register, a summer, and multipliers (often called tap coefficients). Each tap is associated with a multiplication coefficient. The outputs from these multipliers are added together in a summing network to provide the equalized output [61].

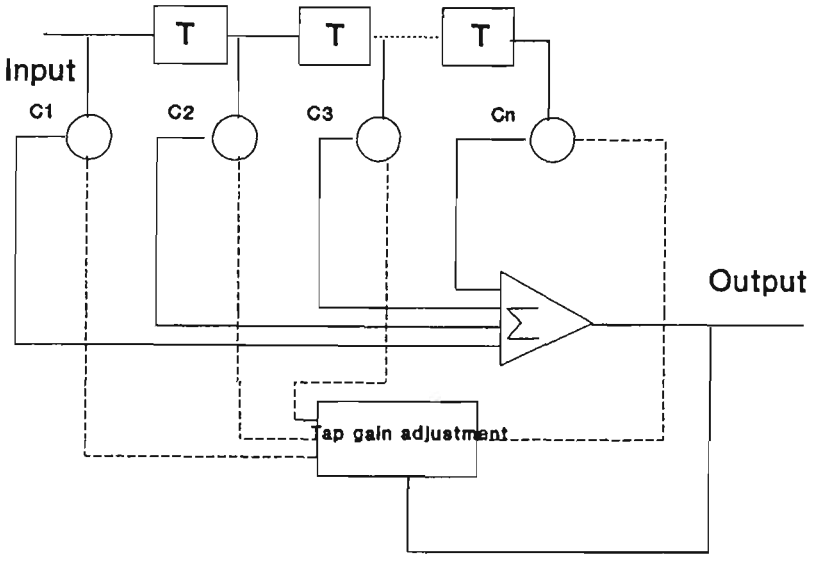

Figure 6.4.1.1 Linear transversal equaliser

As PLC characteristics are time varying, it is necessary to make the equalization process adaptive, which is achieved by dynamic adjustment of tap coefficients. The design of the adaptive equalizer involves the selection of the criterion (or cost function) for optimizing the filter tap weight coefficients. The algorithm uses error samples e(n) to adjust the filter tap coefficients in order to reduce the cost function iteratively. In adaptive equalization, the error voltage e(n) is continually estimated during the course of normal data transmission, and

corrections to the equalizer are effected as required. Since the most meaningful measure of performance for a digital communications system is the average probability of error, it is convenient to choose the coefficients to minimize this performance index. However, the probability of error is a highly nonlinear function of tap coefficients, and as result it is impractical as a criterion for optimizing the tap weight coefficients of the equalizer. Two criteria have found widespread use in optimizing the equalizer coefficients. One is the peak distortion criterion and the other is the mean-square-error criterion [60].

The PLC modem does not require fast initialization, only on-line tracking of small variations in the channel. Algorithms for adjusting the equalizer coefficients to track time variations in the channel may range from a simple LMS (least-mean-square) algorithm which converges relatively slowly, to a recursive least squares Kalman algorithm or a recursive least squares lattice algorithm which converge relatively fast. The latter is also more accurate, but requires more processing time for its implementation [61]

6.4.1 LMS algorithm

The MSE criterion is defined as the statistical average of the square of the error samples. It can be minimized by incrementally adjusting the tap coefficients in a direction opposite the gradient of the cost function (in the direction of the steepest descent). The resulting algorithm for at n+1-th iteration is [61]:

$$\mathbf{H}(n+1) = \mathbf{H}(n) + u.E[\mathbf{e}(n).\mathbf{X}(n)] \qquad (6.4.1.1)$$

where $\mathbf{H}(n)$ is the vector of k filter coefficients, u is the gain constant, $\mathbf{e}(n)$ is an error signal, and $\mathbf{X}(n)$ is the vector of the k input signals at n-th sampling interval. E[] denotes statistical average. The parameter u controls the convergence rate of the equalizer i.e. how fast the coefficients acquire the desired value. It also reflects algorithm stability. Therefore, u is the constant that regulates the speed and stability of convergence. Also, if the coefficient u decreases, the residual mean squared error decreases too, and vice versa. However, it is impractical to compute the exact

statistical average in real time, so a suitable estimate must be made. A simple, yet effective estimate is to just use the argument e(n).**X**(n) without averaging. The result:

$$\mathbf{H}(n+1) = \mathbf{H}(n) + u \,.\, \mathbf{e}(n) \,.\, \mathbf{X}(n) \qquad (6.4.1.2)$$

is known as the LMS gradient algorithm. The LMS algorithm should be adequate in tracking the time variations in PLC channels where the time variation of the channel is extremely slow relative to the data rate.

By analyzing the typical impulse response of the PLC cannel, corresponding to a power line 100 km long, it has been found that the equalizer should have at least 5-6 taps, as it was previously mentioned. Taking the number of the taps in the T-spaced equalizer as N, the effect of N and u on the rate of convergence would be described by following equations [60]:

Convergence of the steepest-descent algorithm is ensured if u satisfies the inequality:

$$u < 2/(N.\text{signal power}) \qquad (6.4.1.3)$$

In order to establish the convergence properties of the recursive algorithm, normally selected value of u is given as:

$$u = 0.2/(N.\text{signal power}) \qquad (6.4.1.4)$$

Taking N = 6 (signal power = 1), it is:

$$= 0.03333 \qquad (6.4.1.5)$$

Convergence time constant t_{mse} is given as:

$$t_{mse} = T/(4.u.\text{signal power}) \qquad (6.4.1.6)$$

And settling time τ is:

$$\tau = 4.t_{mse} \qquad (6.9.1.7)$$

Here in the DSP implementation, tap coefficients are updated so that in each baud (See the block diagram of the TMS320C25 assembler program) only one coefficient is updated. It is not necessary to update all the coefficients at the same time, because the PLC channel varies relatively slowly compared to the data rate. This greatly reduces the number of instructions in the DSP implementation.

The samples, x(n-k), are readily available, since they are contents of the shift register. However, e(n) = y(n) - a(n), requires knowledge of the transmitted data a(n), which is unknown by the receiver. y(n) are the outputs of the equalizer. Here the error in an adaptive equalizer can be computed by assuming that the receiver decisions for a(n) have a high probability of being correct, and thus can be substituted for the actual values. This operation is called a decision-directed (the equalizer algorithm is driven by receiver decision). Since the error signal e(n) is a function of both channel characteristics and transmitted data, adjusted tap coefficients are determined not only by the channel characteristics, but also by the autocorrelation of the transmitted data sequence a(n). If the transmitted data is uncorrelated, the channel can be equalized to obtain a flat frequency characteristic. If it is not the case, whitening of the correlated digital data sequence is possible using a scrambler and descrambler. Here, in test system, there is no need for whitening of the data sequence, because a PN generator is used to generate the input data test sequence. Only commercial application of the modem is likely to require such a scrambler.

6.4.2 Complex equalizer

As the demodulated QAM-16, can be resolved into two quadrature components, each component must be equalized separately. Since both signal components pass through the same channel, the two input signals can be considered as the real and imaginary part of a complex signal and likewise, the main and cross-modulation coefficients of the equalizer as the real and imaginary parts of an array of complex equalizer coefficients. The corresponding equalizer is a two dimensional (complex) equalizer [60]. The MSE cost function can be defined and the gradient algorithm can then be determined in two dimensions, resulting in both in-phase and quadrature tap updates. The complex equalizer with complex input

is equivalent to four parallel equalizers with real-valued tap coefficients (Figure 6.4.2.1).

$$(I + i.Q)(a + i.b) = I' + j.Q' \qquad (6.4.1.1)$$

where:

$$I' = a.I - b.Q \qquad (6.4.2.2)$$

and $$Q' = b.I + a.Q \qquad (6.4.2.3)$$

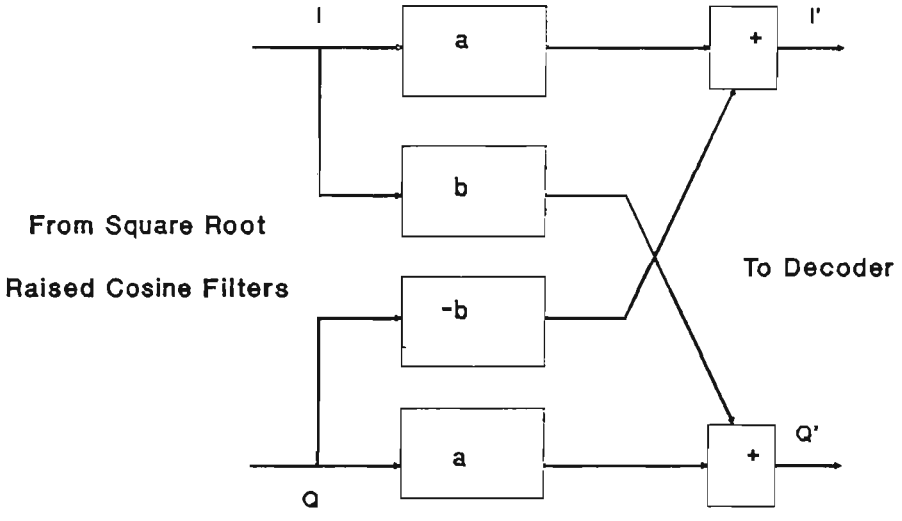

Figure 6.4.2.1 Complex equaliser

The location of the equalizer in the receiver varies from case to case. Here equalization has been performed in the baseband stage after the demodulation. In the case where equalization is located after coherent demodulation and inside the loop for decision-directed phase compensation, the equalizer itself introduces a

many symbol-interval delay between input and output; therefore the estimated phase sequence is a delayed version of the true phase sequence, which prevents the receiver from correctly compensating any time varying phase shift introduced by the channel.

For this configuration the problem is circumvented; it places phase compensation after the equalizer (See the demodulator block diagram), while the demodulation is performed using a free running oscillator before the equalizer. Taking into account the tap-rotation property, the equalizer can track small amounts of the phase jitter and frequency offset so that the phase compensation loop after the equalizer is not required [62].

In this case, however, a relatively large frequency offset is expected, so that the carrier recovery function block cannot be omitted. Also, one additional operation is needed to rotate the error backward. This gives the unrotated decision error, Eur = Eux + i.Euy (which is used in the equalization algorithms), to rotate the signal an angle G. The following expressions are used:

$$Eux = Ex.\cos G + Ey.\sin G \qquad (6.4.2.3)$$

$$Euy = Ex.\sin G + Ey.\cos G \qquad (6.4.2.4)$$

where E = Ex + i.Ey is the decision error.

6.4.3 Fractional spaced equalizer

A fractional spaced equalizer is one whose delay line taps are spaced at an interval which is less than the symbol interval T (Figure 6.4.3.1) [103]. It must be kept in mind that the signal at the output of the equalizer is still sampled at a rate of 1/T. The filter output is given by the following expression for a T/2 spaced equaliser:

$$\mathbf{Y}(nT) = \mathbf{H}(nT).\mathbf{X}(\tau + kT - nT/2) \qquad (6.4.3.1)$$

The coefficients of a T/2 equalizer may be updated once per symbol, based on the error computed for the symbol, according to

$$\mathbf{H}(n+1) = \mathbf{H}(n) - u.e(k).\mathbf{X}(\tau + kT - nT/2), \qquad (6.4.3.2)$$

for $n = 0,1,...,N-1.$

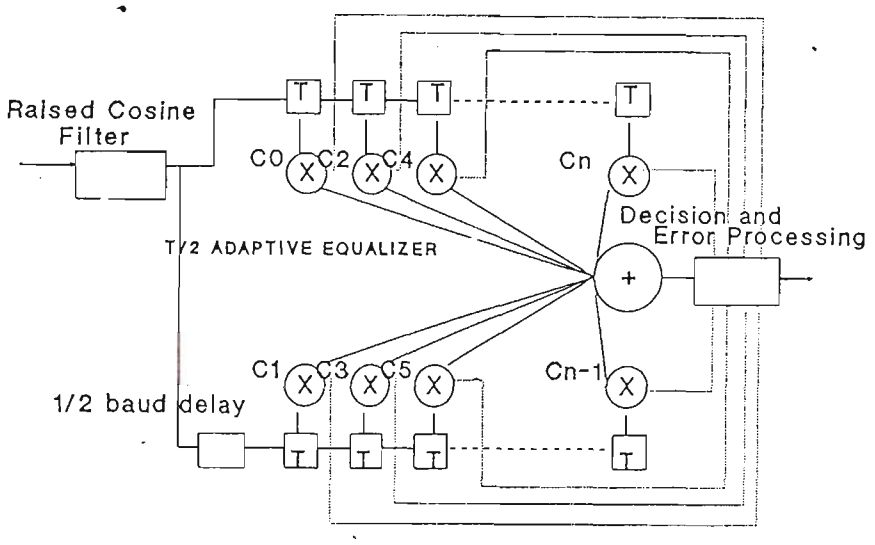

Figure 6.4.3.1 Fractional spaced equaliser

where τ is the initial time. Simulation of equalizers whose delay line taps are spaced at an interval which is half of the symbol interval, QAM modulation and data transmission over typical voice grade circuits seems to confirm the improvements over nonfractional spaced equalization, predicted by the theory. In particular (1) The T/2 equalizer performs almost as well or even better than a T equalizer with the same number of TDL coefficients (i.e. half the time span), (2) A receiving filter preceding the equalizer (raised cosine filter) is not required with a T/2 equalizer (but the filter may still improve the performance of the system), (3) For channels with a severe band-edge

distortion, the T/2 equalizer outperforms the T equalizer regardless of the choice of the sampling instant.

Symbol rate sampling at the input to a T equalizer causes spectral overlap or aliasing. When the phases of the overlapping components match they add constructively; when the phases are 180 degree apart, they add destructively, which results in the cancellation or reduction of the amplitude. Variation in the sampler phase or timing instants corresponds to a variable delay in the signal path; a linear phase component with a variable slope is added to the signal spectrum. Thus, changes in the sampler phase strongly influence the effect of aliasing; i.e. they influence the amplitude and delay characteristics in the spectral overlap region of the sampled equalized input.

In contrast, there is no spectral overlap at the input to fractional spaced equalizer. Therefore, it can adjust the channel spectrum (amplitude and phase) at the two band-edge regions before symbol rate sampling (and spectral overlap) at the equalizer output. An FSE can effectively compensate for more severe delay distortion and deal with amplitude distortion with less noise enhancement than a T equalizer. That was the reason for choosing T/2 fractional spaced equalizer, as well as to combat distortions caused by the ripple peaks in frequency characteristic of PLC channel. The fractionally spaced equalizer, by virtue of its sampling rate, can synthesize the best combination of the characteristics of an adaptive matched filter and T-spaced equalizer, within the constraints of its length and delay. Although the fractional spaced equalizer is insentive to a absolute timing phase, it is still sensitive to the eye opening during training. Therefore, it is necessary to locate the optimum sampling on start up. Pretraing is necessary. In this case tap and carrier recovery adaption is inhibited until after symbol timing has been obtained.

Here (in DSP implementation) the number of taps used in the fractional spaced equalizer is N = 13, selected to completely combat reflections problems in a PLC power line of 100 Km length.

The operation of the algorithm in a PLC environment was simulated on the simulation model. The following complex channel was used.

$$X = X + 0.1 \,.\, X \,.\, Z^{-10} - 0.05 \,.\, Y \,.\, Z^{-10} \qquad (6.4.3.3)$$

$$Y = Y + 0.1 \,.\, Y \,.\, Z^{-10} + 0.05 \,.\, X \,.\, Z^{-10} \qquad (6.4.3.4)$$

here Z is delay element (a baud).

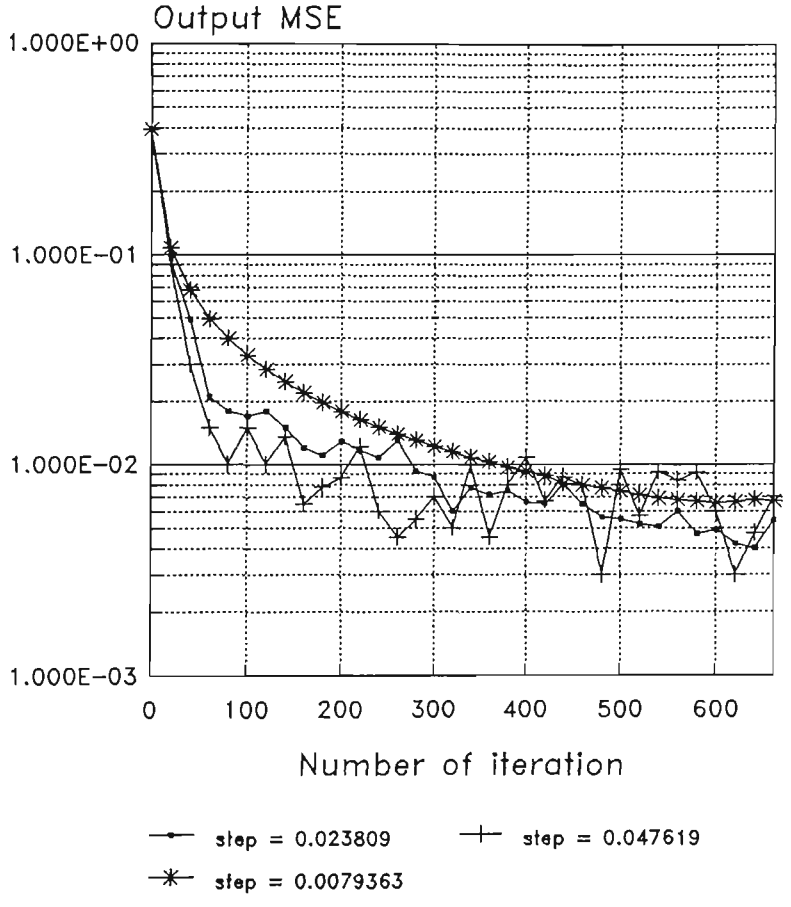

Figure 6.4.3.2 Initial convergence characteristic of the LMS algorithm with different step size for the given channel - normalised output MSE

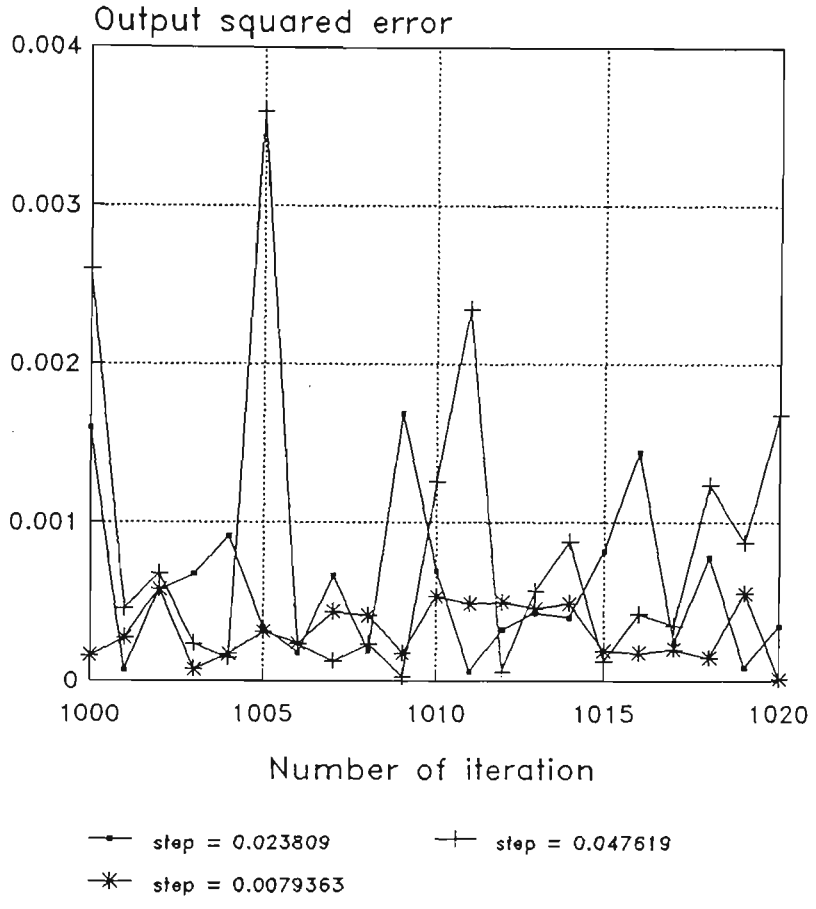

Figure 6.4.3.3 Residual squared error of the LMS algorithm with different step size-normalised output squared error

The channel represents a single echo of relatve amplitude 0.15.

Figure 6.4.3.2 shows the dependence of the convergence speed of the simulated fractionally spaced equalizer for different u coefficient values. The residual mean square error is shown in Figure 6.4.3.3. The number of taps of the simulated filter is N = 21. Also, Figure 6.4.3.4 and Figure 6.4.3.5 show the tap coefficients convergence for the real and imaginary part of C[20]. The initial value for the tap coefficient C[10] is (1,0). Symbol recovery and carrier recovery are suspended, and the sampling point is kept at its optimal value.

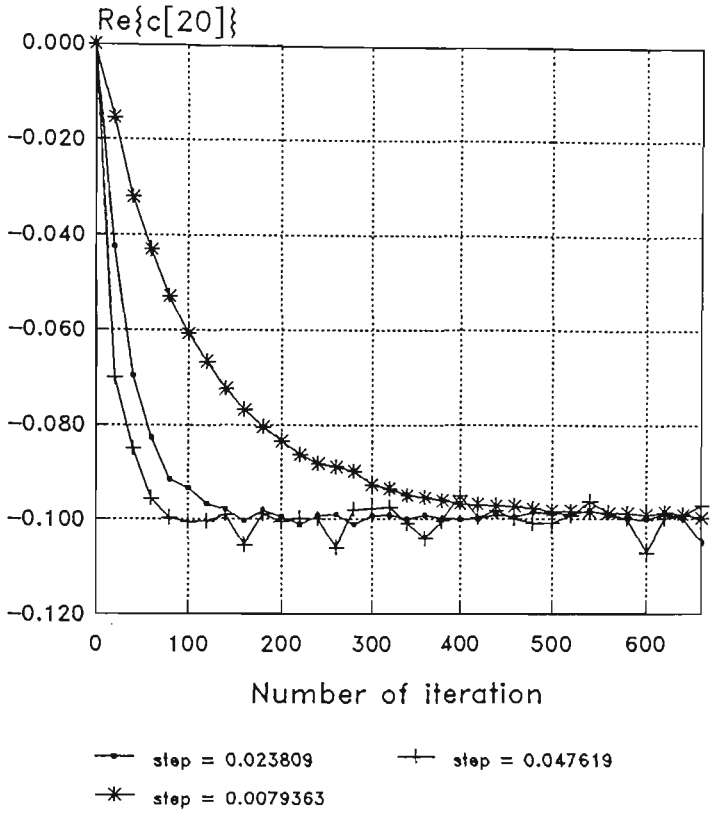

Figure 6.4.3.4 Initial convergence of the LMS algorithm with different step size for the given channel - real part of c[20]

6.4.4 Asymmetric equalizer

Imperfections in the analog parts of the modem typically lead to an asymmetric overall channel [65]. For efficient compensation of the resulting signal distortions, the use of an asymmetric baseband equalizer could be more appropriate. Specifically, the four parallel transversal filters that form identical pairs in conventional baseband equalizers are made independent by an appropriate modification of the adaptation algorithm (Figure 6.4.4.1).

To show how powerful is the algorithm two photographs (Figure 6.4.4.2 and Figure 6.4.4.3) are included: the first is a signal constellation with a raised cosine filter instead of the square root raised cosine filter at the demodulator side (this will

render the constellation points less distinct). The carrier signal for modulator is connected to the demodulator, in order to enable them to work with the same carrier frequency. There is obvious distortion of the signal constellation. Possibly due to differential gain and phase problems in the analog processing of the signals as well as the imperfect filters. The second photograph is the signal constellation with the adaptive equalizer placed immediately before the decision block of the demodulator. The signal constellation is in fact a rectangular grid, with proper shape without impairments.

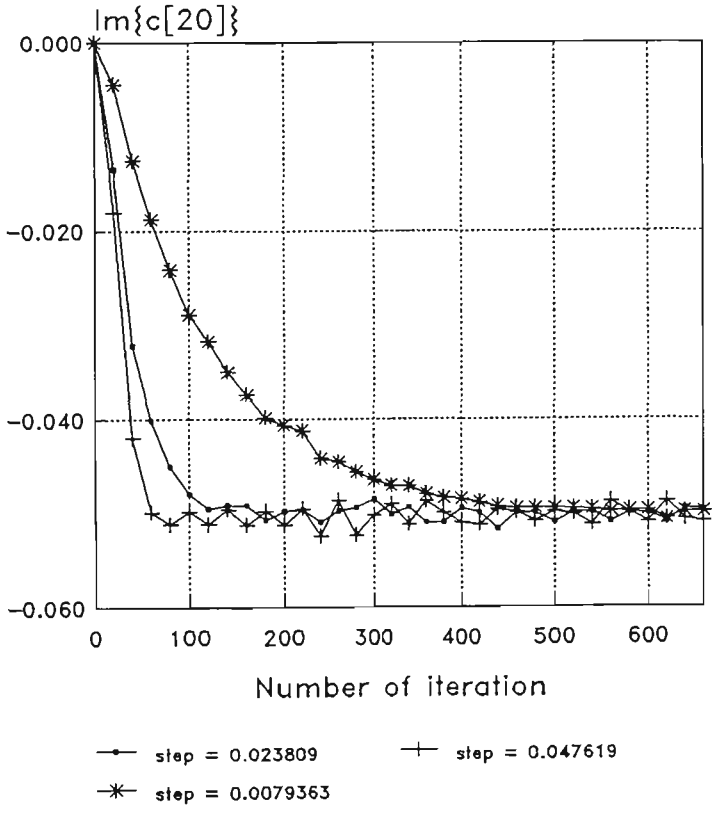

Figure 6.4.3.5 Initial convergence of the LMS algorithm with different step size for given channel - real part of c[20]

To counter the problem associated with unavoidable different DC offsets for the I and Q channels, the adaptive equalizer was modified with the addition of two additional taps, with 0.25 V permanently placed in their storage locations. The

taps are d_{ci} and d_{cq} iteratively adjusted in order to cancel out different offset voltages for I and Q axes using the same LMS algorithm.

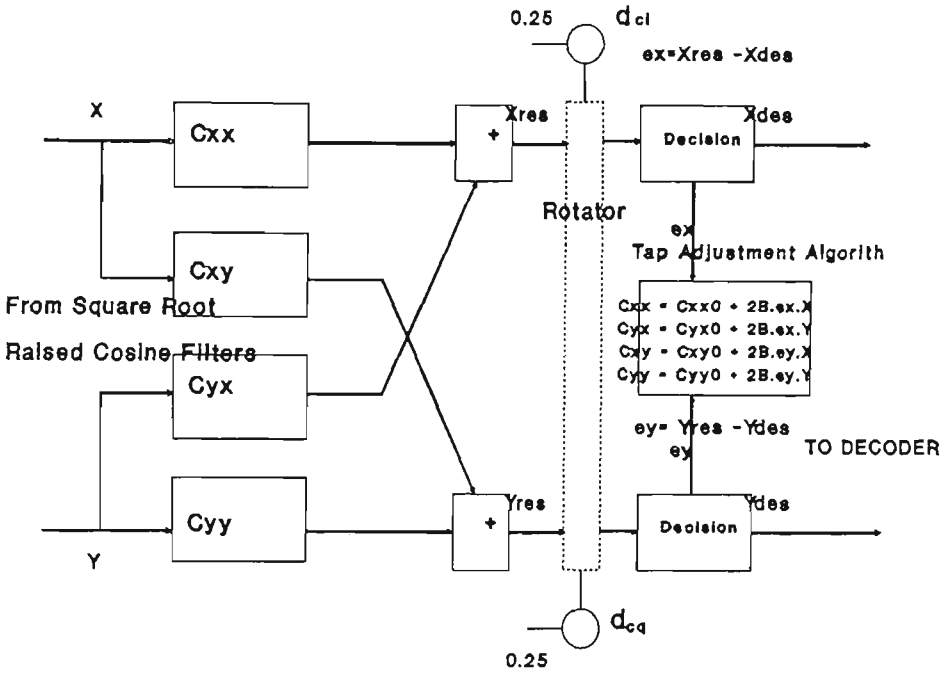

Figure 6.4.4.1 Complex equaliser

6.4.5 Another solution

For the baseband channel with severe amplitude distortion both T spaced and fractional spaced equalizer enhance channel noise, because they introduce gain to combat the amplitude losses. A decision feedback equalizer was considered to be included in the design. This equalizer consists of: a part where the detected data symbols are used as the input to a transversal filter, whose output is subtracted from the received signal. In this manner ISI samples that follow are removed by the transversal filter, whose taps are equal to ISI samples. The decision feedback

equalizer virtually operates in the same manner as an ISI canceler. It is usually preceded by a T spaced equalizer.

In the presence of significant amplitude distortion, linear equalizers are inferior to decision feedback equalizers, especially when the signal bandwidth is such that severe distortion is large at the edges of the signal spectrum. Even more, it was constituted that DFE equalizer is very efficient for removing echos with no noise enhancement (echoes cause pronounced ripples in the amplitude frequency response) [44]. Also, it was found that it is no more sensitive to quantization errors than the linear equalizer, and a training sequence was not necessary for adaptation. Accordingly, the decision feedback equalizer could be considered as a second alternative for the PLC proposed equalization technique. It is easily implemented with DSP hardware, but its analysis is complicated.

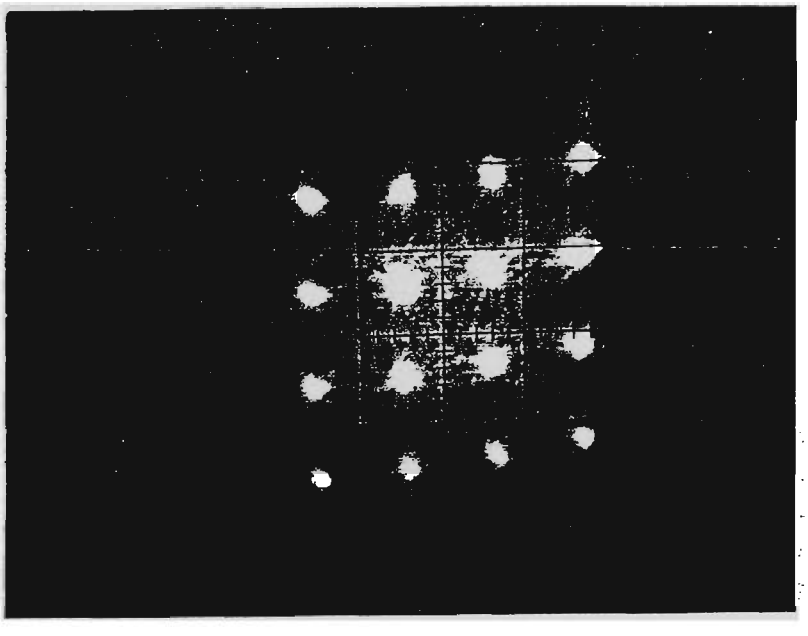

Figure 6.4.4.2 Signal constellation before equalisation

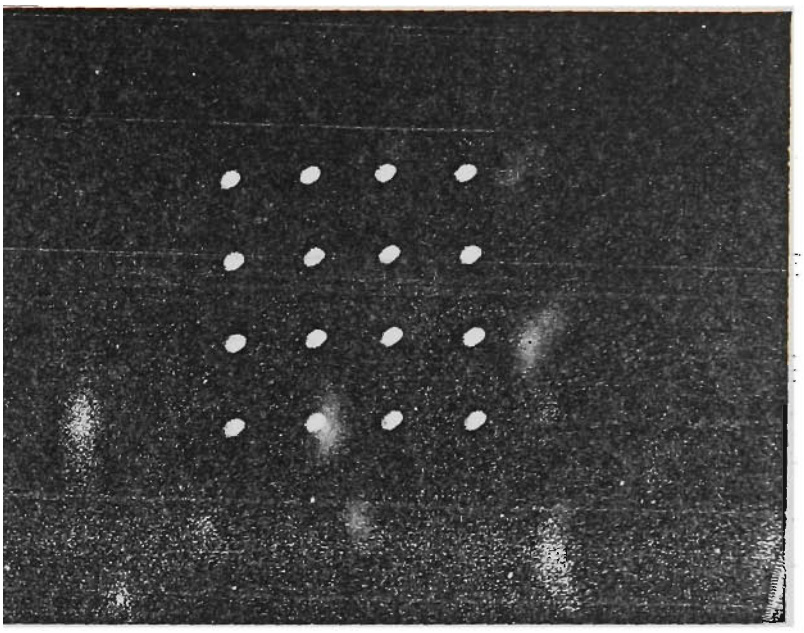

Figure 6.4.4.3 Signal constellation after equalisation

7 Conclusion

7.0 Introduction

This final chapter presents the performance and measurements carried out on the prototype in section 7.1. Section 7.2 concludes the work and suggests improvements.

7.1 Performance Measurements

For the BER measurement a special circuit configuration suitable for the labaratory was used in order to obtain accurate measurements. An additional circuit, consisting of a passive summer and a bandpass filter was placed just before the analog demodulator (see Figure 7.1.1). It was built from passive components in order to avoid saturation effects. Noise is added to the analog passband signal using the mixer which matches to the output impedance of the noise generator and the modulator. The passive filter bandlimits the noise. It consist of a simple parallel RLC circuit with Q factor = 4 and a center frequency of 75 KHz (the carrier frequency of the measured signal was 75 KHz).

The required bit energy, E_b, to noise power spectral density N_0, is a convenient quantity for system calculations and performance comparisons. Unfortunately, in practical measurements it is a more convenient to measure the average carrier to average noise (C/N) power ratio. (Bit energy meters are not commercially available). The following formula has been used:

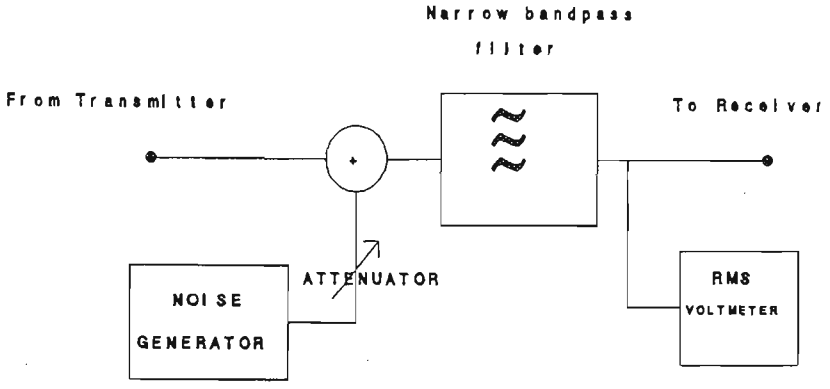

Figure 7.2.1 Setup for performance measurement

$$E_b/N_0 = (C/N).(B_f/f_b) \qquad (7.1.1)$$

The E_b/N_0 ratio equals the product of the C/N ratio as measured on rms voltmeter and the noise bandwidth to bit frequency ratio (B_f/f_b), B_f is calculated as:

$$B_f = \int_0^\infty H(f)df \qquad (7.1.2)$$

where H(f) is the narrow band filter frequency transfer function. The simulation BER measurements are shown in Figure 7.2.2. The graphs show the influence of the synchronization algorithms, frequency offset (150 Hz) and channel distortion

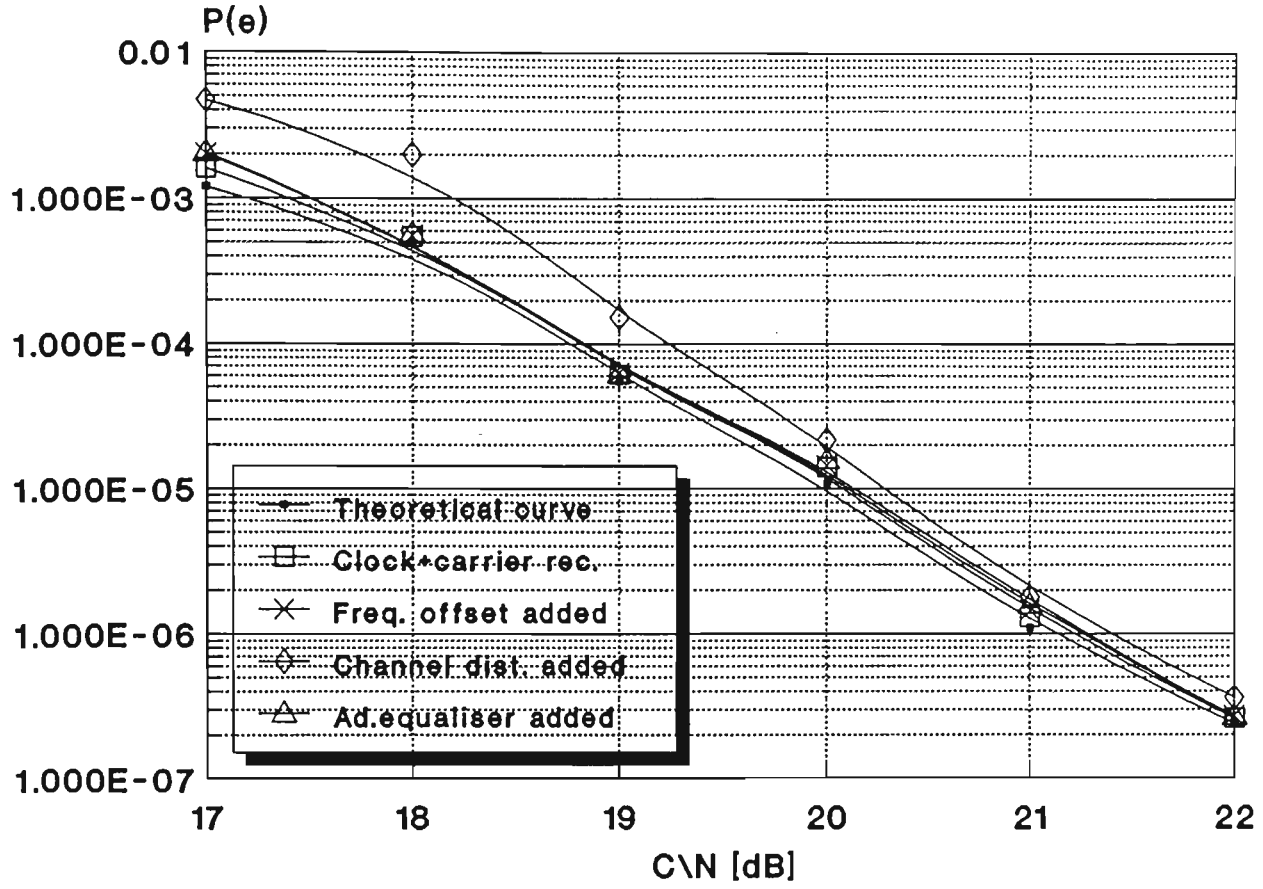

Figure 7.2.2 P(e) performance of QAM-16. The rms C/N specified in double-sided Nyquist bandwidth

given by equations 6.4.3.3 and 6.4.3.4. The differential encoder and decoder were not included in the experimental setup. The BER performance of the PLC modem as found by laboratory measurements is shown against the ideal characteristic of the QAM-16 modulation scheme in Figure 7.2.3 The graphs show an implementation loss of 1.3 dB at a BER of 10^{-5}. It could operate satisfactorily in the PLC environment. The HP 1645 data error analyzer was used in the above mentioned measurements.

7.2 Conclusion

PLC communication systems are used primarily to provide communication services for power system operation. In large power systems, it is not possible to provide all communication needs by means of PLC because of the limited spectrum availability. Furthermore, the rapid development of the electrical network has increased the

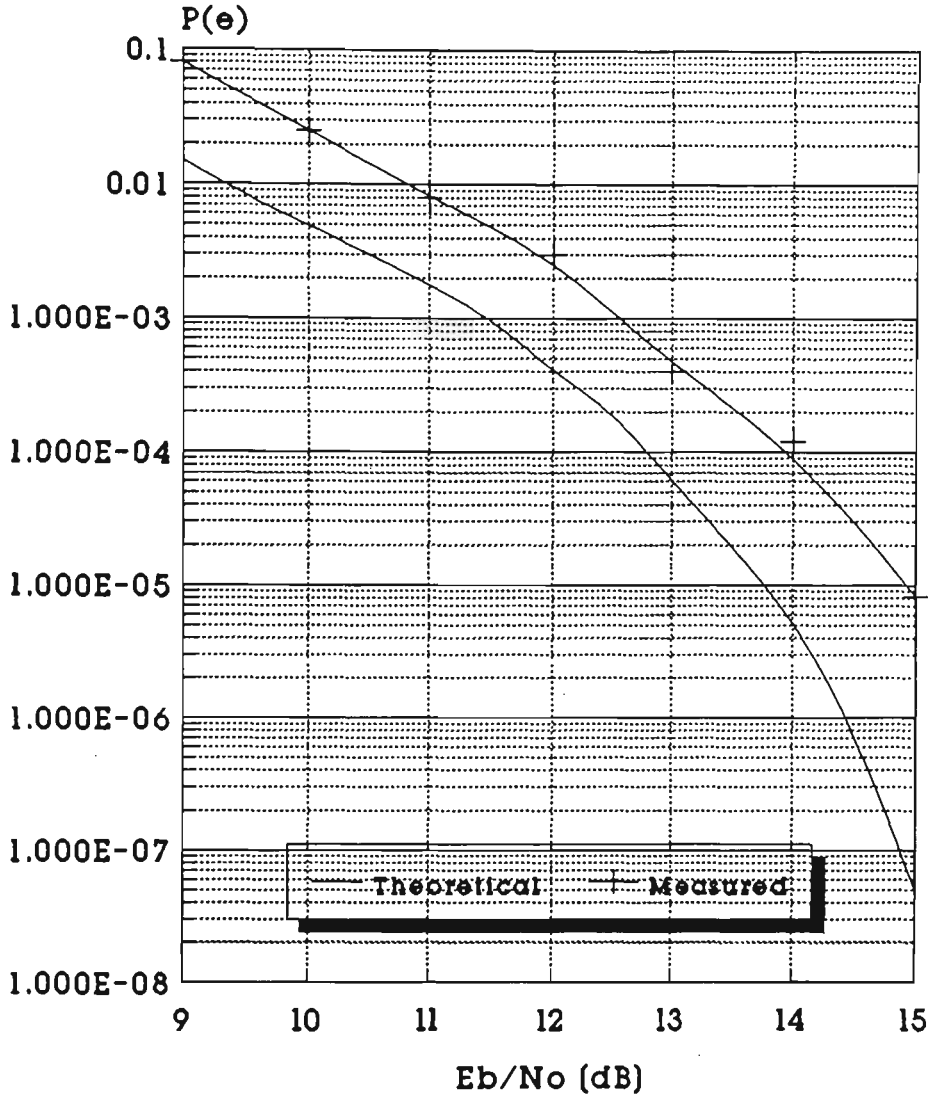

Figure 7.2.3 BER performance for QAM-16. Theoretical and measured curves

requirement for new communications, control and monitoring facilities.

Lack of sufficient spectra in which enough carrier channels could be placed is being recognized as a critical limitation to the future expansion of PLC communications system. Capacity can only be increased by more efficient use of the spectrum. This will lead to a gain in system capacity which will defer the requirement for major capital investments in alternative communications system.

With present technology, it is difficult to control mutual interference between PLC channels, because high levels of isolation between channels on the same frequency are difficult to achieve. Line traps ensure that the larger portion of the signal coupled to the line flows in the desired direction, but still a certain amount of interference to another channel operating on the same frequency can not be eliminated. This prevent the frequency reuse in adjacent line sections.

The system planner seeks to keep a minimum separation of at least one trapped line for voice transmission or two trapped lines for protection signalling, thereby taking advantages of propagation losses. Although this techniques is very wasteful in terms of spectral utilization, it is essential for reliable communication.

The main idea of the project is to employ digital modulation instead of analog modulation, because digital modulation can provide an improvement in signal to interference ratio which can eliminate any such separation requirement.

Digital PLC communication systems can operate in a much higher interference environment compared to existing SSB links. This feature can be used to reduce the guard distance between co-channel users leading to an increase in capacity for grided networks provided the bandwidth occupancy is not to large. Out of the different modulation schemes QAM-16 appears to provide the compromise between interference handling and bandwidth conservation to produce an increase in capacity. QAM-16 can handle 35 dB more noise and interference than SSB modulation, but requires three times the bandwidth when using the 32 Kbps ADPCM voice coding algorithm. Even so, a small capacity improvement of 10% is obtained as was shown in the present case. More important, however, is that it paves the way to substantial increase in capacity with more efficient voice coding.

Simulations on a 500 KV horizontal power line has shown that bandlimiting filters and reflections are the dominant cause of ISI. The reflections are by far the most predominant cause at low frequencies specially on shorter lines where the line attenuation is small.

The use of an adaptive transversal equalizer to reduce the effect of ISI has been demonstrated. It has been proved that the length of the equalizer delay line has to span the impulse response of the channel for both the signal and its first reflection. Longer lines will have weaker reflection which will produce negligible ISI, and shorter lines will have stronger reflections which will have to be countered by the equalizer. A line length a 100 km (with propagation delay of 0.86 ms) appears a suitable design benchmark. In this case the equalizer would require 8 taps for the data rate considered in the example (or 15 taps for the fractionally spaced equalizer). These requirements are well within the capabilities of modern signal processing devices.

Simulation of the proposed PLC modem, consisted the algorithms for the clock and carrier recovery and has been written to be particularly applicable to power line channels. Several graphs have been plotted, describing the influence of the noise and frequency offset on the algorithms' behavior. Several studies were made to determine the most suitable equalization technique. The assymetrical adaptive complex fractionally spaced equalizer has been selected, investigated and implemented. It provides compensation for signal distortions in the analog section of the modem.

A modem suitable for PLC communications has been developed. It uses two TMS 320C25 DSP devices to provide baseband processing in the transmitter and receiver. Analog circuits are used for up and down converting the signal to and from the RF carrier frequency. The modem achieved a 1.3 dB impementation loss at a BER of 10^{-5}.

The modem performance could be improved by using faster and more powerful DSP microprocessors, which are currently appearing in the market. With these better filters, which improve the adjacent channel performance and, more efficient equalization algorithms could be implemented. Circuits for initial (pretraining) synchronization should be included to acquire a more rapid signal acquisition. Likewise other circuits such as data scrambling and echo cancellation could be accommodated for better results.

The C25-based modem can be easily upgraded to a C5x-based design. For example, C51 is the Texas Instrument's latest high performance fixed point DSP microprocessor. With two, or nearly four times, the performance of C25, the C5X offers high system integration, reduced cost and faster operation. Alternatively there is also the possibility of improving the system performance by using the Texas Instruments TMS320C40. This microprocessor is the fastest floating point DSP chip available, operating at a speed corresponding to 40 ns instruction cycle time, with a data transfer rate of 320 Mbit/s.

Digital PLC can be used to provide services other than voice. It can be used for protection signalling, telemetering, load frequency control, supervisory control, fault location and for many other miscellaneous services. These services require different security levels and response times. They could be fulfilled by the application of different coding schemes to suit the particular case.

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Appendix 1

Measurements of cross station interference

Set of measurements were performed by the SECV in order to assess the level of cross station interference. The attenuated interfering signal is measured on several lines sharing the same substation. Only one line was energized by injecting a communication signal of certain frequency, and interference levels were measured on the other lines. The results are shown in Table 1.

Line 1 and Line 2 (for example: MBTS 1 and MBTS 2) are adjacent lines sharing the same tower. They are subject to strong near-end interference of values in the range -23.5 to -34 dB. Under rare conditions interference level of nearly -10 dB have been observed. Another type of the interference is cross station interference generally in the range from -35 dB to -85 dB. Under rare conditions interference levels of up -30 dB have been observed.

Table 1. Measurements were taken for MSS1 station operating on the frequency of 160 KHz

measured line	attenuation [dB]
MSS2	34
SMTS1	49
SMST2	62
MBTS1	46
MBTS2	63
GNTS1	45
GNTS2	52
JIND	35

Legend:

SMTS1	South Morang Terminal Station 1
SMTS2	South Morang Terminal Station 2
MBTS1	Mt. Beauty Terminal Station 1
MBTS2	Mt. Beauty Terminal Station 2
GNTS1	Glenrowan Terminal Station 1
GNTS2	Glenrowan Terminal Station 2
MSS1	Murray Switching Station 1
JIND	Jinderra Station

All of the above level were measured on the coupling coaxial cables on the separation filters groups. The instrument was a H/P wave analyser on a 100 Hz bandwidth.

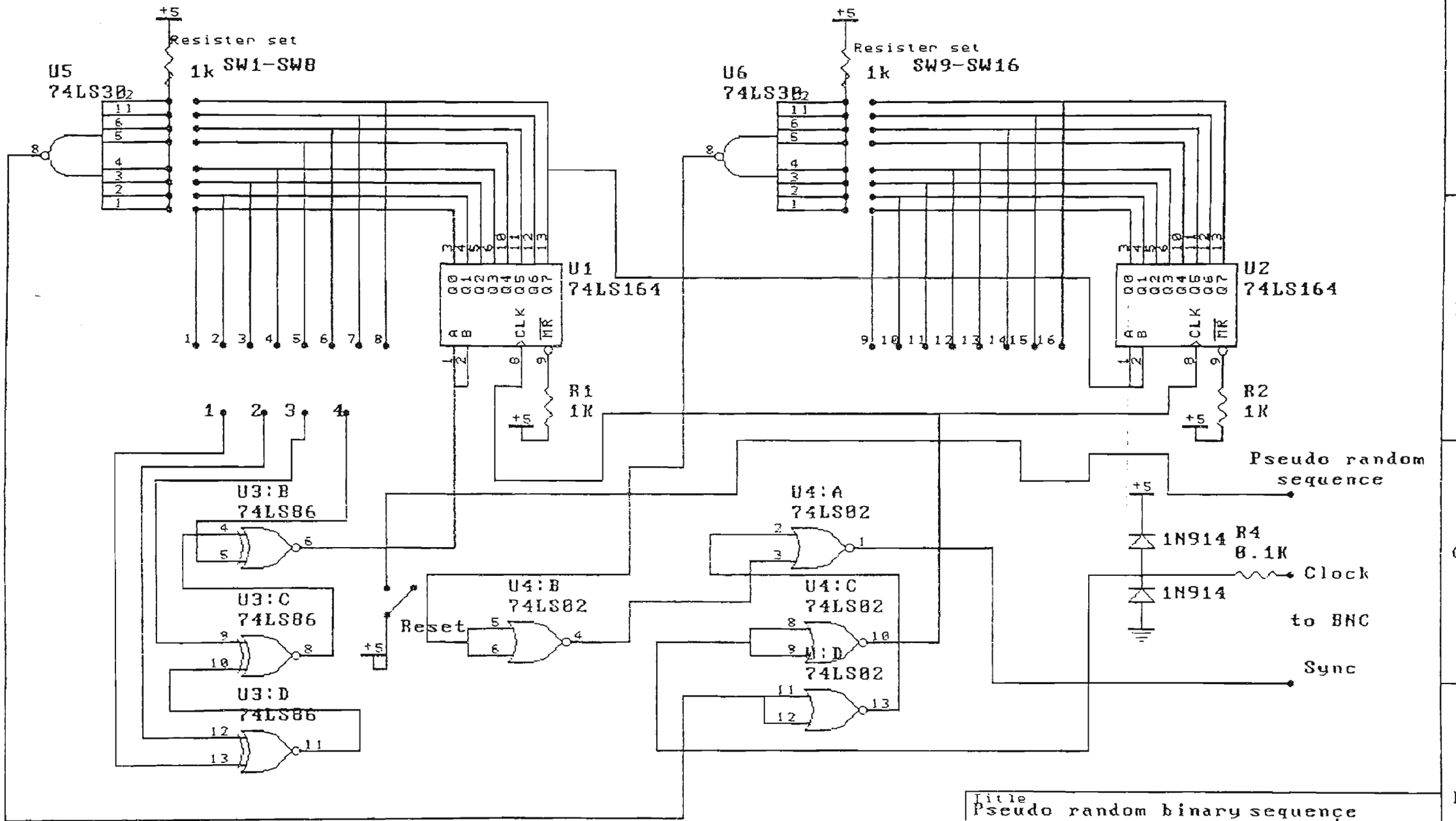
Appendix 2

Pseudo random binary sequence generator

For data input, pseudo random binary sequence generator (PRBS) was used, because it is a convinient means of approximating a random binary signal. It is easily generated by shift registers with appropriate feedback connections. the sequences are actually of deterministic nature and periodic.

The same principle of data generation was used in the software simulation program as well as in the hardware implementation [27]. Initially, the shift register is set at some initial state other than all zeros state. The clock signal successively shift the contents of the shift register stages to the right. The TMS 320C25 signal XF, external flag output (latched software programmable signal), usually use as a general purpose output pin, is employed in this case to drive the clock for the PRBS generator.

A separate card has been designed to generate pseudo random sequences for different maximal lengths. In this way the modulator is completely synchronised with the data input clock rate. Implementation involves the "modulo" addition (XOR) of the tapped shift register values, yielding either a 1 or a 0, which is then inserted as the LSB of the shift register. The register used is 16 bit long.

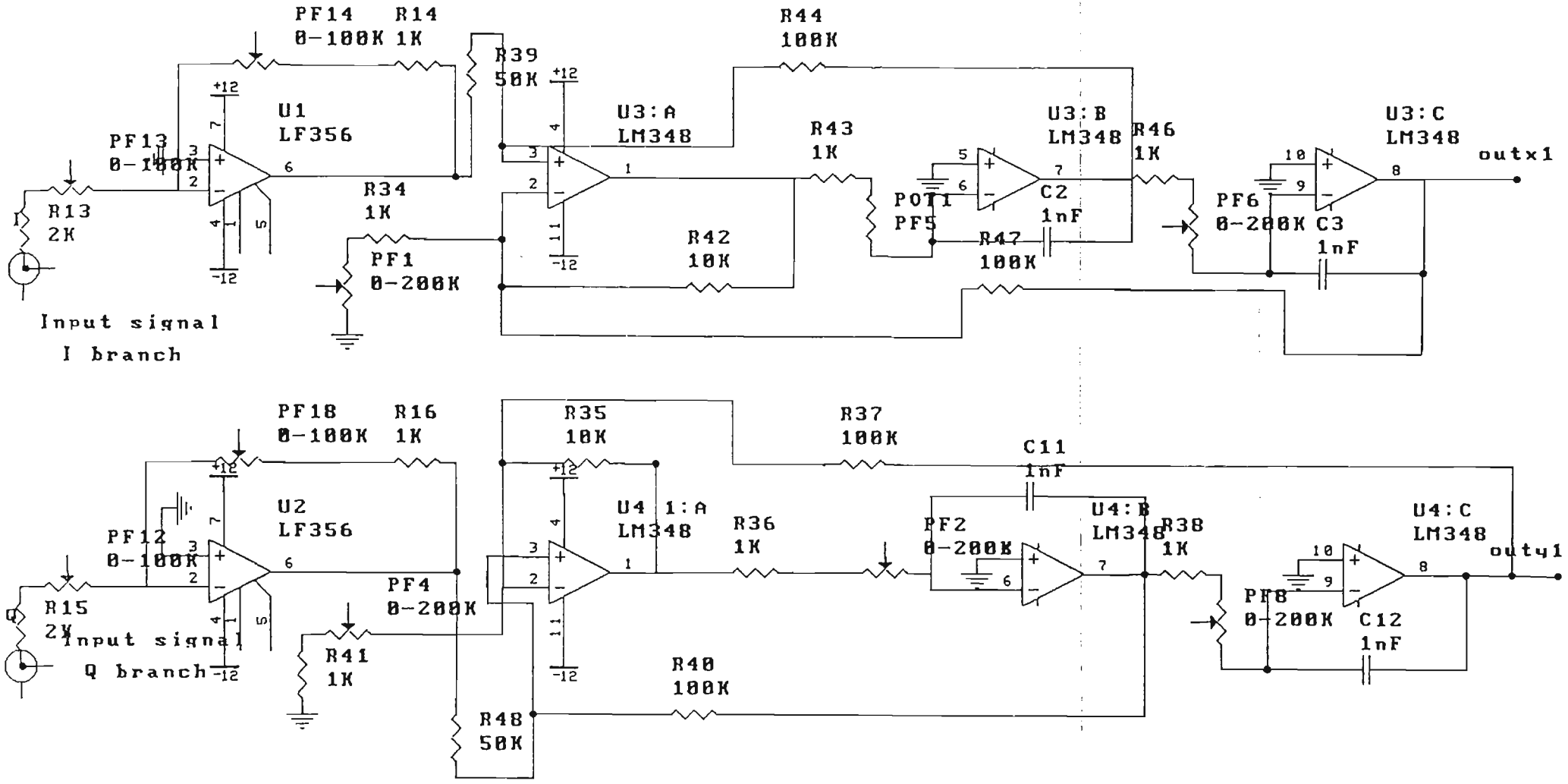


Title	Pseudo random binary sequence generator
Size A4	Number
Revision	
Date: 26-JUN 1990	Sheet 1 of 1
File: prbs/1	Drawn By: Cosic A.

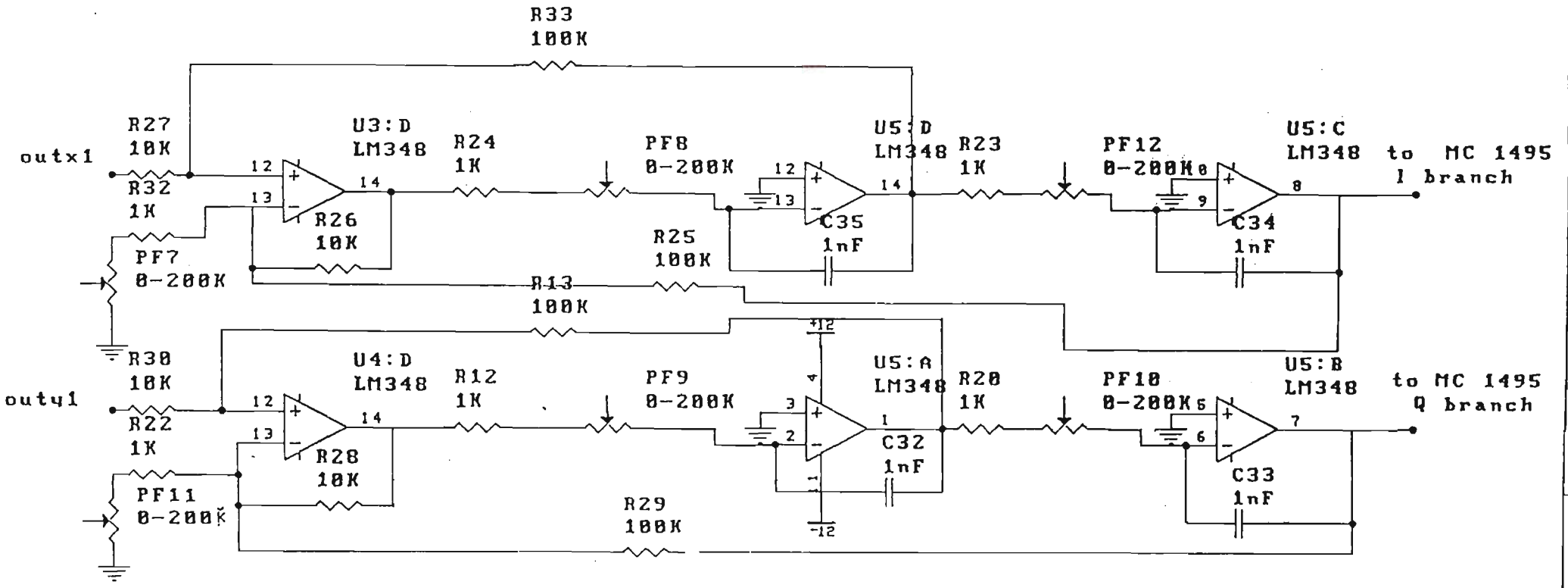
Appendix 3

Analog section of modulator

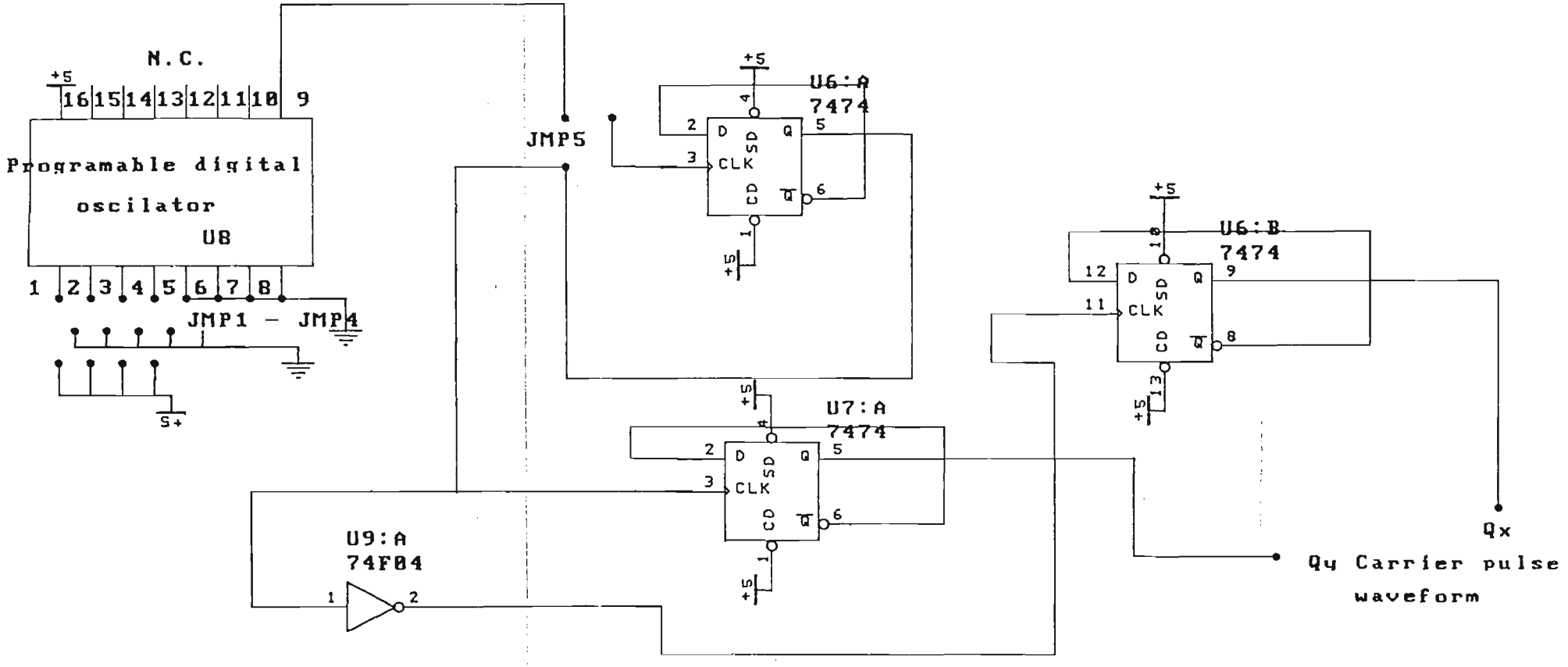
- Schematics
- Harmonic band-pass modulator filter



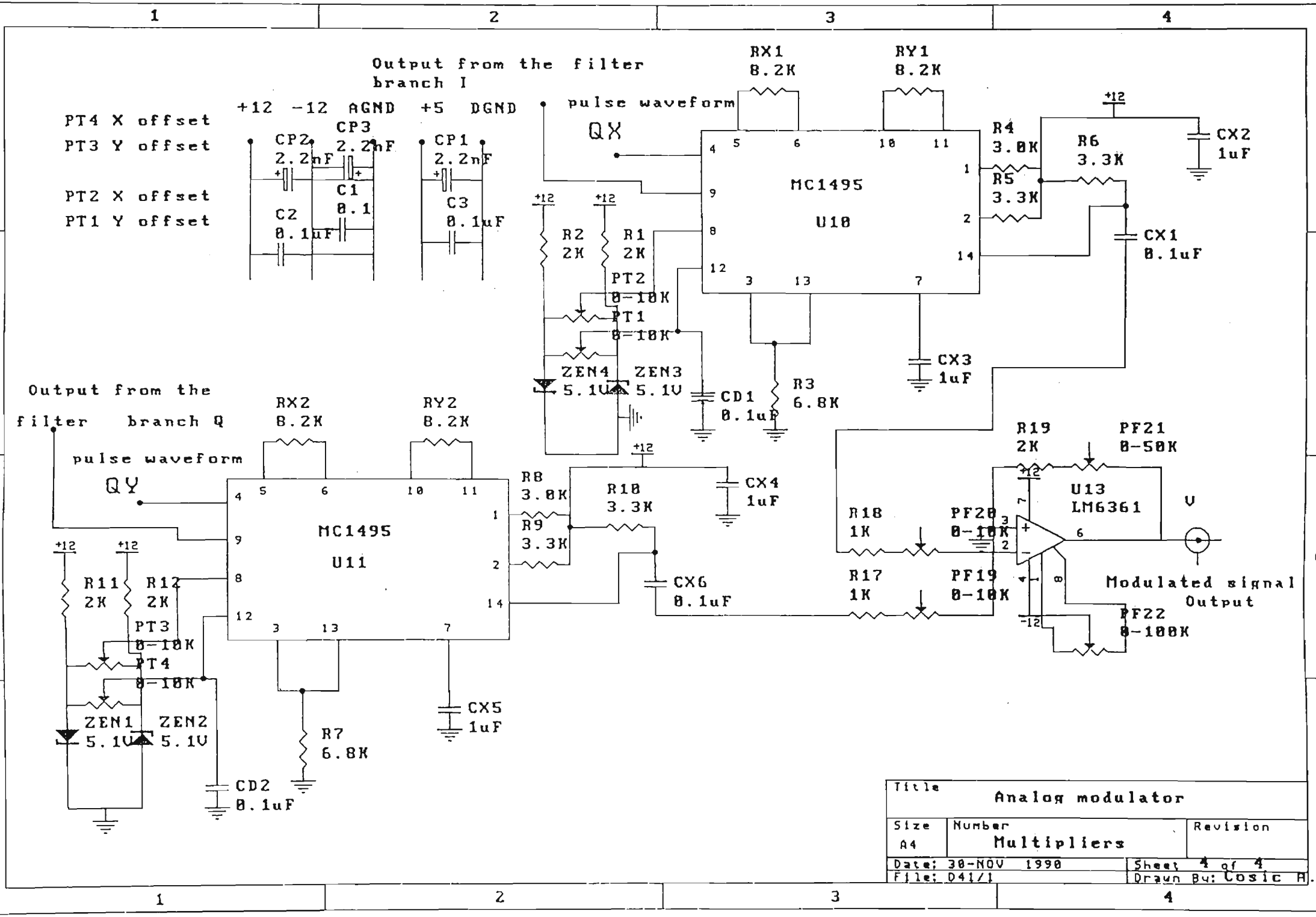
Title: Analog modulator		
Size: A4	Number: Filter/1	Revision
Date: 29-NOV 1990		Sheet 1 of 4
File: D1/1		Drawn By: Cosic A.

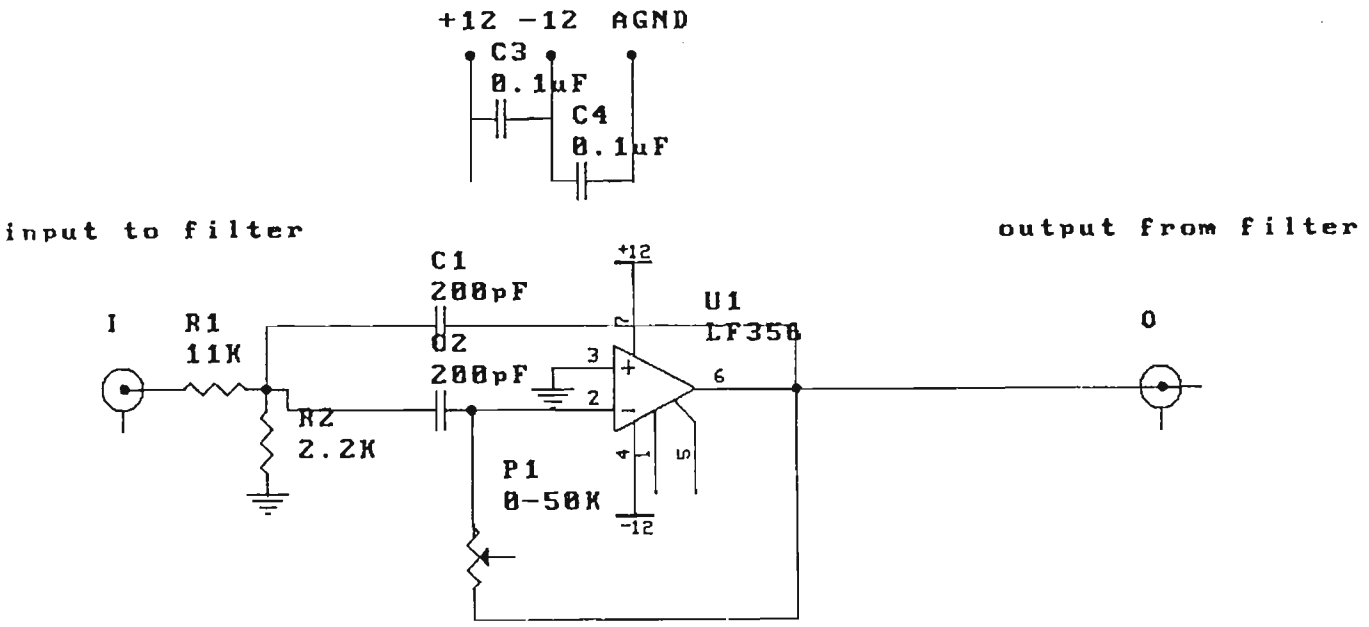


Title: Analog modulator		
Size: A4	Number: Filter/2	Revision:
Date: 30-NOV 1990		Sheet 2 of 4
File: D12/1		Drawn By: Cosic A.



Title: Analog modulator		
Size: A4	Number: Digital part	Revision:
Date: 30-NOV 1990		Sheet 3 of 4
File: D31/1		Drawn By: Cosic A.


Output from the filter branch I
+12 -12 AGND +5 DGND
PT4 X offset
PT3 Y offset
PT2 X offset
PT1 Y offset
CP2 2.2nF
CP3 2.2nF
CP1 2.2nF
C1 0.1
C2 0.1uF
C3 0.1uF
pulse waveform
QX
RX1 8.2K
RY1 8.2K
MC1495
U10
R2 2K
R1 2K
PT2 0-10K
PT1 0-10K
ZEN4 5.1V
ZEN3 5.1V
CD1 0.1uF
R3 6.8K
CX3 1uF
R4 3.0K
R5 3.3K
R6 3.3K
CX2 1uF
CX1 0.1uF
Output from the filter branch Q
pulse waveform
QY
RX2 8.2K
RY2 8.2K
MC1495
U11
R8 3.0K
R9 3.3K
R10 3.3K
CX4 1uF
CX6 0.1uF
R11 2K
R12 2K
PT3 0-10K
PT4 0-10K
ZEN1 5.1V
ZEN2 5.1V
R7 6.8K
CX5 1uF
CD2 0.1uF
R19 2K
PF21 0-50K
U13 LM6361
V
R18 1K
PF20 0-10K
R17 1K
PF19 0-10K
PF22 0-100K
Modulated signal Output
Title
Analog modulator
Size A4
Number Multipliers
Revision
Date: 30-NOV 1990
Sheet 4 of 4
File: D41/1
Drawn By: Cosic A.

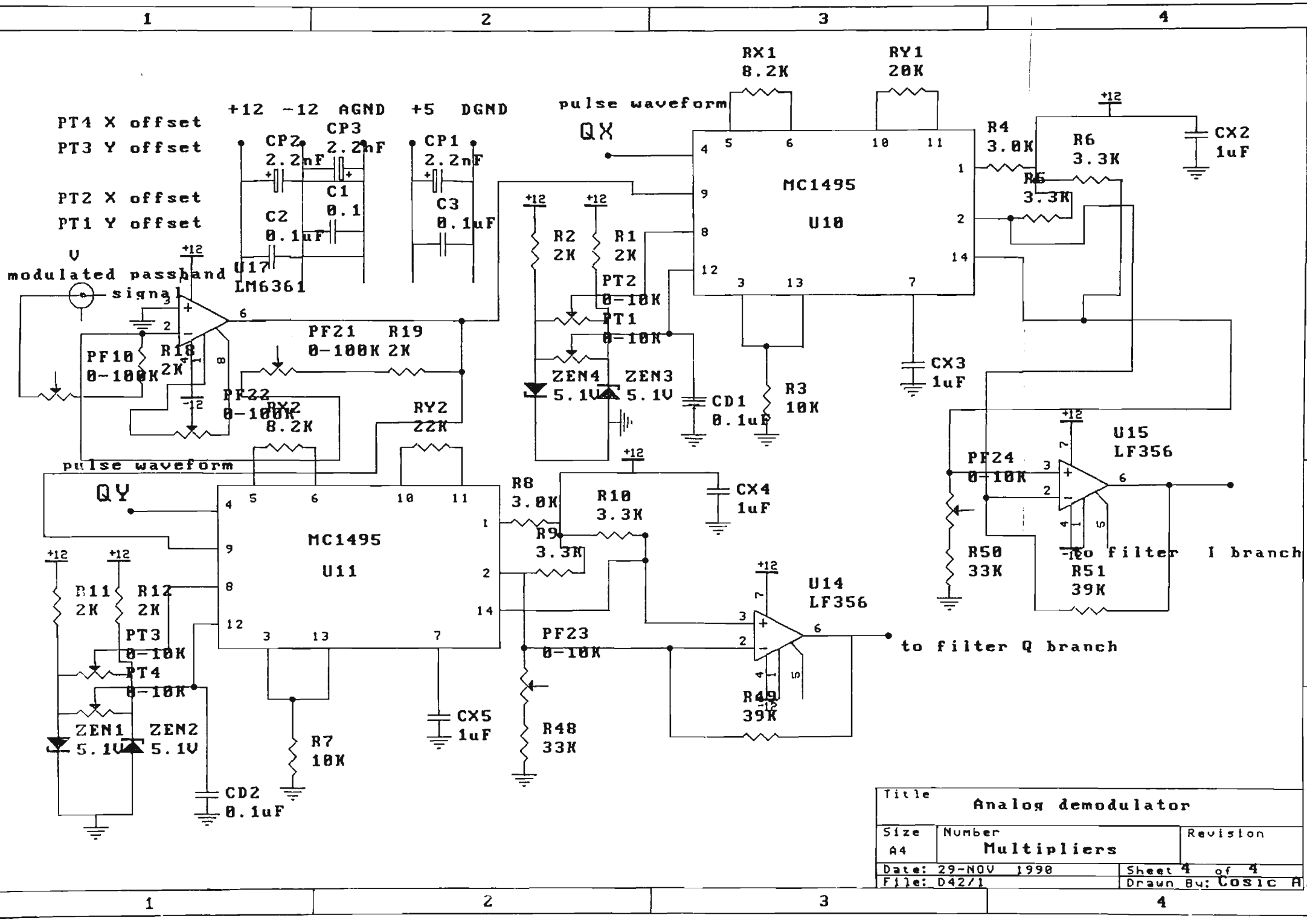


Title: Band-pass filter		
Size: A4	Number:	Revision:
Date: 30-NOV 1990		Sheet 1 of 1
File: D51/1		Drawn By: Cosic A.

Appendix 4

Analog section of demodulator

- Schematics
- the filter and clock generator circuits are the same as the modulator.


PT4 X offset
PT3 Y offset
PT2 X offset
PT1 Y offset
+12 -12 AGND +5 DGND
CP2 2.2nF
CP3 2.2nF
CP1 2.2nF
C1 0.1
C2 0.1uF
C3 0.1uF
U17 LM6361
V modulated passband signal
PF10 0-100K
R18 2K
PF21 0-100K
R19 2K
PF22 0-100K
RX2 8.2K
RY2 22K
pulse waveform
QY
MC1495 U11
R11 2K
R12 2K
PT3 0-10K
PT4 0-10K
ZEN1 5.1V
ZEN2 5.1V
CD2 0.1uF
R7 10K
CX5 1uF
R8 3.0K
R9 3.3K
R10 3.3K
CX4 1uF
PF23 0-10K
R48 33K
RX1 8.2K
RY1 20K
pulse waveform
QX
MC1495 U10
R2 2K
R1 2K
PT2 0-10K
PT1 0-10K
ZEN4 5.1V
ZEN3 5.1V
CD1 0.1uF
R3 10K
CX3 1uF
R4 3.0K
R6 3.3K
R5 3.3K
CX2 1uF
U14 LF356
R49 39K
to filter Q branch
U15 LF356
PF24 0-10K
R50 33K
R51 39K
to filter I branch
Title
Analog demodulator
Size A4
Number Multipliers
Revision
Date: 29-NOV 1990
Sheet 4 of 4
File: D42/1
Drawn By: Cosic A.

Appendix 5

Assembler demodulator program on a TMS 320C25

```
        .title  'demodulator.asm '
*****************************************************************
* Algorithm for QAM 16 decision circuit. Output is only 2.5 V max.
* Clock Recovery Circuits. Spectral line method, baseband signal is
* passed through a non - linearity such as a magnitude - square, and
* the timing tone is bandpass filtered. After that it was used peak
* locator or actually zero - cross  point of sine waveform from band
* pass filter to locate best sampling point. Carrier recovery added.
* One version for frequency generating.Square root  cosine filter
* added. Eqalisation added.Fractional space. Assymetric Equalisation
* DC cancellation added
*****************************************************************
        .global  INIT
PRD     .set    03h             ; period register
IMR     .set    04h             ; timer interrupt register
UL      .set    060h            ; random walk filter tresh.
XN      .set    00h             ; X raised cosine output
YN      .set    01h             ; Y raised cosine output
X       .set    02h             ; output from xi*xi + yi*yi
B2      .set    05h             ; feedback constant for NBF
K1      .set    06h             ; scaling constant  for NBF
SAMPLE  .set    07h             ; sample mem. location
DEL     .set    08h             ; delay NBF
DEL1    .set    09h             ; delay NBF
DEL2    .set    0Ah             ; delay NBF
MASK    .set    0Bh             ; modulo 256
RESLT   .set    0Dh             ; output from narrow bandpass filter
TEMP1   .set    0Eh             ; task address pret. subroutine
XTEM    .set    0Fh             ; temp.  for equal. input.
ONE     .set    10h             ; +5V output
ZERO    .set    11h             ; -5V output
X1      .set    12h             ; data memory location 4 output bit
X2      .set    13h             ; data memory location 3 output bit
X3      .set    14h             ; data memory location 2 output bit
X4      .set    15h             ; data memory location 1 output bit
TRSH    .set    016h            ; input tresh.
Z       .set    017h            ; output memory location
MMAL    .set    018h            ; negative low level
MVEL    .set    019h            ; negative high level
PVEL    .set    01Ah            ; negative high level
PMAL    .set    01Bh            ; negative smal level location
XDES    .set    01Ch            ; decision for I
YDES    .set    01Dh            ; decision for Q
STEP    .set    01Eh            ; update for sine look up table
SINE    .set    01Fh            ; memory location for sine
COS     .set    020h            ; memory location for cosine
COUNT   .set    021h            ; counter  value for sine look up
BETA    .set    022h            ; equaliser convergence coefficients
XRES    .set    024h            ; I magnitude at slicer
YRES    .set    025h            ; Q magnitude at slicer
DRV     .set    026h            ; carrier rec. phase error
COR     .set    027h            ; output from loop filter
CRG     .set    028h            ; crect. phase coeff.
```

```
XI        .set    029h          ; input I
YI        .set    02Ah          ; input Q
DLY1      .set    02Ch          ; loop filter delay1
DLY       .set    02Dh          ; loop filter delay
CF1       .set    02Eh          ; loop filter coefficient C2
CF2       .set    02Fh          ; loop filter coefficient C1
TEMP      .set    030h          ; temporary memory location
OFFSET    .set    031h          ; offset for sine look up table
LIMIT     .set    032h          ; angle limit
ERX       .set    033h          ; x error for equaliser
ERY       .set    034h          ; y error for equaliser
EX        .set    035h          ; unrotated error - x
EY        .set    036h          ; unrotated error - y
TRNG      .set    037h          ; number of pretraining cycles
ACNT      .set    038h          ; address to jump from pretr. subrout.
IMD       .set    039h          ; temp. mem.loc. for diff. dec.
YTEM      .set    03Ah          ; temp. for.  Q equal. input
CNT       .set    03Bh          ; pointer to tap to be updated
OND       .set    03Ch          ; binary 1
XE        .set    03Eh          ; equaliser I output
YE        .set    03Fh          ; equaliser Q output
X3I       .set    040h          ; temp. loc. for 2 out.bit
X4I       .set    041h          ; temp. loc. for 1 out.bit
X3D       .set    042h          ; diff. dec. for 2 out.bit
X4D       .set    043h          ; diff. dec. for 1 out.bit
ERRX      .set    046h          ; error x
ERRY      .set    047h          ; error y
XXK       .set    048h          ; XX memory loc.
XYK       .set    049h          ; XY memory loc.
YXK       .set    04Ah          ; YX memory loc.
YYK       .set    04Bh          ; YY memory loc.
CXX       .set    04Ch          ; CXX equaliser coef.
CYY       .set    04Dh          ; CYY equaliser coef.
CYX       .set    04Eh          ; CYX equaliser coef.
CXY       .set    04Fh          ; CXY equaliser coef.
X00       .set    050h          ; equaliser input
Y00       .set    05Dh          ; equaliser input
          .sect "init_vecs"
          B       INIT
          .space 22 * 16
          B       TINT
          .space 6 * 16
        .data
ALMT:   .word     10543
ACF1:   .word     1692
ACF2:   .word     10526
AONE:   .word     32000
AZERO:  .word     0
AB2:    .word     -31755
AK1:    .word     2007
ATRSH:  .word     01900h
ACORG:  .word     5215
ABETA:  .word     -1500
AMSK:   .word     0FFFFh
*****************************************************************
* Square root raised cosine filter - coefficients               *
*****************************************************************
```

```
COEF:   .word   -517            ;C033- 34th tap
        .word    478            ;C032
        .word   512             ;C031
        .word   327             ;C030
        .word   -75             ;C029
        .word   -352            ;C028
        .word   -130            ;C027
        .word   536             ;C026
        .word   1017            ;C025
        .word   544             ;C024
        .word   -1016           ;C023
        .word   -2663           ;C022
        .word   -2630           ;C021
        .word   463             ;C020
        .word   6404            ;C019
        .word   13087           ;C018
        .word   17513           ;C017
        .word   17513           ;C016
        .word   13087           ;C015
        .word   6404            ;C014
        .word   463             ;C013
        .word   -2630           ;C012
        .word   -2663           ;C011
        .word   -1016           ;C010
        .word   544             ;C009
        .word   1017            ;C008
        .word   536             ;C007
        .word   -130            ;C006
        .word   -352            ;C005
        .word   -75             ;C004
        .word   327             ;C003
        .word   512             ;C002
        .word   478             ;C001
        .word   -517            ;C000- 1st tap
*****************************************************************
* Sine waveform generation; look up table 256 + 64 memory location *
*****************************************************************
ASINE:  .word    00h
        .word    804
        .word    1608
        .word    2410
        .word    3212
        .word    4011
        .word    4808
        .word    5602
        .word    6393
        .word    7179
        .word    7962
        .word    8739
        .word    9512
        .word    10278
        .word    11039
        .word    11793
        .word    12539
        .word    13279
        .word    14010
        .word    14732
```

```
.word    15446
.word    16151
.word    16846
.word    17530
.word    18204
.word    18868
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.word    20159
.word    20787
.word    21403
.word    22005
.word    22594
.word    23170
.word    23731
.word    24279
.word    24811
.word    25329
.word    25832
.word    26319
.word    26790
.word    27245
.word    27683
.word    28105
.word    28510
.word    28898
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.word    29956
.word    30273
.word    30571
.word    30852
.word    31113
.word    31356
.word    31580
.word    31785
.word    31971
.word    32137
.word    32285
.word    32412
.word    32521
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.word    32767
.word    32757
.word    32728
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.word    32521
.word    32412
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.word    32137
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.word    31785
.word    31580
.word    31356
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.word    3212
.word    2410
.word    1608
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.word    0
.word    -804
.word    -1608
.word    -2410
.word    -3212
.word    -4011
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.word    -7179
.word    -7962
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.word    -10278
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.word    -20159
.word    -20787
.word    -21403
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.word    -23731
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.word    28898
.word    29268
.word    29621
.word    29956
.word    30273
.word    30571
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```
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        .word   31113
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        .word   31580
        .word   31785
        .word   31971
        .word   32137
        .word   32285
        .word   32412
        .word   32521
        .word   32609
        .word   32678
        .word   32728
        .word   32757
        .word   32767
AM1:    .word   07FFFh
        .text
INIT    ROVM
        DINT
        LDPK    0
        ZAC                     ; zero the accumulator
        LARP    7
        LARK    AR7,060h        ; point block B2
        RPTK    31
        SACL    *+              ; clearing in chip data memory
        LRLK    AR7,200h        ; point block B0
        RPTK    255
        SACL    *+
        LRLK    AR7,0300h       ; point block B1
        RPTK    255
        SACL    *+
        LARP    0
        LRLK    0,0200h         ; pointer to data memory
        CNFD
        RPTK    33
        BLKP    COEF,*+         ; block move from program memory to da
        CNFP                    ; memory 34 coefficients
        LACK    08h             ; enable timer interrupt
        OR      IMR
        SACL    IMR
        LALK    319             ; load the period register
        SACL    PRD             ; 319 + 1 instruction cycles
        LDPK    6               ; = bit rate
        LALK    AONE
        TBLR    ONE
        LALK    AZERO
        TBLR    ZERO
        LALK    AB2
        TBLR    B2
        LALK    AK1
        TBLR    K1
        LRLK    AR3,32564
        LRLK    AR4,-3564
        LALK    ATRSH
        TBLR    TRSH
        LALK    ACF1
        TBLR    CF1
```

```
        LALK    034Fh
        SACL    CNT
        LALK    ASINE
        SACL    OFFSET
        LALK    ACF2
        TBLR    CF2
        LALK    ACORG
        TBLR    CRG
        LALK    AM1
        TBLR    MASK
        LALK    ALMT
        TBLR    LIMIT
        LALK    AMSK
        TBLR    MSK
        LALK    800h
        SACL    TRNG
        LALK    VNT
        SACL    ACNT
        LALK    ABETA
        TBLR    BETA
        LACK    1
        SACL    OND
        LALK    2000h           ; load fixed value in equaliser taps
        SACL    XXK             ; used to combat DC offset between
        SACL    YYK             ; two channels
        LALK    0500h
        SACL    YXK
        SACL    XYK
        LAC     TRSH,15
        SACH    PMAL            ; calculating ideal signal constellat
        NEG                     ; coordinates
        SACH    MMAL
        NEG
        ADDH    TRSH
        SACH    PVEL
        NEG
        SACH    MVEL
        SACH    XTEM
        SACH    YTEM
        LDPK    0
        LARP    7
        LRLK    7,0350h
        RPTK    25
        SACH    *+
        LALK    07D00h
        LRLK    7,037Dh
        SACL    *
        LRLK    7,0397h
        SACL    *
        SSXM
        SPM     1
        LDPK    6
        SOVM
        EINT                    ; enable interrupt
*****************************************************************
* Task controller: this main task controls the order of execution   *
* and scheduling of tasks. This routine selects the task appropriate*
```

```
* for the current sample cycle, calls the task as the soubroutine,  *
* and branches back  when sheduled task has completed execution.    *
* When an interupt service routine occurs, the interupt  routine    *
* is executed. After the interupt service routine has completed, the*
* processor begins execution with the instruction following the idle*
* instruction.                                                      *
*********************************************************************
*  Training for the timing recovery                                 *
*********************************************************************
WAIT1     IDLE                    ; wait for timer interupt
          LDPK    6
          IN      XI,0
          RPTK    7
          NOP
          LAC     SAMPLE          ; fetch sample count value
          SUBK    1               ; decrement sample count value
          BGEZ    OVRSAM1         ; test for end of the baud interval
          LAC     TRNG            ; decrement pretraing number
          SUBK    1
          BGEZ    CN1T            ; test for end of pretraining
          ZALS    ACNT
          BACC
CN1T      SACL    TRNG
          LACK    3               ; init count for new baud interval
OVRSAM1   RPTK    6
          NOP
          SACL    SAMPLE
          DMOV    DEL1            ; delay 1 for narrow band pass filter
          DMOV    DEL             ; delay for narrow bad pass filter
          LRLK    1,03DEh         ; pointer to newest sdample
          LARP    1
          SSXM
          SPM     1
          MPYK    0
          IN      XI,1            ; input XI, trigger 1
          ZALS    XI
          XORK    08000h
          SACL    XI              ; conversion in two's complement
          LAC     XI,15           ; get and scale input
          SACH    *               ; square root raised cosine filter
          LRLK    1,03FFh         ; pointer to data memory
          ZAC
          RPTK    33
          MACD    0FF00h,*-       ; 34 tap FIR calculation
          IN      YI,1            ; input YI, trigger 1
          APAC
          SACH      XN              ; save input
          ZALS    YI
          XORK    08000h          ; comnversion in two's complement
          SACL    YI
          LRLK    1,03BAh         ; pointer to newest sample
          LAC     YI,15
          SACH    *
          LRLK    1,03DBh         ; pointer to data memory
          MPYK    0
          ZAC
          RPTK    33
```

```
          MACD    0FF00h,*-       ; 34 tap FIR calculation
          APAC
          SACH    YN
          SPM     0
          SQRA    XN              ; squaring of X input.
          ZAC
          SQRA    YN              ; squaring of Y input
          APAC
          SACH    X,1             ; X*X + Y*Y
          LT      X               ; input timing signal
          MPY     K1              ; multiply scaling factor
          LTP     DEL2            ; second delay constant
          MPY     B2              ; feedbackconstant
          APAC
          SACH    DEL,1           ; save first delay
          SUB     DEL2,15         ; calculate result
          SACH    RESLT,4         ; save result
          RSXM
          LAC     SAMPLE          ; fetch sample couint value
          ADLK    TSKSEQ1         ; add task table base address
          TBLR    TEMP1           ; read subroutine task address
          LAC     TEMP1           ; load accumulator for task call
          CALA                    ; execute apprropriate task
*****************************************************************
* This main task routine controls the order of execution and    *
* scheduling of tasks. When an interrupt occurs, the            *
* interrupt service routine is executed to process the input    *
* and output data samples. After the interrupt service routine  *
* has completed, the processor begins execution with the instruc-*
* tion following the idle instruction. This routine selects the *
* task appropriate for the current sample cycle, calls the task *
* as a subroutine, and branches back to the idle  to wait for   *
* the next sample interrupt when the scheduled task has         *
* completed execution                                           *
*****************************************************************
          B       WAIT1
TSKSEQ1   .set    $               ; task controller
          .word   SC41
          .word   SC31
          .word   SC21
          .word   SC11
SC11       RET
SC21       RET
SC31       SSXM
           LAC    RESLT           ; random walk filter for pretraining
           LDPK   0               ; period
           BGEZ   P1i
           LAC    UL
           ADDK   1
           SACL   UL
           B      P2i
P1i        LAC    UL
           SUBK   1
           SACL   UL
           NOP
           NOP
P2i        SUBK   1
```

```
          DINT
          BGEZ    P3i
          ADDK    2
          BGZ     P4i
          ZAC
          SACL    UL
          LALK    318             ; decrease baud period for 1
          SACL    PRD
          B       P5i
P3i       ZAC                     ; increase baud period for 1
          SACL    UL
          LALK    320
          SACL    PRD
          NOP
          NOP
          B        P5i
P4i       LALK     319            ; baud period is same
          SACL     PRD
          RPTK     2
          NOP
P5i       EINT
          LDPK     6
          RSXM
          RET
SC41      RET
*****************************************************************
*  Main Programme                                               *
*****************************************************************
WAIT      IDLE                    ; wait for timer interupt
          IN       XI,0           ; input XI, trigger 0
          RPTK     3
          NOP
          SOVM
          LAC      SAMPLE         ; fetch sample count value
          SUBK     1              ; decrement the sample count
          BGEZ     OVRSAM         ; test for the end of baud interval
VNT       LACK     3              ; init count for new baud interval
OVRSAM    SACL     SAMPLE
          OUT      Z,0            ; output bit
          DMOV     DEL1           ; delay1
          DMOV     DEL            ; delay
          LRLK     1,03DEh        ; pointer to newest sample
          LARP     1
          SSXM
          SPM      1
          MPYK     0
          IN       XI,1           ; input XI, trigger 1
          ZALS     XI
          XORK     08000h
          SACL     XI             ; conversion in two's complement
*****************************************************************
*  Square root raised cosine filter - X                         *
*  Sampling frequency: 34400 Hz                                 *
*  Cut off: 4300                                                *
*  Roll off: 39.5%                                              *
*  Number of taps: 34                                           *
*****************************************************************
```

```
        LAC     XI,15           ; get and scale I input
        SACH    *
        LRLK    1,03FFh         ; point to the oldest sample
        ZAC
        RPTK    33
        MACD    0FF00h,*-       ; 34 tap FIR filter
        IN      YI,1            ; input YI, trigger 1
        APAC
        SACH      XN              ; save output
        ZALS    YI
        XORK    08000h
        SACL    YI
*****************************************************************
*  Square root raised cosine filter - X                         *
*  Sampling frequency: 34400 Hz                                 *
*  Cut off: 4300                                                *
*  Roll off: 39.5%                                              *
*  Number of taps: 34                                           *
*****************************************************************
        LRLK    1,03BAh         ; point to the newest sample
        LAC     YI,15           ; get and scale Q input
        SACH    *               ; point to the oldest sample
        LRLK    1,03DBh
        MPYK    0
        ZAC
        RPTK    33              ; 34 tap FIR filter
        MACD    0FF00h,*-
        APAC
        SACH    YN              ; save result
        SPM     0
        SQRA    XN              ; squaring of I input.
        ZAC
        SQRA    YN              ; squaring of Q input
        APAC
        SACH    X,1             ; save result
*****************************************************************
*Narrow bandpass filter( Q = 50, center frequency fc = 8.6 KHz)    *
*****************************************************************
        LT      X               ; input signal
        MPY     K1              ; scaling constant
        LTP     DEL2            ; second delay element
        MPY     B2              ; feedback constant
        APAC
        SACH    DEL,1           ; save first delay
        SUB     DEL2,15
        SACH    RESLT,4         ; save result
        LAC     SAMPLE          ; fetch sample count value
        ADLK    TSKSEQ          ; add task table base address
        TBLR    TEMP1           ; read subroutine task address
        LAC     TEMP1           ; load accumulator for task call
        CALA                    ; execute appropriate task
        B  WAIT
TSKSEQ  .set    $
        .word   SC4
        .word   SC3
        .word   SC2
        .word   SC1
```

```
SC1       LAC     X4              ; load the first bit
          SACL    Z               ; to the output
*****************************************************************
* Sine and cosine generation using a lookup table               *
*****************************************************************
          LAC     COUNT           ; load accumulator
          ADD     STEP            ; update count
          AND     MASK            ; modulo 256
          SACL    COUNT
          LAC     COUNT,9         ; isolate integer portion
          SACH    TEMP
          LAC     TEMP
          ADD     OFFSET
          TBLR    SINE            ; sine value from the table
          ADDK    64
          TBLR    COS             ; cosine value from the table
*****************************************************************
*  Error calculation                                            *
*****************************************************************
          ZALH    YRES
          SUBH    YDES
          SACH    ERRY            ; erry = yres - ydes
          ZALH    XRES
          SUBH    XDES
          SACH    ERRX            ; errx = xres - xdes
*****************************************************************
* Multiplying with sine and cosine to remodulate error          *
*****************************************************************
          LT      COS
          MPY     ERRX
          LTP     SINE
          MPY     ERRY
          LTS     COS
          SACH    EX,1            ; ex = cos*errx - sin*erry
          MPY     ERRY
          LTP     SINE
          MPY     ERRX
          APAC
          SACH    EY,1            ; ey = sin*erry + cos*erry
*****************************************************************
* Error calculation                                             *
*****************************************************************
          SPM     1
          LT      EX
          MPY     BETA
          PAC
          ADD     OND,15
          SACH    ERX             ; erx = beta*ex
          OUT     XRES,3
          LT      EY
          MPY     BETA
          PAC
          ADD     OND,15
          SACH    ERY             ; ery = beta*ey
*****************************************************************
* Coeficient updating for the complex equaliser                 *
*  cr = cr - delta*[xi*erx + yi*ery]                            *
```

```
*  ci = ci - delta*[xi*ery - yi*erx]                                    *
*************************************************************************
         LARP    1              ; pointer to a tap to be updated
         LAC     CNT
         ADDK    1
         SACL    CNT
         SUBK    035Dh
         BNZ     JPL
         LALK    0350h
         SACL    CNT
JPL      LAR     1,CNT
*************************************************
*                                               *
*              Memory   structures              *
*                X        0350h                 *
*                Y        035Dh                 *
*                CXI      036Ah                 *
*                CXR      0377h                 *
*                CYI      0384h                 *
*                CYR      0391h                 *
*                                               *
*************************************************
*                                               *
* Updating Coefficients of the adaptive equaliser *
*                                               *
*    cxr = cxr0 - 2.B.erx.X                     *
*************************************************
         LT      ERX
         LDPK    0
         MPY     *
         ADRK    39
         ZALR    *
         APAC
         SACH    *
*     cyi = cyi0 - 2.B.erx.Y
         SBRK    26             ; T still has ERX
         MPY     *
         ADRK    39
         ZALR    *
         APAC
         SACH    *
*      cxi  = cxi - 2.B.ery.X
         LDPK    6
         LT      ERY
         LDPK    0
         SBRK    52
         MPY     *
         ADRK    26
         ZALR    *
         APAC
         SACH    *
*       cyr  = cyr0  - 2.B.ery.y
         SBRK    13             ; T still has ERY
         MPY     *
         ADRK    52
         ZALR    *
         APAC
```

```
        SACH    *
        LRLK    1,035Bh
        RPTK    11
        DMOV    *-              ; shifting X value of equaliser
        ADRK    25
        RPTK    11              ; shifting Y value of equaliser
        DMOV    *-
        LDPK    6
        ZALR    CXX
        LT      ERX
        MPY     XXK
        MPYA    YXK
        SACH    CXX
        ZALR    CYX
        LTA     ERY
        MPY     YYK
        SACH    CYX
        ZALR    CYY
        MPYA    XYK
        SACH    CYY
        ZALR    CXY
        APAC
        SACH    CXY
        SPM     0
        RSXM
        RET
SC2     LAC     X3              ; load 2 bit
        SACL    Z
        SSXM
        LDPK    6
        ZALH    XTEM             ; new equaliser I input
        SACH    X00
        ZALH    YTEM             ; new equaliser Q input
        SACH    Y00
*****************************************************************
* Two dimensinal  MSE adaptive equaliser                        *
*****************************************************************
        LDPK    0
        LRLK    1,035Bh         ; pointer to data memory location
        RPTK    11
        DMOV    *-              ; shifting X value of equaliser
        ADRK    25
        RPTK    11              ; shifting Y value of equaliser
        DMOV    *-
        ZALH    XN              ; new equaliser I input
        SACH    X00
        ZALH    YN              ; new equaliser Q input
        SACH    Y00
        LDPK    0
*****************************************************************
*   Complex adaptive filters I - branch:                        *
*       XE = X*Cxx + Y*Cyx                                      *
*       13 taps                                                 *
*****************************************************************
        LRLK    1,0350h         ; pointers to the X,Y
        LRLK    7,0384h         ; pointers to CXr and CXi
        LRLK    5,035Dh
```

```
LRLK    6,0377h
LARP    1
LDPK    0
LT      *+,6            ; 1st tap
MPY     *+,5
LTP     *+,7
MPY     *+,1
LTA     *+,6            ; 2nd tap
MPY     *+,5
LTA     *+,7
MPY     *+,1
LTA     *+,6            ; 3rd tap
MPY     *+,5
LTA     *+,7
MPY     *+,1
LTA     *+,6            ; 4th tap
MPY     *+,5
LTA     *+,7
MPY     *+,1
LTA     *+,6            ; 5th tap
MPY     *+,5
LTA     *+,7
MPY     *+,1
LTA     *+,6           ; 6th tap
MPY     *+,5
LTA     *+,7
MPY     *+,1
LTA     *+,6           ; 7th tap
MPY     *+,5
LTA     *+,7
MPY     *+,1
LTA     *+,6           ; 8th tap
MPY     *+,5
LTA     *+,7
MPY     *+,1
LTA     *+,6           ; 9th tap
MPY     *+,5
LTA     *+,7
MPY     *+,1
LTA     *+,6           ; 10th tap
MPY     *+,5
LTA     *+,7
MPY     *+,1
LTA     *+,6           ; 11th tap
MPY     *+,5
LTA     *+,7
MPY     *+,1
LTA     *+,6           ; 12h tap
MPY     *+,5
LTA     *+,7
MPY     *+,1
LTA     *+,6           ; 13th tap
MPY     *+,5
LTA     *+,7
MPY     *
LDPK    6
LTA     XXK
```

```
        MPY     CXX
        LTA     YXK
        MPY     CYX
        APAC
        SACH    XE
        ZALH    XE
        ADDH    XE              ; save result
        SACH    XE
        LDPK    0
        LRLK    AR7,037Eh
        LARP    7
        OUT     *,1
        LDPK    6
        RSXM
        RET
SC3     LAC     X2              ; load 3 bit
        SACL    Z
        NOP
        NOP
        ZALH    RESLT
*****************************************************************
* RWF - random walk  filter. Up/down counter reacts to the lag/lead *
* pulses by counting up or down for each input pulse generated by   *
* zero crossing detector. When either an upper or lower pulse tres- *
* hold is  reached  an appropriate phase step command results, and  *
* counter is reset. Treshold is 10 pulse                            *
*****************************************************************
        LDPK    0
        SSXM
        BGZ     P1              ; test zero crossing algorithm
        LAC     UL
        ADDK    1
        SACL    UL
        B       P2
P1      LAC     UL
        SUBK    1
        SACL    UL
        NOP
        NOP
P2      SUBK    10              ; test whether the treshold is greater
        DINT
        BGEZ    P3
        ADDK    20              ; test whether the treshold is less th
        BGZ        P4
        ZAC
        SACL      UL
        LALK      318             ; decrease baud interval for 1 inst.
        SACL      PRD
        B         P5
P3      ZAC
        SACL      UL
        LALK      320             ; increase baud interval for 1 inst.
        SACL    PRD
        NOP
        NOP
        B          P5
P4      LALK    319             ; neither upper or lower treshold is r
```

```
          SACL     PRD
          RPTK     2
          NOP
P5        EINT
          LDPK     6
          LRLK       1,0350h          ; set pointers
          LRLK       7,036Ah
          LRLK     5,035Dh
          LRLK       6,0391h
          LDPK       0
          LARP     1          LDPK     0
*****************************************************************
*   Complex adaptive filters Q - branch:                        *
*        YE = Y*Cyy + X*Cxy                                     *
*        13 taps                                                *
*****************************************************************
          LT           *+,7             ; 1st tap
          MPY        *+,5
          LTP        *+,6
          MPY        *+,1
          LTA        *+,7             ; 2nd tap
          MPY      *+,5
          LTA      *+,6
          MPY      *+,1
          LTA      *+,7             ; 3td tap
          MPY      *+,5
          LTA      *+,6
          MPY      *+,1
          LTA      *+,7             ; 4th tap
          MPY      *+,5
          LTA      *+,6
          MPY      *+,1
          LTA      *+,7             ; 5th tap
          MPY      *+,5
          LTA      *+,6
          MPY      *+,1
          LTA      *+,7             ; 6th tap
          MPY      *+,5
          LTA      *+,6
          MPY      *+,1
          LTA      *+,7             ; 7th tap
          MPY      *+,5
          LTA      *+,6
          MPY      *+,1
          LTA      *+,7             ; 8th tap
          MPY      *+,5
          LTA      *+,6
          MPY      *+,1
          LTA      *+,7             ; 9th tap
          MPY      *+,5
          LTA      *+,6
          MPY      *+,1
          LTA      *+,7             ; 10th tap
          MPY      *+,5
          LTA      *+,6
          MPY      *+,1
          LTA      *+,7             ; 11th tap
```

```
        MPY     *+,5
        LTA     *+,6
        MPY     *+,1            ; 12th tap
        LTA     *+,7
        MPY     *+,5
        LTA     *+,6
        MPY     *+,1            ; 13th  tap
        LTA     *+,7
        MPY     *+,5
        LTA     *+,6
        MPY     *
        LDPK    6
        LTA     YYK
        MPY     CYY
        LTA     XYK
        MPY     CYX
        APAC                    ; equaliser tap that is used to combat
        SACH    YE              ; DC offset
        ZALH    YE
        ADDH    YE              ; save result
        SACH    YE
        LRLK    AR7,0398h
        LARP    7
        LDPK    0
        LDPK    6
        RSXM
        RET
SC4     LAC     X1              ; load 4 bit
        SACL    Z
        ZALH    XN              ; sample 2nd equaliser input
        SACH    XTEM
        ZALH    YN
        SACH    YTEM
*****************************************************************
* Multiplying with sine and cosine to correct for carrier offset  *
*****************************************************************
        LT      COS
        MPY     XE              ; xe*cos
        LTP     SINE
        MPY     YE              ; ye*sin
        LTA     COS
        SACH    XRES,1          ; xres = xe*cos - ye*sin
        MPY     YE              ; ye*cos
        LTP     SINE
        MPY     XE              ; xe*sin
        SPAC
        SACH    YRES,1          ; yres = ye*cos - xe*sinx
*****************************************************************
* Demodulator algorithm                                         *
*****************************************************************
        ZALH    XRES            ; load I magnitude
        BGZ     PX1             ; test if it is positive
        ABS
        SUBH    TRSH            ; level test
        BGZ     GE2
        ZALH    YRES            ; load Q magnitude
        BGZ     PB1             ; test if it is positive
```

```
        ABS
        SUBH    TRSH            ; level test
        BGZ     S11
S3      SAR     AR4,X4          ; 1110
        SAR     AR3,X3          ; load bit X1,X2,X3,X4
        SAR     AR3,X2          ; to output through A/D
        SAR     AR3,X1
        LAC     MMAL            ; load X and Y magnitude
        SACL    YDES
        SACL    XDES
        B       EN
S11     SAR     AR4,X4          ; 0110
        SAR     AR3,X3          ; point in signal constellation
        SAR     AR3,X2
        SAR     AR4,X1
        LAC     MVEL
        SACL    YDES
        LAC     MMAL
        SACL    XDES
        B       EN
PB1     SUBH    TRSH
        BGZ     S10
S2      SAR     AR3,X4          ; 1101
        SAR     AR4,X3
        SAR     AR3,X2
        SAR     AR3,X1
        LAC     MMAL
        SACL    XDES
        LAC     PMAL
        SACL    YDES
        B       EN
S10     SAR     AR3,X4          ; 1001
        SAR     AR4,X3
        SAR     AR4,X2
        SAR     AR3,X1
        LAC     MMAL
        SACL    XDES
        LAC     PVEL
        SACL    YDES
        B       EN
GE2     ZALH    YRES
        BGZ     PU1
        ABS
        SUBH    TRSH            ; level test
        BGZ     S15
S7      SAR     AR4,X4          ; 1010
        SAR     AR3,X3
        SAR     AR4,X2
        SAR     AR3,X1
        LAC     MVEL
        SACL    XDES
        LAC     MMAL
        SACL    YDES
        B       EN
S15     SAR     AR4,X4          ; 0010
        SAR     AR3,X3
        SAR     AR4,X2
```

```
        SAR     AR4,X1
        LAC     MVEL
        SACL    XDES
        SACL    YDES
        B       EN
PU1     SUBH    TRSH
        BGZ     S14
S6      SAR     AR3,X4          ; 0101
        SAR     AR4,X3
        SAR     AR3,X2
        SAR     AR4,X1
        LAC     MVEL
        SACL    XDES
        LAC     PMAL
        SACL    YDES
        B       EN
S14     SAR     AR3,X4          ; 0001
        SAR     AR4,X3
        SAR     AR4,X2
        SAR     AR4,X1
        LAC     MVEL
        SACL    XDES
        LAC     PVEL
        SACL    YDES
        B       EN
PX1     SUBH    TRSH
        BGZ     GX1
        ZALH    YRES            ; load Q magnitude
        BGZ     PJ1
        ABS
        SUBH    TRSH            ; level test
        BGZ     S12
S4      SAR     AR3,X4          ; 1111
        SAR     AR3,X3
        SAR     AR3,X2
        SAR     AR3,X1
        LAC     PMAL
        SACL    XDES
        LAC     MMAL
        SACL    YDES
        B       EN
S12     SAR     AR3,X4          ; 1011
        SAR     AR3,X3
        SAR     AR4,X2
        SAR     AR3,X1
        LAC     MVEL
        SACL    YDES
        LAC     PMAL
        SACL    XDES
        B       EN
PJ1     SUBH    TRSH
        BGZ     S9
S1      SAR     AR4,X4          ; 1100
        SAR     AR4,X3
        SAR     AR3,X2
        SAR     AR3,X1
        LAC     PMAL
```

```
          SACL    XDES
          SACL    YDES
          B       EN
S9        SAR     AR4,X4          ; 0100
          SAR     AR4,X3
          SAR     AR3,X2
          SAR     AR4,X1
          LAC     PVEL
          SACL    YDES
          LAC     PMAL
          SACL    XDES
          B       EN
GX1       ZALH    YRES
          BGZ     PY1
          ABS
          SUBH    TRSH
          BGZ     S16
S8        SAR     AR3,X4          ; 0111
          SAR     AR3,X3
          SAR     AR3,X2
          SAR     AR4,X1
          LAC     PVEL
          SACL    XDES
          LAC     MMAL
          SACL    YDES
          B       EN
S16       SAR     AR3,X4          ; 0011
          SAR     AR3,X3
          SAR     AR4,X2
          SAR     AR4,X1
          LAC     PVEL
          SACL    XDES
          LAC     MVEL
          SACL    YDES
          B       EN
PY1       SUBH    TRSH
          BGZ     S13
S5        SAR     AR4,X4          ; 1000
          SAR     AR4,X3
          SAR     AR4,X2
          SAR     AR3,X1
          LAC     PVEL
          SACL    XDES
          LAC     PMAL
          SACL    YDES
          B       EN
S13       SAR     AR4,X4          ; 0000
          SAR     AR4,X3
          SAR     AR4,X2
          SAR     AR4,X1
          LAC     PVEL
          SACL    XDES
          SACL    YDES
          B       EN
*****************************************************************
*     Differential decoder                                      *
*****************************************************************
```

```
EN      RSXM                    ; binary value converting
        ZALH    X3
        BGZ     F0
        LACK    0
        B       F1
F0      LACK    1
        NOP
        NOP
F1      SACL    X3
        ZALH    X4
        BGZ     E0
        LACK    0
        B       E1
E0      LACK    1
        NOP
        NOP
E1      SACL    X4              ; modulo 4 subtraction
        LACK    4
        ADD     X4
        ADD     X3,1
        SUB     X4I
        SUB     X3I,1
        SACL    IMD
        ANDK    2
        SFR
        SACL    X3D             ; second bit delay
        LAC     IMD
        ANDK    1
        SACL    X4D             ; first bit delay
        LAC     X4
        SACL    X4I             ; converting back first and second bit
        LAC     X3              ; in appropriate value
        SACL    X3I
        LAC     X4D
        BNZ     E2
        SAR     AR4,X4
        B       E3
E2      SAR     AR3,X4
        NOP
        NOP
E3      LAC     X3D
        BNZ     E4
        SAR     AR4,X3
        B       E5
E4      SAR     AR3,X3
        NOP
        NOP
*****************************************************************
*    Calculation of Im{Zin*Zdes}                                *
*****************************************************************
E5      LT      YRES
        MPY     XDES            ; ydes*xdes
        LTP     XRES
        MPY     YDES            ; xres*ydes
        SPAC
        SACH    DRV,1           ; drv = ydes*xdes - xres*ydes
*****************************************************************
```

```
*    Loop  filter                                                    *
*****************************************************************
          SOVM
          LT        DRV             ; drv*cf2 (1st coefficients)
          MPY       CF2
          PAC
          SACH      DRV,1           ; delay
          LT        DRV
          MPY       CF1             ; delay*cf1
          PAC
          APAC
          ADDH      DLY
          SACH      DLY1
          ZALH      DRV
          ADDH      DLY
          SACH      COR
          DMOV      DLY1
          ROVM
*****************************************************************
*  Limiter - limits amgle to +-9.216615 degrees                   *
*****************************************************************
          ZALH      COR
          BLEZ      LM2
          NOP
          NOP
          SUBH      LIMIT           ; test if the value is greater then lim
          BLEZ      LM1
          ZALH      LIMIT
          SACH      COR             ; store limit
          B         CMD
LM1       NOP
          B         CMD
LM2       ADDH      LIMIT           ; test if the value is less then limit
          BGEZ      LM3
          ZALH      LIMIT
          NEG
          SACH      COR             ; store -limit
          B         CMD
LM3       NOP                       ; value between limits
          NOP
          B         CMD
CMD       NOP
*****************************************************************
*    Scaling of the angle                                       *
*****************************************************************
          LT        COR             ; multiply with small number
          MPY       CRG
          PAC
          SACH      STEP,1
          RET
TINT      EINT                      ; Timer subroutine
          RET
          .end
```