# DESIGN AND IMPLEMENTATION OF A RECONFIGURABLE DATA ACQUISITION INTEGRATED CIRCUIT

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SUBMITTED IN FULFILMENT OF THE REQUIREMENTS FOR THE DEGREE OF
**DOCTOR OF PHILOSOPHY**


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*I would like to dedicate this thesis to*
*my wonderful wife Thuy and my dear daughter Han*

# Declaration of Originality

I, Hai Phuong Le, declare that the PhD thesis entitled "Design and Implementation of a Reconfigurable Data Acquisition Integrated Circuit" is no more than 100,000 words in length, exclusive of tables, figures, appendices, references and footnotes. This thesis contains no material that has been submitted previously, in whole or in part, for the award of any other academic degree or diploma. Except where otherwise indicated, this thesis is my own work.

Hai Phuong Le

# Contents

## *Appendix B:*

# List of Figures

# List of Tables

# List of Abbreviations

| | |
|---|---|
| ADC | Analog-to-Digital Converter |
| ASIC | Application Specific Integrated Circuit |
| BiCMOS | Bipolar Complementary Metal-Oxide Semiconductor |
| CM | Common-Mode |
| CMOS | Complementary Metal-Oxide Semiconductor |
| DAC | Digital-to-Analog Converter |
| DAQ | Data Acquisition |
| DI | Differential Input |
| DNL | Differential Non-Linearity |
| DR | Dynamic Range |
| DSP | Digital Signal Processing |
| EDA | Electronic Design Automation |
| EISA | Extended Industry Standard Architecture |
| ENOB | Effective Number of Bits |
| FFT | Fast Fourier Transform |

| | |
|---|---|
| FPGA | Field Programmable Gate Array |
| IC | Integrated Circuit |
| INL | Integral Non-Linearity |
| I/O | Input-Output |
| IP | Intellectual Property |
| ISA | Industry Standard Architecture |
| LPF | Low-Pass Filter |
| LSB | Least Significant Bit |
| LSI | Large Scale Integration |
| LUT | Look-Up Table |
| MOS | Metal Oxide Semiconductor |
| MOSFET | Metal-Oxide Semiconductor Field Effect Transistor |
| MSI | Medium Scale Integration |
| MUX | Multiplexers |
| NF | Noise Figure |
| NMOS | Negative-Channel Metal Oxide Semiconductor |
| OPAM | Operational Amplifier |
| OTA | Operational Transconductance Amplifier |
| PC | Personal Computer |
| PCB | Printed Circuit Board |
| PCI | Peripheral Component Interconnect |
| PE | Pass Element |
| PGA | Programmable Gain Amplifier |
| PMOS | Positive-Channel Metal Oxide Semiconductor |

| | |
|---|---|
| RC | Resistance Capacitance |
| SA | Successive Approximation |
| SC | Switched-Capacitor |
| SE | Single-Ended |
| SHC | Sample and Hold Circuit |
| SNR | Signal-to-Noise Ratio |
| SoC | System-on-a-Chip |
| SSI | Small Scale Integration |
| TG | Transmission Gate |
| THD | Total Harmonic Distortion |
| ULSI | Ultra Large Scale Integration |
| VESA | Video Electronics Standards Association |
| VLSI | Very Large Scale Integration |
| W/L | Width and Length |

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# Abstract

Signal processing is a technique that is used to gather data from real world and make sense of it. For some time, engineers have attempted to develop electronic systems able to extract and process the real world signals and turn them into useful data. Initially this development was done using analog technology. However, since the digital signal processor has developed rapidly due to integrated circuit (IC) technology over the past 20 years, engineers have turned to digital signal processing as a more advanced and convenient method [1]. Data acquisition (DAQ) systems are, therefore, inevitably necessary, as they are the interface between analog and digital world. They have become crucial in a wide range of applications, including biomedical research, geophysics, gravitation measurements, telecommunication, power fault analysis, manufacturing process control and a wide variety of other test/measurement intensive fields.

Traditionally, DAQ systems have been built on Printed Circuit Boards (PCBs) with high quality shielding, grounding and insulation. These are referred to as board-based

DAQ systems, which are currently dominant. They have advantages in flexibility and ease of use since Personal Computers (PCs) have extensive hardware and software support to provide flexible control and implementation for plug-in devices. Rapid development of computer and digital technology has required a corresponding improvement of board-based DAQ systems. The plug-in boards have grown more and more sophisticated and versatile, acquired new functions and become functionality universal. Unfortunately, along the way the price of these systems has grown as well. Also, other major disadvantages of these board-based DAQ systems are high power consumption, large size and high cost. Such disadvantages are the real challenges of the modern electronic circuit and system design.

The primary objective of this research is to design and implement a reconfigurable DAQ system on a single IC for a multi-channel, high-speed, high accuracy microprocessor-based relay for power system protection application; for multi-channel, low-power biomedical instrumentation application and any multi-rate signal systems, e.g. process control application. A DAQ system is a large electronic system, which typically consists of an Analog-to-Digital Converter (ADC), a multiplexer (MUX), a sample and hold circuit (SHC), an amplifier and a system controller. This research work is based on selecting, optimising, modifying and proposing several new component architectures, to achieve a reconfigurable DAQ system with high performance, high-speed, low power consumption, low complexity and low cost for specific applications. In a DAQ system, ADC is the most critical component and its specifications and performance are application specific. The fastest ADC available in practice is the flash ADC. However, the complexity of the ADC circuit increases

exponentially with the increase of the number of bits (resolution), and thus it discourages its feasibility for implementation of a high-resolution system. In this research, the DAQ system implementation is based on a new modified flash ADC architecture, which has been developed to improve the system performance and reduce the system complexity and power consumption. The new flash ADC has been designed and implemented based on the development of a newly optimised comparator that offers an attractive combination of high-speed, low-power and high accuracy.

A mathematical model representing noise performance of the constituent components in the proposed reconfigurable DAQ system has been developed to theoretically justify the devices' performance. The developed model provides a very good estimation of the noise generated by the new circuit architectures and gives an accurate prediction on the circuit noise performance. Also, such model provides good guide for the improvement of the circuits' performance.

Two specific applications at least for the proposed DAQ system include biomedical instrumentation and power system protection. In biomedical instrumentation, it is usually required to acquire, analyse and display biosignals obtained from sensors, which converts a physical measureand from human body to an electric output. The biosignals, in nature, will have different frequency and amplitude range. A novel smart DAQ architecture is proposed to overcome the limitations of the traditional DAQ system in multi-rate biomedical application. Different frequency input channels will be sampled at different rates, so that data storage of the samples are reduced and the system power consumption will be saved, while maintaining the system accuracy.

Power systems occasionally experience faults and abnormal conditions, in such cases relays are used to avoid damage to the system and customer equipments. Digital relays are being increasingly used in power industry due to their advantages and flexibilities over traditional electro-mechanical relays. The function of a DAQ section in digital relays is to sample and digitise line voltages and currents so that a central processor or a host PC can detect and locate a fault and make decision whether or not to trip the relay. During fault conditions, the voltage and current waveforms are usually distorted and consists of numerous harmonics and reflected travelling wave components. Fault detection using short data window method will introduce errors due to the sub-harmonics and super-harmonics. High sampling frequency can reduce errors, but it is unnecessary and superfluous during normal conditions, when line voltage and current frequencies are of 50Hz. To overcome this issue, a novel reconfigurable DAQ architecture has been proposed to increase the system efficiency.

# List of Publications

## Peer-Reviewed Journal Papers

[1] **H. P. Le**, A. Zayegh, J. Singh, "Design and Implementation of a Low Cost Reconfigurable Data Acquisition System for Power System Protection Applications", *IEE Electronic Letters,* vol. 40, no. 20, pp. 1262 - 1263, September 2004.

[2] **H. P. Le**, A. Zayegh, J. Singh, A. Stojcevski, "A Low Power Data Conversion Scheme for a Battery Operated Communication System", *Best-of Book*, AMSE Journal Press., September 2004.

[3] **H. P. Le**, A. Zayegh, J. Singh, "Design and Implementation of the Constituent Components for a High-Speed Low-Power Data Acquisition System", *AMSE Journal Press.*, vol. 77, no. 8, pp. 75-95, August 2004

[4] **H. P. Le**, A. Zayegh, J. Singh, "A Smart Data Acquisition Architecture with Reduced Power And Complexity for a Multirate Process Control Application", *Best-of Book*, AMSE Journal Press., August 2004.

[5] A. Stojcevski, **H. P. Le**, A. Zayegh, J. Singh, "Low Power, New Flash ADC Architecture with Reduced Complexity", *Submitted to Journal of Circuits, Systems, and Computers (JCSC)*, June 2004

[6] **H. P. Le**, A. Zayegh, J. Singh, "Noise Modelling for a High-Speed CMOS Comparator", *Best of Book*, AMSE Journal Press., July 2003.

[7] **H. P. Le**, A. Zayegh, J. Singh, "Performance Analysis of an Optimised CMOS Comparator", *IEE Electronics Letters*, vol. 39, no. 11, pp. 833-835, May 2003.

[8] A. Stojcevski, **H. P. Le**, A. Zayegh, J. Singh, "Flash ADC Architecture," *IEE Electronics Letters*, vol. 39, no. 6, pp. 501-502, March 2003.

## Referred Conference Papers

[1] **H. P. Le**, A. Zayegh, J. Singh, "Control Unit Implementation For A Reduced Complexity Reconfigurable Data Acquisition Architecture", *Accepted for publication in the IEEE Asia-Pacific Conference on Circuits and Systems (APCCAS 2004)*, Taiwan, Taiwan, December 2004.

[2] **H. P. Le**, A. Stojcevski, A. Zayegh, J. Singh, "Performance Analysis of a Highly Efficient Flash ADC", *Proceedings of the 10th International Symposium on Integrated Circuits, Devices & Systems (ISIC 2004),* on CD-ROM, ISBN: 981-05-1787-4, Singapore, September 2004.

[3] **H. P. Le**, A. Zayegh, J. Singh, "Implementation of a Reduced Complexity High Performance Data Acquisition Chip using 0.18 micron Technology", *Presented at the 2nd IEEE International Conference on Circuits and Systems for Communications (ICCSC 2004)*, Moscow, Russia, July 2004.

[4] **H. P. Le**, A. Zayegh, J. Singh, "Noise Analysis of a Low Cost Pipeline ADC", *Proceedings of the IEEE Workshop on Electronic Design, Test & Applications (DELTA 2004)*, Perth, Australia, pp. 360-365, January 2004.

[5] **H. P. Le**, A. Zayegh, J. Singh, "Performance Analysis of High-Accuracy CMOS Sample-And-Hold Circuits", *Proceedings of the SPIE's International Symposium on Microelectronics, MEMS, and Nanotechnology*, Perth, Australia, vol. 5274, pp. 269-276, December 2003.

[6] **H. P. Le**, A. Zayegh, J. Singh, "A 12-Bit High Performance Low Cost Pipeline ADC", *Proceedings of the 10th IEEE International Conference on Electronics, Circuits and Systems (ICECS 2003)*, The United Arab Emirates, pp. 471-474, December 2003.

[7] **H. P. Le**, A. Stojcevski, A. Zayegh, J. Singh, "Low Cost Flash Architecture For A Pipeline ADC," *Proceedings of the 10th International Conference of Mixed Design of Integrated Circuits and Systems (MIXDES),* Lodz, Poland, pp. 238-241, June 2003.

[8] **H. P. Le**, A. Zayegh, J. Singh, "A High-Speed Low-Power CMOS Comparator with 10-bit resolution," *Proceedings of the Fourth International Conference on Modelling and Simulation (MS'02)*, Melbourne, Australia, pp. 138-142, 2002.

# Chapter 1

# Thesis Overview

## 1.1 Introduction

Signal processing is a technique that is used to gather data from real world and analyse it. For some time, engineers have attempted to develop electronic systems able to extract and process the real world signals and turn them into useful data. Initially this development was done using analog technology. However, since the digital signal processor has developed rapidly due to integrated circuit (IC) technology over the past 20 years, engineers have turned to digital signal processing as a more advanced and convenient method [1].

Data Acquisition (DAQ) in a general definition is a process of collecting information or data from the real world that describe a given physical phenomenon or situation. For engineers and scientists, this data is mostly numerical and usually collected, stored and

analysed using computers. However, most of the data cannot be read directly by digital computers because they are generally generated from sensors and transducers, which convert real-world parameters such as pressure, temperature, stress or strain, flow, etc, into equivalent electrical signals. Analog signals are distinguished by continuous values while computers can only recognise digital signals containing only '0's and '1's. DAQ systems are therefore inevitably necessary, as they include the translation requirement from analog signals to digital data. For this reason, they have become crucial in a wide range of applications in modern science and technology [2].

The areas of applications for DAQ systems include biomedical research, geophysics, gravitation measurements, telecommunication, power fault analysis, manufacturing process control and a wide variety of other test/measurement intensive fields [3]. Traditionally, DAQ systems have been built on Printed Circuit Boards (PCBs) with high quality shielding, grounding and insulation. These are referred to as board-based DAQ systems, which are currently dominant. They have advantages in flexibility and ease of use since Personal Computers (PCs) have extensive hardware and software support to provide flexible control and implementation for plug-in devices [2]. Rapid development of computer and digital technology has required corresponding improvement of board-based DAQ systems. The plug-in boards have grown more and more sophisticated and versatile, acquired new functions and become functionality universal. Unfortunately, along the way the price of these systems has grown as well. Also, other major disadvantages of these board-based DAQ systems are high power consumption and large size (e.g. they may consume up to 10W-15W from a 5V to 10V

power supply) [4-8]. Such disadvantages are the real challenges of the modern electronic circuit and system design.

The fast development in microelectronic technologies paved the way for a new methodology of integrating DAQ systems on a single IC (also known as a chip). The first IC was fabricated in 1958 by Jack Kilby and since then there have been several generations of ICs, which are Small Scale Integration (SSI), Medium Scale Integration (MSI), Large Scale Integration (LSI), Very Large Scale Integration (VLSI) and recently Ultra Large Scale Integration (ULSI). Today an IC smaller than a cent can hold 125 million transistors [9].

Using recent sub-micron technologies, it is now possible to integrate millions of transistors on a single chip. The DAQ systems on a chip (chip-based DAQ systems) offer many advantages over the traditional board-based DAQ systems. For example, they are cheaper, faster, smaller and consume less power with better performance compared to the traditional board-based DAQ systems. Recently, some chip-based DAQ systems have been reported [10-15]. They consume only about 200mW at 5V power supply [16]. They, therefore, satisfy requirements of modern technology and have become the optimum solution for most present-day general-purpose applications.

Due to requirements of current and emerging applications, such as high performance wireless communication, high-speed power system fault analysis, multi-rate biomedical instrumentation, there is a continued search for architectures and circuit techniques enabling DAQ systems to attain higher speed, more enhanced performance with smaller

chip area and lower power dissipation. As speed requirement is continuously increasing and power consumption requirement is continuously decreasing in electronic systems, the general-purpose DAQ chips with fix function, resolution and speed can no longer satisfy present day and future applications. For example, high performance wireless communication and battery-based applications require reasonably fast sampling speed DAQ systems with minimum power consumption, whilst modern power protection applications are placing demand for higher speed, better accuracy and better reliability. Therefore, future DAQ systems should adaptively modify or scale their attributes to suit different operating conditions and requirements of several different applications.

The future development of DAQ systems will be to integrate reconfigurable property into DAQ systems. Some of current board-based and chip-based DAQ systems have a degree of *'intelligence'* in the sense that they could be programmed externally to make some decisions, but are not *'reconfigurable'* to scale themselves to optimise their functions. *Reconfigurability* could be defined as an intelligent property with which the DAQ systems can configure themselves to match operating circumstances. This allows the systems to operate at a fraction of their capability to provide optimal performance, and will reconfigure the systems to operate at full capability only when it is required. Traditional chip-based DAQ systems always operate at full-scale function even when it is not required. Such reconfigurable property will optimise the system function by reducing the system power consumption and complexity as well as increasing the system efficiency and performance. The reconfigurable DAQ chips will be the vital development for present day and future applications.

## 1.2 Aim of this Research

The overall goal of this research is to design and implement a reconfigurable DAQ system on a chip for multi-channel, multi-rate, flexible-speed, low-power applications, such as biomedical instrumentation and power system protection devices. The specific aims to achieve a successful completion of this research are:

- *Design and implement the constituent components of a DAQ system*: Appropriate circuit technologies and design techniques to implement the constituent components of a DAQ system are investigated, selected and optimised. The design of each component is aimed at high-accuracy and high-speed as well as low power dissipation and reduced complexity. Several new component architectures are proposed to achieve a DAQ system with high performance, high-speed, low power consumption, low complexity and low cost for specific applications.

- *Develop the DAQ chip using the proposed building block components*: The implemented constituent components are integrated to develop a DAQ system. A suitable controller is implemented to generate strobe signals to ensure proper functional sequences in DAQ systems and to communicate with external PCs using a standard bus.

- *Develop a novel reconfigurable DAQ architecture to improve the system performance and efficiency for power system protection application*: A

reconfigurable structure is developed enabling the DAQ chip adaptively modify or change its operating parameters to suit a change in the operating condition. Statistical analysis on the system performance for power system protection application will be carried out to demonstrate the superiority and efficiency of the reconfigurable architecture.

- *Develop a novel reconfigurable DAQ architecture to improve the system performance and efficiency for biomedical application*: New circuit techniques are developed in order to satisfy the application requirements and to reduce the system power consumption and complexity. An appropriate algorithm is developed so that the DAQ chip can automatically adjust its characteristics, such as its sampling speed, to suit different application requirements at different operating conditions. The DAQ system performance is carried out to highlight the appropriateness of the proposed system for biomedical application.

## 1.3 Research Methodologies and Techniques

This research targets the design and implementation of a reconfigurable DAQ system on a single IC for multi-channel, multi-rate, low-power applications, such as biomedical application or power system protection application. The system design, simulation, implementation and layout verification will be carried out using appropriate Electronic Design Automation (EDA) Tools. The reconfigurable DAQ system should satisfy the requirements of preferred applications concerning the circuit performance for reliability, speed, power consumption and size.

The following tasks need to be addressed first to determine the most suitable technology and circuit design technique to achieve a successful implementation of the complex mixed-signal DAQ system.

(a) Investigate and select the best microelectronic device technology suitable for such large and sophisticated DAQ system.

(b) Investigate and select the most suitable circuit design technique for the DAQ system.

(c) Optimise the selected design techniques to obtain the best circuit performance.

After successfully identifying the most appropriate technology and circuit design technique for the system implementation, the details of proposed methodology and techniques to achieve the requirements of this research project are as follows:

(i) *Analog-to-Digital converter (ADC) design*: This is the core of the data acquisition system. Several types of ADC have to be evaluated to determine the most appropriate ADC architecture that satisfies the system specifications (high speed, low power consumption and small size). The design simulation and implementation of the ADC will be carried out using Cadence Analog Artist Environment, which is a universal industry standard microelectronic design suite.

(ii) *Analog-to-Digital section of the DAQ system design:* After completing the ADC design, implementation and test, a further development of the analog-to-digital section of the DAQ system will be carried outs. Each building block of this section including an analog multiplexer (MUX), a programmable gain amplifier (PGA), an anti-aliasing filter and a sample-and-hold circuit (SHC) will be selected to satisfy the required performance and to complement the function of the ADC designed in section (i).

(iii) *Controller for the data acquisition system:* Investigate and design an appropriate timing and control circuits, required to synchronise the functions of the DAQ unit and to communicate with external PCs via a communication interface standard. Special emphasis will be made on the speed, system control and synchronisation of the DAQ system as well as optimum digital circuit implementation.

(iv) *Data acquisition system design:* This step is to integrate the blocks designed in section (ii) and (iii) to complete the DAQ system design. Specific design steps will be followed to achieve correct timing and functionality of each building block of the system. Noise cancellation between analog and digital sections of the DAQ system will be addressed. Exhaustive simulation and design modification have to be performed to ensure that the design will meet the performance requirements.

(v) *Reconfigurability feature implementation for the preferred applications:* Special control unit will be designed and implemented to provide the necessary modified operating parameters of the unit to adapt to changes in operating conditions. Again, exhaustive circuit simulation and modification will be carried out to meet the performance requirements. Cadence EDA Tool will be used to implement the complete DAQ unit.

(vi) *Performance analysis and testing:* The final unit will be tested for accurate and reliable performance for preferred applications. System performance analysis will be performed to evaluate the efficiency of the proposed reconfigurable DAQ system.

## 1.4 Originality of the Thesis

This research will contribute to knowledge in microelectronic system design by tackling the major issues related to high-speed, low-power and intelligent DAQ design. Since the aim of this research is to design and implement a high speed, low power and reconfigurable DAQ system on a single IC, this research will contribute to knowledge in the following aspects:

- Development of a design methodology to build and integrate such a large and complicated mixed signal system as DAQ system on one chip (single IC) to reduce device size and cost.

- Development of new design techniques and circuit structures to reduce the designed DAQ chip circuit complexity and power dissipations as well as increase its speed and enhance its performance.
- Development of novel circuit structure to enable the integrated DAQ system to be reconfigurable in order to further increase its speed, reduce its power consumption and enhance its performance to adapt to different application requirements.
- Design, implementation and testing of the reconfigurable property of the DAQ chip.

This research is significant since it will address several critical issues of new DAQ system performance in the microelectronic environment. It is important to design and integrate a DAQ system with small size, high speed and low power consumption for modern applications. Speed and power consumption are two of the most important aspects to judge modern microelectronic system performance. It is also significant to attain a DAQ system smaller in size and lower in cost. Size and cost are the most competitive properties of any microelectronic system available in the market. There is currently a large number of DAQ systems available, but most of those are board-based systems. Their main disadvantages are high power consumption, large size and high cost. This research project targets the design and implementation of a reconfigurable DAQ system on a single chip (single IC) which is cheaper, faster, smaller with lower power consumption, and therefore, it will be highly beneficial to industry.

The research is also significant as new circuit techniques and algorithms will be developed, enabling further reduction of device power consumption, area and complexity. The multi-channel DAQ chip should be based on a very fast, high performance ADC. New ADC technique should be developed and implemented to reduce the system complexity, area and power consumption for high-speed DAQ units.

It is also necessary to implement a reconfigurable property into DAQ system. Reconfigurable property is an intelligent property with which the system can adjust its function to match new operating conditions and requirements. Traditional DAQ systems always operate at full-scale function (full capacity) even when it is not required. The above reconfigurable property will adjust the scale function to the necessary level and dramatically increase the speed and performance as well as reduce the power consumption of the DAQ system. For example, a 100MHz DAQ system will be scaled down to 10MHz sampling rate for slower input signal, which will reduce the system power consumption and need for large storage, and hence correspondingly reduce system complexity.

This research is also significant because it will address major risks and challenges related to electronic circuit design and integration, such as: how to implement or integrate such sophisticated systems on a chip; how to determine the most appropriate circuit design technology suitable for this complicated system; how to solve the grounding problem and other issues related to mixed signal system design.

## 1.5 Organisation of the Thesis

This thesis contains eight chapters and is organised as follows:

Chapter 1 provides a basic introduction about the research as well as the aims of this research, the research methodologies and techniques and the contribution of this research to knowledge.

Chapter 2 presents a literature review of DAQ systems as well as industrial applications of the designed DAQ chip. Intense studies on the evolution of several generations of DAQ systems are presented. Previous and current trends of DAQ development are directed towards the implementation of more functions and attributes onto DAQ systems allowing them to perform more complex tasks at higher speed. Current and future trends of DAQ development target the implementation of DAQ system on a single IC to attain higher performance with lower power consumption, less circuit complexity, smaller size and lower cost. Literature reviews also highlights that there has been very limited research on reconfigurable DAQ system, especially for the current and emerging industrial applications.

Design implications and development for all constituent components for DAQ system will be presented in Chapter 3. The typical building blocks of a DAQ system include ADC, MUX, SHC and a system controller, where ADC is the key element in the DAQ device. In-depth study and analysis of various design techniques and methodologies to implement the DAQ system components are discussed and the most appropriate

technique will be chosen. Performance analysis of the system will be considered to justify proper function of the designed components and the appropriateness of the design techniques and methodologies.

Design, implementation and performance analysis of a new, high performance, reduced complexity ADC employed in the proposed DAQ system will be discussed in Chapter 4. Pipeline ADC is selected for the proposed DAQ chip due to its very small power consumption and low complexity along with very high resolution at reasonably fast sampling speed. Typically, a pipeline ADC consists of numerous consecutive stages, each stage employs a low-resolution flash ADC to provide the coarse digital bits. However, in this design a new modified flash ADC architecture will be used instead of the traditional flash ADC to greatly reduce design complexity and power dissipation. In-depth optimisation and analysis of a comparator utilised in the modified flash ADC will also be discussed.

Chapter 5 presents the design, implementation and performance analysis of the complete DAQ unit. Integration of designed constituent components to construct the complete DAQ system will be addressed. DAQ system interface with external PCs and/or other digital controller devices will also be discussed. Performance analysis indicates the system proper function and the suitability of the design technique and technology.

Chapter 6 presents the implementation of a reconfigurable DAQ system for power system protection application. System performance and efficiency analysis will highlight the suitability of the proposed DAQ system for the dedicated application.

Chapter 7 presents the implementation of a reconfigurable property on DAQ system for biomedical instrumentation and its performance analysis for preferred applications. The DAQ architecture is highly efficient for the biomedical application, in a sense that it automatically adjusts its signal conditioning function, including filtering condition and amplification gain, to suit the selected input channel for processing. In addition, it correspondingly varies its sampling frequency, depending on the input channel requirements.

The conclusions and future work for this research are discussed in Chapter 8.

# Chapter 2

# Literature Review

## 2.1 Introduction

Digital signal processors have developed rapidly due to integrated circuit (IC) technology for the past 20 years. Digital signal processing of an analog signal is preferable to processing the signal directly in the analog domain since digital signals are easily stored on magnetic media without deterioration or loss of signal integrity. Moreover, the digital signal processing method also allows for the implementation of more sophisticated signal processing algorithms, while it is very difficult to perform precise mathematical operations on analog signal form. In addition, digital implementation of the signal processing system is cheaper than its analog counterparts. Data acquisition (DAQ) systems are therefore inevitably necessary, as they are the interface between analog and digital signals. For this reason, DAQ systems have become significant in wide range of applications in modern science and technology [1].

Applications of DAQ systems include biomedical instrumentation, geophysics, gravitation measurements, telecommunication, power fault analysis, manufacturing process control and a wide variety of other test/measurement intensive fields of modern technology. Each application places a different demand on DAQ system characteristics, such as higher speed, lower power consumption and higher accuracy [2]. Based on the above needs, this chapter describes the most relevant literature reviewed in order to present an understanding of the research topic. A detailed review of various DAQ systems which are currently available as well as an in-depth revision of major applications of DAQ systems are presented in this chapter.

The literature review is organised into six subsections. The evolution and future trend of DAQ systems is described in Section 2.2. Section 2.3 discusses the design implications of building block components of a high-speed low-power DAQ system. Two major applications for the DAQ system, that include biomedical instrumentation and power system protection, are presented in Section 2.4 and 2.5 respectively. Conclusions of this chapter are presented in Section 2.6.

## 2.2 DAQ System Architecture Review

DAQ systems have currently become a vital instrument for most of the Engineering applications since they provide the ultimate links between digital (computer) world and the traditional analog applications. A DAQ system typically includes a Digital-to-Analog Converter (ADC), considered as the heart of the systems, as well as an analog multiplexer (MUX), a sample and hold circuits (SHC), a programmable gain amplifier

(PGA), a timing circuit and a bus interface with a personal computer (PC), as illustrated in Figure 2.1 [1-3]. Details of these components will be discussed in Section 2.3.

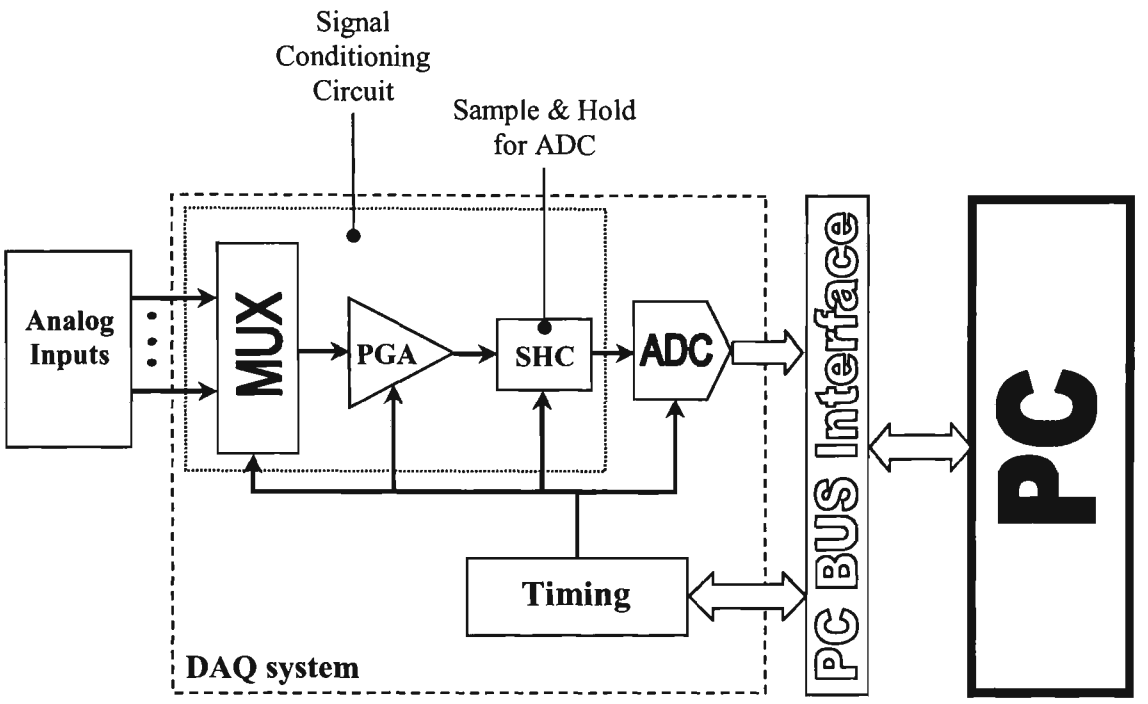



Figure 2.1 Block diagram of a typical Data Acquisition system.

Currently, most of the DAQ systems are available as board-based units (PC-based units) [4-8]. Most of these units were designed for general-purpose applications. They are classified as external or internal DAQ system depending on the method used to communicate with a PC.

- External DAQ systems are normally enclosed in a box outside the PC system. They communicate with PC via external busses, such as RS-232, RS-485 or IEEE-488 etc. They usually contain on-board microprocessor to independently control the DAQ process. The advantages associated with external DAQ systems are: less dependence of PC and remote distribution [2].

- Internal DAQ systems are typically hardware boards that are directly plugged into internal PC buses, such as Industry Standard Architecture (ISA), Extended Industry Standard Architecture (EISA) or Peripheral Component Interconnect (PCI). They normally do not contain on-board microprocessor, but they can directly access PC resources to enhance speed. The advantages of internal DAQ systems are: high speed, low cost and small size [2].

Existing DAQ systems, as reported in [4-16], tended to use reasonably fast and accurate ADC, such as Successive Approximation (SA) ADC. These systems can run at maximum frequency of 50MHz, providing the maximum data sampling rate of 150kS/s. They were the perfect solution for accuracy applications such as process control and test/measurement applications. However, applications, such as high-end video signal processing, high performance wireless communication [17, 18] and power system fault analysis, require the signal sampling rate approaching 100MS/s. The existing DAQ systems cannot fulfil this speed requirement. There is, therefore, a continued search for architectures and circuit techniques enabling DAQ system to attain higher performance with lower power consumption, less complexity and lower cost.

### 2.2.1 Evolution of PC-based DAQ system structure

Current PC-based DAQ systems have been evolved through four generations from simple structures to sophisticated structures adapting wide range of applications, which will be discussed as follows:

- **First generation:** The early PC-based DAQ system was built with the basic components which were an ADC, a PGA, a SHC, bus interface with PCs and a system controller. PC bus interface provides the mechanism for transferring data from PC-based DAQ system into the host computer's memory, and for sending any configuration information, data and command instructions from PCs back to the DAQ system. The system controller is responsible to communicate with the host PC and to generate control signals for DAQ systems. DAQ systems of the first generation only support single-input configuration, which is able to sample only one input channel. An example of this generation is the 10-bit CPCI-510H board (manufactured by DATEL), which contains one input channel. Recently, single-input DAQ systems have been rarely manufactured. Most of the current DAQ systems fall in second or third generations of DAQ systems [19].

- **Second generation:** Most of the applications in Engineering and Science domain need to acquire different parameters (data) from several sources so that they can determine the operating environment and can generate suitable control signals for each circumstance. For this reason, analog MUXs have been included in the DAQ systems in the second generation to establish multiple-input DAQ structure. Using MUX allows several input channels to be serviced by one amplifier and one ADC. The MUX channel selection can be controlled by on-board hardware or by software to select any one channel for processing at a given time. However, since the amplifier and the ADC are shared, the channels are read sequentially causing the overall speed of the system to be reduced [2]. A large number of DAQ systems currently available fall into

this category. An example is the NB-MIO-16X DAQ board, manufactured by National Instruments, has 16 single-ended (SE)/8-differential inputs (DIs) [20].

- **Third Generation:** The development of DAQ system has been expanded further by adding other components on-board to enhance the system performance. The most common element added to current DAQ systems is the memory buffer (memory). The memory provides temporary storage of the converted (digital) data for processing. The size of the on-board memory can vary from a few kilobytes to tens of megabytes, depending on the manufacturer's specifications and techniques. Most of the currently available DAQ systems include memory buffer. For example the DVME630 DAQ board, manufactured by DATEL, has 16-SE/8-DI with build-in 1MB or 4MB (optional) of Random Access Memory (RAM) and 8kB × 32 Expansion (secondary) RAM [2, 17, 19].

- **Fourth Generation:** The widespread use of DAQ systems in test, measurement and control applications encouraged further development of DAQ systems. A further important step has been implemented by adding a degree of intelligence to such systems, by incorporating an on-board microprocessor. A microprocessor is an intelligent device that can be programmed to make logical decisions based on its input data for each system operating condition. The on-board microprocessor handles board timing, data transfer, error checking and provides all necessary instructions allowing the system to operate independently. This dramatically reduces the PC engagement, boosts up system performance and increases system efficiency. In addition, on-board microprocessor provides a flexible approach in which the DAQ system can be

programmed to perform different tasks and to have different set of attributes to better suit specific applications. Current microprocessors support 16-bit or 32-bit address bus and 8-bit to 16-bit data bus. Current trend of DAQ system is to include the on-board microprocessor such as the DT2801 board, manufactured by Data Translation Inc.

Table 2.1 presents summary of currently available PC-based DAQ systems that are manufactured by recognised companies.

Table 2.1 : Summary of currently released PC-based DAQ systems [19-25].

| Name | CPCI-510H | NB-MIO-16X | PCI-6013 | DAQP-308 | DT2801 | DT9834 |
|---|---|---|---|---|---|---|
| **Company** | DATEL | National Instrument | National Instrument | Boston Technology | Data Translation | Data Translation |
| **Resolution** | 12-bit | 16-bit | 16-bit | 16-bit | 12-bit | 16-bit |
| **Clocking Speed** | 10MHz | 7MHz | 20MHz | 5MHz | N/A | N/A |
| **Acquisition Rate** | 10kHz | 55kHz | 200 kHz | 100kHz | 250 kHz | 500kHz |
| **No. of inputs** | 1SE | 16 SE/8 DI | 16 SE/8 DI | 8 SE/4 DI | 16 SE/8 DI | 16 SE/8 DI |
| **On-board memory** | No | No | Yes | Yes | Yes | Yes |
| **On-board micro-processor** | No | No | No | No | Yes | Yes |
| **On-board filter** | No | No | No | No | No | No |
| **PGA Gains** | 1 | 1, 2, 4, 8 or 1, 10, 100, 500 | 1 | 1, 2, 4, 8 | 1, 2, 4, 8 | 1, 2, 4, 8 |
| **Type** | Internal | Internal | Internal | External | Internal | External |
| **DNL** | ± 1.5 LSB | ± 0.2 LSB | ± 0.5 LSB | +3/-2 LSB | ± 0.5 LSB | ± 0.75 LSB |
| **INL** | ± 1 LSB | ± 0.25 LSB | ± 0.5 LSB | ± 3 LSB | ± 0.8 LSB | ± 1 LSB |
| **Released Date** | 1996 | 1997 | 2003 | 2000 | 2001 | 2004 |

## 2.2.2 New trend of DAQ Systems

A large number of advanced and sophisticated PC-based DAQ systems have been developed for a large spectrum of applications. Improved through the four generations, the plug-in boards have grown more and more sophisticated and versatile, acquired new functions and become functionality universal. They, however, suffer from large sizes,

high power consumption and high cost (e.g. they may consume up to 10W-15W from a 5V to 10V power supply) [4-8]. They were typically designed for PC-based applications where power consumption is not really an issue. However, most of the modern applications in Engineering and Science require DAQ system to take advantages of microelectronic developments, DAQ boards will no longer satisfy the requirements of modern applications such as wireless technology where size and power consumption are the main issues. Current applications prefer the DAQ systems to be self-contained and operate at high speed with low power consumption in order to achieve better efficiency.

For the past ten years, Complementary Metal-Oxide Semiconductor (CMOS) technology has become a dominant fabrication process for relatively high performance and low cost Very Large Scale Integration (VLSI) circuits. The fast development in microelectronic technology has paved the way for a new methodology of integrating a mixed-signal (digital and analog) system on a single IC (chip). The demand for performance, speed, accuracy, area and power consumption has motivated the design and implementation of DAQ on a single chip. Recently, some DAQ systems on a single chip have been reported [10-16, 26, 27]. Chip-based DAQ systems are cheaper, faster, smaller than PC-based DAQ systems and consume less power with better performance. They, therefore, satisfy requirements of modern technology and become the optimal solution for present day applications.

Table 2.2 shows summary of the recently released DAQ chips from Burr-Brown Corporation. Table 2.3 shows summary of the recently released DAQ chips from Analog Devices Inc [22, 23].

Table 2.2 : Summary of chip-based DAQ systems from Burr-Brown Corporation.

| Chip Name | ADS1250 | VECANA01 | ADS7869 |
|---|---|---|---|
| Released Date | December 1999 | October 2000 | November 2003 |
| Built-In Devices | PGA, 20-bit 4$^{th}$-Order $\Delta\sigma$ Modulator ADC, 1 Digital Filer, Timing Control, Serial Output | 3 MUXs, 3 S/Hs, 3 PGAs, 3 12-bit ADCs, 8-bit DAC, Control Logic, Voltage Reference | 5 MUXs, 7 S/Hs, 3 ADCs, 10 Comparators, 2 Counters, Control Logics |
| Resolution | 20-bits | 12-bit | 12-bit |
| Throughput Rate | 25kSample/s | 78kSample/s | 1MSample/s |
| Clock Frequency | 10MHz | 50MHz | 16MHz |
| MUX Input | N/A | 10-fully DI | 8-SE/4-DI |
| PGA Gains | 1, 2, 4, 8 | 1, 1.25, 2.5, 5 | N/A |
| Voltage Supply | 4V | 5V | 5V |
| Analog Input | -0.3-4V | 0-5V | 0.5-2.5V |
| Power Dissipation | 100mW | 225mW | 250mW |
| DNL | N/A | ±0.5 LSB | ±2 LSB |
| INL | 0.002%FSR | ±0.5 LSB | ±1 LSB |

Table 2.3 : Summary of chip-based DAQ systems from Analog Devices Inc.

| Chip Name | ADUC824 | AD7490 |
|---|---|---|
| Released Date | Nov. 2000 | May 2002 |
| Built-In Devices | 2 MUXs, PGA, 24-bit Σ-Δ ADC, 16-bit Σ-Δ ADC, 12-bit DAC, RAM, micro-controller | MUX, 1 SHC, 12-bit SA ADC, Control Logic |
| Resolution | 24- or 16-bit | 12-bits |
| Throughput Rate | 10kS/s | 1MS/s |
| Clock Frequency | 13MHz | 15MHz |
| MUX Input | 4 DI | 8DI |
| PGA Gains | 1, 2, 4, 8 | N/A |
| Voltage Supply | 5V | 3.3V and 5V |
| Power Dissipation | 70mW | 12.5mW |
| DNL | ±0.5 LSB | -0.95/+1.5 |
| INL | ±0.5 LSB | ±1 LSB |

## 2.2.3 Future trends of DAQ Systems

DAQ chips have been continuously designed and improved towards smaller size, faster system processing speed, lower power consumption and lower cost [28-30].

The rapid development of microelectronic technology provides possibilities to implement more functions on single IC. The development of chip fabrication technology [31-33] moved quickly from 0.5-μm technology down to 0.25-μm technology and 0.18-μm technology. This will enable complex System-on-a-Chip (SoC) to be implemented and to have smaller size, low power consumption and higher speed.

The chip-based DAQ system supply voltage [31-33] has been reduced continuously from 10V down to 5V, to 2.5V and recently to 1V to obtain low power consumption. Currently, as the silicon technology is moving toward 0.1 μm and below, millions of transistors can now be integrated into a single chip. All the required functions, such as ADC, SHC, memories, microprocessor etc. can be integrated into a single chip. However, there will be different voltage requirements of the on-chip components (e.g. digital circuits can operate at a much lower supply voltage than analog circuits). Therefore, instead of using the same supply voltage for all constituent components, the trend of modern technology is to develop on-chip reference voltage device to provide the optimum set of different supply voltages to different on-chip devices to obtain minimum power consumption.

Cost of SoC is another important emerging issue. Development of better technologies and techniques brings down the chip-fabrication cost. However, the chip-testing cost will increase. It is difficult to perform the full test and scan for the DAQ chip comprising analog, digital, memory, and mixed-signal functionality. Bringing the

testing cost down is yet another challenge. The future trend is to develop an optimised testing methodology for DAQ chips [34].

Another approach of the future development of DAQ systems is to integrate reconfigurable property into DAQ systems. Some of current board-based and chip-based DAQ systems have a degree of *'intelligence'* in the sense that they could be programmed externally to make some decisions, but are not *'reconfigurable'* to scale themselves to optimise their functions. *Reconfigurability* could be defined as an intelligent functionality where a system can modify or scale its operating parameters to suit a change in operating conditions. Such reconfigurable property will yield optimum system power consumption efficiency, as well as dramatically reduce the cost and increase the performance of DAQ systems.

## 2.3 Design Implications for Data Acquisition System

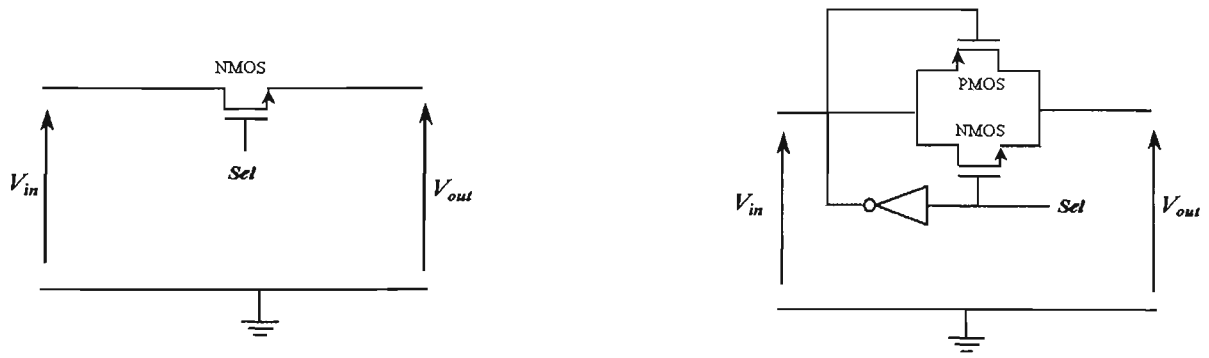
This section presents detailed revisions of the most critical building block components of a typical DAQ system, including analog MUXs, PGAs, SHCs and ADCs. Anti-aliasing filters are not typically integrated into a DAQ system due to its high complexity and cost. Filters are not implemented in PC-based DAQ systems that are presented in Table 2.1 and reported in [29, 35-38], where signal filtering is sometimes performed using a microprocessor or Digital Signal Processing (DSP) core in digital domain or using an external signal-conditioner. Only few currently available DAQ units, as reported in [39, 40], contain on-board anti-aliasing filters. However, their

power consumption is very high compared to their counterparts. Therefore, a review of anti-aliasing filters is not presented in this section.

### 2.3.1 Analog Multiplexer (MUX)

An analog MUX is one of the most sensitive parts in the design of the DAQ system. It is the most essential device for accurate sampling of multi-input channels. A MUX typically comprises of several switches connecting all of the input channels to the output end of the MUX. Depending on the given address code, the switches will be appropriately turned "ON" or "OFF" to construct a path from a specific signal input to the output of the MUX for processing at a given time [41, 42].

In Metal-Oxide Semiconductor Field Effect Transistor (MOSFET) technology, the most popular method to implement the switch is using Negative-Channel Metal Oxide Semiconductor (NMOS) pass element (PE) or CMOS transmission gate (TG), as illustrated is Figure 2.2 (a) and (b) [42].




(a) (b)

Figure 2.2 (a) NMOS PE, (b) CMOS TG.

When the select signal (*Sel*) is high, they act like a linear resistor, allowing the input $V_{in}$ to be connected to the output $V_{out}$. When *Sel* is low, the transistors are cut off, isolating the input from the output.

In general, both of the NMOS PE and CMOS TG can be used as switches to design MUXs. However, CMOS TG is typically chosen due to its superior characteristics compared to the NMOS PE [41, 43], which are:

- Dynamic analog signal range of the CMOS TG in on-state is greatly increased, since the CMOS does not encounter any signal delegation due to the threshold voltage and its related body bias effect.
- Since CMOS TG has n- and p- channel device in parallel and requiring opposing clock signals, the clock feedthrough effect (which is the principal source of error in MUX) in CMOS TG is partially cancelled.

### 2.3.2 Programmable Gain Amplifier (PGA)

A PGA is usually placed in front of a data conversion system to boost up small input signal and to adapt the loss variation in transmission channels so as to ease the dynamic range requirements for ADCs. In broadband systems, it is critical for the PGA to maintain its linearity over the entire signal bandwidth as well as gain range [44].

A high-speed PGA that is introduced in [45] exhibits a 35-dB range and 50-MHz bandwidth. It exploits the use of parasitic lateral bipolar transistor, implementing a semi-logarithmic gain characteristic. It produces maximum undistorted of 1V p-p

differential and a 2mV (rms) output noise in the circuit, which would clearly not degrade the original Signal-to-Noise Ratio (SNR) for low noise applications. Moreover, the output noise remains relatively constant over the entire gain range of the PGA. However, the PGA topology linearity is limited by the transconductance and supplementary linearisation schemes are required to obtain wide input range.

An improved method using degenerated source-coupled pair with transconductance enhancement proposed in [46] can significantly improve PGA linearity. It exhibits low-distortion characteristic (total harmonic distortion figures are below -60dB) for high-frequency applications. Another major advantage of this PGA architecture is that the amplifier can be designed to produce both gain and attenuation by tuning the ratio of load and degeneration resistors. For high-frequency applications, wide-band noise specifications limit the value of the degeneration and load resistors to the range. Practical values for the transconductance of the differential pair are limited to the mA/V range for modern CMOS processes. As a first consequence of the limited range for these resistors values, the degeneration gain will be relatively low, resulting in a moderate gain accuracy and linearity of the voltage-to-current (VI) conversion. However, the open-loop nature of the PGA makes the linearity of the circuit heavily depend on the inherent linearity of the input stages.

A class of closed-loop PGAs employing negative feedback approach to achieve high linearity requirement has been reported in [47, 48]. DC offset cancellation technique approach, which is constructed of active MOS resistors, has been introduced in [49] to speed up the offset suppression loop during transient without applying any external

component. Although the closed-loop architectures can achieve high linearity, the previous work designs involved trade-off among bandwidth, linearity and power dissipation.

A PGA using current-mode amplifier and resistor-network feedback technique has been introduced in [50]. It can achieve constant bandwidth, high linearity, and optimal power dissipation. The voltage gain is digitally controlled through the switched-resistor network, and the distortion of the switched resistors can be predicted by a closed-form formula. The distortion is heavily dependent on the associated linear resistor, gate overdrive voltage, and the size of the MOS transistor, thus leading to a need of an optimisation method to optimise the circuit performance.

### 2.3.3 Sample and Hold Circuit (SHC)

SHC is used to sample an analog signal and store its value for a finite length of time. SHC is an important building block in DAQ system and other data-converter systems since the system throughput and accuracy are limited by the speed and precision at which the input is sampled and held.

Using a SHC before ADC is highly valuable. Firstly, the SHC will hold the analog sampled-value constant for a certain time as required by most of ADCs. Secondly, the SHC will prevent the harmonic distortion resulting from the nonlinearity of ADC input-capacitance, which arises from a large number of comparators together with the source impedance. Thirdly, it will moderate the input dependent offset from each comparator

offset introduced by the capacitive feedback from the input signal to the resistive ladder. Fourthly, it will reduce the sparks appearing in the thermometer code in each stage of a pipelined ADC due to mismatch in sampling instants of neighbouring comparators [51].

In CMOS technology, traditional switched capacitor techniques take advantage of the excellent properties of MOS capacitors and switches and permit the realisation of numerous analog sampled-data circuits. The simplest SHC, which is reported in [52, 53], is illustrated in Figure 2.3.

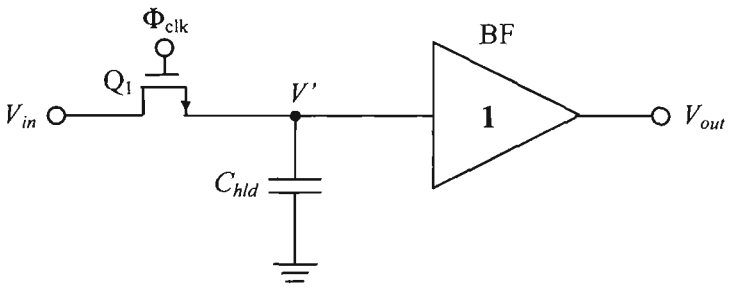



Figure 2.3 Simplest MOS SHC [52, 53].

There are several practical limitations to this circuit that will cause several errors affecting the performance of the SHC. The limitations are: aperture error, signal feedthrough error, droop error, charge injection error and clock feedthrough error. [52-54].

### *2.3.3.1 Alternative CMOS Sample-And-Hold Circuit Approaches*

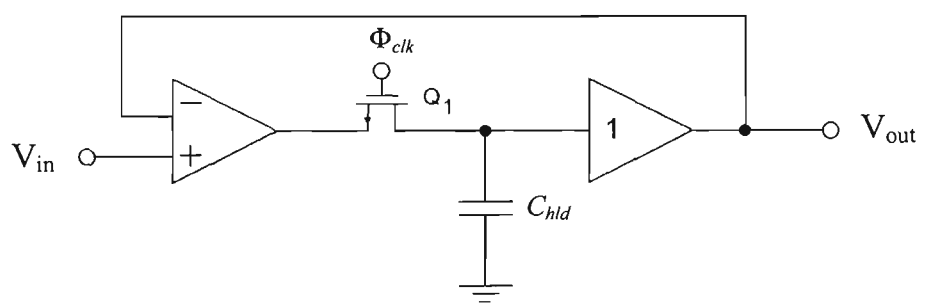
Out of all types of errors, charge injection and clock feedthrough errors are the most critical errors, which limit the SHC performance. Several alternative methods to

implement SHC to compensate these errors have been reported in the literature. These methods will be discussed further in this section.

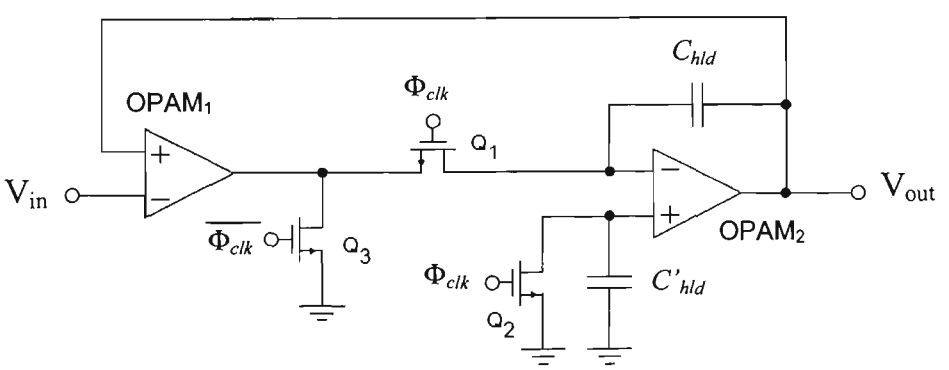
A series sampling technique, which is reported in [55], the sampling capacitor is in series with the signal, thereby isolating the common-mode (CM) level of the input and the output. In addition to isolated input and output CM levels, the charge injected from the switch to the output node is constant, which can be eliminated through differential operation. The series sampling technique, therefore, does not exhibit the charge injection error. However, series sampling suffers from the nonlinearity of the parasitic capacitance at the output, which introduces distortion to the sampled-and-held signal, thus requiring the sampling capacitor to be much larger than the parasitic capacitance [55].

NMOS switches can only pass signals at low voltage levels without degradation. An alternative way to implement the switch is to use a CMOS TG switch comprising of a NMOS and PMOS pair, which is reported in [56, 57]. A CMOS TG switch has an approximately uniform on-resistance and can pass large analog signal swing. Intuitively, a TG switch can help reduce the clock feedthrough due to the opposite clock signals controlling the NMOS and PMOS transistors. However, it is difficult to exactly match the NMOS and PMOS transistors. Another obvious disadvantage of such a simple implementation is that it adds extra load to the previous stage. To reduce the error, the holding capacitance has to be fairly large, resulting in more power consumption [56, 57].

A better SHC with an OPAM in a feedback loop, as illustrated in Figure 2.4a, is reported in [58] and [59]. Using this configuration, the sampling error, resulting from input-dependent charge injection of the sampling switch, is attenuated since the holding capacitance is effectively increased during the transition to hold mode through the action of the Miller feedback. This results in an increase of SHC precision without significantly reducing the circuit sampling speed. In addition, since both sides of the switch are fixed close to ground, the clock rise time and fall time will not cause any sampling jitter. However, this SHC topology suffers from the following disadvantages: the system power consumption and complexity increase due to overall feedback network; the clock feedthrough effect causes an offset error at the output and the system sample time is input signal dependent [58, 59].




(a)




(b)

Figure 2.4 SHC using (a) closed loop configuration; (b) using feedback loop with compensation capacitor.

An improved SHC configuration to eliminate the charge injection and clock feedthrough error, as illustrated in Figure 2.4b, is reported in [60, 61]. In this configuration, the holding capacitor is not connected to ground, but rather is placed in the feedback path of a second OPAM as a Miller capacitor. In addition, a compensation capacitor and supplementary NMOS switch are added to effectively eliminate the clock feedthrough error. In this circuit, the sampling switch is maintained at a virtual ground during the sampling phase. This virtual ground ensures that the charge injection is independent of the input signal, such that the charge injection error is effectively removed. However, the disadvantages of the closed-loop SHC architecture typically include lower speed, limited bandwidth and increased design complexity. Nevertheless, it is recommended the SHC using feedback loop with compensation capacitor should be used in a DAQ system due to its superior high-accuracy characteristic [60, 61].

### 2.3.4 Analog-to-Digital Converter (ADC)

A high-speed ADC is the most essential part in a DAQ system and also several other signal processing systems because it is the boundary between the analog and digital signal processing. The function of an ADC is to transform an analog signal into equivalent digital data for further storage and processing. Currently, many different types of ADC have been reported. The overview of various ADC architectures [18, 62, 63] is discussed in the following sections:

### 2.3.4.1 Sigma-Delta (Σ-Δ) ADC

Sigma-Delta (Σ-Δ) ADC digitises the input analog signal by varying the density of logic '1's in a bit stream of serial data. Σ-Δ ADC is an oversampling device which means that it effectively samples the analog information more often than the minimum sample rate. Therefore, the Σ-Δ ADC is a high accuracy and low cost device, but its speed is quite slow. Σ-Δ ADC has been used widely in industry where better accuracy is required [64].

### 2.3.4.2 Successive approximation (SA) ADC

SA ADC typically comprises of a comparator, a Digital-to-Analog Converter (DAC), a SA Register and a control logic circuit. SA ADC digitises the input signal by processing and deciding to put '1' to each successive output bits. This method has been widely used since it produces reasonably fast conversion rate with low power consumption and small size [18, 33].

### 2.3.4.3 Flash ADC

Flash ADC is the fastest ADC out of all current techniques. Its basic operation is to compare input voltages to certain number of reference voltages to obtain a digital code which is then converted to corresponding digital level [63, 65].

The only source of delay of flash ADC is the delay of comparator and encoding logic. Therefore, the data conversion time could be less than 5ns that allows flash ADC to run at a very high speed. However, flash ADC requires $2^N$-1 comparators to obtain N bit digital output. Due to this large number of comparators required, flash ADC suffers its main disadvantages in very large die size and large power consumption. Another concern with the flash ADC is that it is not feasible to create flash ADC with resolution grater than 10-bit, since it would require too many comparators and a too complex encoder logic circuit [63, 65].

#### *2.3.4.4 Two-step ADC*

In a two-step ADC, two stages (coarse and fine tuning) of flash ADCs are cascaded to reduce the number of comparators needed in a flash ADC without losing accuracy. The input analog signal first is digitised to obtain the $n_1$ coarse bits. These coarse bits then are converted back to analog signal using a DAC in order to subtract the coarse signal from the input signal. The output of the subtractor is then sent to the fine ADC where the last $n_2$ fine bits are generated. The number of comparators, thus, is reduced to $(2^{n1}+2^{n2})$ comparators and hence the power consumption and die size of the two-step ADC would be greatly reduced comparing with the flash ADC. However, the speed of the two-step ADC would also be reduced due to the two-step operation [66, 67].

#### *2.3.4.5 Pipelined ADC*

The pipeline ADC effectively overcomes limitation of flash ADC. It is an extension of two-step ADC in the sense of cascading not only two stages, but several consecutive

stages. Each stage contains a sample/hold (S/H), a low-resolution flash ADC, DAC and an interstate amplifier. First the S/H acquires the analog input signal. The flash ADC then converts the sampled signal to digital data, which is output of the current stage. The digital signal, then, is converted back to analog using DAC and its output is subtracted from the sample signal to obtain the residual signal. The residual signal, then, is amplified and sent to the next stage in the pipeline to be sampled and converted so far. Therefore, pipeline ADC requires only $k \times 2^m$ comparators to provide $m \times k$ bit of resolution. For that reason, pipelined ADCs provide the optimum balance of size, speed, power dissipation and resolution [18, 51, 68].

In conclusion, although there are several different types of ADCs, most of the current published data acquisition systems (DAQ) were designed using $\Sigma$-$\Delta$ ADC [26] and successive approximation ADC [69, 70] due to their advantages in low power consumption, low cost and high resolution. Flash ADC could be used to construct very fast data acquisition systems where power is not really an issue. Nevertheless, in the near future, pipeline ADC will be used largely to implement DAQ systems providing fast sampling speed (up to hundreds of MHz) with low power consumption and complexity.

## 2.4 Power System Protection Application

A power system basically consists of generators, circuit breakers, transformers, transmission and distribution circuits. In such a large network, it is inevitable that some failure (fault) will occur somewhere in the system. A fault is the intentional or

unintentional connecting together of two or more conductors that ordinarily operate with a difference of potential between them. At the fault, the voltage between the two parts is reduced to zero in the case of metal-to-metal contact or to a very low value in case of connection through an arc. Currents of abnormally high magnitude and frequency flow through the network to the point of fault. These short circuit currents will usually be much greater than the designed thermal ability of the conductors in the lines or machines feeding the fault. The resultant rise in the temperature may cause damage by the annealing of conductors. A fault or short circuit may occur due to [71, 72]:

- Deterioration of insulation
- Damage due to unpredictable causes or accidental short circuiting
- Abnormal voltage, such as lighting or switching surges.

The probability of such failures is more on the power transmission lines, because of their greater length and base exposure at atmosphere. For transmission line protection, relays are used to avoid damage to the system and customer equipments. In early development of power systems, protection functions were performed by electro-mechanical relays, which are still in use. Recently, digital relays (microprocessor-based relays) are being increasingly used in power industry due to their advantages namely: digital relays generally use fewer parts, they are not required to be tuned individually to obtain consistent result, they provides remote targets and fault location information to assist operators in restoration of electrical service and system changes can be made simply by changing software [71, 73].

A variety of algorithms have been proposed for processing samples of currents and voltages. Protective relays developed for power system protection [74] describes the possibility of a microprocessor based inverse time overcurrent relay having selectable characteristic which greatly relieves the application difficulties that have been associated with fixed characteristic of electromechanical counterpart.

In recent years, various researchers have applied the concept of multi-function to protective relay [75]. In a digital relay, the input line voltages and currents are sampled and converted by a DAQ section so that a central processor can locate fault location and give decision whether or not to trip the relay. Traditionally, the DAQ section has been built on PCBs with high quality shielding, grounding and insulation, inducing high cost, high power consumption, fixed sampling rate, large data storage and large size. Therefore, there is a need for further DAQ section improvement enabling relays to attain better performance and lower cost.

A Field Programmable Gate Array (FPGA) approach to implement DAQ section in a digital relay is reported in [76]. It can sample and convert the input signals of 16-channel phase voltages and currents at an operating frequency of 8MHz. The DAQ system is implemented in Altera's ACEX EP1K100QC208-3 and utilises 84% of total hardware resources. The work is based on FPGA, which provides multi-function, high reliability, flexibility and a fast design time. However, the FPGA approach suffers high cost, high complexity, high power consumption and low system efficiency.

To reduce the device cost and increase device performance, an improved SOC design of the DAQ system for digital protective relay based on Intellectual Property (IP) cores is reported in [77]. The DAQ design comprises of several IP blocks, including data acquisition control block, data processing block, data distribution block and procedure management block. The implemented system provides many benefits as compared to its counterparts, namely reduced cost and complexity as well as increased performance and the system efficiency. In this work, the line voltages and currents are, however, only processed and analysed in digital domain. The implemented DAQ system does not include any signal conditioning and filtering circuit, resulting in errors due to high frequency harmonics of the line voltages and currents when fault occurs.

## 2.5 Biomedical Application

In the 1960s, computers in medicine began with the processing of hospital's information technology. In late $20^{th}$ century, computerised biomedical screening became popular, and automated analysis of blood and urine was emerging. The microcomputers has literally revolutionised biomedical instrument and control system design. It has allowed the generation of computerised patient monitoring, and it has enabled automation and instant analysis of medical events for modern medical diagnoses and treatments [78, 79].

Biomedical signals are frequently complex waveforms that occur in a very noisy environment. Although the information content and the best way to present this information is under constant study in the medical and research community, advanced

signal processing techniques have proven to be invaluable to the analysis of biomedical signals. With the increased capability of personal computers (PCs), the analysis of biomedical signals is becoming practical at the individual physician level. However, biomedical signals are analog in nature while computers can only read digital signals containing '1's and '0's. A DAQ system is, therefore, inevitably necessary as it will acquire, amplify, filter and digitise the analog signals for further analysis using computers [80].

The most popular biopotential signals typically include electrocardiogram (ECG), electroencephalogram (EEG), electroneurogram (ENG), electromyogram (EMG) and electroretinogram (ERG), which are related to different measuring and analysis processes in biomedical application. Different signal types have different requirements on signal acquisition, and therefore suitable DAQ system should be implemented for each signal type. Detailed information of these signals is presented in Table 2.4 [81-84].

Table 2.4 : Biopotential signal parameters [81].

| **Type of Signal** | **Amplitude Range** | **Max Frequency** | **Standard Sensor or Method** |
|---|---|---|---|
| Electrocardiogram (ECG) | 0.5-8mV | 250 Hz | Heart Function |
| Electroencephalogram (EEG) | 0.01-5mV | 150 Hz | Brain-surface |
| Electroretinogram (ERG) | 0.05-0.7mV | 300 Hz | Eye potential |
| Electroneurogram (ENG) | 0.01-0.5mV | 10 kHz | Nerve Potential |
| Electromyogram (EMG) | 0.1-5mV | 10 kHz | Skeletal muscle motor unit |

A multi-channel PC-based DAQ system for EEG signal is proposed in [85]. The system includes high impedance preamplifiers, differential software-controlled gain amplifiers and digitising control circuitry, compatible to a PC. The system provides sample-and-hold circuitry on all channels and obtains an approximate bandwidth of 1000Hz and a sampling rate up to 2kHz per channel. However, the DAQ system was implemented on PCB, which results in high power consumption and large size.

To reduce system power consumption and cost, a DAQ IC for biomedical application was implemented in [86]. The functionality of the IC provides capturing, processing, sampling and digitising nine analog signals from external sensors for ECG signal. It includes amplifiers, SHC and a 13-bit SA ADC. It provides a maximum sampling speed of 44kS/s. However, in this DAQ system, separate SHC and amplifier, are implemented for each channel, resulting in a high system complexity and high power consumption.

In [87], an alternative approach to implement DAQ system for biomedical by employing a DSP core is reported. The DAQ system has sixteen input channels, each one is linked to an external transducer by a suitable connector. The signals from the transducers are converted into a digital form by a 10-bit ADC, which is integrated into the DSP. The acquisition mode is programmable using a remote PC. This approach has great advantages in flexibility, programmability and ease of use. However, analog conditioning circuits are not implemented in the DAQ system, which limits the device signal range and bandwidth. In addition, the DSP core drastically increases system complexity, size, power consumption and cost, as compared to its IC counterparts.

A DAQ system suitable for ERG, ECG, EEG and surface EMG signals is reported in [88]. The DAQ system employs a Σ-Δ ADC (AD7716) from Analog Devices, resulting in a very high accuracy characteristic. In addition, the high resolution of the Σ-Δ ADC allows ECG or EEG signals to be acquired directly, without the use of instrument amplifiers. However, the low speed characteristic of the Σ-Δ ADC significantly limits the sampling rate of the DAQ system. In addition, the low speed feature induces the need for separate ADCs for each input channel, which significantly increases system complexity.

## 2.6 Conclusion

Literature review highlights that traditional DAQ systems are implemented on PCB units with high quality shielding, grounding and insulation. The major disadvantages of these board-based DAQ systems are high power consumption, large size and high cost. There is an emerging approach of implementing such sophisticated system on a single chip, which provides the necessary high speed, small size, low cost, low power consumption and low complexity. Literature review also illustrates that there has been no report associated with the implementation of a reconfigurable DAQ system.

Literature review on typical constituent components of a DAQ system reveals that there are several topologies to implement each building-block component. Each topology comprises of some advantages and disadvantages. Thus, the DAQ system performance can be greatly improved by selecting, modifying and optimising the device architectures. It is also necessary to propose several new component architectures to

achieve a DAQ system with high performance, high-speed, low power consumption, low complexity and low cost for specific applications.

ADC is the heart of a DAQ system. The fastest ADC available in practice is the flash ADC, involving a conversion time equal to the propagation delay of the comparator and the encoding logic. However, the complexity of the circuit increases exponentially with the increase in the number of bits (resolution), and thus it discourages its feasibility for implementation of a high-resolution ADC. Pipeline ADC overcomes the complexity in the flash topology, and it has become the optimum solution for speed, power consumption and accuracy. However, ADCs are the bottleneck in existing DAQ systems. The need for new architectures allowing ADCs to attain more enhanced performance with reduced power consumption and complexity, therefore, is necessary.

Literature review shows that digital and microprocessor-based relays are increasingly used in power system protection applications. They provide a high level of reliability, security and repeatability, as well as high speed and accuracy. Traditionally, DAQ sections of digital relays have been built on PCBs with high quality shielding, grounding and insulation, inducing high cost, high power consumption and large size. There are new approaches of implementing the DAQ section on FPGA and SoC to increase the system performance as well as reduce the system cost and complexity. However, literature review indicates that a reconfigurable multi-channel DAQ system on a single IC for power system protection relay has not been reported. The reconfigurable DAQ IC should be capable of reconfiguring itself, depending on the operating conditions and the occurrence of a fault on the power system. Such a

reconfigurable DAQ architecture will enable the design of a multi-channel digital relay with more enhanced features and performance.

Biomedical applications of DAQ systems include measuring and detection of a variety of signal types, where each type places a different signal conditioning and sampling requirement at DAQ level. Several DAQ systems have been implemented for biomedical applications but they are limited to low speed, high power consumption and high device complexity. Moreover, biomedical instruments require low power consumption and low complexity to reduce the size and cost of the devices to enable the design of portable biomedical measurement and analysis devices to monitor and/or assist patients outside hospitals. This leads to the need of a universal reconfigurable DAQ system that efficiently monitors and analyses different channels containing different signal types. In addition to these requirements, the system should consume less power and have better performance at a reduced cost.

# Chapter 3

# Design and Implementation of Building Block Components for a DAQ System

## 3.1 Introduction

The general aim of this work is to develop a reconfigurable data acquisition (DAQ) system, which attains low cost, small size, high speed, high efficiency and low complexity for bio-medical and power system protection applications. As highlighted in Chapter 2, a conventional DAQ system contains an analog Multiplexer (MUX), a Programmable Gain Amplifier (PGA), a Sample-and-Hold circuit (SHC) and an Analog-to-Digital converter (ADC).

The focus of this chapter is on the design and implementation of the building block components for a multi-channel DAQ system. The design of each component is aimed

at high-accuracy and high-speed as well as low power dissipation and reduced complexity. The findings in Chapter 2 yielded that anti-aliasing filters had not been usually included in DAQ systems. In this chapter, an anti-aliasing filter using Switched-Capacitor (SC) technique will be designed and implemented to provide a programmable aspect to the proposed DAQ system.

Findings in Chapter 2 also indicated that ADC is the most important component as well as the most power consumptive and area utilising component of a DAQ system. In this chapter, a new modified flash ADC topology will be proposed, enabling better performance and further reduction of the device complexity, cost, area and power consumption. The proposed ADC requires only $(2^{n-2}+2)$ comparators for an n-bit resolution, instead of $(2^{n}-1)$ comparators like a traditional full flash ADC, and hence it enables a great area and power consumption savings.

This chapter is structured as follows: Section 3.2 details the design and implementation of an analog MUX. Details of the design and implementation of an anti-aliasing filter is presented in Section 3.3. Section 3.4 presents the design and implementation of PGA architecture. Design and implementation of SHC will be described in Section 3.5. Section 3.6 is dedicated for the design and in-depth analysis of the modified flash ADC. The implementation of a high performance reduced complexity pipeline ADC employing the new ADC topology is also described in this section. Conclusions of this chapter are presented in Section 3.7.

## 3.2 Analog Multiplexer Design

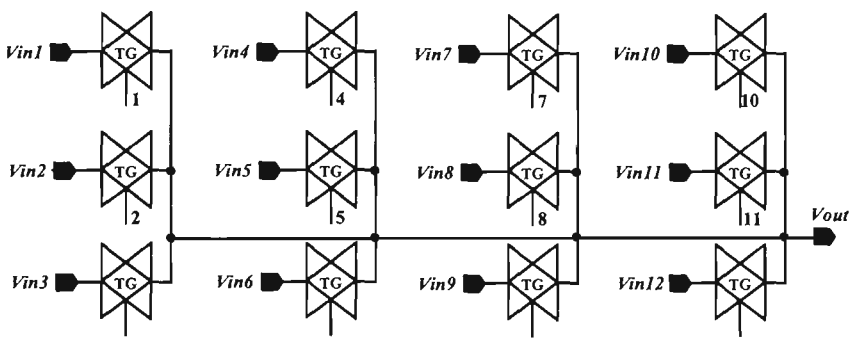
A high-speed, high precision analog MUX is essential for DAQ devices in order to process multiple input signals. An important parameter of an analog MUX is the input analog signal range ($V_S$) over which reasonable accurate switching will take place. For a typical MUX design, $V_S$ will be smaller than voltage span between the voltage supplies. Note that other parameters such as on-resistance ($R_{ON}$) and leakage currents are guaranteed over a smaller input range, and would tend to degrade towards the $V_S$ limits [42].

Delay is another important factor in comparing the structures of analog MUXs. In general, the delay of a MUX consists of two components. One is the delay of the address decoder, which can be reduced by a careful decoder circuit design. The other is the delay of a signal path from any signal input end to the output end of the multiplexer, through analog switches. These analog switches are typically implemented using Complementary Metal-Oxide Semiconductor (CMOS) transmission gate (TG) or Negative-Channel Metal Oxide Semiconductor (NMOS) pass element (PE), therefore we cannot insert any non-analog device or circuit (such as inverters or basic gates) to reduce delay [41].

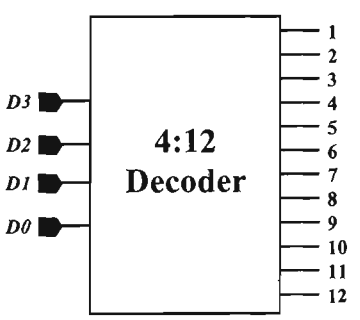
In this design, CMOS TG is chosen to implement the switches due to its superior characteristics over NMOS PE. That is, unlike the NMOS PE, the CMOS TG does not encounter any signal degradation due to the threshold voltage and its related body bias effect. In addition, the CMOS TG has less effect on clock feedthrough than the NMOS

PE. However, the CMOS TG has longer delay than the NMOS PE because it is composed of both NMOS and Positive-Channel Metal Oxide Semiconductor (PMOS) transistors and thus has larger input and output capacitances. Therefore, careful device sizing has been taken into consideration to reduce the effect of resistance-capacitance (RC) delay chain.

For the proposed DAQ system, a 12:1 analog MUX was designed allowing 12 channels to be processed. Its schematic diagram is shown in Figure 3.1, where *Vin1* to *Vin12* are the twelve input signals. Typical analog MUXs employ a heterogeneous-tree structure of switches, which can be partitioned into number of stages, therefore the device delay increases. In this design, there is only one stage of CMOS TG switches from input to output in order to reduce the delay of signal path.




(a)




(b)

Figure 3.1 Schematic diagram of (a) TG switches; (b) address decoder of 12:1 MUX.

The binary control word (*D3D2D1D0*) selects the input channel using the appropriate 4:12 decoder as shown in Table 3.1. The proposed 12:1 MUX has been implemented in Cadence Analog Design Environment (Analog Artist). The performance of the MUX is summarised in Table 3.2.

Table 3.1: Decoder Truth Table for 12:1 analog MUX

| **Input Signals** | | | | **Output Signals** | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **D3** | **D2** | **D1** | **D0** | **1** | **2** | **3** | **4** | **5** | **6** | **7** | **8** | **9** | **10** | **11** | **12** |
| 0 | 0 | 0 | 0 | **1** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 1 | 0 | **1** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 | 0 | **1** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 | 0 | **1** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | **1** | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | 0 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | 0 | 0 | 0 |
| 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **1** | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | **1** |
| 1 | 1 | 0 | 0 | **1** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 1 | **1** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 0 | **1** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | **1** | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

Table 3.2: Performance summary of the 12:1 MUX

| **Property** | **Result** |
|---|---|
| Total Device Delay | 190ps |
| Max Speed per channel | 5GHz |
| Signal Swing | 1V |
| Max Error | 0.5mV<br>(0.05% of 1V FSR) |
| Supply Voltage | 2.5 V |
| Power Consumption | 0.4 mW |
| Technology | 0.18μm CMOS |

## 3.3 Anti-Aliasing Filter Design

Filters are essential in DAQ systems in order to eliminate frequency components at or higher than half the sampling frequency (Nyquist criterion) to maintain the integrity of sampled signals. SC techniques have demonstrated an enormous potentiality for the monolithic implementation of anti-aliasing filters. One of the most attractive features of SC circuits is programmability. This feature is very desirable in many systems, especially in those applications where the specifications are either not well known in advance or time dependent [89].

The anti-aliasing filter employed within the DAQ system is based on an improvement/modification to the anti-aliasing filter presented in Figure 3.2 [90]. Before analysing the modified anti-aliasing filter, illustrated in Figure 3.3, the anti-aliasing filter of Figure 3.2 must first be analysed.

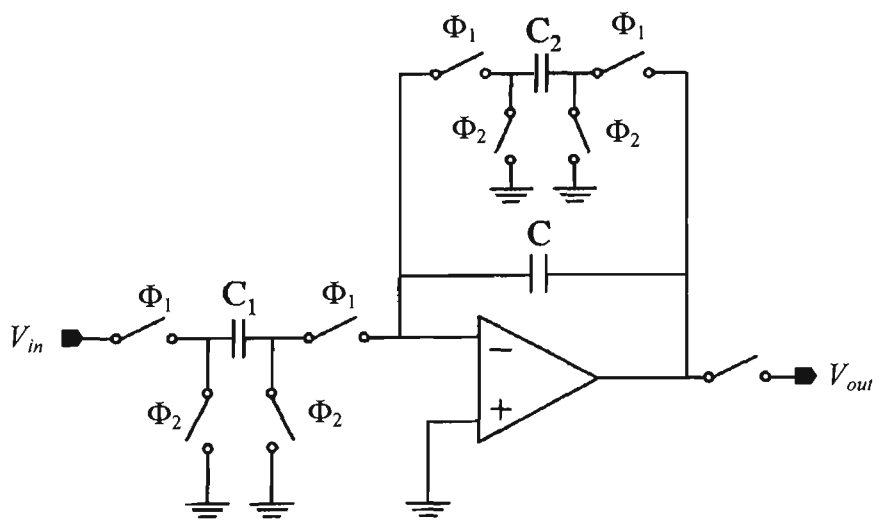



Figure 3.2 Schematic Diagram of a Basic SC anti-aliasing filter [90].

The anti-aliasing filter architecture in Figure 3.2 employs an inverting integrator. It utilises a non-overlaping control signals $\Phi_1$ and $\Phi_2$. The z-domain transfer function of the anti-aliasing filter is given by equation (3.1). The major disadvantage with this SC filter is the large offset error and limited gain inducing low accuracy.

$$H(z) = \frac{A_1 z}{A_2 z - 1} \tag{3.1}$$

where coefficients $A_1$ and $A_2$ and are equal to $-C_1/C$ and $(C+C_2)/C$ respectively.

The SC anti-aliasing filter employed within the DAQ system is shown in Figure 3.3 [90]. It achieves an increase in the device gain, accuracy and stability. It comprises of both an inverting integrator and a non-inverting integrator. The transfer function of the filter is described in equation (3.2). In this design, capacitors ($C_1$ and $C_6$) compensate the offset voltage and DC gain error of the operational amplifiers (OPAMs) $A_1$ and $A_2$ respectively, and capacitor $C_5$ eliminates spikes (providing continuous feedback to the first OPAM).

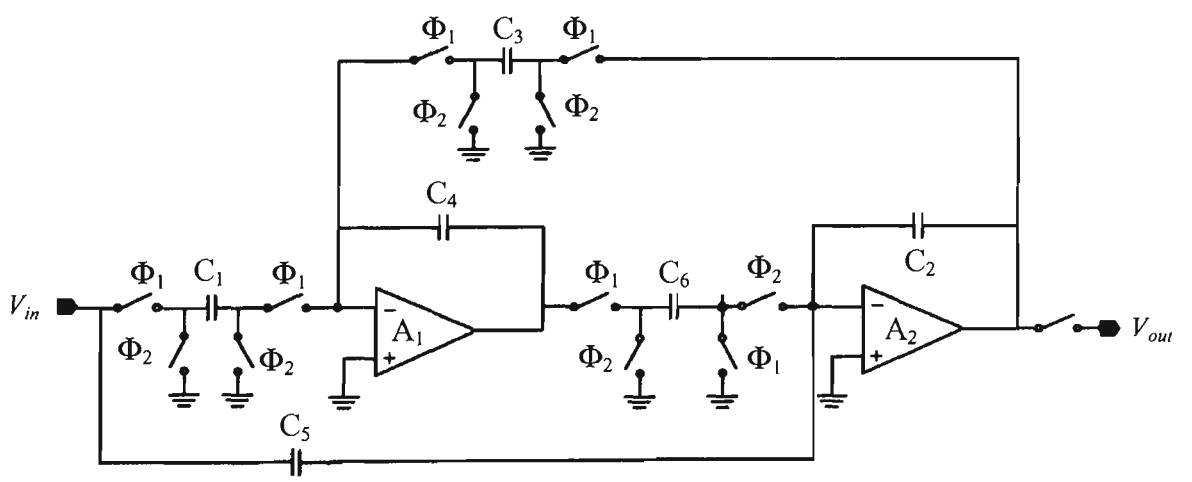



Figure 3.3 Schematic Diagram of a modified SC anti-aliasing Filter [90].

$$H(z) = \frac{N_1.z + N_0}{z^2 + D_1.z + D_0} \tag{3.2}$$

where $N_1 = (C_4\text{-}C_1C_6)/(C_4C_2+C_4C_5)$, $N_0 = C_4/(C_4C_2+C_4C_5)$.

$D_1 = (C_4C_2+C_4C_5+C_4C_2)/(C_4C_2+C_4C_5)$, $D_0 = (C_2+C_4)/(C_2+C_5)$.

Another advantage of this circuit as compared to the circuit of Figure 3.2 is that the frequency positions of the complex conjugate pole pairs of the corresponding integrators are modified by means of $\Phi_1$ and $\Phi_2$ so that it is possible to guarantee the stability of the SC circuit. The circuit has been implemented and tested using Cadence Analog Design Environment. The performance analysis results of the SC anti-aliasing filter employed within the designed DAQ chip are shown in Table 3.3.

Table 3.3: Performance summary of the anti-aliasing Filter.

| Property | Result |
|---|---|
| Signal Swing | 1V |
| Supply Voltage | 2.5 V |
| Power Consumption | 9.5 mW |
| Frequency tuning range | 0.2kHz – 1MHz |
| Passband ripple | 0.2dB |
| Stopband Rejection level | -60dB |
| Technology | 0.18μm CMOS |

## 3.4 Programmable Gain Amplifier Design

PGA is a critical function block in DAQ systems. It is used for adjusting the amplitude of input signal to match the input range of the on chip ADC to maintain overall system linearity. The PGA employed within the DAQ system is illustrated in Figure 3.4. It

employs linear resistors in the feedback network to achieve high linearity. The voltage gain can be adjusted by changing the ratios of $R_f/R_{eq}$. A voltage-mode operational amplifier is typically employed in the conventional PGA design. Thus, whenever the values of $R_f/R_{eq}$ changes, the PGA's frequency bandwidth and the total harmonic distortion (THD) also change accordingly, due to the variation of the feedback factor. The designed PGA architecture uses a current-mode OPAM, $\mathbf{A_m}$, with constant feedback resistance of $R_f$, to maintain a high linearity. The variation of the distortion of the PGA is small regardless of the change of resistance $R_{eq}$. This makes the distortion insensitive to the gain change [50].

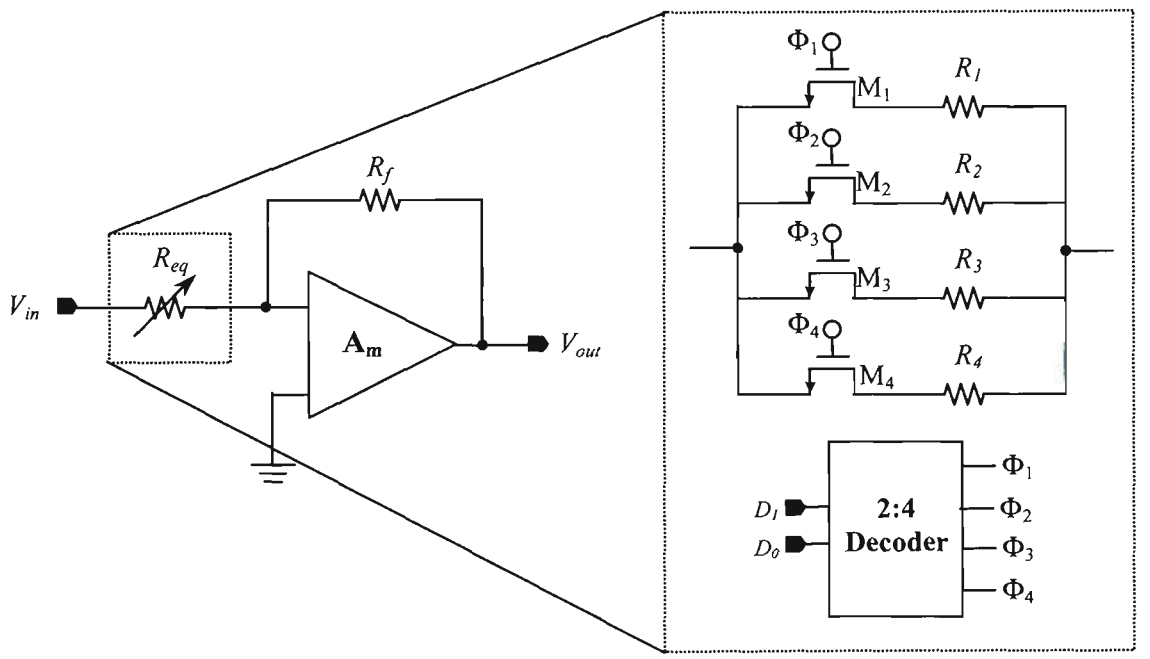



Figure 3.4 Schematic diagram of the PGA

The PGA voltage gain can be varied by changing the equivalent resistance $R_{eq}$, which is controlled by a digital code word ($D_1D_0$). As shown in Figure 3.4, the resistor $R_{eq}$ is realised using linear resistors in series with NMOS switches biased in the triode region.

However, the nonlinearity of a Metal Oxide Semiconductor (MOS) transistor can introduce harmonic or intermodulation distortions, and degrade the linearity of the entire circuit. A proper design of the transistor dimension to minimise PGA distortion is essential. Consider the switches $M_1$ to $M_4$ and resistors $R_1$ to $R_4$, they can be lumped into an equivalent resistor in a series with an equivalent transistor. The drain current, $I_D$, of the equivalent transistor can be expressed as [50]:

$$I_D = \frac{\mu_{eff} C_{ox} W_{EQ}}{L_{EQ}} \left[ \left( V_{GS} - V_{FB} - E_0 - \gamma\sqrt{E_0 + V_{SB}} \right) V_{DS} - \frac{1}{2}\left( 1 + \frac{\gamma}{2\sqrt{E_0 + V_{SB}}} \right) V_{DS}^2 + \frac{1}{24}\left( \frac{\gamma}{2\sqrt{(E_0 + V_{SB})^3}} \right) V_{DS}^3 \right] \quad (3.3)$$

$$\mu_{eff} = \mu_E \left[ 1 - \frac{1}{2(L_{EQ}.\varepsilon_C)^2} V_{DS} \right] \quad (3.4)$$

where: $\mu_{eff}$ is the effective surface mobility, $C_{ox}$ is the gate oxide capacitance per unit area, $W_{EQ}$ and $L_{EQ}$ are the transistor width and length respectively, $V_{FB}$ is the flat-band voltage, $V_{GS}$ is the gate-to-source voltage, $V_{DS}$ is the drain-to-source voltage, $V_{SB}$ is the source-to-body voltage, $\gamma$ is the body-effect factor, and $E_0$ is the surface potential, $\mu_E$ is the surface mobility under the effect of vertical electrical field, and $\varepsilon_C$ is the critical electric field.

When the MOS transistor is in the "ON" mode. Input voltage $V_{in}$ is converted into nonlinear current $I_{in}$ flowing into the current-mode amplifier of the PGA. In this weakly nonlinear network, THD is expressed as [50]:

$$THD = \frac{V_{in}}{2R_{eq}^2 \beta^2 V_{ov}^3} \left[ 1 - \frac{V_{in}(R_{eq} - R_{DS})}{2R_{eq}^2 . \beta . V_{ov}^2} \right] \left[ \frac{1}{2} + \frac{\gamma}{4\sqrt{E_0 + V_{SB}}} \right] + \frac{V_{in}^2}{4R_{eq}^3 \beta^3 V_{ov}^4} \left[ \frac{V_{ov}}{2(L_{EQ}.\varepsilon_c)^2} - \frac{\gamma}{24\sqrt{(E_0 + V_{SB})^2}} \right]^2 \quad (3.5)$$

where $\beta = \mu_{eff} C_{ox} W_{EQ}/L_{EQ}$, $V_{ov} = g_{ds}/\beta$ is the gate overdrive voltage, $R_{DS}$ is the NMOS switch drain-to-source resistance.

The THD, thus, decreases significantly as $R_{eq}$, $\beta$, and $V_{ov}$ increase. In addition, the effective mobility ($\mu_{eff}$) of the NMOS switch is dependent on the switch drain-to-source voltage ($V_{DS}$) and channel electric field, as illustrated in equation (3.5). Increasing $V_{DS}$ will cause a reduction of $\mu_{eff}$, which causes the distortion in the switched resistor, and thus increases the THD of the PGA. The NMOS switch with wider channel width obviously exhibits better linearity for a given channel length and $R_{eq}$. However, the associated larger gate capacitance and parasitic capacitance can degrade the stability and settling time of the PGA. As a result, to minimise the THD of the PGA and to obtain an optimum PGA performance, the NMOS switch size can be calculated approximately as [50]:

$$\frac{W_{EQ}}{L_{EQ}} \approx \frac{1}{\mu_E} \sqrt[3]{\frac{V_{in}^2.(R_{eq} - R_{DS})}{8.THD.R_{EQ}^4.V_{ov}^5}} \tag{3.6}$$

With properly sizing all MOS switches, the PGA can achieve constant bandwidth, high linearity, and optimal power dissipation. The PGA voltage gain is digitally controlled through the switched-resistor network, and the distortion of the switched resistors has been minimised. The performance results of the proposed PGA are shown in Table 3.4.

Table 3.4: Performance summary of the PGA.

| **Property** | **Result** |
|---|---|
| Bandwidth | 10MHz |
| Signal Swing | 1V |
| Supply Voltage | 2.5 V |
| Power Consumption | 6.8 mW |
| THD (0.1V-pp input @ 1MHz) | -80dB |
| Gain | 1, 5, 10, 20 |
| Technology | 0.18μm CMOS |

## 3.5 Sample-and-Hold Circuit (SHC)

SHC plays a crucial role in the design of DAQ systems since the system throughput and accuracy are limited by the speed and precision at which the input signal is sampled and held. In CMOS technology, traditional switched capacitor techniques take advantage of the excellent properties of MOS capacitors and switches and permit the realisation of the basic SHC as shown in Figure 3.5.

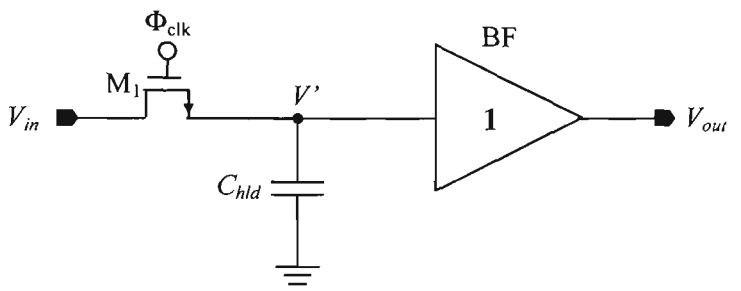



Figure 3.5 Basic MOS SHC.

There are several practical limitations to this circuit that will cause several major types of errors affecting the performance of the SHC. Charge injection and clock feedthrough errors are the most critical errors, which limit the conventional SHC performance. An alternative way to implement the switch is to use CMOS TG, as illustrated in Figure 3.6. This increases the device accuracy.

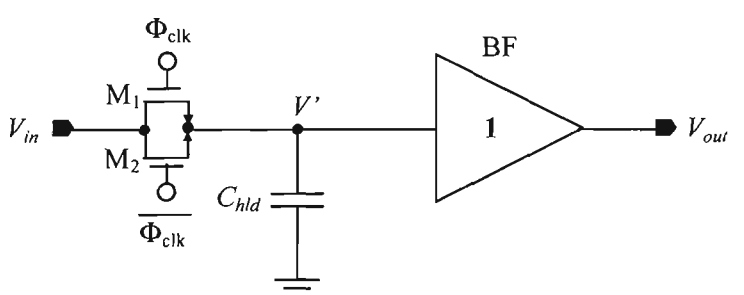



Figure 3.6 SHC with CMOS TG.

In this design, the contrary clock feedthrough effects caused by the PMOS transistor ($M_1$) and NMOS transistor ($M_2$) will eliminate the device overall clock feedthrough error. However, in reality, it is very hard to match p- and n-type transistors. The most effective technique to remove the charge injection and clock feedthrough error is to use feedback loop SHC with a compensation capacitor, which is illustrated in Figure 3.7 [60].

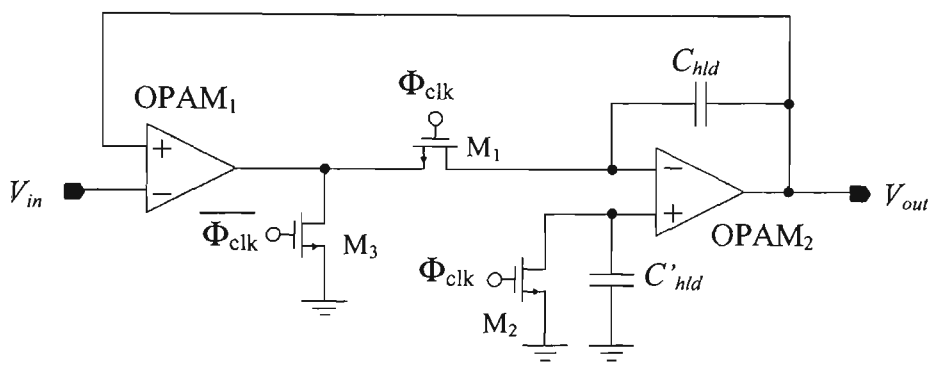



Figure 3.7 SHC using feedback loop with compensation capacitor.

The closed loop architecture employs the series sampling technique, and the output is fedback to the first OPAM. In this circuit, the sampling switch $M_1$ is maintained at a virtual ground during the sampling phase. This virtual ground ensures that the charge injection is independent of the input signal, such that the charge injection error is effectively removed [60]. In this architecture, a supplementary NMOS switch $M_2$, identical to $M_1$, and a compensation capacitor $C'_{hld}$, identical to $C_{hld}$, are added to eliminate the clock feedthrough error. The clock feedthrough error induced by the $M_1$ to the holding capacitor $C_{hld}$ is completely cancelled by the offset voltage induced by the $M_2$ to the compensation capacitor $C'_{hld}$.

Three SHC architectures, namely basic SHC, SHC using TG and SHC using feedback loop, have been implemented. The performance results of the three SHC approaches are presented in Table 3.5 with a 1V peak-to-peak sine wave applied to the three SHC inputs. For comparison purposes, the three SHCs were operated at a speed of 330MHz and 2.5V power supply.

Table 3.5: Performance Comparison results of the three SHC architectures.

| **Property** | **Basic SHC** | **Using TG** | **Using feedback loop** |
|---|---|---|---|
| Max Error | 20mV | 3.5 mV | 1mV |
| Max delay | 1.1ns | 1.4n | 950ps |
| Signal swing | 1V | 1V | 1V |
| Operating Frequency | 330MHz | 330MHz | 330MHz |
| Power consumption @330MHz | 1.05 mW | 1.86 mW | 5.67 mW |
| Max sampling rate | 450MHz | 360MHz | 530MHz |
| Technology | 0.18μm CMOS | 0.18μm CMOS | 0.18μm CMOS |
| Voltage Supply | 2.5V | 2.5V | 2.5V |

From the recorded results, it is observed that the SHC using feedback loop is the most accurate technique as compared to its counterparts. Results indicate that the error of the SHC using feedback loop is reduced by 95% comparing to the basic SHC, therefore an increase of accuracy of 95% is available. It also achieves an increase of accuracy of 71% comparing to the SHC using TG. Being able to be operated at maximum frequency of 530MHz, the SHC using feedback loop attains an increase of maximum speed by 15% and 32% comparing to the basic SHC and the SHC using TG respectively.

## 3.6 Analog to Digital Converter Design

Out of all existing ADC architectures, pipeline ADC is an optimum choice due to its small size, low power consumption, and low complexity along with very high resolution at reasonably fast sampling speed. Typically, pipeline ADC consists of numerous consecutive stages, each stage employs a low-resolution flash ADC to provide the coarse digital bits. However, such flash ADC suffers from high device power consumption and complexity. In this section a novel modified flash ADC architecture, which will be discussed in detail in Section 3.6.2, is proposed instead of the traditional flash ADC to reduce design complexity, and power consumption. The new ADC architecture employs a new high-speed high accuracy optimised CMOS comparator, which is discussed in Section 3.6.1.

### 3.6.1 Proposed Comparator Circuit

In any ADC, a comparator is the most critical component because its accuracy and speed determine the ADC overall performance. This section describes the design and in-depth analysis of an optimised latch-type comparator using CMOS technology. The latched-type comparator offers three main advantages, namely high speed, small device size and no static power dissipation. However, the offset error of the latch-type comparator is typically large. In this section, an optimisation method is proposed to minimise the offset error.

### 3.6.1.1 Comparator Design

This section describes the design of a latch-type comparator using CMOS technology. The schematic diagram of the proposed comparator is shown in Figure 3.8. It consists of a CMOS latch circuit and an S-R latch circuit.

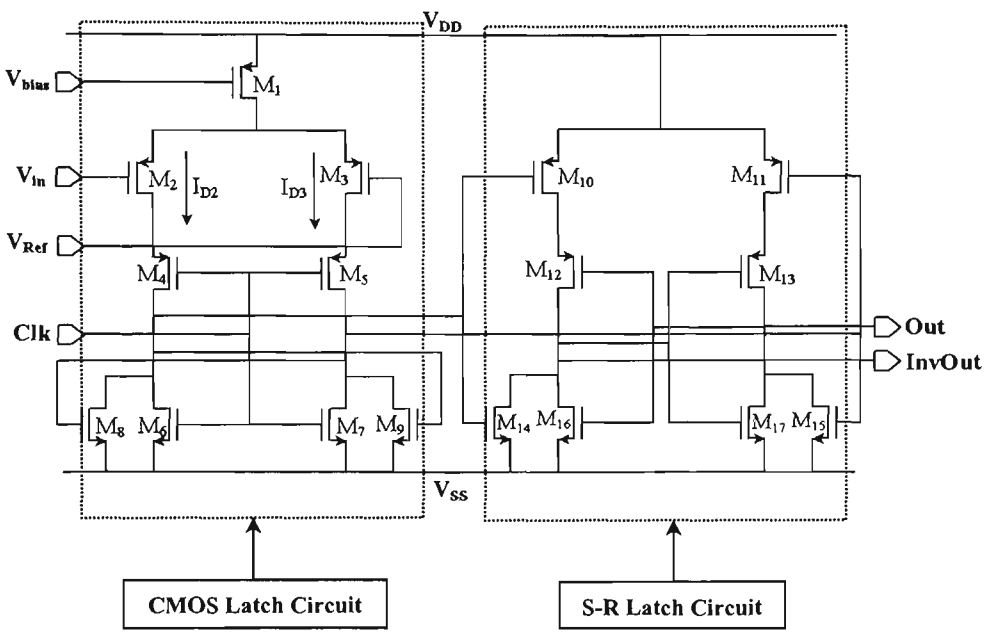



Figure 3.8 Schematic diagram of the comparator

The CMOS latch circuit consists of a differential pair using PMOS ($M_1$ to $M_3$) and a cross-coupled circuit using NMOS transistors ($M_8$, $M_9$). The roles of PMOS switch transistors ($M_4$, $M_5$) and NMOS switch transistors ($M_6$, $M_7$) are to isolate the differential pair and the cross-coupled pair and to discharge the drains of $M_8$ and $M_9$ to ground to hold the output of S-R latch circuit during the re-charge mode. The S-R latch circuit ($M_{10}$ to $M_{17}$) basically holds the outputs of the comparator when the comparator is in recharge-mode.

A Bipolar Complementary Metal-Oxide Semiconductor (BiCMOS) latched comparator has been presented in [91]. The main advantages of this CMOS comparator, illustrated in Figure 3.8, over the previous BiCMOS comparator are:

- The differential pair has been merged with regeneration cross-coupled circuit to provide smaller circuit size (less device count) with better performance.
- The comparator was designed using fully CMOS technology, which produces very small leakage current when the comparator is in re-charge mode.
- The differential pair directly controls the currents feeding to the regeneration state, which will give the ability to optimise the transistor W/L ratios to obtain optimum performance.

Considering the circuit in Figure 3.8, in re-charge mode (when the clock signal is high), the differential pair and cross-coupled circuit are isolated. The drains of the NMOS transistors are pulled to ground while the drain gates of PMOS transistors are pulled to $V_{DD}$. When the clock signal goes low, $M_1$ acts as a current source providing current $I_D$, which is given by:

$$I_D = \frac{k'}{2}\frac{W}{L}(V_{bias} - V_{DD} - V_T)^2 \tag{3.7}$$

where: $k' = \mu_P C_{ox}$ is the transconductance parameter, $C_{ox}$ is the gate oxide capacitance per unit area, $W$ and $L$ are the transistor width and length respectively, $V_{DD}$ is the supply voltage, $V_T$ is the threshold voltage of $M_1$, $V_{bias}$ is the bias voltage of $M_1$.

The voltage difference between $V_{in}$ and $V_{Ref,}$ will induce difference currents $I_{D2}$ and $I_{D3}$ flowing in two perfectly matched PMOS transistors ($M_2$ and $M_3$) given by:

$$I_{D2} = \frac{I_D}{2} + \frac{k}{4}\frac{W}{L}\Delta V\sqrt{\frac{4I_D}{k(W/L)} - \Delta V^2} \tag{3.8}$$

$$I_{D3} = \frac{I_D}{2} - \frac{k}{4}\frac{W}{L}\Delta V\sqrt{\frac{4I_D}{k(W/L)} - \Delta V^2} \tag{3.9}$$

where: $\Delta V = V_{in}-V_{Ref}$.

The difference of these currents ($I_{D2}$ and $I_{D3}$) creates the regeneration process of the two bottom NMOS transistors ($M_8$ and $M_9$). We consider the regeneration section of the comparator as in Figure 3.9. The principle of regeneration process can be described as follows:

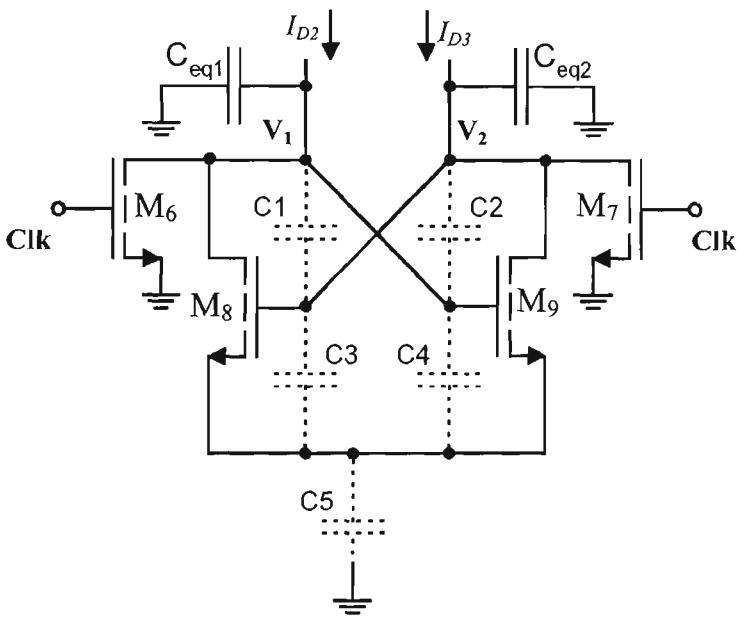



Figure 3.9 Cross-coupled pair of the comparator.

The capacitors $C_1$ to $C_5$ are lumped into $C_{eq1}$ and $C_{eq2}$. This approximation is valid because grounded capacitances have dominant values and one can represent the much smaller coupling capacitances due to the Miller effect as grounded capacitors. These coupling capacitances have no effect on accuracy of comparison since the Miller effect

enhancement takes place only during the latch up process, which occurs when currents are already compared [92].

The input currents initially charge input capacitances $C_{eq1}$ and $C_{eq2}$ while transistors $M_6$ and $M_7$ are turned off. The rising of gate voltage of $M_8$ and $M_9$ will increase the drain current. The regenerative action starts when the closed-loop gain through transistors $M_8$ and $M_9$ becomes greater than one, i.e.:

$$g_{m8}R_{L8}g_{m9}R_{L9} > 1 \tag{3.10}$$

where $g_{m8}$ and $g_{m9}$ are the transconductances of transistors $M_8$ and $M_9$ respectively, $R_{L8}$ and $R_{L9}$ are load resistances of transistors $M_8$ and $M_9$ respectively.

This occurs when both of the transistors are in deep subthreshold region and the regenerative action starts when [92]:

$$\frac{I_{DM8}I_{DM9}}{I_{D2}I_{D3}} > (\lambda\eta V_t)^2 \approx 3\times10^{-6} \tag{3.11}$$

where $I_{DM8}$ and $I_{DM9}$ are the drain currents of transistors $M_8$ and $M_9$ respectively. $I_{D2}$ and $I_{D3}$ are determined from equation (3.8) and (3.9) respectively.

Suppose that $V_{in} > V_{Ref}$ then $I_{D2} < I_{D3}$, so $V_2$ will rise faster than $V_1$. Due to the regenerative action, increasing $V_2$ will further decrease $V_1$. When $V_2 > V_1+V_T$, where $V_T$ is the NMOS transistor threshold voltage, the NMOS transistor $M_8$ will go into

saturation mode, and will pull voltage $V_1$ to ground. This will cause the NMOS transistor $M_9$ to be cut-off, and pull $V_2$ to $V_{DD}$.

Figure 3.10 shows the regeneration process. Note that the regenerative action starts when transistors are operating in a subthreshold conduction mode. After that, it will take some time for parasitic capacitances on the rejected branch (with larger input current) to be charged up to high logic level. This undesirable effect does not affect comparison accuracy but leads to longer time to reach the steady state [92].

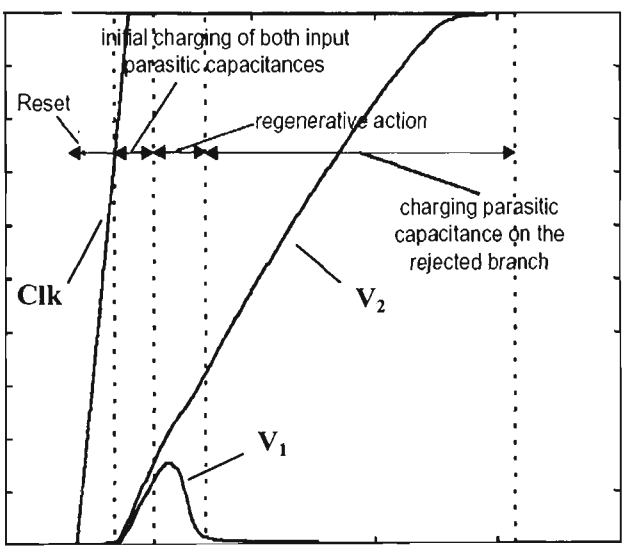



Figure 3.10 Regeneration process diagram [92]

### *3.6.1.2 Optimisation of the Comparator*

The proposed comparator offers three main advantages, namely small circuit size, high speed and low power dissipation. However, the main disadvantage of this circuit type is that its offset error is typically large. When $V_{in}$ is approximately equal $V_{Ref}$, the

currents, $I_{D2}$ and $I_{D3}$, are roughly equal, inducing longer time for the voltage difference between $V_1$ and $V_2$ to reach the threshold voltage to saturate either $M_8$ or $M_9$.

The offset error of the comparator can be minimised by optimising the width and length (W/L) ratios of the PMOS and NMOS transistors. As observed in Figure 3.10, the regeneration process consists of main four actions: the reset action (two switching transistor $M_6$ and $M_7$ are turning off), the initial charging of both input capacitances $C_{eq1}$ and $C_{eq2}$, the regenerative action and the charging of the parasitic capacitances on the rejected branch. Among these four actions, the delay times of the initial charging of both input capacitances $C_{eq1}$ and $C_{eq2}$ and the charging of the parasitic capacitances on the rejected branch can be reduced by optimising PMOS transistors of the differential pair. This will provide large enough $I_{D1}$ and $\Delta I$ ($\Delta I = I_{D2} - I_{D3}$) to speed up the initial charging and the parasitic capacitance charging to high logic level. The delay times of the reset action and the regenerative action can be reduced by optimising NMOS transistors of the regeneration circuit.

#### *3.6.1.2.1 Optimisation of the PMOS differential pair*

The difference between input currents of the regeneration stage can be deduced from equations (3.8) and (3.9) as:

$$\Delta I = I_{D2} - I_{D3} = \frac{k}{2}\frac{W}{L}\Delta V\sqrt{\frac{4I_D}{k(W/L)} - \Delta V^2} \tag{3.12}$$

Figure 3.11 presents the offset voltage versus the W/L ratio of the PMOS transistors in the differential pair at 500MHz sampling frequency. Increasing W/L ratios of the

PMOS transistors of the differential pair will produce larger $\Delta I$ to saturate either $M_8$ or $M_9$ for a smaller difference between $V_{in}$ and $V_{Ref}$ and hence the offset error will be reduced. Increasing W/L of $M_1$ will also reduce the time required to charge up the rejected branch.

However, if W/L ratios of the transistors are too large, it will produce too large current $I_{D2}$ and $I_{D3}$ that will make $V_1$ and $V_2$ to reach high logic level to disable the S-R latch before the regeneration appears. This will cause the increase of voltage offset to maintain the proper function of the comparator. Thus, the offset error first decreases as the W/L ratios are increased, and then it increases as the W/L ratios are further increased. The optimised W/L ratios of the PMOS transistors, $(W/L)_1 = 5.6$ and $(W/L)_2 = (W/L)_3 = 2.94$, are obtained when the comparator offset error is at its minimum value.

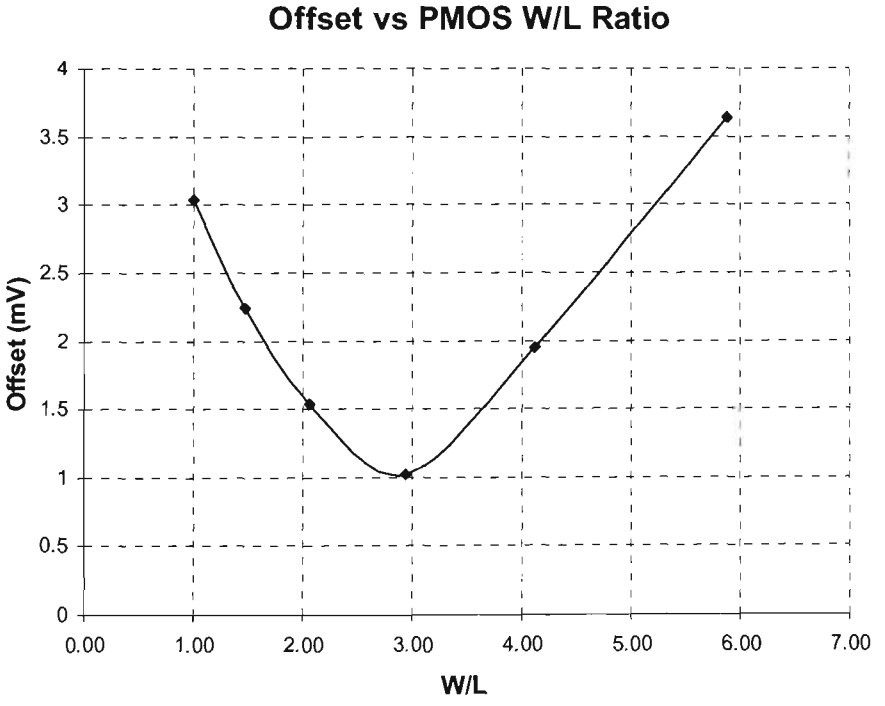



Figure 3.11 Optimisation of the PMOS differential pair

### 3.6.1.2.2 Optimisation of the NMOS regeneration circuit

The switching frequency of NMOS transistor is given by [93]:

$$f_T = \frac{1}{2\pi} \times \frac{I_D}{V_T} \times \frac{1}{WLC_{js}} \tag{3.13}$$

where $C_{js}$ is the capacitance per unit area of the depletion region under the channel and $I_D$ is the NMOS transistor drain current.

Alternatively the switching time of the transistor is given as follows [93]:

$$T_T = \frac{1}{f_T} = 2\pi \frac{V_T WLC_{js}}{I_D} \tag{3.14}$$

Reduction of the widths and lengths of $M_6$ and $M_7$ will produce a smaller switching time. However, their widths and lengths will be limited by the technology used.

For the cross-coupled pair, the drain current of the NMOS transistor in subthreshold region (while the regeneration action occurs) is given by [93]:

$$I_D = \frac{W}{L} qXD_n n_{po} e^{k+\frac{V_t}{n}} e^{\frac{V_{GS}-V_T}{nV_t}} \left[ 1 - e^{\frac{V_{DS}}{V_t}} \right] \tag{3.15}$$

where $q$ is the electron charge, $X$ is the depletion layer width, $D_n$ is the diffusion constant for electrons, $n_{po}$ is the equilibrium concentration of electrons in the substrate, $V_{GS}$ is the gate-to-source voltage, $V_{DS}$ is the drain-to-source voltage, $V_T$ is the transistor threshold voltage, $V_t = kT/q$ is the thermal voltage, $k$ is the Boltzman constant and $T$ is the absolute temperature.

Increasing W/L ratios of NMOS transistors will produce larger drain currents and thus the regeneration process will start faster as stated in equation (3.11). However, too large drain current will discharge the two branches too quickly, which will cause the increase of offset voltage to maintain a proper regeneration process. Figure 3.12 shows a plot of the offset voltage as a function of W/L ratios of the NMOS transistors in regeneration circuit at 500MHz sampling frequency. The comparator offset error reduces as the widths and lengths of $M_6$ and $M_7$ are decreased. When we increase W/L ratios of $M_8$ and $M_9$, the error first decreases, and then it increases as the W/L ratios are further increased. The minimum offset error is obtained when W/L ratios of the NMOS transistors are $(W/L)_6 = (W/L)_7 = 1.24$ and $(W/L)_8 = (W/L)_9 = 2.18$.

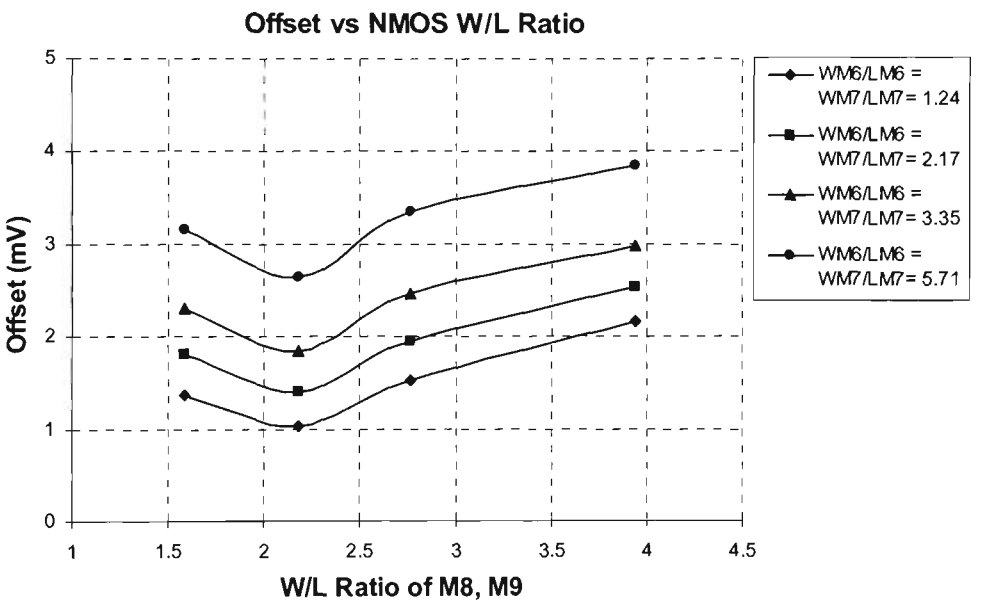



Figure 3.12 Optimisation of the NMOS regeneration circuit

### *3.6.1.2.3 Optimisation of S-R Latch circuit*

The S-R latch circuit holds the outputs of the comparator when the comparator is in recharge-mode. Hence, the data must be ready at the outputs of the S-R latch circuit before the comparator changes to re-charge mode. Therefore, the larger the delay time

of the S-R latch the less time left for the generation process in a half clock cycle. The optimisation of S-R latch circuit involves minimising the widths and lengths of n-type and p-type transistors while trying to balance the rise and fall time of the output signals.

The comparator accuracy, therefore, mainly depends on the proper configuration of the PMOS differential pairs and NMOS regeneration circuit. Figure 3.13 shows a plot of the offset voltage versus the W/L ratios of the PMOS transistors ($M_2$, $M_3$) and the NMOS transistors ($M_6$ to $M_9$) at 500MHz sampling frequency. It can be seen that the optimum combination of the W/L ratios of the MOS transistors provides the smallest comparator offset error enabling proposed comparator to achieve a 10-bit resolution.

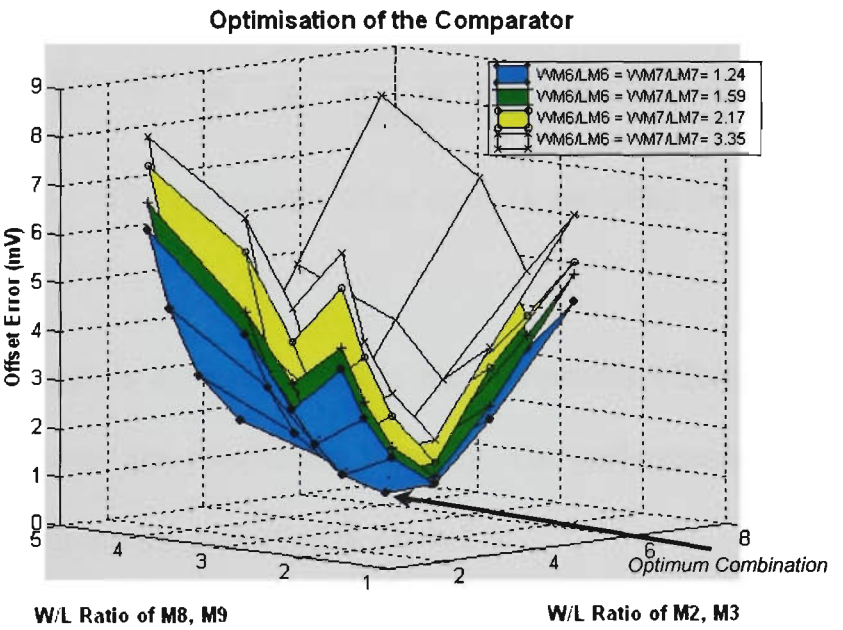



Figure 3.13 Optimisation of the proposed comparator circuit.

### *3.6.1.2.4 Offset error versus sampling frequency*

Optimising the widths and lengths of MOS transistors will minimise the comparator offset error at a given sampling frequency. However, the offset error will also depend

on the sampling frequency. Figure 3.14 shows a plot of the comparator offset error as a function of sampling frequency. Longer period (i.e. lower sampling frequency) will give more time for difference voltage between $V_1$ and $V_2$, as illustrated in Figure 3.9, to reach the level to saturate either $M_8$ or $M_9$, hence the offset error will be smaller.

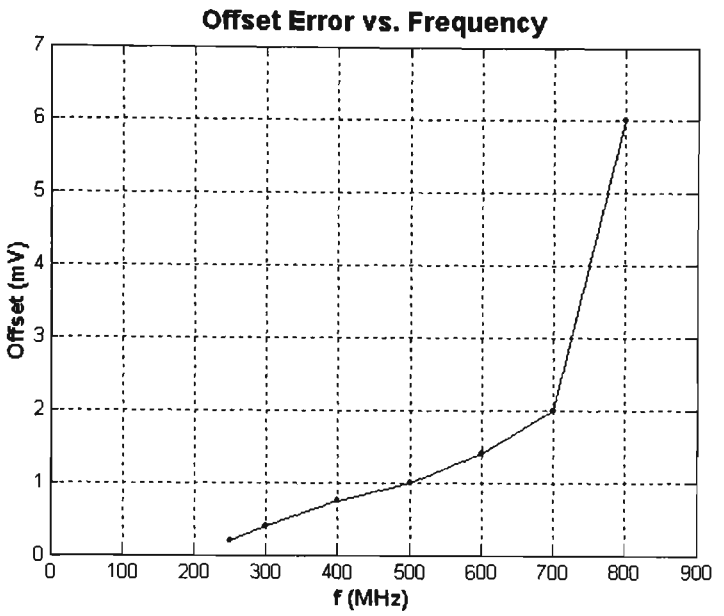



Figure 3.14 The comparator offset error vs. sampling frequency

The proposed optimisation approach reduces the comparator offset error and hence correspondingly increases the comparator accuracy. The performance analysis results of the proposed comparator are presented in Table 3.6.

Table 3.6: Proposed Comparator Circuit Performance

| **Device Performance** | **Performance Value** |
|---|---|
| Max sampling speed (10-bit resolution) | 500MS/s |
| Signal swing | 1 V |
| Resolution | 10-bit |
| Supply voltage | 2.5V |
| Power consumption @500MS/s | 271.6 μW |
| Max offset error @500MS/s | 1mV |
| Technology | 0.18μm CMOS |

## 3.6.2 Modified Flash ADC Architecture

Flash ADCs are very fast with typical sampling speed ranging from 20 MS/s to 800 MS/s, with 6 to 8-bit resolution. The major disadvantages of the full flash ADC architectures are large size, high device power consumption, high device complexity and high device input capacitance (12 to 30 pF). Also, it is practically very difficult to implement high resolution (beyond 8 bit) flash ADC due to a very large number of comparator required [51].

When speed is the first priority in the design of an ADC, flash topology ADC is considered as first choice, but when we add the complexity of the flash ADC, we are forced to compromise between performance and complexity. A modified flash architecture is, therefore, proposed to reduce the design complexity, size and power dissipation while maintaining a high sampling speed.

### *3.6.2.1 Modified Flash ADC Design*

The following steps are followed to design the proposed 4-bit modified flash ADC:

(i) Start with 6 comparators and label them in ascending order, as shown in Figure 3.15. The analog input voltage $V_{in}$ is connected to the non-inverting inputs of all the comparators and the inverting inputs of the first three comparators ($comp_1$, $comp_2$ and $comp_3$) are set to $8V_{Ref}/16$, $4V_{Ref}/16$ and $12V_{Ref}/16$ respectively.

(ii) The outputs of these 3 comparators are used to control the switches (MUXs), which are connected to the appropriate fractions of the reference voltage, $V_{Ref}$.

(iii) The outputs of the comparators ($comp_4$, $comp_5$, $comp_6$) are encoded to appropriate values as presented in Table 3.7.

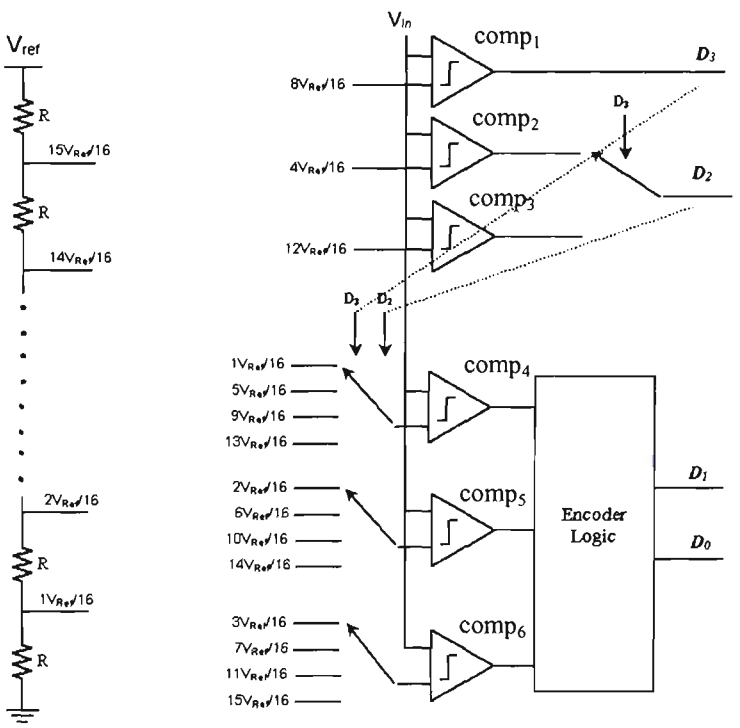



Figure 3.15 Four-bit Modified Flash ADC.

The main advantage of the modified flash ADC approach is a great reduction of the number of comparators, which is most critical and the most area-consuming component in the flash ADC design. For n-bit of resolution, the modified ADC architecture requires only $(2^{n-2} + 2)$ comparators, comparing with $(2^n - 1)$ comparators required by the full flash ADC topology. Also, the modified flash ADC requires a much less complex encoder than that of the traditional full flash ADC. Moreover, the modified

flash approach does not require any other components, such as DAC, subtractors, amplifiers..., as required in subranging ADC architectures.

Table 3.7: Relationship between comparator outputs and ADC outputs

| O15 | O14 | O13 | O12 | O11 | O10 | O9 | O8 | O7 | O6 | O5 | O4 | O3 | O2 | O1 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 1 |
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

$O_8 = 1, O_{12} = 1$

$O_8 = 1, O_{12} = 1$

$O_8 = 1, O_{12} = 1$

$O_8 = 1, O_{12} = 1$

Another key characteristic of the proposed ADC architecture in Figure 3.15 is that it can perform the Analog-to-Digital (A/D) conversion in one clock cycle (like full flash ADC). The reasons are described as follows:

- The traditional flash ADC and the proposed modified ADC both employ the dynamic latched-type comparator, which includes an optimised SR latch to hold the comparator output during its recharge-mode. In the traditional full flash ADC topology, to maximise the sampling speed, its 15 comparators perform

their comparison simultaneously in the first half clock-cycle, and its logic encoder performs its function in the other half clock-cycle while the comparators maintains their output values (in recharge-mode). Thus, the digital data should be ready after one-clock cycle.

- In the modified flash ADC architecture, as illustrated in Figure 3.15, the first three comparators ($comp_1$, $comp_2$ and $comp_3$) complete the comparison, the 2:1 switches perform the selection and the appropriate reference voltages propagate through the 4:1 switches to the bottom three comparators in the first clock-cycle. In the other half clock-cycle, while all the data are maintained since the first three comparators keep their values in recharge-mode, the bottom comparators ($comp_4$, $comp_5$ and $comp_6$) perform the comparison and the last two bits ($D_1$ and $D_0$) will be encoded (since the encoder of the modified flash ADC is very simple). Thus, the digital data is also ready after one clock-cycle.

- Obviously, there will be a slight reduction of the sampling frequency of the modified flash ADC comparing with that of the full flash. Since there will be supplemented delays of the switches and the encoder logic that have to be counted in half clock-cycle. The encoder of the modified flash ADC is actually a 2:1 MUX. However, the delays of switches are very small (less than 200ps), and thus the sampling frequency reduction is minor.

The number of 4:1 multiplexers increases with increasing resolution, but more complex multiplexers would not be required. However, the complexity of an ADC depends not

only on the number of comparators and multiplexers but also on the size of the digital encoder. In this design, the complexity of the digital encoder substantially decreases compared to the standard direct flash conversion, no matter how high the resolution is. This will compensate for the increased number of MUXs, therefore an area saving is achieved.

### *3.6.2.2 Modified Flash ADC Performance Analysis*

The full flash ADC and the modified flash ADC have both been implemented and compared for performance. Figure 3.16 presents the plots of differential nonlinearity (DNL) and integral nonlinearity (INL) errors of the new modified flash ADC at a sampling frequency of 500MHz. It can be seen that the DNL and INL achieved are 0.36 and 0.41 Least Significant Bit (LSB) respectively.

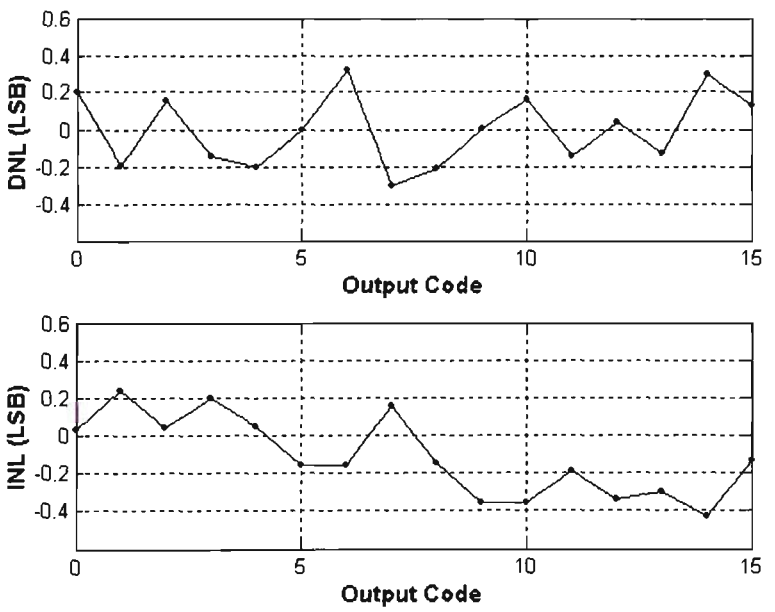



Figure 3.16 DNL and INL at 500MHz.

The performance analysis of the two ADCs are summarised in Table 3.8. The results indicate that a 59% power saving is obtained and 53% of the total number of transistors could be saved when the modified flash ADC is used instead of a full flash ADC. For comparison reasons the two ADCs were operated at a speed of 500 MHz.

Table 3.8: Comparison results of the ADC circuit performance

| **Description** | **4-bit Full Flash ADC** | **4-bit Modified Flash ADC** |
|---|---|---|
| Number of Devices | | |
| NMOS | 179 | 84 |
| PMOS | 194 | 90 |
| Resistors | 16 | 16 |
| Power Consumption | 12.87 mW | 5.08 mW |
| Speed | 500 MHz | 500 MHz |
| Resolution | 4 bits | 4 bits |
| Voltage Supply | 2.5 V | 2.5 V |
| Technology | 0.18µm CMOS | 0.18µm CMOS |

When the operating frequency of the analog to digital converter is increased, the power consumption increases dynamically and is proportional to the frequency. Figure 3.17 illustrates the power consumption of the two ADCs with increase in frequency.

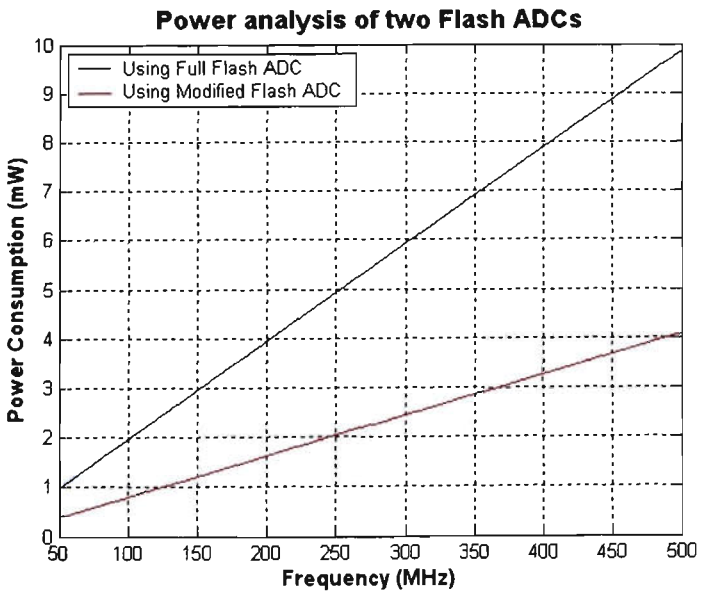



Figure 3.17 Power Analysis of the two ADCs

As mentioned earlier, the comparator is the most critical and the most area-consuming component of the flash ADC design. Table 3.9 shows the number of comparators required for the two flash ADC circuits.

Table 3.9: Number of Comparators required for each Flash design

| **Resolution (bits)** | **4-bit Full Flash** $(2^n - 1)$ | **4-bit modified Flash** $(2^{n-2} + 2)$ |
|---|---|---|
| **4** | 15 | 6 |
| **6** | 63 | 18 |
| **8** | 255 | 66 |
| **10** | 1023 | 258 |
| **12** | 4095 | 1026 |
| **14** | 16383 | 4098 |
| **16** | 65535 | 16386 |

From the above results, we can conclude that the advantages of the new ADC architecture include fewer components, less complexity, therefore smaller size and lower power consumption. These characteristics make this new device better candidate for most applications since power, size and device complexity are the major factors in current electronic system design.

## 3.6.3 Pipeline ADC Architecture

In this section, the design and implementation of a high performance 12-bit pipeline ADC architecture, along with the details analysis of its performance, are presented. The pipeline ADC employs the modified flash ADC, implemented in Section 3.6.2.1, to reduce the device complexity and power consumption.

### 3.6.3.1 Pipeline ADC Design

A pipeline ADC basically consists of numerous consecutive stages, as illustrated in Figure 3.18. Each stage processes the input signal, performs analog-to-digital conversion to provide a $m_i$-bit digital output code. It then performs digital-to-analog conversion to obtain the analog value of the digitised $m_i$ bits. The analog value is, then, subtracted from the input signal of this stage, to provide a residual voltage, which will be processed in the next stage.

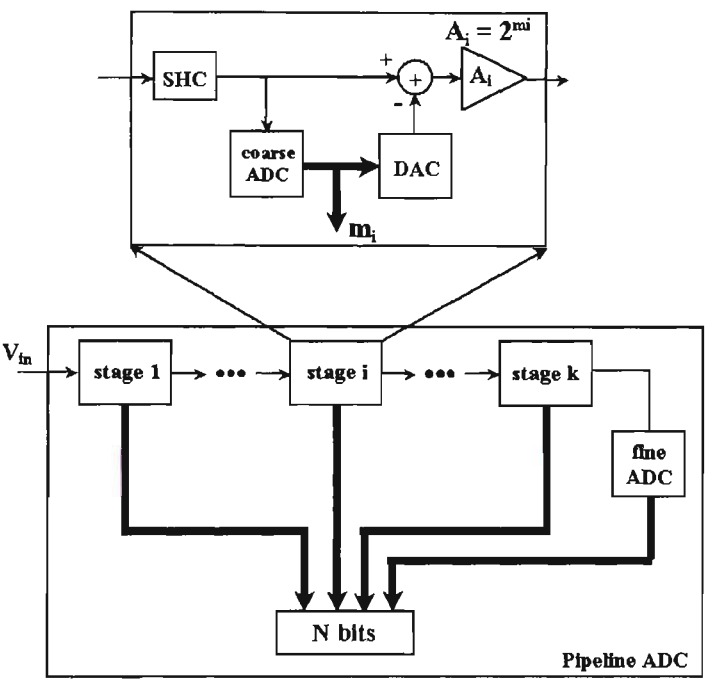



Figure 3.18 Pipeline ADC Architecture.

The output of the entire system comes from the bits generated by each stage. Due to the fact that the dynamic range of the residual voltage is smaller than the input by a factor of $2^{mi}$, many architectures foresee an amplification of the residual voltage by the same factor, to keep the dynamic range constant along the pipeline design. To obtain 12-bit

resolution, the designed pipeline ADC comprises three single stages, each stage contributes 4-bit of resolution.

Figure 3.19 describes the detailed implementation of 4-bit one stage of the 3-stage pipeline ADC. The design of the components for the 4-bit stage is described as follows:

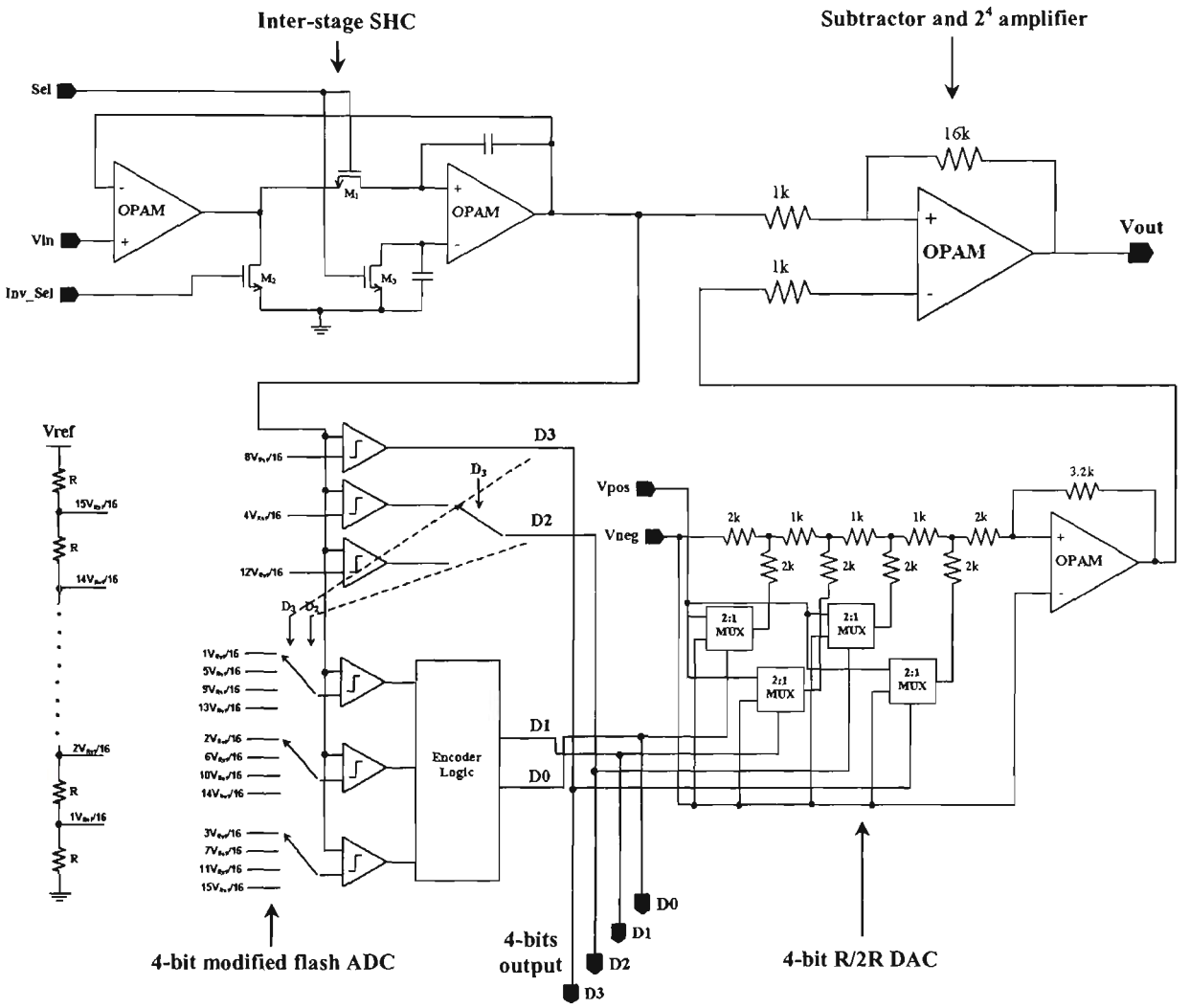



Figure 3.19 A 4-bit single stage block employed in the pipeline ADC.

Flash ADCs are typically employed as sub-ADCs in a pipeline ADC architecture. In this pipeline ADC scheme, a modified flash ADC, which was described in Section 3.6.2, is used instead of the traditional full flash ADC to reduce design complexity and

power dissipation. Since the modified flash ADC achieves a great reduction in the number of comparators, the designed 12-bit pipeline ADC will attain a great reduction in the device complexity and area.

The inter-stage SHC architecture, which was described in Section 3.5, is utilised in the designed 4-bit stage in order to attain a high speed and precision at which the input and residue analog voltages are sampled and held.

The technique used to implement the sub-DAC in the single stage pipeline block is R/2R ladder due to its advantages that are simple configuration and only two resistor values required, whose exact values are not critical. Therefore it is well suited to integrated circuit realisation. The stage subtractor and amplifier was implemented using typical linear amplifier due to its advantages in low design complexity, low power consumption and good accuracy [93, 94].

### *3.6.3.2 Pipeline ADC Analysis*

In order to fully understand the performance of any ADC, the specifications of the static and dynamic domains need to be addressed. Firstly, in static domain, where the INL and DNL of the converter are described. Secondly, the dynamic domain where the communication specifications, such as signal-to-noise ratio (SNR) and effective number of bits (ENOB) are described.

### 3.6.3.2.1 Static Specifications

The most considerable evaluation of static specifications of an ADC is the DNL and INL. The properties of these specifications include the quantisation error or noise ($Q_n$) of the converter, which is associated with the accuracy of the ADC.

DNL is a metric of uniformity of the individual quanta step sizes. DNL consists of a set of $N$-1 data values, where $N$ is the total number of points. Each value is the difference between the actual step size and the LSB step size normalised to one LSB. The DNL can be expressed as [95]:

$$DNL(i) = \frac{data[i] - data[i-1]}{V_{LSB}} - 1 \tag{3.16}$$

The $V_{LSB}$ is the LSB of the ADC and is expressed as:

$$V_{LSB} = \frac{data[N] - data[1]}{N} \tag{3.17}$$

where $data[i]$, $i$ is equal to 1...($N$-1), is the ADC transition voltage.

INL is a metric of cumulative match of the ADC transfer function to the best-fit line. One could also compare to the endpoint line or target design but these methods would include gain error. INL consists of a set of N data values. Each value is the difference between the sample point and the best-fit line and normalised to one LSB. The INL of an ADC can be expressed as follows [95]:

$$INL(i) = \frac{data[i] - (V_{LSB} \cdot i + data[1])}{V_{LSB}} \tag{3.18}$$

where the $V_{LSB}$ is also equivalent to $\frac{data[N] - data[1]}{N}$.

### *3.6.3.2.2 Dynamic Specifications*

Distortion measurement is obtained by sourcing the input sine wave to the system. The analog response is first captured and then analysed in the frequency domain. This means that the processed waveform is converted into its spectrum using the Fast-Fourier-Transform (FFT) algorithm, and the calculations are based on the frequency components. Typical distortion measurements are:

- **Signal-to-Noise Ratio (SNR):** The SNR is calculated as the ratio of the rms value of the input signal to the rms sum of all other spectral components below the Nyquist frequency, excluding harmonics. The SNR is expressed as [96, 97]:

$$SNR = 20 \cdot \log \frac{F_f}{\sqrt{\sum_{\min_{BW}}^{\max_{BW}} M_j^{\,2}}} \tag{3.19}$$

where $F_f$ is the fundamental of the input signal, $M_j$ are the spectral noise components excluding harmonics, $max_{BW}$ and $min_{BW}$ are the maximum and minimum bandwidths, respectively. Equation (3.19) could also be expressed in terms of dB for a single-tone sine signal, where SNR is given by [98]:

$$SNR = (6.02N + 1.76) \quad \text{dB} \tag{3.20}$$

Equation (3.20) indicates that each additional bit, $N$, enhances the SNR by 6.02 dB.

- **Effective Number of Bits (ENOB):** This specification is defined as the number of bits required in an ideal ADC so that the mean squared noise power in the ideal ADC equals the mean squared power of the residual error in the real ADC. ENOB defines the

available resolution, which is influenced by: Noise, quantisation error, DNL and INL errors. For a linear ADC, this characteristic is described as [98]:

$$ENOB = \frac{SNR - 1.76}{6.02} \tag{3.21}$$

### 3.6.3.3 *Pipeline ADC Performance Analysis*

The designed pipeline ADC employing the modified flash ADC topology and the pipeline ADC employing the full flash ADC approach have been both implemented and simulated in Cadence Analog Environment, and comparisons of their performance have been made.

Figure 3.20 presents the plots of DNL and INL errors of the designed pipeline ADC at a sampling frequency of 500MHz. It can be seen that the DNL and INL achieved are 0.6 and 0.5 LSB respectively. The DNL and INL achieved are smaller than those of the ADCs reported in [99, 100].

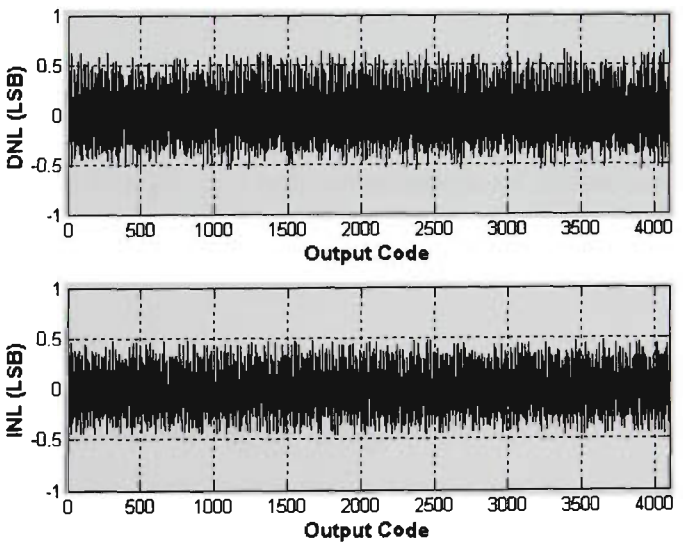



Figure 3.20 DNL and INL at 500MHz.

Table 3.10 summaries the performance analysis of the two 12-bit pipeline ADCs. Results indicate that a 40% power saving is obtained and 60% of comparators could be saved when the modified flash ADC is used instead of a full flash ADC to construct the pipeline ADC.

Table 3.10 : Comparison results of the two pipeline ADC architecture performance

| **Parameter** | **Using traditional flash ADC** | **Using modified flash ADC** |
|---|---|---|
| Operating frequency | 500MHz | 500MHz |
| Max. data rate | 125MS/s | 125MS/s |
| Power Consumption @ 125MS/s | 72.9mW | 40.6mW |
| Number of Comparator Required | 45 | 18 |
| Critical Path | 8ns | 8ns |
| Technology | 0.18 μm CMOS | 0.18 μm CMOS |
| DNL | ±0.5 LSB | +0.6/-0.5 LSB |
| INL | ±0.5 LSB | ±0.5 LSB |
| SNR | 72dB | 70dB |
| Core Supply Voltage | 2.5 V | 2.5 V |

## 3.6 Conclusion

This chapter presents the design and implementation of constituent components for a multi-channel high performance reduced complexity DAQ chip.

A 12:1 analog MUX has been designed using only one stage of CMOS TG switches from input to output in order to reduce the delay and also increase system accuracy. A programmable SC anti-aliasing filter employing both inverting and non-inverting

integrators to improve device accuracy and stability level is also presented. The anti-aliasing filter achieves a frequency tuning range from 0.2kHz to 1MHz, and hence it provides the DAQ system an attractive feature of programmable sampling rate. The design and implementation of the PGA is also discussed in this chapter. It employs linear resistors in the feedback network to achieve high linearity, permitting the device to achieve a THD of -80dB. This chapter also presents the design and implementation of a SHC employing feedback loop and a compensation capacitor. The main advantage of this architecture is that the charge injection error and the clock feedthrough error are effectively removed, inducing a very high-accuracy characteristic.

ADC is the most critical and the most area and power consuming block in a DAQ system. In this chapter, a new modified flash ADC has been proposed and implemented to reduce the system complexity and power consumption. It requires only $(2^{n-2} + 2)$ comparators to implement an n-bit flash ADC. The modified flash ADC has been implemented based on the development of an optimised comparator that offers an attractive combination of high-speed, low-power and high accuracy. Results indicate that 40% power saving is obtained and 60% of comparators could be saved when the modified flash ADC is used instead of a full flash ADC to construct a pipeline ADC. This enables a realisation of a high-speed, high-accuracy DAQ chip with reduced power consumption and complexity.

Performance analysis and testing on all of the building-block components of a DAQ system have been performed to demonstrate the quality of each circuit design. In order to improve the performance of the proposed components, a mathematical model

representing noise generated within all of the proposed devices will be developed and presented in Chapter 4. The developed model provides a good estimation of the noise generated by the circuits and gives an accurate prediction on the circuit noise performance.

# Chapter 4

# Noise Modelling and Performance Analysis

## 4.1 Introduction

This chapter presents the analysis of noise generated within the proposed building block components, which have been implemented in Chapter 3 for a Data Acquisition (DAQ) system. The study of noise is important on overall device performance since it represents the lower limit to the size of electrical signal that can be read by the devices, or an integrated circuit (IC) in general, without significant deterioration in signal quality. The noise in Complementary Metal-Oxide Semiconductor (CMOS) ICs is typically caused by the small current and voltage fluctuations that are generated within the devices themselves. The existence of the noise is basically due to the fact that electrical charge is not continuos but is carried in discrete amounts to the electron

charge, and thus noise is associated with fundamental processes in the IC devices. When working at high frequencies, the noise generated within the device itself will play an increasingly important role in its overall performance [93]. Therefore, a model that can accurately predict the noise characteristics of the device is crucial for IC design.

The pipeline ADC is the most complex and the main building block component of the proposed DAQ system, thus, the noise analysis of the pipeline ADC is analysed first. Therefore, this chapter is structured as follows: Section 4.2 presents the noise analysis of the latch-type comparator, employed in the proposed pipeline ADC architecture. A novel model representing the noise generated within the device is developed and presented in Section 4.2. Section 4.3 details the noise analysis of the modified flash ADC architecture, which is the core of the proposed pipeline ADC. The noise analysis of the entire pipeline ADC is presented in Section 4.4. The noise analysis of the 12:1 Multiplexer (MUX), Programmable Gain Amplifier (PGA), anti-aliasing filter and Sample-and-Hold Circuit (SHC) is presented in Section 4.5. Conclusions of this chapter are presented in Section 4.6.

## 4.2 Noise Analysis of the Proposed Comparator

The latch-type comparator, proposed and optimised in Chapter 3, is the most significant component in the modified flash ADC, which is employed in the proposed pipeline ADC architecture. Therefore, in this section, the noise generated within the comparator should be analysed because it will significantly affect the overall noise performance of the pipeline ADC.

The proposed comparator includes two stages: The CMOS latch amplifier circuit and the S-R latch, as illustrated in Figure 4.1. It is observed that the CMOS latch amplifier circuit and S-R latch circuit consist of Metal Oxide Semiconductor (MOS) transistors ($M_1$ to $M_{18}$). Therefore, in order to analyse the noise generated within the comparator, there are two issues that need to be addressed. The first issue is to establish a model of a noise generator of a MOS transistor, which is presented in Section 4.2.1. The other issue is to analyse the noise of both stages, which is presented in Section 4.2.2. A mathematical model representing the noise generated within the comparator is consequently developed and is also presented in Section 4.2.2.

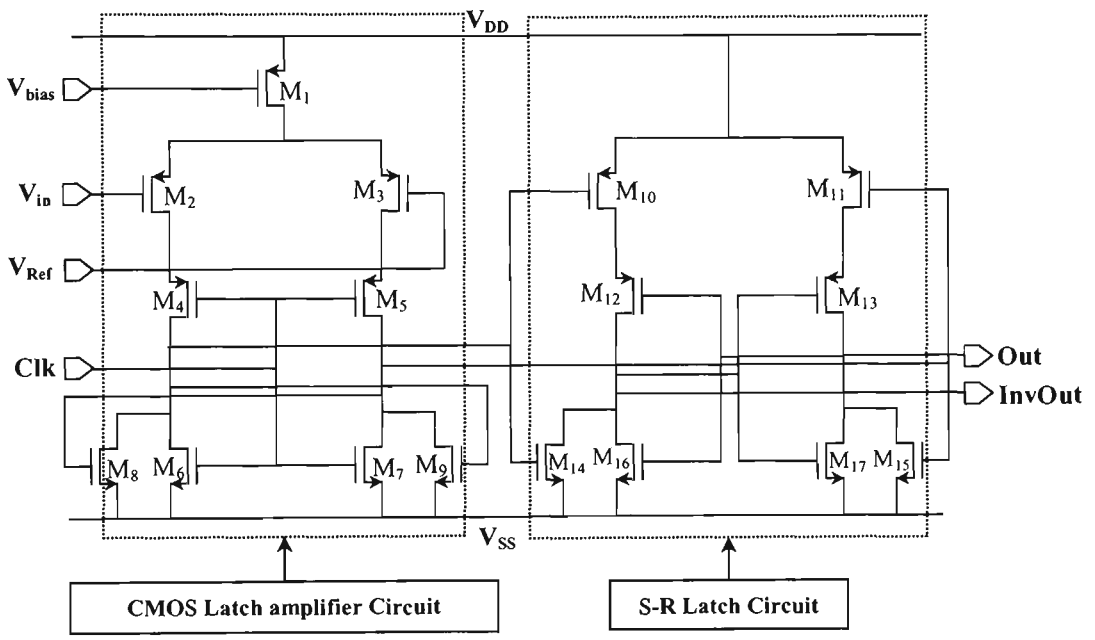



Figure 4.1 Schematic diagram of the optimised comparator.

## 4.2.1 MOS Transistor Noise Model

Noise is always present in MOS transistors. Since noise is purely random signal, the instantaneous value of the noise signal cannot be predicted. Therefore, the noise signal is typically defined in terms of mean square value and has no polarity. Theoretically,

the noise signal in CMOS transistors is considered to be generated by different sources that are classified based on the origin of the noise The major noise sources in MOS transistors are [93, 101-103]:

- *Thermal noise*: is due to the random thermal motion of electrons (Johnson effect) since the typical electron drift velocities in a semiconductor are much less than electron thermal noise. Since this source of noise is the thermal motion of electrons, it is related to temperature and is independent of frequency ans is given by:

$$\overline{v_{thermal}^2} = 4kT\frac{2}{3g_m}\Delta f \tag{4.1}$$

where $k$ is the Boltzmann's constant and $T$ is the absolute temperature, $g_m$ is the MOS transconductance of the transistor and $\Delta f$ is the bandwidth (in Hertz).

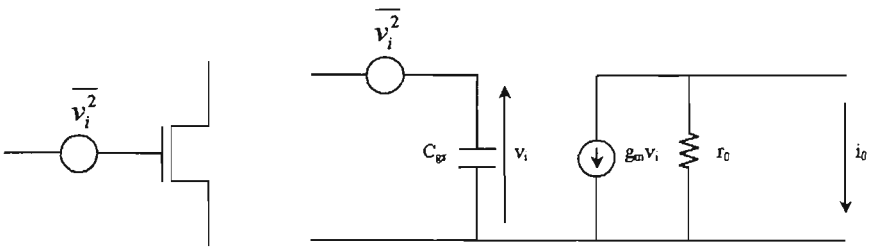
- *Flicker noise (also called 1/f noise)*: is caused by traps associated with contamination and crystal defects. These traps capture and release charge carriers in a random fashion and the time constants associated with the process give rise to a noise signal with energy concentrated at low frequencies. Therefore, flicker noise in MOS transistors is inversely proportional to frequency and is given by:

$$\overline{v_{flicker}^2} = K\frac{I_D^a}{f \cdot g_m^2}\Delta f \tag{4.2}$$

where $I_D$ is the drain current, $K$ is a constant for a particular device and $a$ is a constant in the range of 0.5 to 2.

Various studies on noise models of MOS transistors have been reported [93, 101-104]. The most popular noise model of a MOS transistor is shown in Figure 4.2 [93], where all the noise sources are lumped into an equivalent input noise generator $\overline{v_i^2}$ :

$$\overline{v_i^2} = \frac{8kT}{3g_m}\Delta f + K\frac{I_D^a}{f.g_m^2}\Delta f \tag{4.3}$$




(a) (b)

Figure 4.2 MOSFET equivalent input noise generator (a) device symbol (b) equivalent circuit.

In equation (4.3), the first term represents the thermal noise component and the second term represents the flicker (1/f) noise component.

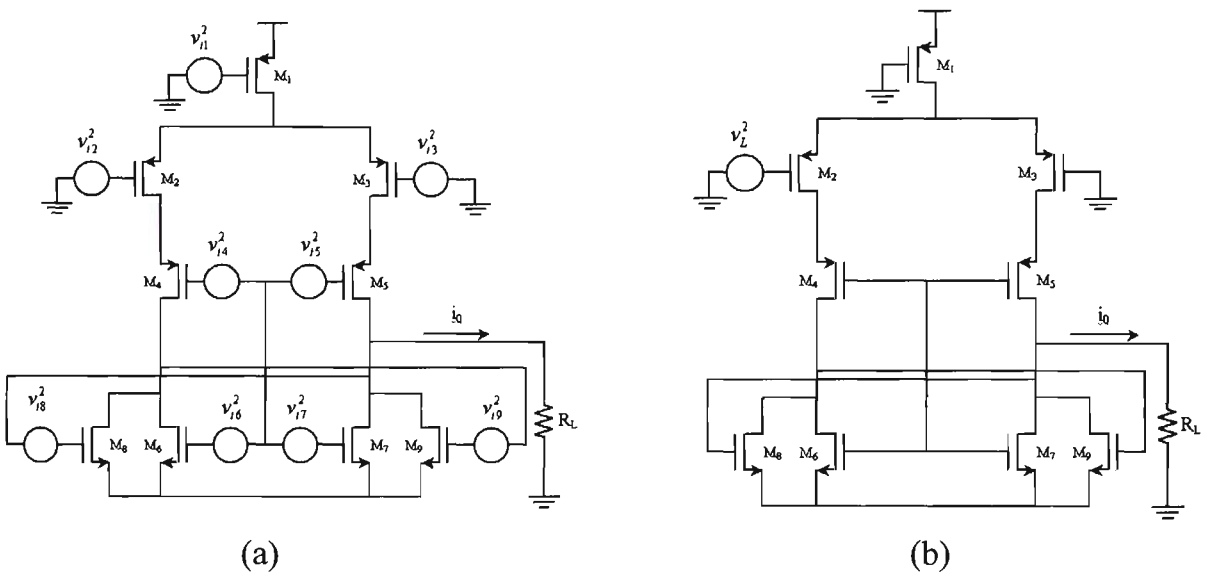
Practical results showed that for a typical MOS transistor, the flicker noise is approximately independent of bias current and voltage and inversely proportional to the active gate area of the transistor. It is also observed experimentally that the flicker noise is an inverse function of the gate-oxide capacitance per unit area. The noise generator of a MOS transistor, thus, can be expressed as follows [93]:

$$\overline{v_i^2} = \frac{8kT}{3g_m}\Delta f + \frac{K_f}{WLC_{ox}f}\Delta f \tag{4.4}$$

Measurements show that the typical value for constant $K_f$ is $3 \times 10^{-24}$ ($V^2F$) [93].

## 4.2.2 Comparator Noise Model Development

The proposed comparator includes two stages: The CMOS latch circuit and the S-R latch, as illustrated in Figure 4.1. The CMOS latch circuit is analysed for noise first. Figure 4.3a shows the CMOS latch circuit with noise contribution, and Figure 4.3b shows the circuit with equivalent input noise voltage.




(a) (b)

Figure 4.3 Latch circuit with (a) noise generators; (b) equivalent input noise voltage.

By equating output noise currents in Figure 4.3a and Figure 4.3b, the equivalent input noise voltage can be calculated as follows:

$$\overline{v_L^2} = \left(\frac{g_{m1}}{g_{m2}}\right)^2 \overline{v_{i1}^2} + \overline{v_{i2}^2} + \overline{v_{i3}^2} + \left(\frac{g_{m4}}{g_{m2}}\right)^2 \overline{v_{i4}^2} + \left(\frac{g_{m5}}{g_{m2}}\right)^2 \overline{v_{i5}^2} + \left(\frac{g_{m6}}{g_{m2}}\right)^2 \overline{v_{i6}^2}$$

$$+ \left(\frac{g_{m7}}{g_{m2}}\right)^2 \overline{v_{i7}^2} + \left(\frac{g_{m8}}{g_{m2}}\right)^2 \overline{v_{i8}^2} + \left(\frac{g_{m9}}{g_{m2}}\right)^2 \overline{v_{i9}^2} \qquad (4.5)$$

where $g_{mi}$ ($i = 1 \ldots 9$) is the transconductance of transistor $M_i$, $\overline{V_i^2}$ ($i = 1 \ldots 9$) is the noise source generator of transistor $M_i$ which can be calculated by equation (4.4).

Since the two branches of the latch circuit are symmetrical, equation (4.5) can be simplified to:

$$\overline{v_L^2} = \left(\frac{g_{m1}}{g_{m2}}\right)^2 \overline{v_{i1}^2} + 2\overline{v_{i2}^2} + 2\left(\frac{g_{m4}}{g_{m2}}\right)^2 \overline{v_{i4}^2} + 2\left(\frac{g_{m6}}{g_{m2}}\right)^2 \overline{v_{i6}^2} + 2\left(\frac{g_{m8}}{g_{m2}}\right)^2 \overline{v_{i8}^2} \tag{4.6}$$

Substituting (4.4) into (4.6), we obtain the equivalent noise generator for circuit in Figure 4.3b:

$$\overline{v_L^2} = \frac{2K_p}{fW_2L_2C_{ox}}\left[1 + \frac{L_2^2}{L_1^2} + \frac{L_2^2}{L_4^2} + \frac{1}{2}\frac{\mu_n K_n L_2^2}{\mu_p K_p L_6^2} + \frac{1}{2}\frac{\mu_n K_n L_2^2}{\mu_p K_p L_8^2}\right]\Delta f$$

$$+ \frac{16kT}{3g_{m2}}\left[1 + \sqrt{\frac{1}{2}\frac{(W/L)_1}{(W/L)_2}} + \sqrt{\frac{(W/L)_4}{(W/L)_2}} + \sqrt{\frac{1}{2}\frac{\mu_n(W/L)_6}{\mu_p(W/L)_2}} + \sqrt{\frac{1}{2}\frac{\mu_n(W/L)_8}{\mu_p(W/L)_2}}\right]\Delta f \tag{4.7}$$

The noise figure (NF) is a commonly used method to specify the noise performance of a circuit or device. It is defined as [93, 101]:

$$NF = \frac{Total\ output\ noise}{That\ part\ of\ noise\ due\ to\ the\ source\ resistance} = 1 + \frac{\overline{v_i^2}}{4kTR_S\Delta f} \tag{4.8}$$

Therefore, the NF of the latch circuit of the comparator is determined by:

$$NF_L = 1 + \frac{\overline{v_L^2}}{4kTR_S\Delta f} \tag{4.9}$$

In a similar manner, we will analyse the noise in the S-R latch of the proposed comparator. Figure 4.4a shows the S-R latch with noise contribution, and Figure 4.4b shows the S-R latch with equivalent input noise voltage. By equating output noise currents in Figure 4.4a and Figure 4.4b, the equivalent input noise voltage can be

calculated as in equation (4.10), where it has been assumed that the left and right braches of the S-R latch are symmetrical.

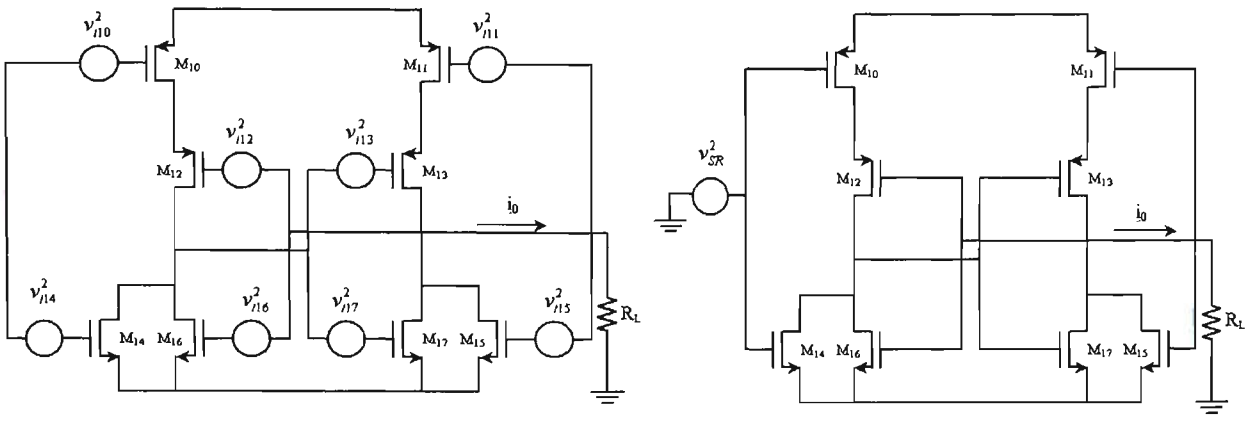



Figure 4.4 SR Latch circuit with (a) noise generators, (b) equivalent input noise voltage.

$$\overline{v_{SR}^2} = 2\left(\frac{g_{m10}}{g_{m10}+g_{m14}}\right)^2 \overline{v_{i10}^2} + 2\left(\frac{g_{m12}}{g_{m10}+g_{m14}}\right)^2 \overline{v_{i12}^2} + 2\left(\frac{g_{m14}}{g_{m10}+g_{m14}}\right)^2 \overline{v_{i14}^2} + 2\left(\frac{g_{m16}}{g_{m10}+g_{m14}}\right)^2 \overline{v_{i16}^2} \qquad (4.10)$$

The design of the S-R latch of the comparator comprises of PMOS and NMOS transistors that have equal dimensions. Equation (4.10) can be reduced to:

$$\overline{v_{SR}^2} = 4\left(\frac{g_{m10}}{g_{m10}+g_{m14}}\right)^2 \overline{v_{i10}^2} + 4\left(\frac{g_{m14}}{g_{m10}+g_{m14}}\right)^2 \overline{v_{i14}^2} \qquad (4.11)$$

Substituting equation (4.4) into equation (4.11), we obtain:

$$\overline{v_{SR}^2} = 4\left(\frac{g_{m10}}{g_{m10}+g_{m14}}\right)^2 \left(\frac{K_P}{C_{ox}W_{10}L_{10}f} + \frac{8kT}{3g_{m10}}\right)\Delta f + 4\left(\frac{g_{m14}}{g_{m10}+g_{m14}}\right)^2 \left(\frac{K_N}{C_{ox}W_{14}L_{14}f} + \frac{8kT}{3g_{m14}}\right)\Delta f \qquad (4.12)$$

The noise figure of the S-R latch, therefore, can be calculated as follows:

$$NF_{SR} = 1 + \frac{\overline{v_{SR}^2}}{4kTR_S\Delta f} \qquad (4.13)$$

The total NF of the proposed comparator, including the cascaded latch circuit and S-R latch circuit, is presented by:

$$NF_{Comp} = NF_L + \frac{NF_{SR} - 1}{A_L} \tag{4.14}$$

$$A_L = \frac{g_{m6}}{g_{m9}} \frac{r_{o2}}{r_{o2} + r_{o4}} \tag{4.15}$$

where $A_L$ is the gain of the latch stage of the comparator.

Figure 4.5 illustrates the simulation of the noise model in MATLAB. The result shows that the NF of the designed comparator is large at low frequency due to the flicker (1/f) noise component. However, the flicker noise does not commonly extend into the megahertz region, where the NF becomes constant due to the thermal noise only. The comparator NF at 500MHz is 4.747dB.

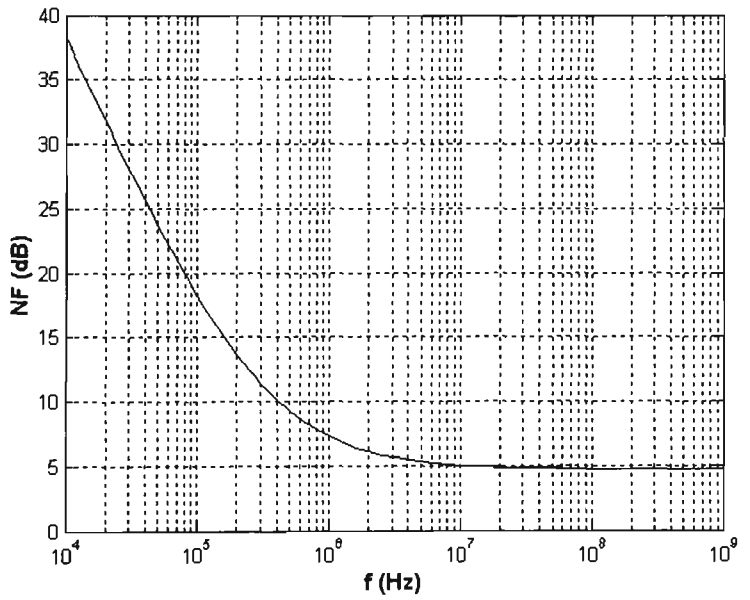



Figure 4.5 Comparator NF (a) using the developed model.

Figure 4.6 shows the NF simulation obtained using Cadence Analog Artist Environment. It can be seen that the noise mathematical model developed has provided

a result in agreement with the circuit simulation result generated by the EDA package. The NF results of the proposed comparator are summarised in Table 4.1.

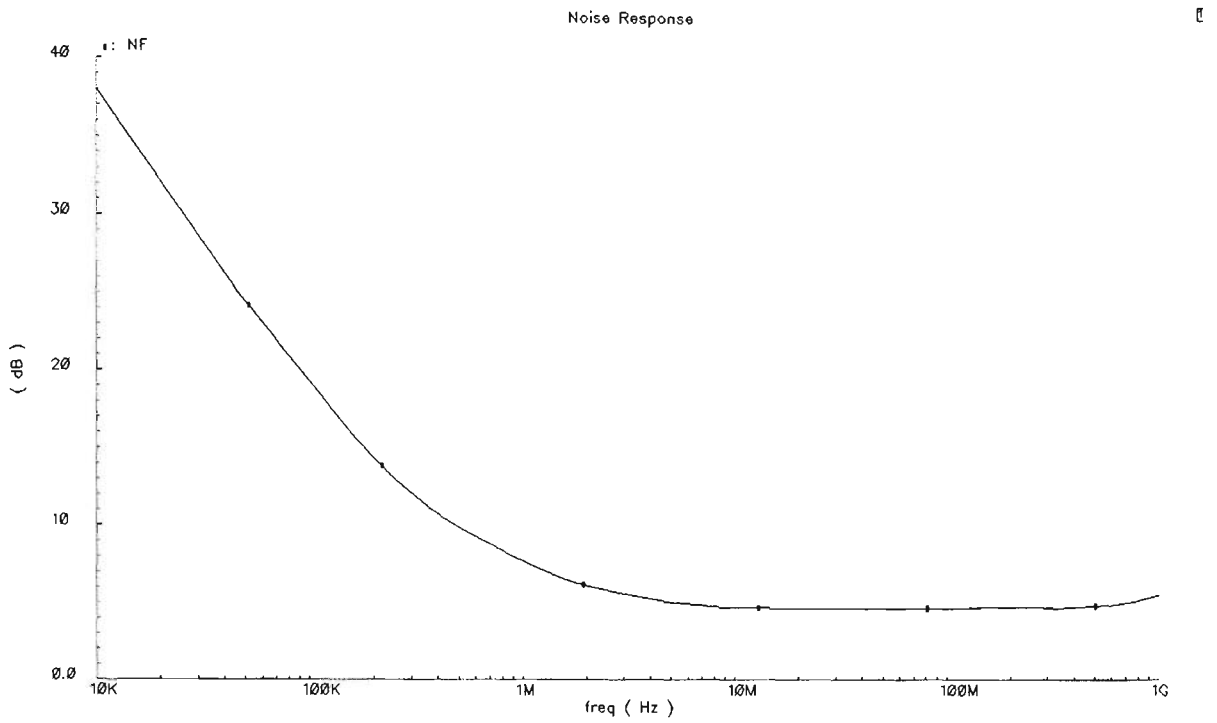



Figure 4.6 Comparator NF using the Cadence Analog Artist Environment.

Table 4.1 : Noise Figure of the proposed comparator

| **Device Noise Performance** | **Value** |
|---|---|
| Noise Figure @500MS/s (*Cadence Simulation*) | 4.751dB |
| Noise Figure @500MS/s (*Developed Model*) | 4.747dB |

## 4.3 Noise Analysis of the Modified Flash ADC Architecture

As illustrated in Figure 4.7, the modified flash ADC architecture, proposed in Chapter 3, contains a resistor ladder, which consists of 16 resistors, two 2:1 switches (multiplexers (MUXs)), three 4:1 switches (MUXs) and six comparators. The noise

model of each of these components as well as the noise model of the modified flash ADC is analysed mathematically and presented in this section.

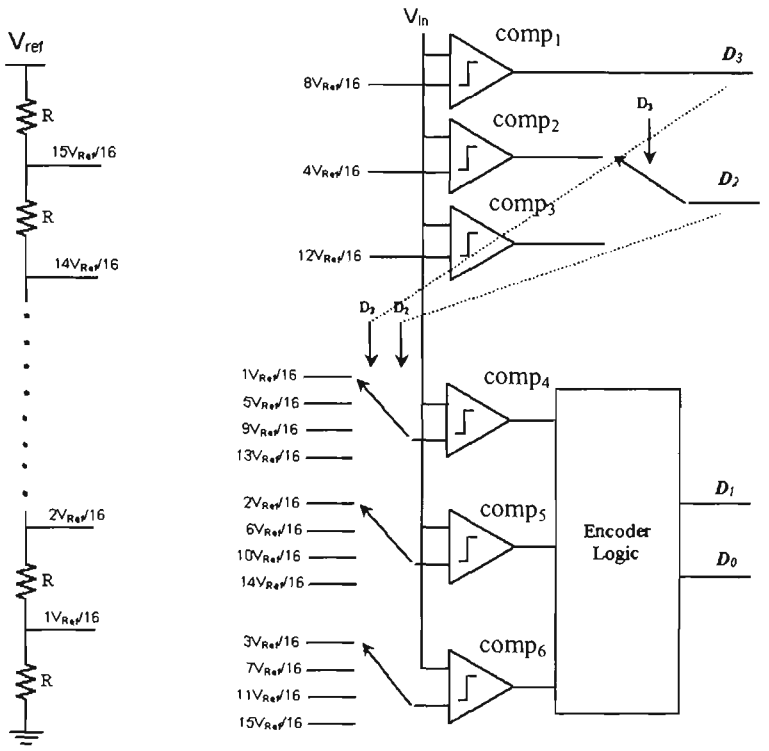



Figure 4.7 Four-bit Modified Flash ADC.

## 4.3.1 Resistor Noise Analysis

In a passive resistor, thermal noise is the most dominant source of noise, so here we only consider this type of noise. This noise source is a fundamental physical phenomenon and is present in any linear passive resistor. In a conventional resistor $R_L$, as illustrated in Figure 4.8, the noise source can be represented by a series voltage generator $\overline{v_R^2}$. This type of noise is due to the random thermal motion of the electrons and is unaffected by the presence or absence of direct current [93]:

$$\overline{v_R^2} = 4kTR_L\Delta f \tag{4.16}$$

Using equation (4.16), one resistor in the flash ADC resistor chain generates a noise power of $1.66\times10^{-17}\cdot\Delta f$ ($V^2$). The entire resistor chain, thus, will generate a total noise power of $2.656\times10^{-16}\cdot\Delta f$ ($V^2$).

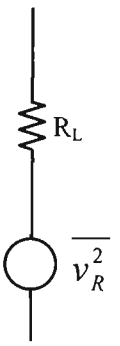



Figure 4.8 Noise source in a resistor.

## 4.3.2 2:1 MUX Noise Analysis

A 2:1 MUX basically comprises of six MOS transistors, as illustrated in Figure 4.9a. As seen in equation (4.4), each transistor in the 2:1 MUX will contribute a specific value to the entire device noise power. All of these MOS noise sources, however, can be lumped into an equivalent input noise source that will generate an equivalent noise power [93].

Figure 4.9a shows the 2:1 MUX circuit with noise contribution, and Figure 4.9b shows the circuit with an equivalent input noise voltage, $\overline{v_{MUX2}^2}$. By equating the total output noise currents in Figure 4.9a and Figure 4.9b, the equivalent input noise generator of the 2:1 MUX can be calculated as:

$$\overline{i_{MUX2}^2} = g_{m5}^2\overline{v_5^2} + g_{m4}^2\overline{v_4^2} + g_{m3}^2\left(\overline{v_3^2} + r_{o1}^2 g_{m1}^2\overline{v_1^2} + g_{m2}^2\overline{v_2^2}r_{o2}^2\right)$$
$$+ g_{m6}^2\left(\overline{v_6^2} + r_{o1}^2 g_{m1}^2\overline{v_1^2} + g_{m2}^2\overline{v_2^2}r_{o2}^2\right) \quad (4.17)$$

where $\overline{v_i^2}$ ($i$ = 1...6) is the noise source generator of transistor $M_i$ which can be calculated by (4.4) and $r_{oi}$ ($i$ = 1,2) is the output resistance of transistor $M_i$.

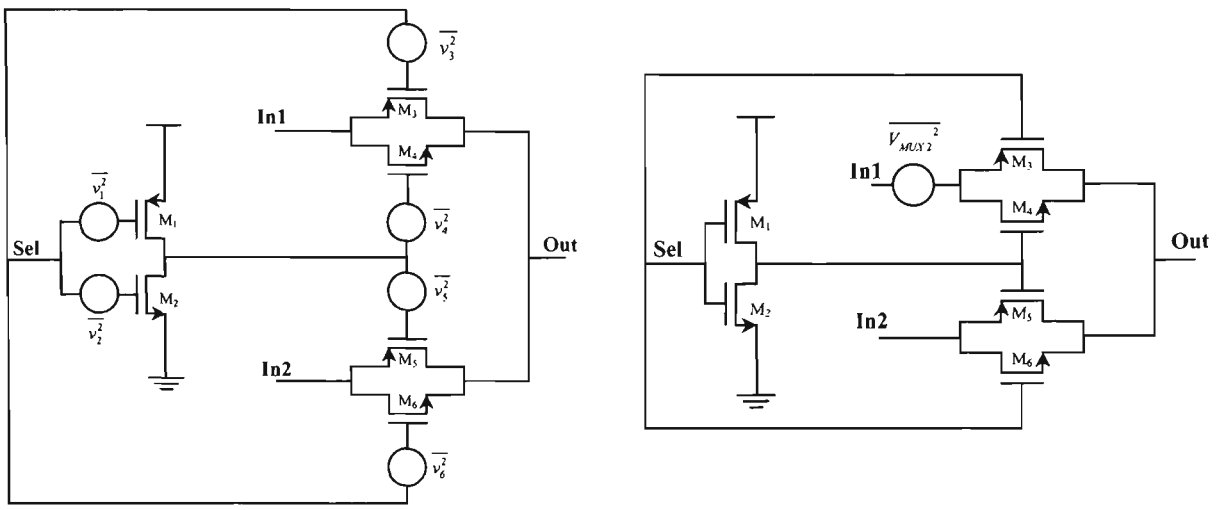



Figure 4.9 2:1 MUX (a) with noise generators (b) with equivalent input noise voltage.

From equation (4.17), the equivalent input noise generator of the 2:1 MUX can be calculated by:

$$\overline{v_{MUX2}^2} = \overline{i_{MUX2}^2}(r_{o3} // r_{o4})^2 = \overline{i_{MUX2}^2}\left(\frac{r_{o3} \cdot r_{o4}}{r_{o3} + r_{o4}}\right)^2 \tag{4.18}$$

Using equation (4.18), it is possible to determine that one 2:1 MUX generates a total noise power of $4.41 \times 10^{-16} \cdot \Delta f$ ($V^2$) at an operating frequency of 500 MHz.

Therefore the total noise power generated by the two 2:1 MUX is $8.82 \times 10^{-16} \cdot \Delta f$ ($V^2$) at this frequency.

### 4.3.3 4:1 MUX Noise Analysis

Noise analysis of the 4:1 MUX is considered in this section. Figure 4.10 illustrates the 4:1 MUX with the equivalent input noise generator included. Let:

$$\overline{v_{IN1}^2} = r_{o1}^2 g_{m1}^2 v_1^2 + r_{o2}^2 g_{m2}^2 v_2^2 \tag{4.19}$$

$$\overline{v_{IN2}^2} = r_{o3}^2 g_{m3}^2 v_3^2 + r_{o4}^2 g_{m4}^2 v_4^2 \tag{4.20}$$

From the mathematical analysis on the 4:1 MUX, the total output noise current is: given by:

$$\begin{aligned}\overline{i_{MUX4}^2} &= g_{m5}^2 \overline{v_5^2} + g_{m6}^2 \left(\overline{v_6^2} + \overline{v_{IN1}^2}\right) + g_{m7}^2 \overline{v_7^2} + g_{m8}^2 \left(\overline{V_8^2} + \overline{v_{IN1}^2}\right) \\ &+ g_{m9}^2 \left(\overline{v_9^2} + \overline{v_{IN1}^2}\right) + g_{m10}^2 \overline{v_{10}^2} + g_{m11}^2 \left(\overline{v_{11}^2} + \overline{v_{IN1}^2}\right) + g_{m12}^2 \overline{v_{12}^2} \\ &+ g_{m13}^2 \overline{v_{13}^2} + g_{m14}^2 \left(\overline{v_{14}^2} + \overline{v_{IN2}^2}\right) + g_{m15}^2 \left(\overline{v_{15}^2} + \overline{v_{IN2}^2}\right) + g_{m16}^2 \overline{v_{16}^2} \\ &+ g_{m17}^2 \overline{v_{17}^2} + g_{m18}^2 \left(\overline{v_{18}^2} + \overline{v_{IN2}^2}\right) + g_{m19}^2 \left(\overline{v_{IN2}^2} + \overline{v_{19}^2}\right) + g_{m20}^2 \overline{v_{20}^2}\end{aligned} \tag{4.21}$$

where $\overline{v_i^2}$ ($i$ = 1...20) is the noise source generator of transistor M$i$ which can be calculated by (4.4) and $r_{oi}$ ($i$ = 1...4) is the output resistance of transistor $M_i$.

From equation (4.19), the equivalent input noise generator of the 4:1 MUX can be calculated as:

$$\overline{v_{MUX4}^2} = \overline{i_{MUX4}^2} \cdot \left[\left(r_{o5} \,//\, r_{o6}\right) + \left(r_{o13} \,//\, r_{o14}\right)\right] = 2 \cdot \overline{i_{MUX4}^2} \cdot \left(\frac{r_{o5} \cdot r_{o6}}{r_{o5} + r_{o6}}\right) \tag{4.22}$$

Using equation (4.22), it is possible to determine that one 4:1 MUX generates a total noise power of $7.07\times10^{-16}\cdot\Delta f$ ($V^2$) at an operating frequency of 500 MHz. Therefore the total noise power generated by the three 4:1 MUX is $2.121\times10^{-15}\cdot\Delta f$ ($V^2$).

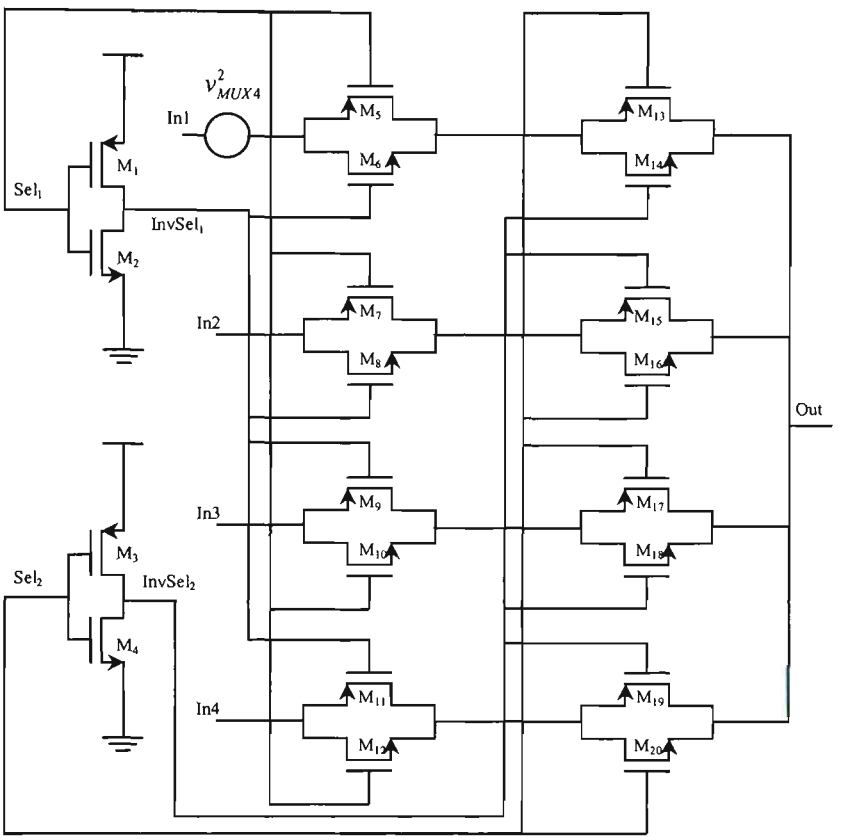



Figure 4.10 4:1 MUX with input equivalent noise generator.

## 4.3.4 Comparator Noise Analysis

The CMOS voltage comparator was analysed for noise in Section 4.2. The input noise generator for one comparator can be described as:

$$\overline{v^2_{comp}} = \left(\frac{g_{m1}}{g_{m2}}\right)^2 \overline{v_1^2} + 2\overline{v_2^2} + 2\left(\frac{g_{m4}}{g_{m2}}\right)^2 \overline{v_4^2} + 2\left(\frac{g_{m6}}{g_{m2}}\right)^2 \overline{v_6^2} + 2\left(\frac{g_{m8}}{g_{m2}}\right)^2 \overline{v_8^2}$$

$$+ 4\left(\frac{g_{m10}}{g_{m10}+g_{m14}}\right)^2 \overline{v_{10}^2} + 4\left(\frac{g_{m14}}{g_{m10}+g_{m14}}\right)^2 \overline{v_{14}^2} \qquad (4.23)$$

Using equation (4.23), it is possible to calculate that one comparator generates a total noise power of $5.3\times10^{-16}\cdot\Delta f$ ($V^2$) at an operating frequency of 500 MHz. Therefore, at this frequency, the total noise power generated by six comparators working full time will be $3.18\times10^{-15}\cdot\Delta f$ ($V^2$).

### 4.3.4.1 *Probability Analysis*

The modified flash ADC contains six comparators. The probability of each comparator switching is calculated mathematically, in order to find out how much of the load each comparator carries. To calculate the probability of each comparator a sine wave input has been applied to the ADC. The mathematical model for the sine input is [105]:

$$V_{in} = \frac{1}{2}\sin(2\pi ft) + \frac{1}{2} \tag{4.24}$$

where $f$ is the input signal frequency.

The probability of each comparator switching has been analysed. The probability that comparator 1 ($comp_1$) outputs a '1' can be described by the following model:

$$P(Comp_1 = '1') = \text{the fraction of time in a period that } Vin \geq 0.25\ V$$

$$= t\,[Vin \geq 0.25\ V] \tag{4.25}$$

Similarly, the probability of the rest of the comparators switching were calculated and are as follows.

$$P(Comp_2 = '1') = t\,[V_{in} \geq 0.5\ V] \tag{4.26}$$

$$P(Comp_3 = '1') = t\,[V_{in} \geq 0.75\ V] \tag{4.27}$$

$$P(Comp_4 = '1') = t[V_{in} \geq 0.8125\ V] + t[0.5625 \leq V_{in} < 0.75] + t[0.3125 \leq V_{in} < 0.5] + t[0.0625 \leq V_{in} < 0.25] \quad (4.28)$$

$$P(Comp_5 = '1') = t[V_{in} \geq 0.875\ V] + t[0.625 \leq V_{in} < 0.75] + t[0.375 \leq V_{in} < 0.5] + t[0.125 \leq V_{in} < 0.25] \quad (4.29)$$

$$P(Comp_6 = '1') = t[V_{in} \geq 0.9375\ V] + t[0.6875 \leq V_{in} < 0.75] + t[0.4375 \leq V_{in} < 0.5] + t[0.1875 \leq V_{in} < 0.25] \quad (4.30)$$

The probability of a certain comparator is off can be described as:

$$P(Comp_i = '0') = 1 - P(Comp_i = '1') \quad (4.31)$$

where $i$ is the comparator number ( $i = 1 \ldots 6$).

Table 4.2 presents the switching probability of all six comparators. *P(Output = '1')* describes the probability that a certain comparator output is on, and *P(Output = '0')* describes the probability that a comparator output is zero. The probability of a certain comparator being 'on' or 'off' will affect the noise generated by the new flash ADC.

Table 4.2: Probability of each comparator

| **Comparator** | ***P(Output = '1')*** | ***P(Output = '0')*** |
|---|---|---|
| $Comp_1$ | 0.75 | 0.25 |
| $Comp_2$ | 0.5 | 0.5 |
| $Comp_3$ | 0.25 | 0.75 |
| $Comp_4$ | 0.707 | 0.293 |
| $Comp_5$ | 0.5 | 0.5 |
| $Comp_6$ | 0.293 | 0.707 |

From the probability analysis of each comparator, it can be stated that the six comparators are equivalent to three of the comparators working full time. Therefore the total noise power generated can be said to be:

$$Noise\ Power = \frac{3.18\times10^{-15}\cdot\Delta f}{2}\ (V^2),\ \text{or}\ 1.59\times10^{-15}\cdot\Delta f\ (V^2). \qquad (4.32)$$

### 4.3.5 Modified Flash ADC Noise Performance

Table 4.3 presents a summary of the noise analysis for each component within the modified flash ADC architecture at an operating frequency of 500MHz. The total noise power of the modified flash ADC at this frequency has also been calculated and presented in Table 4.3.

Table 4.3: Summary of noise power in the modified ADC.

| | **Noise in one component** | **Number of components in new flash ADC** | **Total Noise in specific components** |
|---|---|---|---|
| **Resistor ($V^2$)** | $1.66\times10^{-17}\cdot\Delta f$ | 16 | $2.65\times10^{-16}\cdot\Delta f$ |
| **2:1 MUX ($V^2$)** | $4.41\times10^{-16}\cdot\Delta f$ | 2 | $8.82\times10^{-16}\cdot\Delta f$ |
| **4:1 MUX ($V^2$)** | $7.07\times10^{-16}\cdot\Delta f$ | 3 | $2.12\times10^{-15}\cdot\Delta f$ |
| **Comparator ($V^2$)** | $5.30\times10^{-16}\cdot\Delta f$ | 3 (operating full time) | $1.59\times10^{-15}\cdot\Delta f$ |
| **Total Noise of ADC ($V^2$)** | | | $\mathbf{4.86\times10^{-15}\cdot\Delta f}$ |

## 4.4 Pipeline ADC Noise Analysis

Figure 4.11 shows a typical pipeline scheme. A pipeline ADC basically consists of numerous consecutive stages, each stage contains a sub-ADC, an inter-stage sample-and-hold circuit (SHC), a sub-digital-to-analog converter (sub-DAC), and a substractor

that includes an amplifier to provide gain. Each stage generates a coarse $m_i$-bit. The final stage, however, only includes an inter-stage SHC and a fine ADC since no analog conversion will be required [51]. To obtain 12-bit resolution, the proposed pipeline ADC is designed to have three stages, each stage contributes 4-bit resolution.

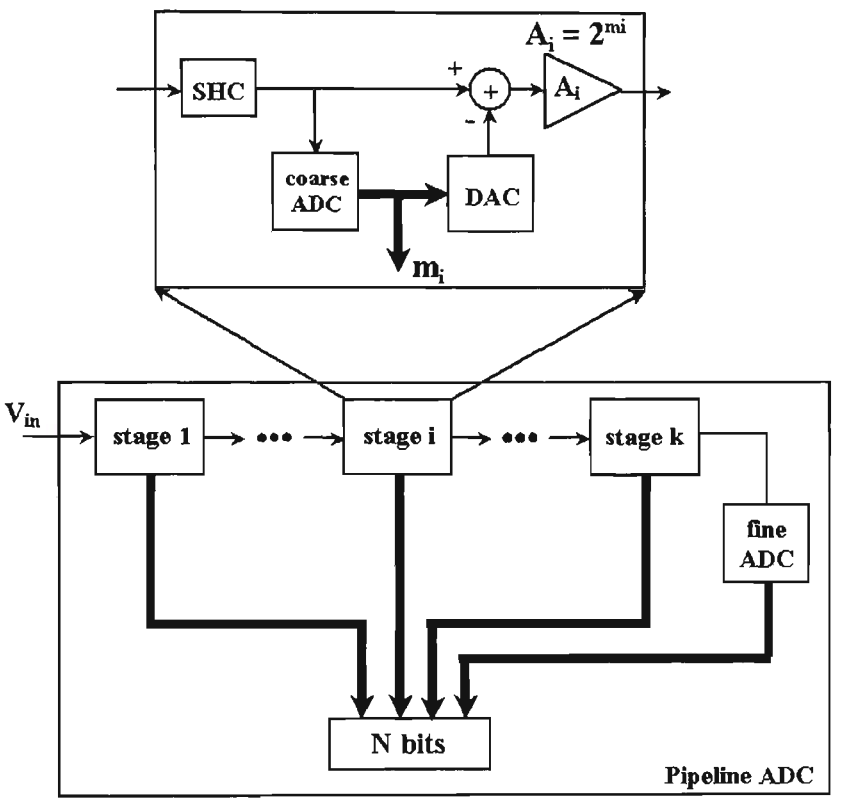



Figure 4.11 Pipeline ADC Architecture.

Figure 4.12 depicts the detailed implementation of 4-bit one stage of a 4-stage pipeline ADC. Flash ADCs are typically employed as sub-ADCs in a pipeline ADC architecture. In this pipeline ADC scheme, a modified flash ADC, which was described in Section 3.6.2, is used instead of the traditional full flash ADC to reduce design complexity and power dissipation.

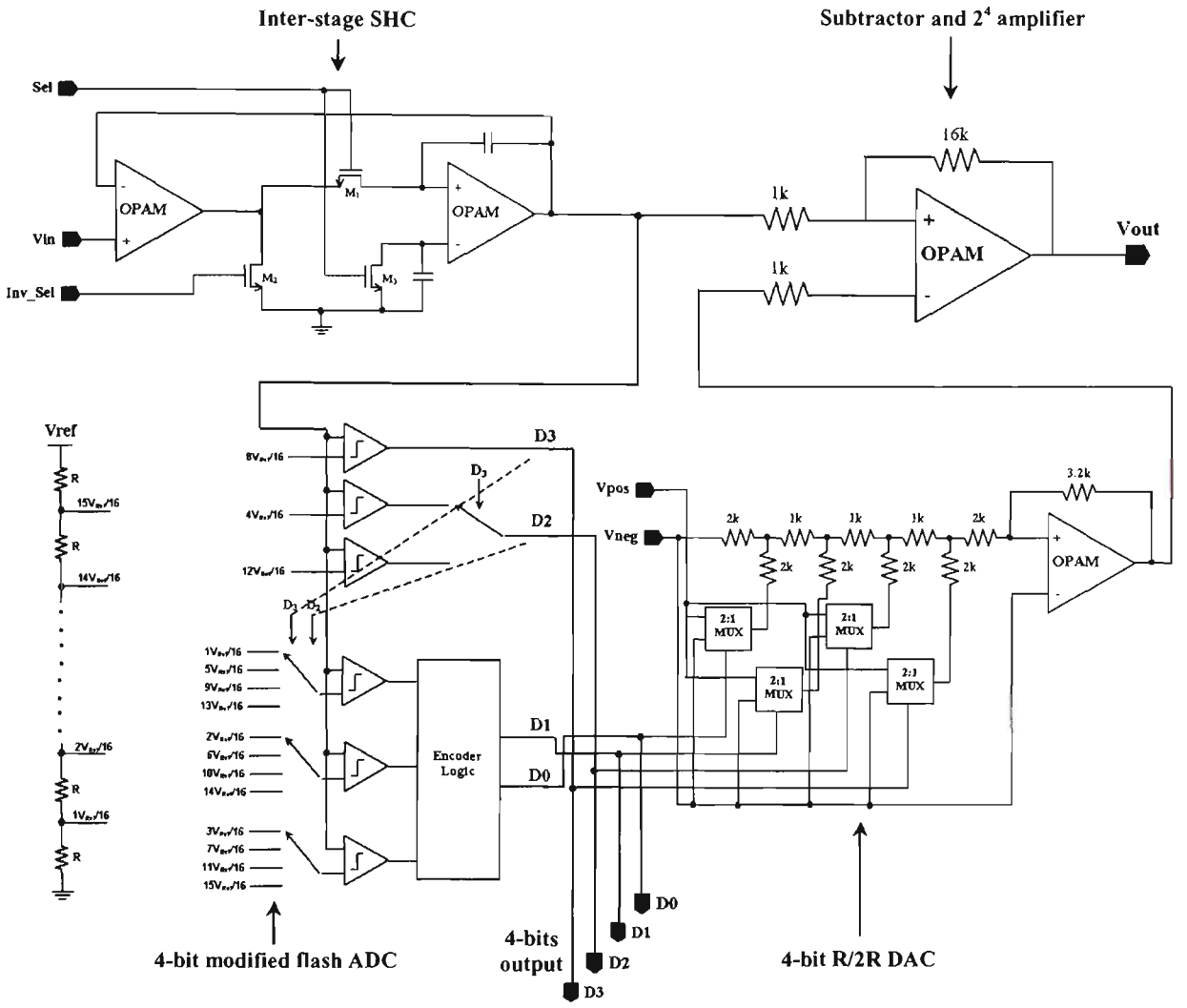



Figure 4.12 A 4-bit single stage block employed in the pipeline ADC.

In the following section, a mathematical model of noise in the proposed reduced complexity 12-bit pipeline ADC is presented to demonstrate the effect of noise on the device performance.

## 4.4.1 Sub-ADC Noise Analysis

The modified flash ADC was fully analysed for noise in Section 4.3. The modified flash ADC generates a total noise power of $4.86\times10^{-15}\cdot\Delta f$ ($V^2$) at a sampling frequency

of 500MHz. Using the technique described in Section 4.3, the noise in the other building block components in the 12-bit pipeline ADC will be analysed.

### 4.4.2 Sub-DAC Noise Analysis

The 4-bit sub-DAC consists of one OPAM, four 2:1 multiplexers (MUX), five 1kΩ-resistors and five 2kΩ-resistors. To obtain the overall noise for the 4-bit sub-DAC, initially each component is analysed for noise.

2:1 MUX has been analysed for noise in Section 4.3.2 and it generates a total of noise power of $8.82\times10^{-16}\cdot\Delta f$ ($V^2$) at an operating frequency of 500MHz.

Using the technique described in Section 4.3, an OPAM [106], employed within the sub-DAC, is analysed for noise. By equating the output noise current that is contributed by all the MOS noise sources with the output noise current that is generated by an equivalent input noise source, we can determine the equivalent input noise source of the OPAM as shown in equation (4.33):

$$\overline{v_{OPAM}^2} = \frac{1}{g_{m1}^2}\left[29\times\overline{v_1^2}\times g_{m1}^2 + 20\times\overline{v_3^2}\times g_{m3}^2 + 3\frac{\overline{v_{R1}^2}}{R_1}\right] \tag{4.33}$$

where $\overline{v_i^2}$ ($i$ = 1,3) is the noise generator of transistor $M_i$ which can be calculated by (4.4), $\overline{v_{R1}^2}$ represents a passive resistor noise generator calculated using equation (4.16).

Using equation (4.16), at 500 MHz operating frequency, one 1kΩ resistor and one 2kΩ resistor in the sub-DAC generate a noise power of $1.66\times10^{-17}\cdot\Delta f$ ($V^2$) and $3.32\times10^{-17}\cdot\Delta f$ ($V^2$) respectively. Using equation (4.33), one OPAM in the DAC will generate a noise power of $1.54\times10^{-15}\cdot\Delta f$ ($V^2$) at an operating frequency of 500 MHz. Besides, one 2:1 MUX in the DAC will generate a noise power of $4.43\times10^{-16}\cdot\Delta f$ ($V^2$) at 500 MHz operating frequency. Therefore the 4-bit sub-DAC will generate a total noise power of $3.56\times10^{-15}\cdot\Delta f$ ($V^2$) at this frequency.

### 4.4.3 Inter-stage SHC Noise Analysis

In the same design structure, the inter-stage SHC will be considered for noise in this section. It comprises of two OPAM and three transistors, as illustrated in Figure 4.12. Using equation (4.4), one transistor in the inter-stage SHC stage generates a noise power of $5.90\times10^{-19}\cdot\Delta f$ ($V^2$) at an operating frequency of 500 MHz. Using equation (4.33), one OPAM in the designed SHC generates a noise power of $1.54\times10^{-15}\cdot\Delta f$ ($V^2$) at 500 MHz operating frequency. Therefore the entire SHC will generate a total noise power of $3.07\times10^{-15}\cdot\Delta f$ ($V^2$) at this frequency.

### 4.4.4 Inter-stage Amplifier Noise Analysis

Using similar technique (methodology), the total noise power generated by the designed inter-stage amplifier is analysed. The amplifier comprises of one OPAM and three resistors (two 1kΩ and one 16kΩ). The noise power generated within the OPAM and

the resistors can be determined by equation (4.33) and (4.16) respectively. Therefore, it is possible to determine that the amplifier generates total noise power of $1.84\times10^{-15}\cdot\Delta f$ ($V^2$) at an operating frequency of 500MHz.

### 4.4.5 The Proposed 12-bit Pipeline ADC Noise Performance

Table 4.4 presents a summary of the noise analysis for each stage within the 12-bit pipeline ADC. Since the noise analysis presented in this chapter is concentrated on the total noise generated within the ADC itself, it is feasible to assume that the input signal to the 12-bit pipeline ADC is noiseless. In another word, the input noise power to the ADC stage 1 is zero. From the second stage, however, the noise generated within its previous stage will be considered as its input noise power.

In addition, as illustrated in Figure 4.12, each ADC stage generates two output signals, its output digital signal and an analog signal to the next stage. Therefore, the total noise power seen from output port of each stage only includes the noise generated within the SHC and the sub-ADC. While the total noise power delivered to the next stage includes the total noise power of the inter-stage amplifier and the noise power of the sub-ADC, the SHC and the sub-DAC with the amplification factor of $2^4$, which is the gain of the inter-stage amplifier. The total noise power of the ADC is also calculated and presented in this table.

Table 4.4 : Summary of noise power in the designed 12-bit pipeline ADC

| Component | Noise in one component | Amplification factor | Noise power to output | Amplification factor | Noise power to next stage |
|---|---|---|---|---|---|
| ***4-bit ADC Stage 1*** | | | | | |
| Stage Input Noise Power ($V^2$) | $0 \cdot \Delta f$ | 1 | $0 \cdot \Delta f$ | 16 | $0 \cdot \Delta f$ |
| Coarse ADC ($V^2$) | $4.86\times10^{-15} \cdot \Delta f$ | 1 | $4.86\times10^{-15} \cdot \Delta f$ | 16 | $7.78\times10^{-14} \cdot \Delta f$ |
| Inter-stage SHC ($V^2$) | $3.07\times10^{-15} \cdot \Delta f$ | 1 | $3.07\times10^{-15} \cdot \Delta f$ | 16 | $4.91\times10^{-14} \cdot \Delta f$ |
| Sub-DAC (V2) | $3.56\times10^{-15} \cdot \Delta f$ | N/A | N/A | 16 | $5.70\times10^{-14} \cdot \Delta f$ |
| Inter-stage Amplifier ($V^2$) | $1.84\times10^{-15} \cdot \Delta f$ | N/A | N/A | 1 | $1.84\times10^{-15} \cdot \Delta f$ |
| **Noise power to output ($V^2$)** | | | **$7.93\times10^{-15} \cdot \Delta f$** | | |
| **Noise power to next stage ($V^2$)** | | | | | **$1.86\times10^{-13} \cdot \Delta f$** |
| | | | | | |
| ***4-bit ADC Stage 2*** | | | | | |
| Stage Input Noise Power ($V^2$) | $1.86\times10^{-13} \cdot \Delta f$ | 1 | $1.86\times10^{-13} \cdot \Delta f$ | 16 | $2.98\times10^{-12} \cdot \Delta f$ |
| Coarse ADC ($V^2$) | $4.86\times10^{-15} \cdot \Delta f$ | 1 | $4.86\times10^{-15} \cdot \Delta f$ | 16 | $7.78\times10^{-14} \cdot \Delta f$ |
| Inter-stage SHC ($V^2$) | $3.07\times10^{-15} \cdot \Delta f$ | 1 | $3.07\times10^{-15} \cdot \Delta f$ | 16 | $4.91\times10^{-14} \cdot \Delta f$ |
| Sub-DAC (V2) | $3.56\times10^{-15} \cdot \Delta f$ | N/A | N/A | 16 | $5.70\times10^{-14} \cdot \Delta f$ |
| Inter-stage Amplifier ($V^2$) | $1.84\times10^{-15} \cdot \Delta f$ | N/A | N/A | 1 | $1.84\times10^{-15} \cdot \Delta f$ |
| **Noise power to output ($V^2$)** | | | **$1.94\times10^{-13} \cdot \Delta f$** | | |
| **Noise power to next stage ($V^2$)** | | | | | **$3.17\times10^{-12} \cdot \Delta f$** |
| | | | | | |
| ***4-bit Fine Stage (final stage)*** | | | | | |
| Stage Input Noise Power ($V^2$) | $3.17\times10^{-12} \cdot \Delta f$ | 1 | $3.17\times10^{-12} \cdot \Delta f$ | N/A | N/A |
| Coarse ADC ($V^2$) | $4.86\times10^{-15} \cdot \Delta f$ | 1 | $4.86\times10^{-15} \cdot \Delta f$ | N/A | N/A |
| Inter-stage SHC ($V^2$) | $3.07\times10^{-15} \cdot \Delta f$ | 1 | $3.07\times10^{-15} \cdot \Delta f$ | N/A | N/A |
| **Noise power to output** | | | **$3.18\times10^{-12} \cdot \Delta f$** | | |
| | | | | | |
| ***Total 12-bit pipeline noise ($V^2$)*** | | | **$3.38\times10^{-12} \cdot \Delta f$** | | |

## 4.5 Noise Analysis of the DAQ System Building Block Components

The noise analysis of other building block components in the DAQ system outside the ADC is presented in section. The analog MUX has been analysed in Sections 4.3.2 and 4.3.3 for the total noise generated within the device itself. Amplifiers are analysed for noise in Section 4.4.4 at an operating frequency of 500MHz. SHC has been analysed for noise in Section 4.4.3 and it generates a total noise power of $3.07\times10^{-15} \cdot \Delta f$ ($V^2$) at an operating frequency of 500MHz.

Using the technique (methodology), the anti-aliasing filter has also been analysed for noise. The filter consists of two OPAMs, twelves transistors and six capacitors, as illustrated in Figure 3.3. Noise analysis shows that the filter generates a total noise of $3.21\times10^{-15}\cdot\Delta f$ ($V^2$) at an operating frequency of 500MHz. Table 4.5 presents the summary of the noise analysis of the constituent blocks of a DAQ system at an operating frequency of 500MHz.

Table 4.5 : Summary of noise power in MUX, anti-aliasing filter, PGA and SHC

| Component | Total Noise |
|---|---|
| 12:1 MUX | $8.72\times10^{-16}\cdot\Delta f$ ($V^2$) |
| PGA | $3.44\times10^{-15}\cdot\Delta f$ ($V^2$) |
| Anti-aliasing Filter | $3.21\times10^{-15}\cdot\Delta f$ ($V^2$) |
| SHC | $3.07\times10^{-15}\cdot\Delta f$ ($V^2$) |
| ADC | $3.38\times10^{-12}\cdot\Delta f$ ($V^2$) |

## 4.6 Conclusion

The latch-type comparator, proposed and optimised in Chapter 3, is the most critical component in the modified flash Analog-to-Digital Converter (ADC) and is employed in the proposed pipeline ADC architecture. The noise generated within the comparator is analysed because it will significantly affect the overall noise performance of the pipeline ADC. The result shows that the NF of the designed comparator is large at low frequency due to the flicker (1/f) noise component. However, the flicker noise does not commonly extend into the megahertz region, where the NF becomes constant due to the thermal noise only. The comparator NF at 500MHz is 4.747dB.

In order to analyse the noise generated within the modified flash ADC architecture, the probability of each of these comparators is calculated mathematically in order to find out how much of the load each comparator carries. The probability of a certain comparator being 'on' or 'off' will affect the noise that the new modified flash ADC will generate. From the probability analysis of each comparator, it can be stated that the six comparators are equivalent to three of the comparators working full time. Results indicate that the modified flash ADC architecture generates total noise power of $4.86\times10^{-15}.\Delta f$ ($V^2$) at an operating frequency of 500MHz.

A methodology to determine the total noise power of the high performance pipeline ADC with reduced complexity, which was proposed in Chapter 3, has been presented. At operating frequency of 500MHz, the 12-bit pipeline ADC generates a total noise power of $3.38\times10^{-12}\cdot\Delta f$ ($V^2$). Using the same methodology, the other constituting components, including the 12:1 MUX, PGA, anti-aliasing filter and SHC, have been analysed for noise. Analysis shows that the total noise power generated by the 12:1 MUX, PGA, anti-aliasing filter and SHC are $8.72\times10^{-16}\cdot\Delta f$ ($V^2$), $3.44\times10^{-15}\cdot\Delta f$ ($V^2$), $3.21\times10^{-15}\cdot\Delta f$ ($V^2$) and $3.07\times10^{-15}\cdot\Delta f$ ($V^2$) respectively. The developed methodology provides a good estimation of the noise generated by the circuit and gives an accurate prediction on the circuit noise performance. Also, such methodology provides good guide for further improvement of the circuit performance.

The implementation of the final DAQ IC, employing the proposed building block components, will be presented in Chapter 5 along with a new proposal for a reconfigurable architecture for bio-medical and power system protection application.

# Chapter 5

# Multi-Channel Data Acquisition System Implementation

## 5.1 Introduction

This chapter presents the implementation of a multi-channel data acquisition (DAQ) system employing the recommended building block components that have been proposed in Chapter 3.

Also, in this chapter, a communication interface compatible to the Peripheral Component Interconnect (PCI) bus standard will be described so that the proposed DAQ system is able to communicate with and transfer data to and from a Personal Computer (PC) or a Microprocessor. PCI bus standard originated by Intel in the early 1990s and it was first adopted for use in personal computers in about 1994 with Intel's

introduction of the "Saturn" chipset and "Alfredo" motherboard for the 486 processor. With introduction of chipsets and motherboards for the Intel Pentium processor, PCI largely replaced earlier bus architectures such as Extended Industry Standard Architecture (EISA), Video Electronics Standards Association (VESA) Local Bus, Micro Channel Bus, etc. PCI defines methods for orderly transfer of data, address and other status commands and defines the physical details of the interface [17].

The focus of this chapter is also on the design and implementation of DAQ system controller. This controller is responsible for generating strobe signals at the correct time spacing so that all the constituent components in the proposed DAQ system perform their functions optimally and correctly. It is also responsible for communicating with a PC to transfer converted data and other status signals from the DAQ system to the PC's memory and to receive commands, configurations and instructions from the PC. The system controller is a significant element that synchronise the function of all constituent components and also an intelligent device behind the DAQ architecture.

The last section of this chapter describes the layout implementation of the proposed DAQ system. The DAQ unit comprises of both digital and analog circuits. In implementing layouts for digital circuits, the speed and the area are the two most important issues. In contrast, in doing layout for analog circuits, performance characteristics such as speed, area, power consumption and timing should all be considered simultaneously. Due to the fact that the DAQ system is a mixed-signal device, mixed signal layout issues must be considered.

This chapter is structured as follows: Section 5.2 presents the implementation of the proposed DAQ system. Details of the design and implementation of the system interface and the implementation of a system controller are also presented in this Section. Section 5.3 presents the layout issues and considerations for the proposed DAQ system. The DAQ system performance and layout implementation are described in Section 5.4. Conclusions of this chapter are presented in Section 5.5.

## 5.2 System Design and Implementation

This section is dedicated for the integration of a DAQ system on a single Integrated Circuit (IC) employing the proposed building block components that have been selected, implemented and tested in detail in the previous chapter. The building block components include an analog multiplexer (MUX), a Programmable Gain Amplifier (PGA), an anti-aliasing filter, a Sample-and-Hold circuit (SHC) and an Analog-to-Digital converter (ADC). Each component has been implemented, tested and optimised for high-accuracy and high-speed as well as low power consumption and reduced complexity.

Figure 5.1 illustrates the block diagram of the implemented DAQ system. A system controller has been incorporated into the DAQ design. The system controller is responsible for generating strobe signals to ensure the proper function of the constituent components and for communicating with a host PC, a Microprocessor or a Digital Signal Processing (DSP) device through an appropriate communication interface. The

system controller must ensure following general phases of a data acquisition process [17, 107]:

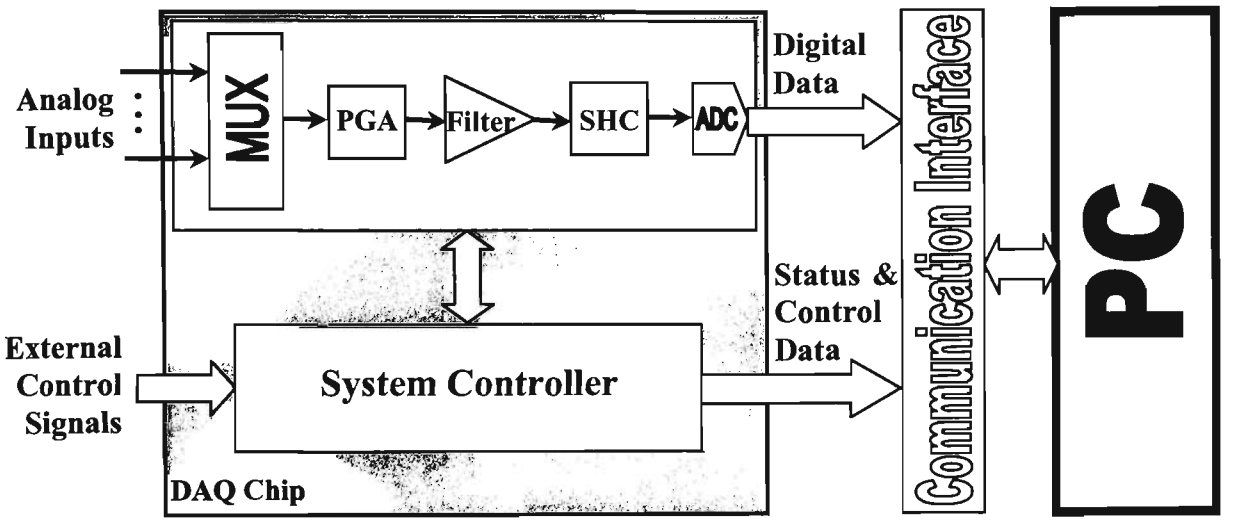



Figure 5.1 Block Diagram of the proposed DAQ system.

1. Once initialised by the host PC, the Microprocessor or the DSP device, the system controller generates control signals to the MUX so that the required channel signal to be converted will be fed to the PGA. It also sets the PGA gain and the filter cut-off frequency that are selected by the host PC. The system controller also puts the SHC in sample mode.
2. The system controller waits for the MUX to settle, the PGA output delay time and lastly for the filter delay time.
3. The SHC is put to hold mode, and the system controller waits for the SHC's aperture time, for the output to become stable.
4. Subsequently, a start signal will be issued to the ADC to initialise the analog-to-digital (A/D) conversion. The system controller waits for the ADC to complete its conversion process.

5. It then generates a request signal to the host PC to notify the availability of the converted data and to request a data transaction.

In order to integrate the complete DAQ system on a single IC, there are two major aspects to be addressed. The first aspect is the system interface mechanism with a host PC or an external DSP device that will be presented in Section 5.2.1. The other is the realisation and implementation of a system controller, which will be presented in Section 5.2.2.

### 5.2.1 System Interface Design

In order to transfer data between the proposed DAQ unit and a PC, a Microprocessor or an external DSP device, the system controller of the DAQ unit will be implemented compatible with the PCI bus standard. The PCI bus is a high performance bus for interconnecting chips, expansion boards, and processor/memory subsystems. It originated at Intel in the early 1990s as a standard method of interconnecting chips on a board. It was later adopted as an industry standard administered by the PCI Special Interest Group (PCI SIG). Under the PCI SIG the definition of PCI was extended to define a standard expansion bus interface connector for peripheral devices [17, 107].

On September 11, 1998 the PCI SIG announced that Compaq, Hewlett-Packard, and IBM had submitted a new specification for review called Peripheral Component Interconnect Extended (PCI-X) architecture. The proposed standard allows for increases in PCI bus speed up to 133 MHz. It also includes suggested changes in the

PCI communications protocol affecting data transfer rates and electrical timing requirements. The present revision adds two new speed grades: PCI-X 266 and PCI-X 533, offering up to 4.3 gigabytes per second of bandwidth, 32 times faster than the first generation of PCI [108, 109].

According to the PCI and PCI-X architecture standard, the DAQ unit interface consists of twelve data lines for the 12-bit data output, a master clock (CLK) that provides the timing reference for all transfers on the PCI bus, a reset signal (RST) that is driven active low to cause a hardware reset of a PCI device, two arbitration lines (REQ and GNT) to request the use of the bus, two error reporting lines (PAR and PERR) for detecting data parity errors during all PCI transactions and seven interface control lines (FRAME, IRDY, TRDY, STOP, LOCK, IDSEL, and DEVSEL) that coordinate the transfer of data. It also consists of four command lines that multiplex Bus Command (BC) and Byte Enable (BE) signals. During the address phase of a transaction, the four command lines carry the BC that defines the type of transfer to be performed. During the data phase of a transaction, these signals carry BE information. The details of these data, interface control and command lines are described in Table 5.1 [107].

For error detection during a PCI transaction, PAR and PERR are introduced. PAR is even parity over the D[11:0] and BC/BE[3:0] signals. Even parity implies that there is an even number of '1's on the D[11:0], C/BE[3:0], and PAR signals. When a data parity error is detected during all PCI transactions, PERR is driven low two clock periods after the data phase with bad parity. After being asserted low, PERR must be driven high one clock before being tri-stated to restore the signal to its inactive state. This

ensures the signal does not remain low in the following cycle because of a slow rise due to the pull-up [108, 109].

Table 5.1 : Six Groups of Signal Lines in PCI interface standard.

| Type | Name | Description |
|---|---|---|
| **Data Lines** | D11 – D0 | Digital Data |
| **System Lines** | CLK | System Clock |
| | RST | Reset |
| **Arbitration Lines** | REQ | Request |
| | GNT | Grant |
| **Error Reporting Lines** | PAR | Parity |
| | PERR | Parity Error |
| **Command Lines** | BC3 – BC0 | Bus command/Byte Enable |
| **Interface Control Lines (Handshaking)** | FRAME | Cycle Frame |
| | IRDY | Initiator Ready |
| | TRDY | Target Ready |
| | STOP | Stop |
| | LOCK | Lock |
| | IDSE | Initialisation Device Select |
| | DEVSEL | Device Select |

To activate a data transaction, the initiator (the DAQ unit) first sends the REQ signal to request use of the bus. The target (the host PC or a DSP device), then, will activate the GNT signal to indicate that the PCI device's request to use the bus has been granted. Then, data is transmitted continuously on the PCI parallel interface and is coordinated by the handshaking voltage signal on the seven interface control lines. Handshaking ensures that the initiator will put a data on the bus only when the target is ready and will keep the data on the bus until it has been read by the target. It also ensures that the target will accept data only when a valid digital value is available on the data bus [107].

Figure 5.2 illustrates a handshaking timing diagram for a data transaction on the PCI bus. To initiate a data transaction, the initiator asserts a FRAME true (voltage low) and

places a read command on the BC/BE signals. The initiator drives BE signals and then asserts IRDY low indicating valid write data is available. The target asserts DEVSEL low as an acknowledgment it has positively receive the read command from the initiator (the target may not assert TRDY before DEVSEL). Subsequently, the target drives TRDY low indicating it is ready to capture data. The data will be transmitted continuously as both IRDY and TRDY are low [108, 109] .

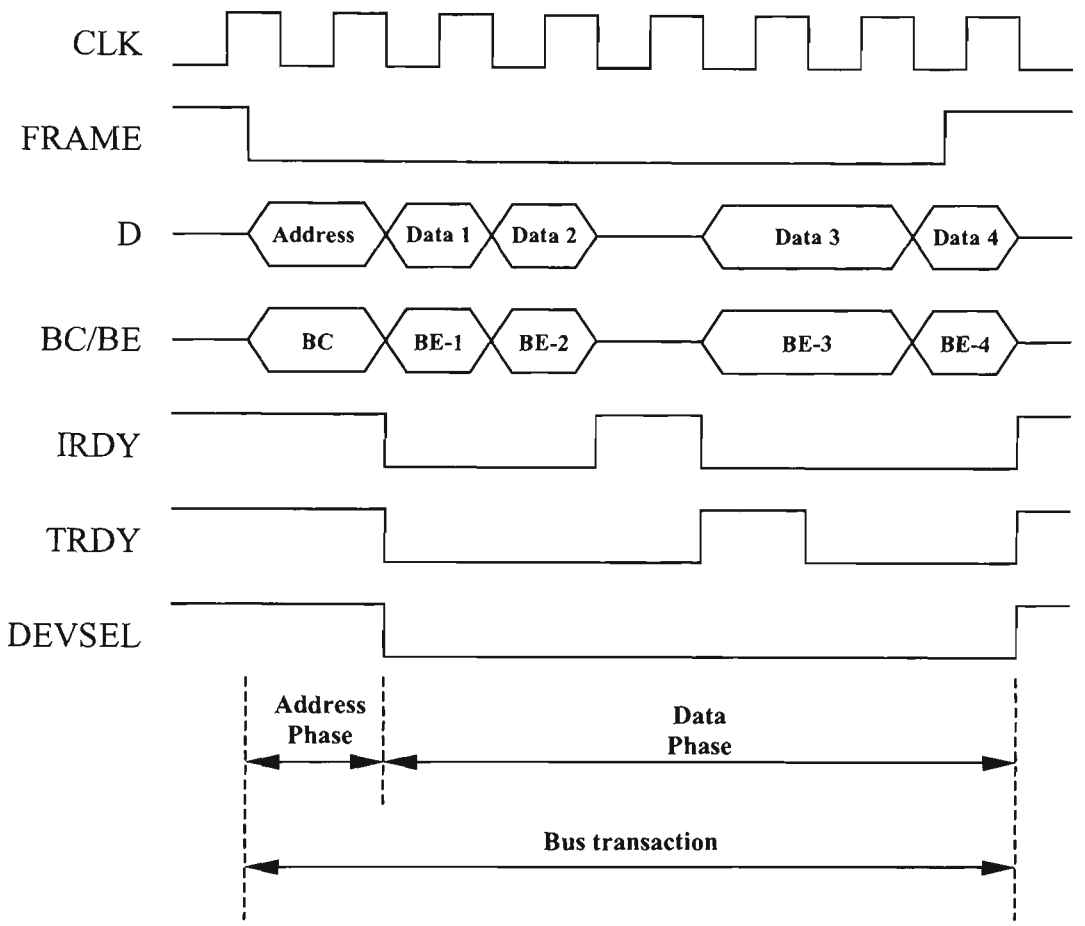



Figure 5.2 The BPIB Handshaking Timing Diagram.

During the data phase, the initiator can deassert IRDY indicating it is not ready to provide the next data, thus, the target must wait until the IRDY to go low again before reading the next data. The target can deassert TRDY indicating it is not ready to capture the next data. In this case, the initiator must wait for the TRDY line to go low, i.e. the target is ready to receive data, before taking the data off the bus [108, 109].

To terminate the data transaction, the initiator drives FRAME high indicating this is the final data phase. After capturing the current data, the target will drive TRDY high to signal the talker that the last data has been successfully accepted. The initiator drives IRDY high and removes its data from the bus. After this time D and BC/BE lines are tri-stated, and FRAM, IRDY, TRDY, and DEVSEL signals are high. It is noted that if the initiator intends to perform a transaction with only a single data phase, then it will return FRAME back high after only one cycle. If multiple data phases are to be performed, the initiator will hold FRAME low in all but the last data phase. The initiator signals its intent to perform a master termination by driving FRAME high during the last data phase of a transaction [108, 109].

The LOCK, STOP and IDSEL are additional control signals to ensure a proper PCI data transaction. LOCK may be asserted by an initiator to request exclusive access for performing multiple transactions with a target. It prevents other initiators from modifying the locked addresses until the agent initiating the lock can complete its transaction. When an abnormal/erroneous situation occurs, STOP can be driven low by the target to request the initiator terminate the current transaction. IDSEL is used as a chip select during PCI data transactions. IDSEL is driven by the PCI system and is unique on a per slot basis [108, 109].

The DAQ controller should be designed to consider all the PC interface control signals. Such controller is the heart of the DAQ system and responsible for the internal and external execution and generation.

## 5.2.2 System Controller Implementation

The system controller is an intelligent device behind the DAQ architecture. It is responsible to receive control signals from outside environment and generate output signals representing the progress of the data conversion procedure to the outside world. Its functions also include executing the input command signals to generate the necessary control signals to the constituent components of the DAQ system for a proper data conversion process. The input-output (I/O) signals between the outside environment and the DAQ system are depicted in Figure 5.3.

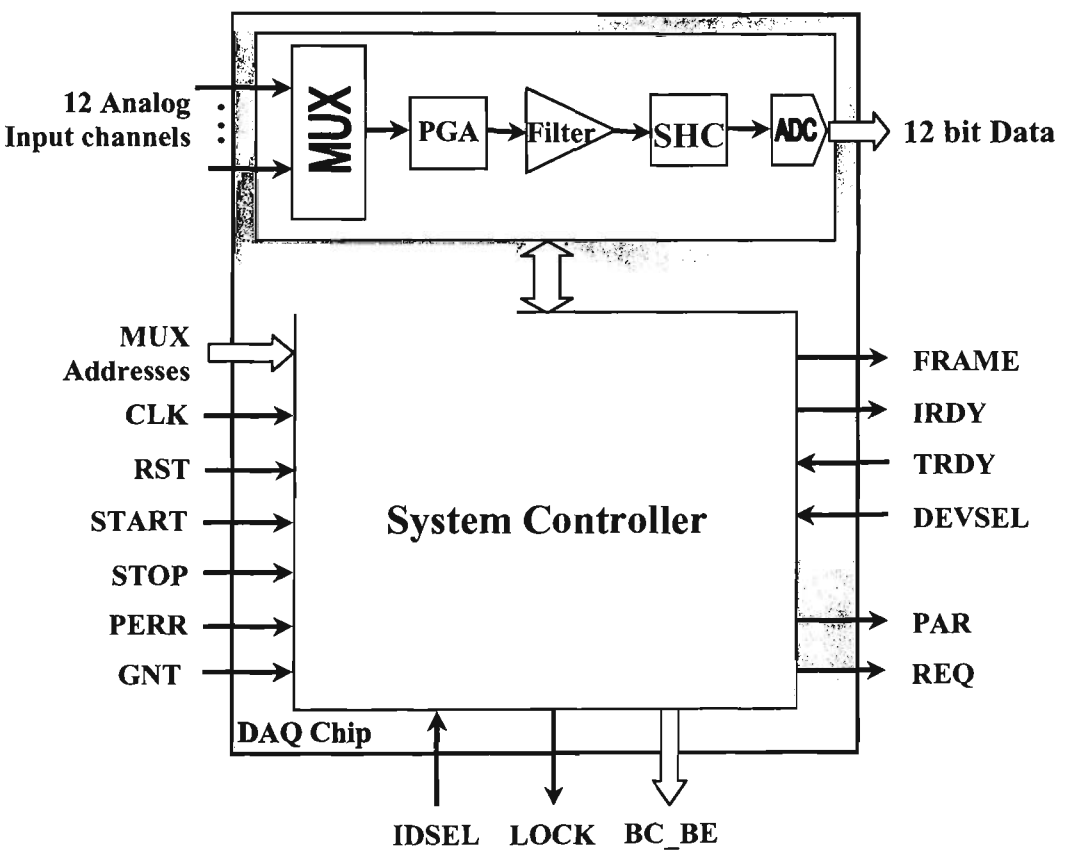



Figure 5.3 I/O signals of the designed DAQ system.

The I/O signals include the 12 analog channels, 4-bit MUX addresses (to show which channel to be processed), a system clock (CLK) signal, a reset (RST) signal, two

arbitration lines (REQ and GNT), two error reporting lines (PAR and PERR), interface control signals (FRAME, IRDY, TRDY, STOP, LOCK, IDSEL, and DEVSEL) and a start signal (to enable the conversion process). Based on which input channel is selected to be processed, the DAQ system should set the suitable system filter cut-off frequency and the PGA gain and then perform its functions to produce 12-bit digital data. At the end of the conversion, the REQ signal will be enabled to interrupt a host PC that the data is ready to be read.

The system controller should make logical decisions based on the input signals to instruct the constituent components, including the 12:1 MUX, PGA, Filter, SHC and 12-bit 3-stage pipeline ADC, to perform their functions properly at the correct instance. Figure 5.4 shows the timing diagram of the constituent components that are directed by the system controller (time not to scale). The designed pipeline ADC includes three consecutive stages, thus the total pipeline ADC conversion time includes the conversion time of the three stages. Besides, the channel selection, signal amplification and filtering can be performed before the start conversion because the SHC will keep the sampled data until a next 'start' signal is applied.

As illustrated in Figure 5.4, the system controller waits for the 'start' signal from the PC before initiating the data acquisition process. After the data acquisition process is completed, a REQ signal is generated as an interrupt to the PC, and thus the PC will no longer waste its processing time by waiting for the completion of the process. After the GNT signal is activated, the controller will assert the FRAME (active low) and

subsequently initiate the handshaking process to transfer the converted data from the DAQ system to the PC.

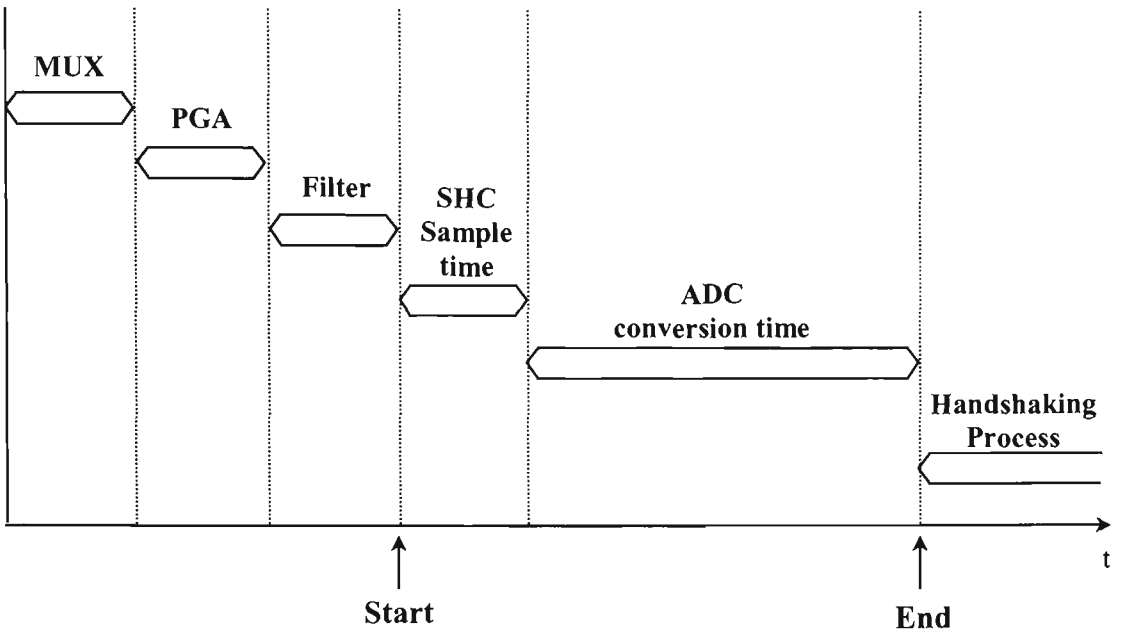



Figure 5.4 DAQ system control signal timing diagram.

To activate the maximum speed mode, the 'start' signal is maintained active high. In this case, the DAQ system will hold the bus, continuously convert data, and then assert IRDY signal (active low) to notify the PC of the availability of the converted data.

One stage of the proposed pipeline ADC includes a SHC, a 4-bit modified ADC, a Digital-to-Analog Converter (DAC) and an inter-stage amplifier, as illustrated previously in Figure 3.22. Therefore, the system controller should send control signals to these elements in the correct order and timing as illustrated in Figure 5.5 (time not to scale). It is noted that since the aperture error of the SHC is very small, the instant the SHC switch to hold mode can be very close to the end of the stage conversion time. It is also noticed that the SHC mentioned in Figure 5.5 is the SHC of the next stage in the pipeline ADC, not the main SHC of the DAQ unit.

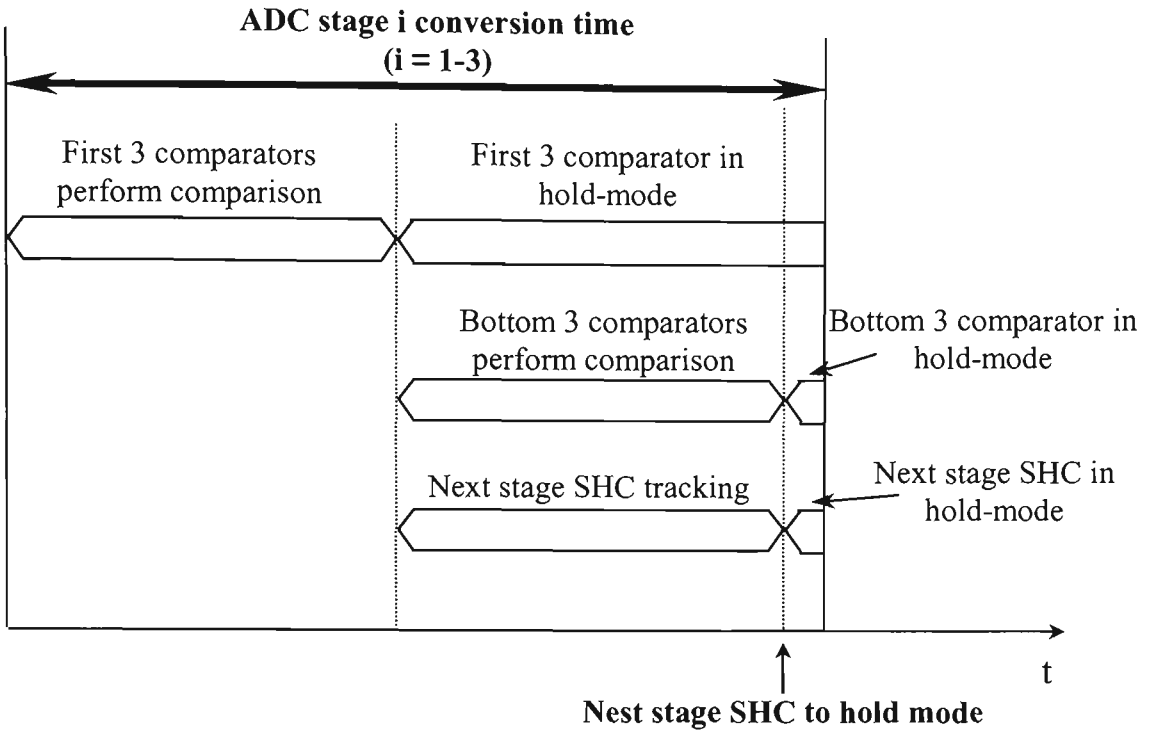



Figure 5.5 One stage pipeline ADC control signal timing diagram.

Figure 5.6 presents the top-level entity of the system controller implemented on ASIC. The controller has been implemented in Analog Environment using full custom 0.18μm Complementary Metal-Oxide Semiconductor (CMOS) process. The analysis results of the system controller are presented in Table 5.2.

Table 5.2 : Performance summary of the system controller ASIC.

| **Property** | **Result** |
|---|---|
| Max delay | 960ps |
| Supply Voltage | 2.5 V |
| Power Consumption @1GHz (master clock) | 1089μW |
| Technology | 0.18μm CMOS |

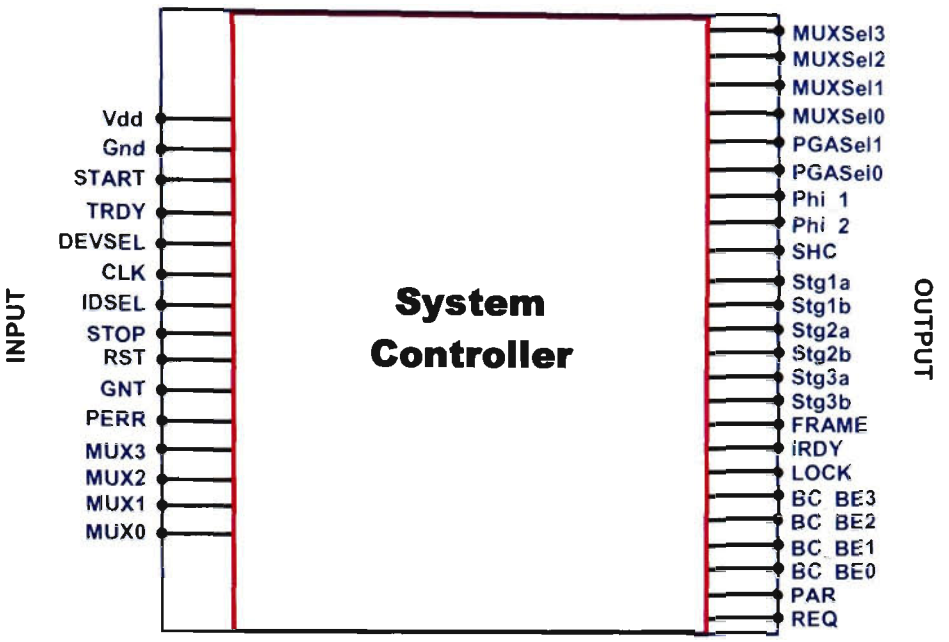



Figure 5.6 System Controller ASIC top-level entity.

## 5.3 DAQ System Layout

This section presents the layout implementation of the proposed DAQ IC. The DAQ unit comprises of both digital and analog circuits. There is a contrast between layout implementation for digital and analog circuits. The speed and the area are the two most critical matters for all digital circuit layout implementation. In contrast, in implementing layout for analog circuits, performance characteristics such as speed, area, power consumption and timing should all be balanced optimally. Without proper layout, the mismatches and the coupled noise would be quite large and would significantly degrade the performance of the analog circuits. Moreover, a good shielding is required to protect critical nodes in analog circuits from being disturbed. Therefore, since the DAQ system is a mixed-signal device, mixed signal layout issues must be considered [93, 110, 111].

Analog ICs, naturally, are more sensitive to noise than digital ICs. Therefore, careful attention must be given to layout issues for any analog design, particularly in a digital environment. Sensitive analog nodes must be protected and shielded from any potential noise sources. Grounding and power supply routing must also be considered when using digital and analog circuitry on the same substrate. Since the majority of the DAQ unit use switches, which are controlled by digital signals, separate routing channels must be provided for each type of signal to minimise the effect of the digital switching on the analog circuitry. Techniques used to increase the success of mixed-signal designs differ in complexity. Approaches regarding minimisation of noise are very critical and should be considered very seriously. A mixed-signal layout approach is shown in Figure 5.7 [112, 113].

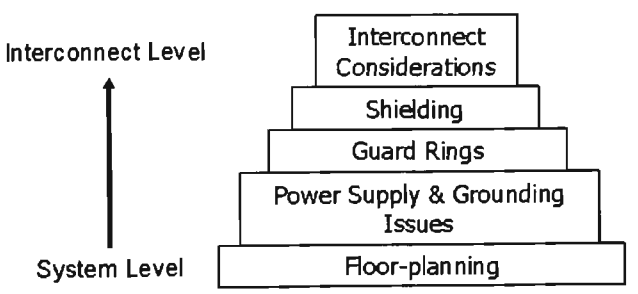



Figure 5.7 Mixed-Signal layout strategy [113].

## 5.3.1 Floor Planning

Floor planing of the design flow involves arranging the circuit blocks on the IC. The goals of floor planning are:

- To arrange the circuit blocks on the IC.
- To decide the location of the I/O pads.

- To decide the location and number of power pads.
- To decide the location of clock distribution nets.
- To minimise the chip area.

The position of responsive analog instances can greatly affect the performance of a circuit. In designing a mixed-signal system, approaches regarding the floor-plan of the circuitry should be analysed before the layout is to take place. The analog circuitry should be classified by the sensitivity of the analog signal to noise. For example, low-level signals or high impedance nodes typically associated with the input signals are considered to be sensitive nodes. These signals should be closely guarded and shielded especially from the digital output pins. High-swing analog circuits such as comparators and output buffer amplifiers should be positioned between the sensitive analog circuits and the digital circuits [112, 113].

The digital circuitry is usually labeled by speed and function. Since digital output buffers are usually designed to drive capacitive loads at very high speeds, they should be kept as far as possible from the sensitive analog signals. The high and low speed digital circuits should be placed between the insensitive analog and the output buffers. Figure 5.8 illustrates these mixed-signal floor-planning approaches [112, 113].

### 5.3.2 Power Supply and Grounding Considerations

Each time analog and digital circuits are on a same chip, noise could be injected from the digital system to the sensitive analog circuitry through the power supply and ground

connections. Much of the intercoupling can be reduced by cautious consideration of how power and ground are supplied to both analog and digital circuits. Figure 5.9 presents three approaches to implement the power and ground connections to digital and analog parts in a mixed-signal design [110, 111].

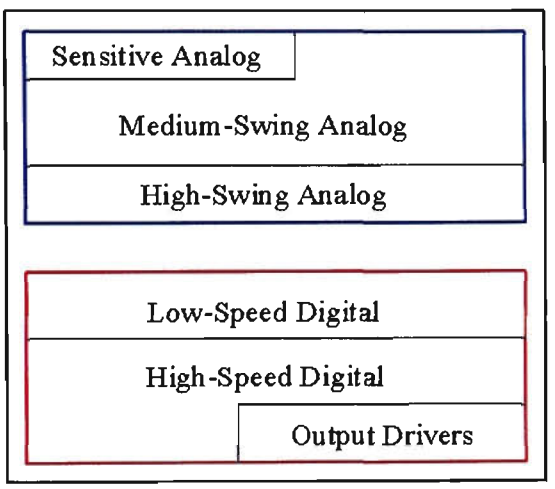



Figure 5.8 Mixed-Signal Floor-Plan.

In Figure 5.9a, the analog and digital circuits share the same routing to a single pad for power and ground. The resistors, $R_1$ and $R_2$ represent the small non-negligible resistance of the interconnects to the pads. The inductors, $L_1$ and $L_2$ represent the inductance of the bonding wire which connects the pads to the pin on the lead frame. Seeing as digital circuitry is characterised by high transient currents due to switching, a small amount of resistance associated with the interconnect can result in major voltage spikes. Low-level analog signals are very sensitive to such interference, therefore resulting in a unreliable analog system [112, 113].

One way to reduce the interference is to exclude the analog and digital circuit from sharing the same interconnect, as illustrated in Figure 5.9b. The routing for the supply and ground for both the analog and digital sections are provided separately. Even

though this removes the parasitic resistance due to the common interconnect, there is still a common inductance due to the bonding wire which will cause interference [112, 113].

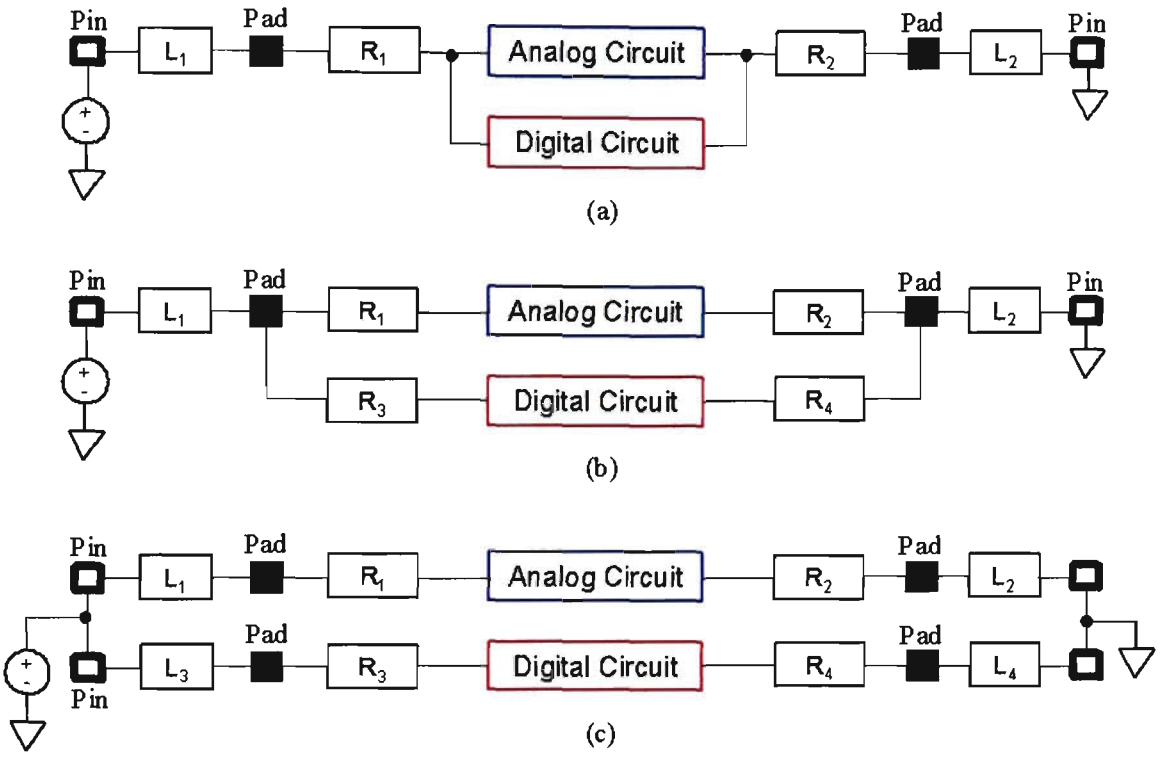



Figure 5.9 Power and ground connection.

Another method that minimises interference even more is the shown in Figure 5.9c. By using separate pads and pins, the analog and the digital circuits are completely decoupled. The current through the analog interconnect is much less sudden than the digital, therefore the analog circuitry has a "quiet" power and ground. However, this technique is dependent on whether extra pins and pads are available for this use. It is a wise choice to use two separate power supplies because if both types of circuits are not powered up simultaneously, latch-up could easily result [112, 113].

### 5.3.3 Guard Rings

The results of noise in an analog circuit can be equally destructive. A typical example would be a high-impedance pin of an operational amplifier located close to a track with a different voltage potential or, even worse, switching noise. A low-impedance guard ring, which separates sensitive sections from higher voltage or noisy environment, is a very useful technique to minimise noise. Low impedance implies that it has low resistance as well as low inductance. Guard rings should be used wisely throughout a mixed-signal environment. This is usually performed on the analog sections of the chip layout [112, 113].

### 5.3.4 Shielding

There have been number of techniques that can shield sensitive, low-level analog signals from noise resulting from digital switching. A shield can take the form of a layer tied to analog ground placed between two other layers, or it can be a barrier between two signals running in parallel.

It is better, if possible, to avoid crossing sensitive analog signals, such as low-level analog input signals, with any digital signals. The parasitic capacitance coupling the two-signal line can be as much as a couple of femto Farad (fF), depending on the process. If it cannot be avoided, then attempt to carry the digital signal using the top layer of metal.

Another situation that should be prevented is running interconnect containing sensitive analog signals parallel and adjacent to any interconnect carrying digital signals. Coupling occurs due to the parasitic capacitance between the lines. If this situation cannot be avoided, then an additional line connected to analog ground should be placed between the two signals. This method can also be used to partition the analog and digital sections of the chip [112, 113].

### 5.3.5 DAQ System Layout

The DAQ system top-level block diagram is presented in Figure 5.10. Partitioning is a critical aspect of the layout implementation and must be considered very decisively. The top-level block diagram of the DAQ ASIC shows all the digital and analog I/Os being at opposites sides, that will satisfy the partitioning requirements

The maximum resolution for the DAQ system is 12 bits where D0...D11 are the digital output pins. Vin1 to Vin12 are the analog input channels to the DAQ system, VrefP and VrefN are the input reference voltages, Vdd_a and Gnd_a are the power supply and ground to the analog section, respectively, Vdd_d and Vss_d are the power supply and ground to the digital section respectively, Vb is the bias voltage. MUX[3..0] is the MUX address to select a channel to be processed. CLK is the master clock of the system, RST is the system reset signal, two arbitration lines (REQ and GNT), two error reporting lines (PAR and PERR). START, FRAME, IRDY, TRDY, STOP, LOCK, IDSEL, BC_BE[3..0] and DEVSEL are the status and control signals for data transaction between DAQ system and a host PC.

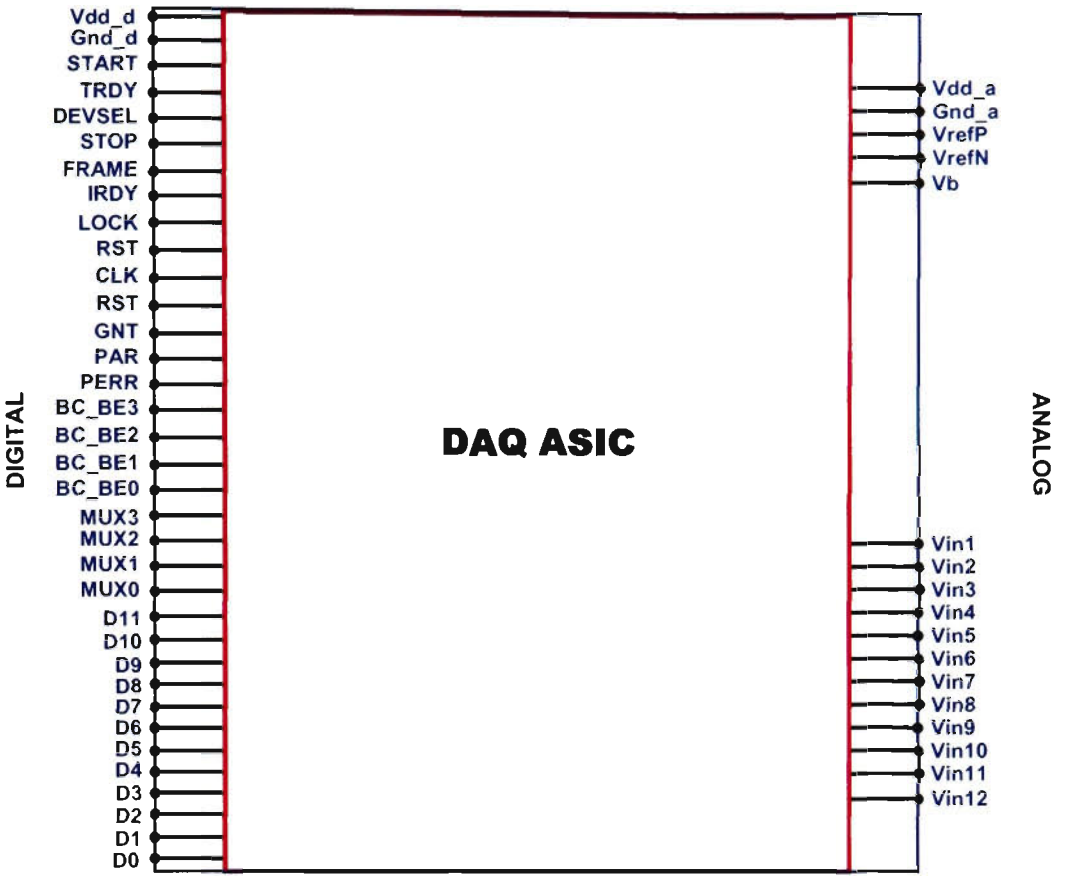



Figure 5.10 Block Diagram of the DAQ ASIC.

The layout of the ADC was performed using Cadence Layout Editor using full custom CMOS 0.18μm technology. Figure 5.11 illustrates the floor plan of the 12-bit multi-channel DAQ system. The DAQ unit floor plan shows the proper partitioning with the analog circuits being separated from the digital circuits. Digital and analog I/O pins are also placed separated from each other as far as possible, preventing the noise from digital pins to affect sensitive analog pins.

Figure 5.12 illustrates the layout of the 12-bit multi-channel DAQ system. Once again the DAQ system layout shows the appropriate partitioning with the analog cells being separated from the digital cells. A guard ring around the analog section is also used to protect and shield the analog cells from noise resulting from digital switching.

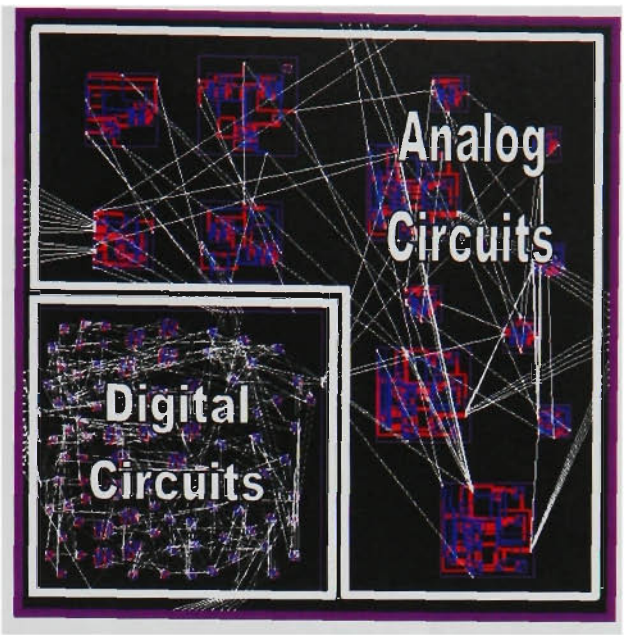



Figure 5.11 Floor-plan of the proposed DAQ system

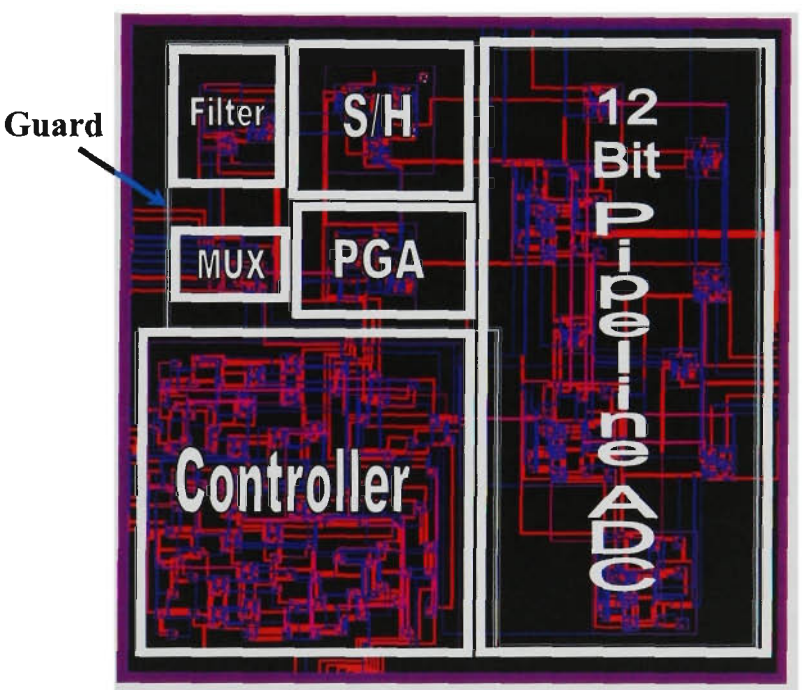



Figure 5.12 Layout implementation of the proposed DAQ system

The results of the layout simulation of the DAQ system have been back annotated and analysed. Table 5.3 presents the simulation results of the DAQ system.

Table 5.3 : Simulation results of the layout DAQ system.

| **Property** | **12-bit DAQ system (using modified flash ADC)** |
|---|---|
| Power Consumption | 67.5mW |
| Max master clock speed | 977MHz |
| Area | $3.72mm^2$ |
| Resolution | 12 bits |
| Technology | 0.18μm CMOS |
| Voltage Supply | 2.5V |

## 5.4 DAQ System Performance Analysis

This section presents the implementation results of the complete DAQ system by integrating the recommended circuit design topologies, including the 12:1 MUX, the PGA, the anti-aliasing filter, the SHC, the 12-bit 3-stage pipeline ADC and the system controller.

Figure 5.13 shows the schematic diagram of the final DAQ system implemented in Cadence Analog Design Environment (Analog Artist) tool.

Two different set of power supply and ground sources are used for the analog and digital sections of the DAQ system, permitting the implementation of separate pads and pins for layout of the analog and the digital circuits of the system. This approach effectively removes the parasitic resistance due to the common interconnect and minimises the interference (noise) that could be injected from the digital system to the sensitive analog circuitry through the power supply and ground connections.

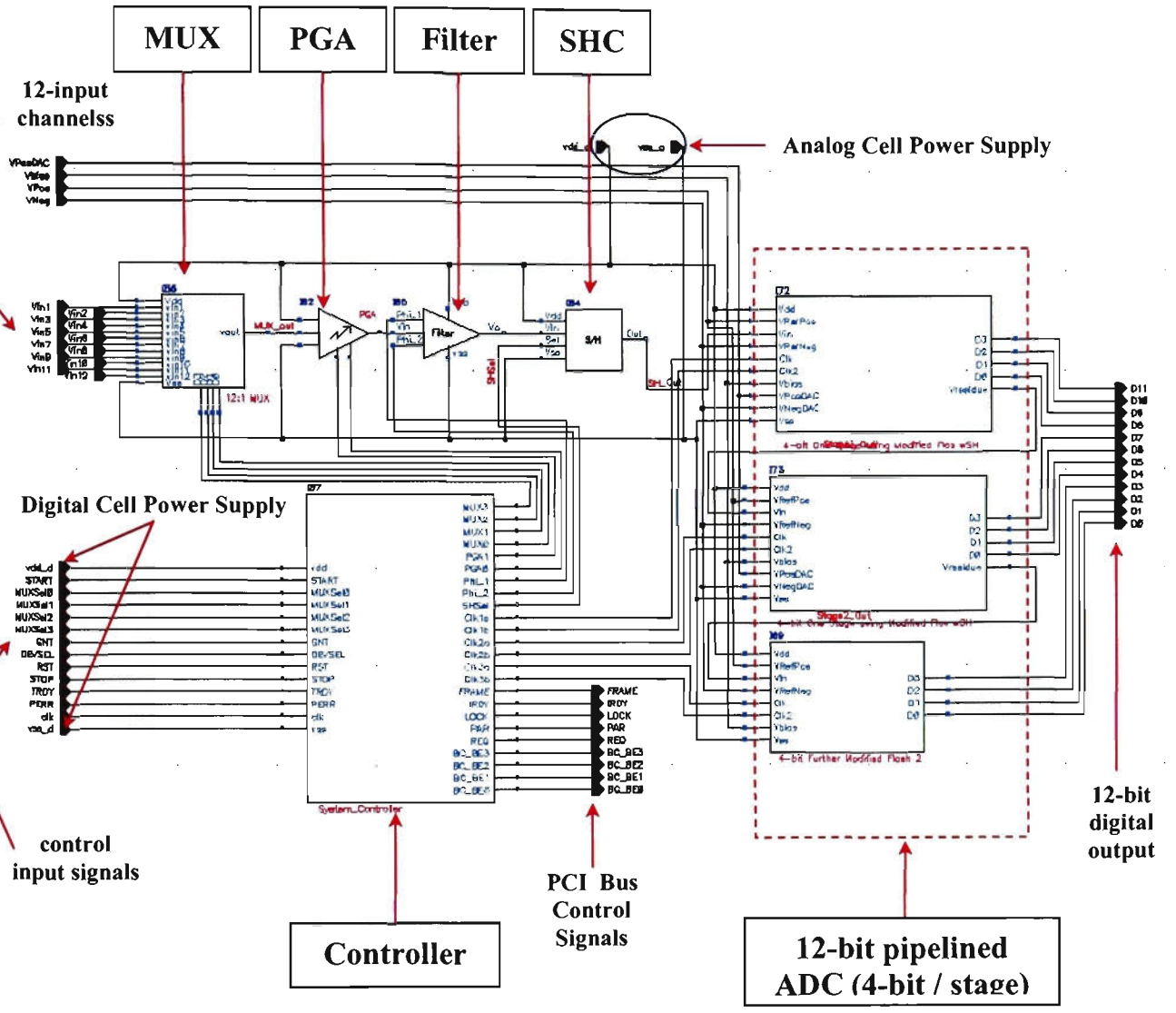



Figure 5.13 DAQ system schematic diagram.

Two DAQ systems using the traditional 4-bit full flash ADC and the modified flash ADC topologies have been both implemented and simulated for comparison to demonstrate the superiority of the modified flash ADC. The performance of the two approaches are summarised in Table 5.4.

Results indicate that the proposed DAQ architecture employing a modified flash ADC architecture operates at 1GHz master clock frequency and achieves a maximum

sampling speed of 125MS/s. It dissipates only 65.6mW of power at this sampling frequency as compared to 97.9mW when traditional flash ADC was used.

Table 5.4 : Comparison results of the two DAQ architecture performance.

| **Property** | **Using traditional flash ADC** | **Using modified flash ADC** |
|---|---|---|
| **Device delay** | | |
| Total delay | 8ns | 8ns |
| Max data rate | 125MS/s | 125MS/s |
| Max master clock speed | 1GHz | 1GHz |
| **Device power consumption @ 1GHz system master clock** | | |
| MUX power consumption | 1.1mW | 1.1mW |
| PGA power consumption | 6.8mW | 6.8mW |
| Filter power consumption | 9.5mW | 9.5mW |
| SHC power consumption | 7.1mW | 7.1mW |
| ADC power consumption | 72.9mW | 40.6mW |
| Controller power consumption | 0.5mW | 0.5mW |
| ***Total Power consumption*** | ***97.9mW*** | ***65.6mW*** |
| **Number of Devices** | | |
| PMOS | 1172 | 860 |
| NMOS | 1211 | 926 |
| Resistors | 87 | 87 |
| Capacitor | 10 | 10 |
| **Other Parameters** | | |
| DNL | ±0.5 LSB | +0.6/-0.5 LSB |
| INL | ±0.5 LSB | ±0.5 LSB |
| Technology | 0.18μm CMOS | 0.18μm CMOS |
| Resolutions | 12 bits | 12 bits |
| Supply Voltage | 2.5V | 2.5V |

Results also indicate that 31% of number of transistors could be saved and a 33% power saving is obtained when the modified flash ADC is used instead of a full flash ADC. This type of DAQ system is well suited for:

- high-speed applications
- low-power applications
- low cost applications

## 5.5 Conclusion

This chapter presented the implementation of a multi-channel 12-bit DAQ system on a single IC by integrating the design recommendations of the building block components proposed in Chapter 3.

In this chapter, a communication interface compatible to the PCI bus standard has been designed so that the proposed DAQ system is able to communicate with and transfer data to and from a host PC or a Microprocessor. The DAQ unit interface consists of twelve data lines for the 12-bit data output, a master clock (CLK) that provides the timing reference for all transfers on the PCI bus, a reset signal (RST) that is driven active low to cause a hardware reset of a PCI device, two arbitration lines (REQ and GNT) to request the use of the bus, two error reporting lines (PAR and PERR) for detecting data parity errors during all PCI transactions and seven interface control lines (FRAME, IRDY, TRDY, STOP, LOCK, IDSEL, and DEVSEL) that coordinate the transfer of data. The PCI has been the most popular, worldwide standard for data communication between a PC and peripheral devices.

The system controller is the intelligence behind the DAQ architecture. It receives control signals from outside environment and generates output signals, representing the progress of the data conversion procedure to the outside world. It is also responsible for generating strobe signals at the correct time spacing so that all the constituent components in the proposed DAQ system perform their functions optimally and correctly to ensure a proper data conversion process. The system controller has been

designed to be compatible with the parallel PCI bus standard. It also generates an REQ signal as an interrupt to the PC, so that the PC will no longer waste processing time by waiting for the completion of the data conversion process.

The complete DAQ system has been implemented by integrating the design recommendations of the building block components in Cadence Analog Design suit, using the 0.18μm full custom CMOS technology. The results show that the final DAQ design can obtain 125MS/s sampling rate. It dissipates only 65.6mW of power as compared to 97.9mW power consumption when the traditional flash ADC was used. Results indicate that 31% of die size could be saved and 33% power saving is obtained when the modified flash ADC is used. The layout of the proposed DAQ system employing the modified flash ADC architecture has been implemented. The results of the layout simulation of the DAQ unit have been back annotated and analysed.

A proposal for reconfigurable architecture of the implemented DAQ system for power system protection and bio-medical application will be presented in Chapter 6 and Chapter 7. Statistical analysis of the reconfigurable DAQ architectures will also be provided, along with a valuation of the performance in terms of area, accuracy, cost, system power consumption and speed.

# Chapter 6

# Power System Protection Application

## 6.1 Introduction

In this chapter, the data acquisition (DAQ) system, implemented in Chapter 5, is proposed for power system protection application. The initial DAQ system has been modified and a novel reconfigurable DAQ architecture approach will be proposed and implemented to enhance the system suitability and efficiency for the specific application.

Power systems occasionally experience faults and abnormal conditions. In such cases relays are used to avoid damage to the system and customer equipments. Recently, digital relays are being increasingly used in power industry due to their advantages and flexibilities over traditional electro-mechanical relays. DAQ section in digital relays

will sample line signals (voltages and currents) so that a Central Processing Unit (CPU) or a personal computer (PC) can use these data to determine the fault location and make decision whether or not to trip the relay. A reconfigurable DAQ architecture is proposed to reduce system complexity, data storage and cost. At the normal operating conditions, the proposed reconfigurable DAQ architecture operates at a low sampling speed. This leads to a low data throughput and host PC processing time saving, enabling a reduction of the system data storage and cost, hence correspondingly reducing the system complexity. The reconfigurable DAQ architecture should be capable of increasing its sampling rate when fault occurs. High-speed sampling permits the system to not only accurately detect and locate the fault but also capture sufficient information for further analysis.

This chapter also focuses on the implementation of a semi-custom application specific integrated circuit (ASIC) of an intelligent controller that will perform the control algorithm for power system protection application. Such controller is the intelligence of the DAQ system and provides a reconfigurable aspect to the system. Advantages of implementing the controller on ASIC over using a Digital Signal Processing (DSP) core includes: high speed, low cost and low power properties. In addition, the ASIC is specific to a certain application, therefore, providing maximum efficiency. This approach also permits the implementation of both the intelligent controller and the DAQ system on a single integrated circuit (IC). However, the control algorithm for power system protection contains complex mathematical functions (square-root and arc-tan operations) that are very difficult to realise in hardware and will significantly increase the controller delay, complexity, power consumption, and size. To overcome

these issues, a novel approach to determine the line impedance angle has been proposed to reduce the cost of the semi-custom ASIC implementation of the intelligent controller.

This chapter is structured as follows: Details of the design and implementation of a novel reconfigurable DAQ architecture for power system protection application are presented in Section 6.2. Section 6.3 describes the hardware realisation issues and solutions for the implementation of the intelligent controller on ASIC. The reconfigurable DAQ architecture performance analysis is described in Section 6.4. Conclusions of this chapter are presented in Section 6.5.

## 6.2 Power System Protection Applications

Power systems occasionally experience faults and abnormal conditions, in such cases relays are used to avoid damage to the system and customer equipments. In early development of power systems, protection functions were performed by electro-mechanical relays, which are still currently used. Digital relays (microprocessor-based relays) are being increasingly used in power industry due to their advantages namely: digital relays generally use fewer parts, they are not required to be tuned individually to obtain consistent result, they provides remote targets and fault location information to assist operators in restoration of electrical service and system changes can be made simply by changing software [71, 73]. DAQ units are the heart of the digital relays. Traditionally, they have been built on Printed Circuit Boards (PCBs) with high quality shielding, grounding and insulation, inducing high cost and large size. There is an

emerging approach of integrating the complete DAQ system on a single chip, which obtains advantages of higher speed, less computation, cheaper, faster, smaller and more reliable. There is, however, a continued search for architectures and circuit techniques enabling DAQ systems to attain higher speed, more enhanced performance with smaller chip area and less complexity.

This section presents the design and implementation of a reconfigurable DAQ architecture for power system protection application. It can detect and adjust its sampling speed depending on the occurrence of a fault in the network, enabling a large reduction of data throughput and a host CPU processing time saving. This also allows a reduction of the system data storage and hence correspondingly reduces the system complexity and cost.

### 6.2.1 Overview of Distance Protection in Power System

In a power system consisting of generators, circuit breakers, transformers, transmission and distribution circuits, it is inevitable that sooner or later, in such large network, as illustrated in Figure 6.1, some failure or fault will occur somewhere in the system. The probability of such failure is more on the power transmission lines, because of their greater length and bare exposure to atmosphere [71].

In general, faults on transmission systems maybe categorised under two headings: series and shunt types. Series faults may involve single-pole switching and one or more conductor opening. These conductors may be at one busbar or at different busbars.

They may occur either due to breaking of the conductors or through the action of the circuit breakers and other devices that may not result in the opening of all the three phases simultaneously. Series fault form a kind of unbalance in the system impedances and does not involve wither earth or any interconnection between phases. Shunt faults, such as single-phase-to-ground, two-phase-to-ground, phase-to-phase, three-phase faults with or without ground and their combination. These types of fault will form some sort of unbalance between phases or between phases and ground. They may occur either through impedances or direct short-circuits [71, 114, 115].

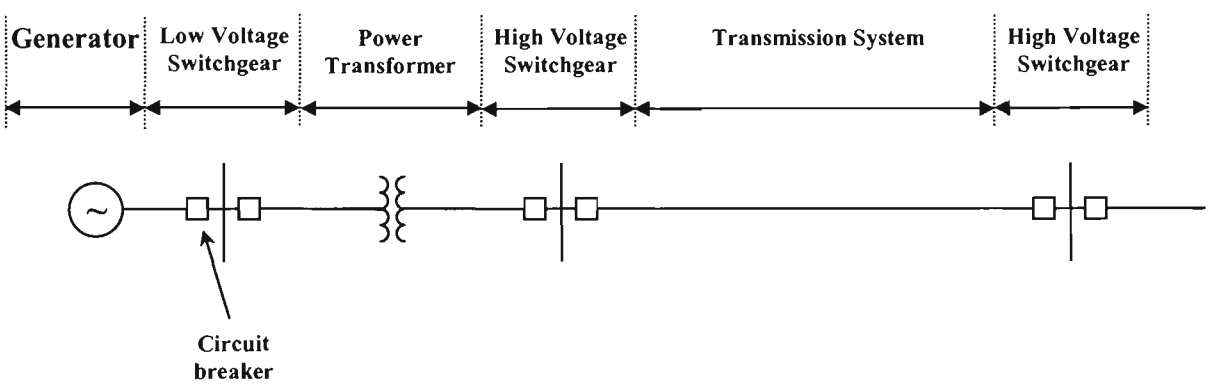



Figure 6.1 Basic Power System Block Diagram

In order to improve the digital relays for the protection of transmission systems, it is necessary to be aware of the frequency of transmission faults. In practice, majority of the faults that occur on power transmission systems are unsymmetrical shunt faults. The frequency of occurrence of these faults is presented in Table 6.1 [71, 116].

Power transmission systems are protected from faults and abnormal conditions by relays. In principle, relays discriminates between faults on the protected line, which should cause fast disconnection of the line at the relay end, and the faults on the

adjacent plants which should be left to the protection of that plant to clear. To prevent the over-reaching, the reference of the impedance for the relay instantaneous tripping is selected so that it corresponds to 80% of the line length, thus it forms a zone of 80% of the line such that fault will be isolated instantaneously. Isolation of faults in the remaining 20% of the line is not instantaneous, but after a determined delay by comparing the measured impedance with another reference.

Table 6.1 : Frequency of fault occurrence on power transmission systems.

| **Type of fault** | **Frequency of Occurrence** |
|---|---|
| Single-lime-to-ground | 90% |
| Line-to-line | 5% |
| Line-to-line-to-ground | 3% |
| Line-to-line-to-line | 2% |

## 6.2.2 A Reconfigurable DAQ Architecture for Digital Relays

As mentioned before, power transmission systems are typically protected by relays to avoid damage to the system and customer equipments. Digital relays are being increasingly used in power industry due to their advantages and flexibilities. Digital relays estimate the location of a fault using instantaneous values of the voltages and currents simultaneously measured (sampled) at fixed time intervals. A typical block diagram of a digital relay is shown in Figure 6.2.

The input line voltages and currents are sampled and digitised by a DAQ section so that a CPU can determine the fault location and make decision whether or not to trip the

relay. Traditionally, the DAQ section has been built on PCBs with high quality shielding, grounding and insulation, inducing high cost and large size. In this work, it has been replaced by the proposed DAQ system implemented in Chapter 5, with specific modifications to incorporate the reconfigurable aspect onto the DAQ system.

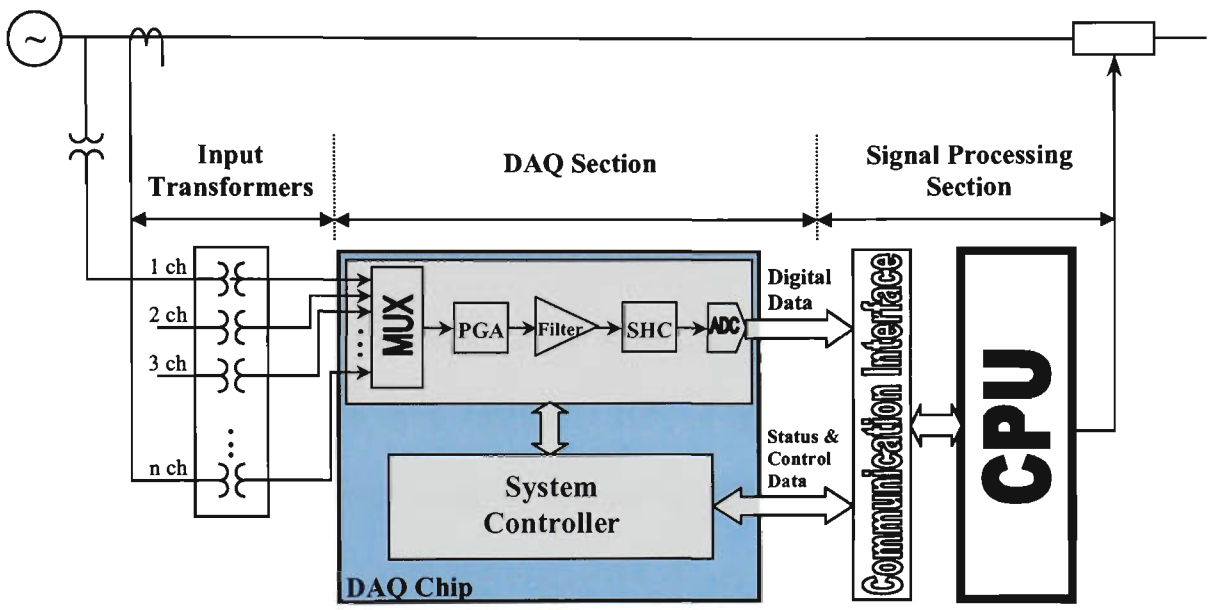



Figure 6.2 Principle of a digital relay [71].

Besides being used by the CPU to accurately locate a fault, the recorded data (voltages and currents) can be used for automated fault analysis. In addition, any occurrence of a fault should be detected and cleared by the protective relaying devices. An analysis of the protective relaying operation is required if an assessment of its performance is needed. In order to perform the analysis, the CPU has to obtain sufficient information to analyse/classify a fault and also to compare the relay operation. This introduces additional difficulty in high-speed tripping situations where the recorded data may not be sufficiently acquired before the line current signals disappear because of the relay operation and breaker opening. This leads to the need of a very high-speed DAQ system in digital relays to get sufficient information [117, 118].

### 6.2.2.1 *Implementation of Reconfigurable DAQ Architecture*

For power protection application, a DAQ system with very high sampling rate is not always required since the normal line current and voltage frequencies are of 50Hz. However, when a fault occurs, the line voltage is reduced to a very low value whist the currents of abnormally high magnitude and high frequency will flow through the network. To demonstrate the effect of fault transients in power systems, a fault is simulated in a 400kV 125 km transmission line between local and remote ends. In here a weak local source of 5GVA short circuit level (SCL) and a strong remote source of 35 GVA SCL is studied with fault applied at 10% of line length from the local end. The pre-fault power flow from local to remote is 1026 MW. Figure 6.3 shows fault inception at voltage peak (90E) and Figure 6.4 shows fault inception at voltage crossing (0E) [119, 120].

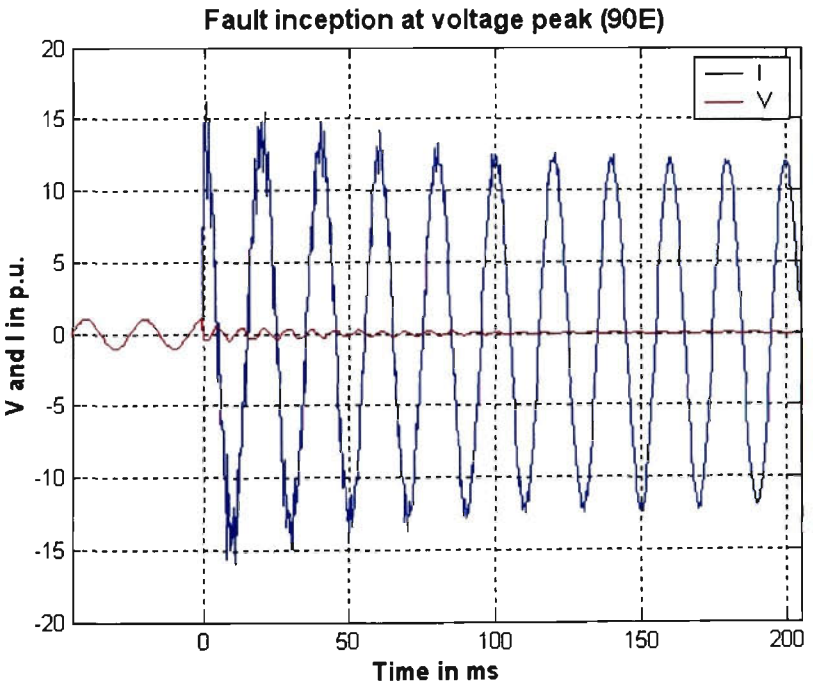



Figure 6.3 Fault Interception at voltage peak.

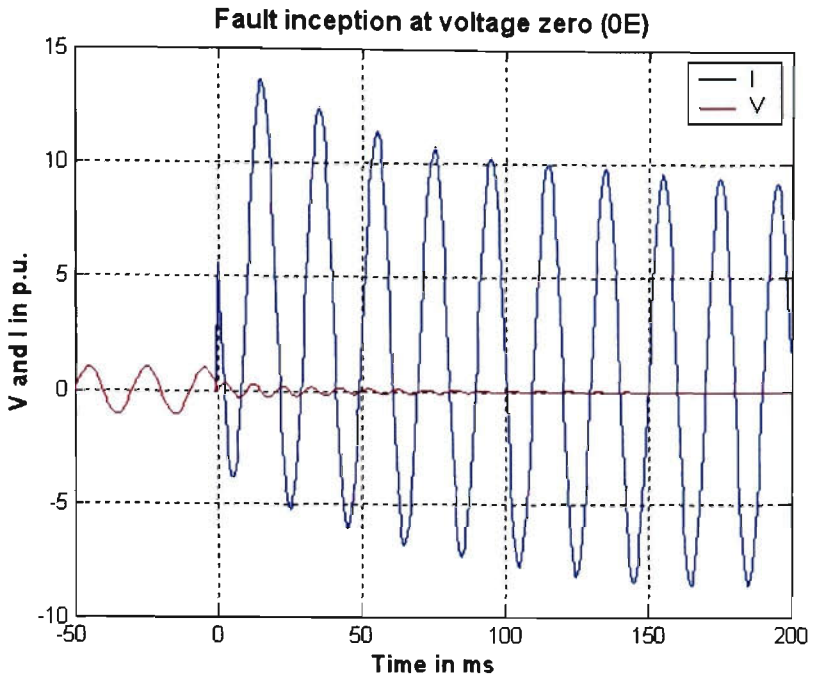



Figure 6.4 Fault Interception at voltage crossing.

During fault conditions, the voltage and current waveforms are usually distorted and consists of numerous harmonics and reflected travelling wave components. System impedance calculation for distance relaying can then be obtained by extracting the fundamental components. Short data window will introduce errors due to sub-harmonics and super-harmonics. High sampling frequency can reduce errors, but it is unnecessary and superfluous during normal conditions, when line voltage and current frequencies are of 50Hz [71, 120].

To overcome this issue, a novel reconfigurable DAQ architecture has been proposed for digital relays, as shown in Figure 6.5. It consists of an intelligent controller unit and a full custom DAQ unit with a variable signal-conditioning unit, including a variable cut-off frequency anti-aliasing filter and a PGA. The DAQ unit sampling frequency is also variable by changing the system master clock generated from a system controller.

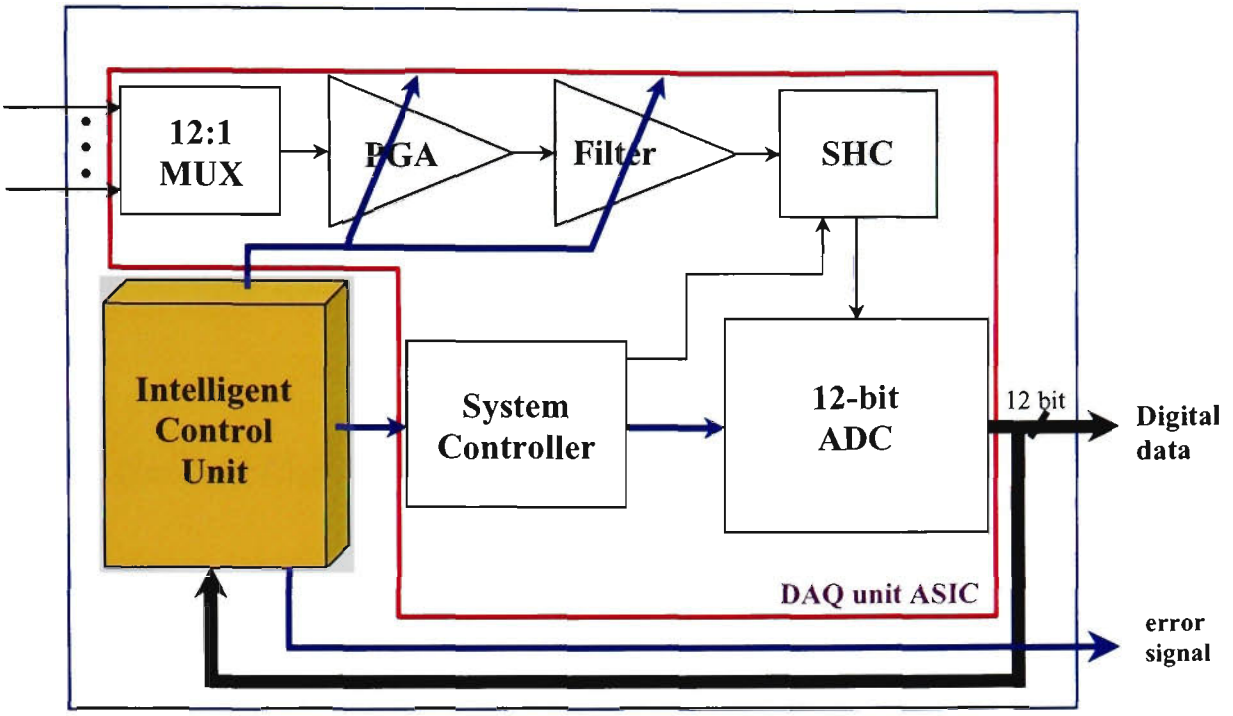



Figure 6.5 Reconfigurable DAQ architecture for a digital relay

At the normal operating conditions, the proposed reconfigurable DAQ architecture operates at a low sampling speed and the anti-aliasing filter cut-off frequency is reduced. This leads to a low data throughput and a host CPU processing time saving, enabling a reduction of the system need for data storage and hence correspondingly reduce the system complexity. The reconfigurable DAQ architecture should be capable of reconfiguring its characteristics, such as increasing its sampling rate, only when fault occurs. High-speed sampling permits the system to not only accurately detect and locate the fault but also capture sufficient information for further analysis.

An intelligent control unit has been incorporated to the reconfigurable DAQ architecture. It is capable of detecting an abnormal condition on the power system network and generates signals to increase sampling rate of the DAQ unit and to adjust

cut-off frequency of the on-chip anti-aliasing filter to sample all sub-harmonics components of high-frequency voltages and currents at faults. It will also generate an "error signal" to notify the central CPU of such abnormal condition detected in the power system. The detailed implementation of the intelligent control unit will be presented in Section 6.2.2.2.

### *6.2.2.2 Control Unit Implementation*

The control unit is the intelligence behind the reconfigurable architecture. It continuously monitors the voltages and currents in which they are used to detect the appearance of an abnormal condition on the power transmission network. The control unit, then, sends signals to adjust the DAQ system's sampling speed, filter cut-off frequency and the PGA gain in order to properly locate and analyse the fault.

In a digital relay for distance protection, further processing of digital representations of voltages and currents at sampling instants may lead to an estimation of magnitudes and angles (vectors) of their fundamental frequency components and subsequently, to the determination of the fault impedance from these components [71]. A reconfigurable algorithm for the intelligent control unit has been developed. During normal conditions a fast method is utilised based on a short data window to detect the occurrence of a fault or an abnormal condition in the network. On detection, it automatically adjusts the system sampling speed and generate error signal to the central CPU.

A simple method of fault detection could be performed from only three samples. Let $v(t-\Delta t)$, $v(t)$ and $v(t+\Delta t)$ be the three samples taken at short intervals. The line voltage is expressed as:

$$v(t) = V_P \sin(\omega t + \phi_V) \tag{6.1}$$

where: $\omega$ is the line voltage signal frequency, $\phi_V$ is the voltage signal phase angle.

The voltage differential, thus, can be determined by:

$$v'(t) = \omega V_P \cos(\omega t + \phi_V) \tag{6.2}$$

Using trapezoidal rule, v'(t) can be estimated by:

$$v'(t) = \frac{v(t+\Delta t) - v(t-\Delta t)}{2 \times \Delta t} \tag{6.3}$$

In the similar manner, $i'(t)$ will be evaluated. Hence, the line impedance magnitude can be calculated based on the squares of voltage and current magnitudes as follows [71]:

$$Z_{line} = \sqrt{\frac{v(t)^2 + \left(\frac{v'(t)}{\omega}\right)^2}{i(t)^2 + \left(\frac{i'(t)}{\omega}\right)^2}} \tag{6.4}$$

The impedance phase angle, $\phi_{line}$, can be expressed as [71]:

$$\phi_{line} = \arctan\left(\omega \times \frac{i(t)}{i'(t)}\right) - \arctan\left(\omega \times \frac{v(t)}{v'(t)}\right) \tag{6.5}$$

Figure 6.6 illustrates the flow chat of the reconfigurable algorithm of the intelligent control unit.

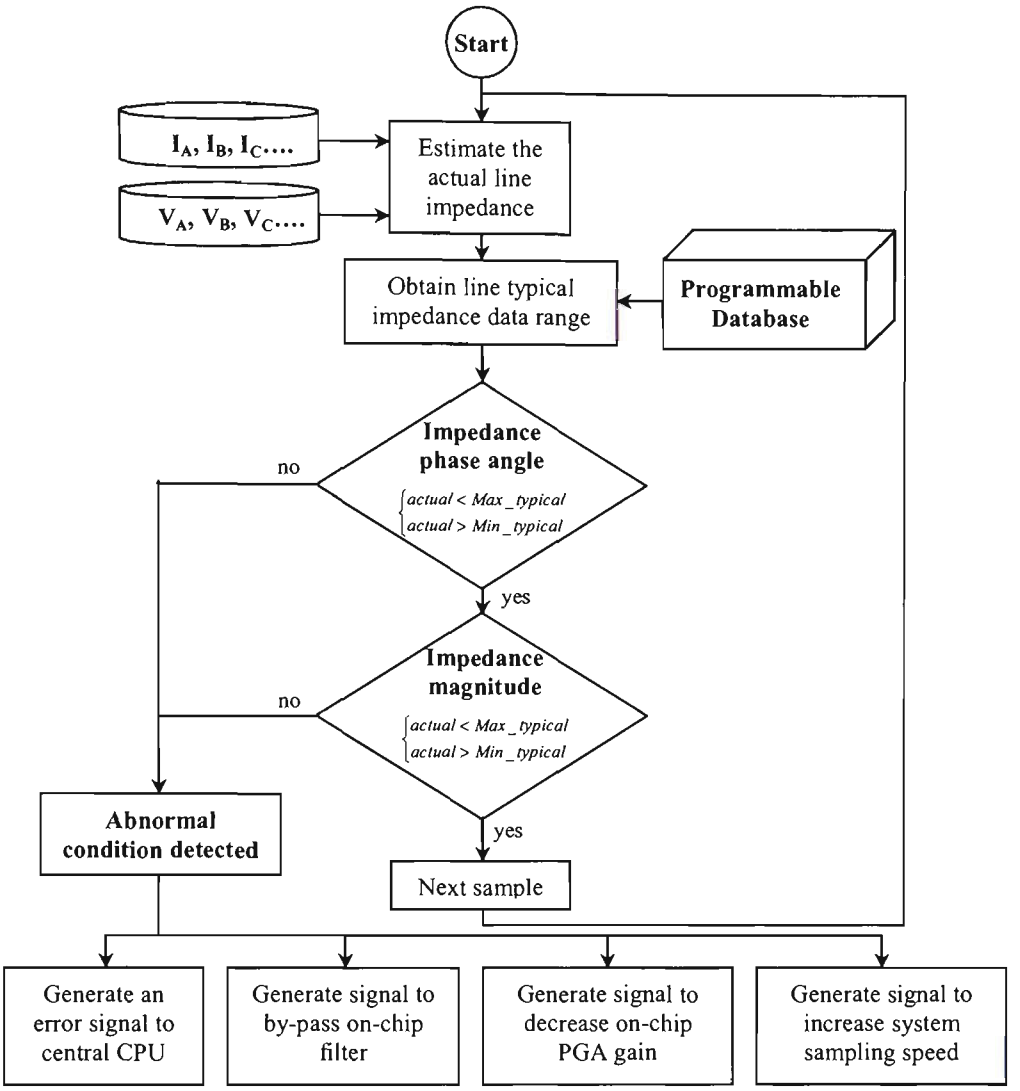



Figure 6.6 Flow chart of the intelligent control unit operation.

At normal conditions, the designed DAQ system operates at a low sampling speed. Based on the above algorithm, the magnitude and phase angle of line impedances will be estimated and compared with typical impedance magnitude and phase angle respectively, allowing a margin for possible measured errors. When an abnormal condition of transmission line is detected, an error signal will be generated to the cental CPU and the DAQ system will automatically increase its sampling speed so that more data will be available allowing cental CPU to more accurately determine the fault location. This process is executed in order to generate trip signals if it is necessary and for future fault analysis.

## 6.3 ASIC Implementation of the Intelligent Control Algorithm

The control units, developed in Section 6.2.2.2 have been implemented on a DSP core. This approach, however, disadvantages the proposed reconfigurable DAQ architecture since the required additional DSP core drastically increases system complexity, size, power consumption and cost. Furthermore, it is difficult to integrate the supplementary DSP core on the same IC with the full-custom DAQ system, implemented in Chapter 5. This section of the chapter describes the semi-custom ASIC implementation of an intelligent controller that will perform the proposed control algorithm for power system application. Advantages of implementing the intelligent controller on ASIC over the DSP approach include high speed, low cost and low power properties. In addition, the ASIC implementation approach is specific to a certain application, therefore, providing maximum efficiency. This approach also permits the implementation of both the intelligent controller and the DAQ system on a single IC. Design considerations of the control algorithms are presented in Section 6.3.1. The structural realisation and implementation of the intelligent control unit is presented in Section 6.3.2.

### 6.3.1 Algorithm Implementation Considerations

The realisation of the intelligent controller should be flexible so that the DAQ system can change its typical operating characteristics when it is employed in different power transmission systems. To achieve such realisation, the controller was hardware partitioned so that it is user programmable, where the operating characteristics can be

selected. Upon the selection, it enters a real-time reconfigurable mode, where it continuously monitors the operating environment, and accordingly reconfigures the parameters of the DAQ system.

Achieving high speed with reduced complexity and size and minimal power dissipation is also considered for the implementation of the intelligent controller. As observed from equation (6.4) and (6.5), the control algorithm for power system protection contains square-root and arc-tan operations that are complex to realise in hardware and will significantly increase the controller delay, complexity, power consumption, and size. To overcome these issues, two approaches have been proposed.

Firstly, to eliminate the square-root operation, the square of the actual magnitude of the protected line impedance will be evaluated and compared to its typical value, instead of the line impedance magnitude. The typical value of the line impedance magnitude is stored in an electrically erasable programmable read-only memory (EEPROM), allowing users to re-program the impedance data when the relay is transferred to another line. When reading the impedance information from the EPPROM, the controller automatically takes the square of the impedance magnitude and compares it to the measured value.

Secondly, to eliminate the arc-tan function to reduce the cost of the control algorithm implementation, a novel approach to determine the phase angle of the protected transmission line is proposed as follows:

Recall from equation (6.1), let $v(t)$ and $i(t)$ be the instant line voltage and current seen from the relay, which can be expressed by [71]:

$$v(t) = V_P \sin(\omega t + \phi_V) = V_P \sin(\phi_1) \tag{6.6}$$

$$i(t) = I_P \sin(\omega t + \phi_I) = I_P \sin(\phi_2) \tag{6.7}$$

where $\phi_1 = \omega t + \phi_V$ and $\phi_2 = \omega t + \phi_I$ are the instant phase angles of the line voltage and current respectively.

Figure 6.7 illustrates the phasor diagram of the line voltage and current at the time instant $t$.

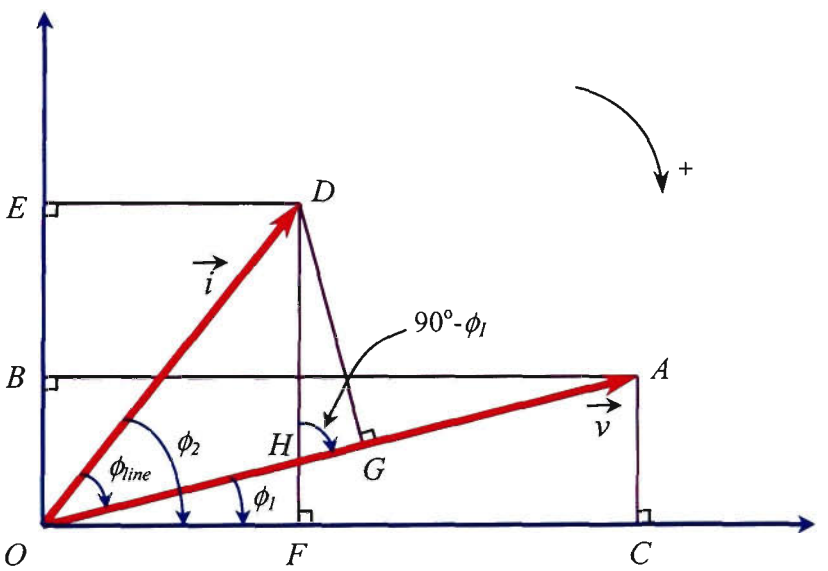



Figure 6.7 Phasor diagram of the line voltage and current.

It is observed that the purpose of equation (6.5) is to determine the phase angle of the protected line impedance ($\phi_{line}$), which is the angle between the line current vector and the line voltage vector, as shown in Figure 6.6.

$$\phi_{line} = \arctan\left(\omega \times \frac{i(t)}{i'(t)}\right) - \arctan\left(\omega \times \frac{v(t)}{v'(t)}\right) = \phi_2 - \phi_1 \tag{6.8}$$

where $-90° \leq \phi_{line} \leq +90°$

From the phasor diagram, we can deduce the following expressions:

$$OA = V_P \tag{6.9}$$

$$OB = V_P \sin(\phi_1) = v(t) \tag{6.10}$$

$$OC = V_P \cos(\phi_1) = v'(t)/\omega \tag{6.11}$$

$$OD = I_P \tag{6.12}$$

$$OE = I_P \sin(\phi_2) = i(t) \tag{6.13}$$

$$OF = I_P \cos(\phi_2) = i'(t)/\omega \tag{6.14}$$

The line voltage and voltage differential, *v(t)* and *v'(t)*, can be determined using equations (6.2) and (6.3) respectively. The magnitude of the line voltage $V_P$, thus, can be determined by:

$$V_P = \sqrt{V_P\left[\sin^2(\phi_1) + \cos^2(\phi_1)\right]} = \sqrt{v(t)^2 + \left(\frac{v'(t)}{\omega}\right)^2} \tag{6.15}$$

In similar manner, *i(t)*, *i'(t)* and $I_P$ can be estimated from the three line current samples taken at short intervals.

Considering two similar triangles $\Delta OHF$ and $\Delta OAC$, we can determine the line section $HF$ as follows:

$$HF = \frac{OF}{OC} \times AC = \frac{OF}{OC} \times OB = \frac{i'(t)/\omega}{v'(t)/\omega} \times v(t) = \frac{i'(t) \times v(t)}{v'(t)} \tag{6.16}$$

Thus, the line section $HD$ can be determined by:

$$HD = FD - HF = OE - HF = i(t) - \frac{i'(t) \times v(t)}{v'(t)} = \frac{i(t) \times v'(t) - i'(t) \times v(t)}{v'(t)} \tag{6.17}$$

Considering the right triangle $\Delta DGH$, $GD$ can be determined using the following formula:

$$GD = HD \times \sin(90° - \phi_1) = HD \times \cos(\phi_1) = HD \times \frac{v'(t)/\omega}{V_P}$$

$$= \frac{i(t) \times v'(t) - i'(t) \times v(t)}{v'(t)} \times \frac{v'(t)/\omega}{V_P} = \frac{i(t) \times v'(t) - i'(t) \times v(t)}{\omega \times V_P} \tag{6.18}$$

Finally, considering the right triangle ΔODG, we have:

$$\sin(\phi_{line}) = \frac{GD}{OD} = \frac{i(t) \times v'(t) - i'(t) \times v(t)}{\omega \times V_P \times I_P} \tag{6.19}$$

However, equation (6.15) implies that a square-root operation will be required to determine the line voltage magnitude ($V_P$) and line current magnitude ($I_P$). To eliminate these square-root operations when realising the control algorithm in hardware, the square of the sine of the line impedance angle will be used instead.

$$\sin^2(\phi_{line}) = \frac{\left[i(t)\times v'(t) - i'(t)\times v(t)\right]^2}{(\omega \times V_P \times I_P)^2} \tag{6.20}$$

$$\therefore \quad \sin^2(\phi_{line}) = \frac{\left[i(t)\times v'(t) - i'(t)\times v(t)\right]^2 \times \omega^2}{\left(v(t)^2 \times \omega^2 + v'(t)^2\right)\left(i(t)^2 \times \omega^2 + i'(t)^2\right)} \tag{6.21}$$

The sign of impedance angle is determined by:

$$sign(\phi_{line}) = sign(\sin(\phi_{line})) = sign\left(i(t)\times v'(t) - i'(t)\times v(t)\right) \tag{6.22}$$

This will also be valid when *i(t)* is lagging compared to *v(t)*, in which case the impedance phase angle is negative. Moreover, this approach has been considered when *v(t)* and *i(t)* are located in the other quadrants and proved to be valid.

In conclusion, to eliminate the arc-tan operation, the square of the sine of the impedance phase angle of the protected line impedance (with sign), instead of the impedance phase angle, will be evaluated and compared to the square of its typical value, which is stored in an EEPROM.

The control algorithm for power system application, presented in Figure 6.6, is modified to reduce the cost of its ASIC implementation and is illustrated in Figure 6.8. It is noticed that the sign of the line impedance phase angle will only be compared to the typical value when the phase angle ($\phi_{line}$) is greater than a margin value (*Min_margin*), to avoid possible errors when the phase angle is approximately equal to zero.

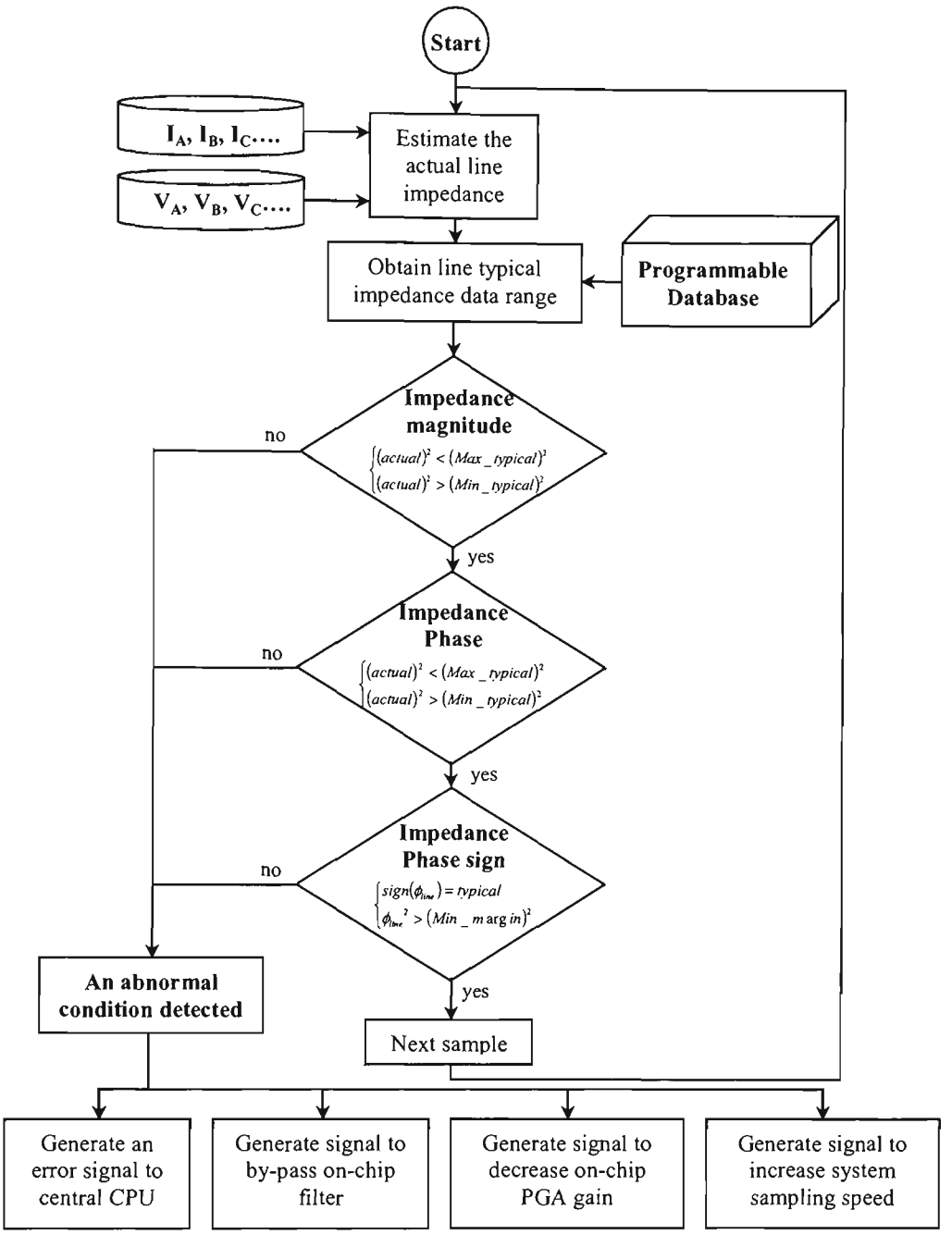



Figure 6.8 Modified control algorithm for power system protection application

## 6.3.2 Design Considerations and Implementation

This section discusses the hardware considerations and implementation of the intelligent controller for power system protection application. The intelligent controller

has been hardware partitioned for an ASIC implementation, whish is illustrated in Figure 6.9.

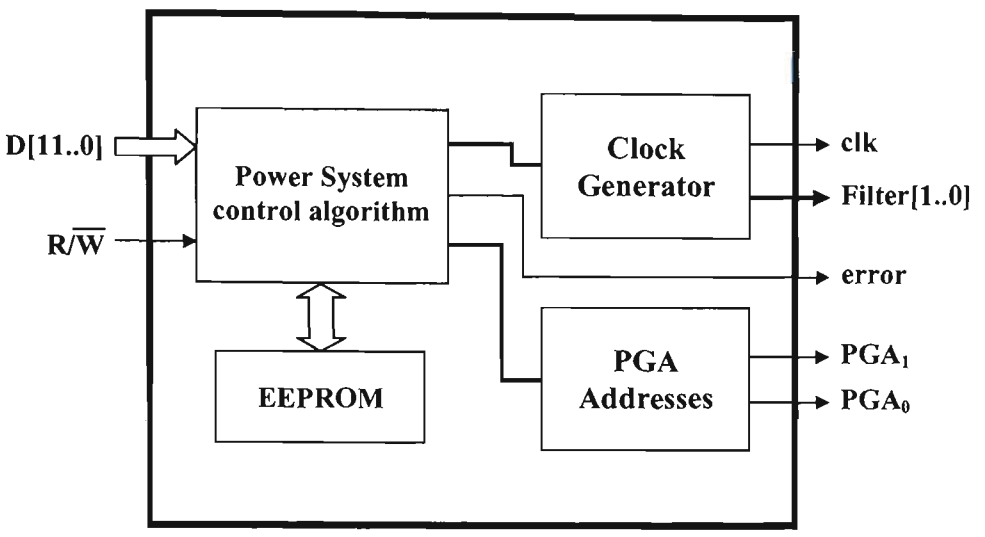



Figure 6.9 Hardware partition diagram of the intelligent controller.

The control algorithm was realised in Very High Speed Integrated Circuit Hardware Description Language (VHDL) - Register Transfer Level (RTL) and synthesised using a standard cell NEC 0.25-micron CMOS process, in Synopsys Design Complier. Figure 6.10 presents the top-level entity of the ASIC and the corresponding synthesised schematic is presented in Figure 6.11.

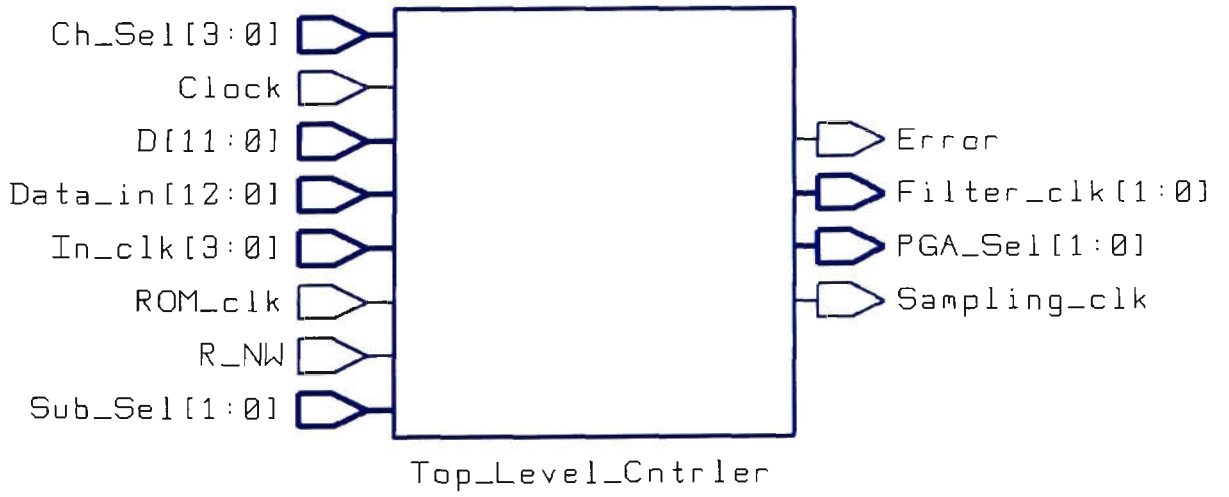



Figure 6.10 The intelligent controller ASIC top-level entity.

A word length of 12 bits is used for the D signal to control the power system application. The R_NW input signal is required to address the DAQ system to read data from the EEPROM or write a new data to the EEPROM. The Clock signal is the system clock. The Ch_Sel signal is used to select the input channel for processing. The output Sampling_clk will control the DAQ system master clock to change its sampling rate. Filter_clk signal will be sent to the on-chip filter while PGA_Sel signal will decide the gain of the PGA. The Error signal will notify the host CPU of any abnormal condition detected on the protected transmission line. ROM_clk is the clock of the internal EPPROM of the controller. Data_in, having a word length of 13 bits, is the input data to re-program the EPPROM. Sub-Sel signal is an additional address signal required to specify the location on the EPPROM to store the re-programmed input data. In_clk signal is required so that the clock generator in the controller is able to generate the Sampling_clk and Filter_clk signals.

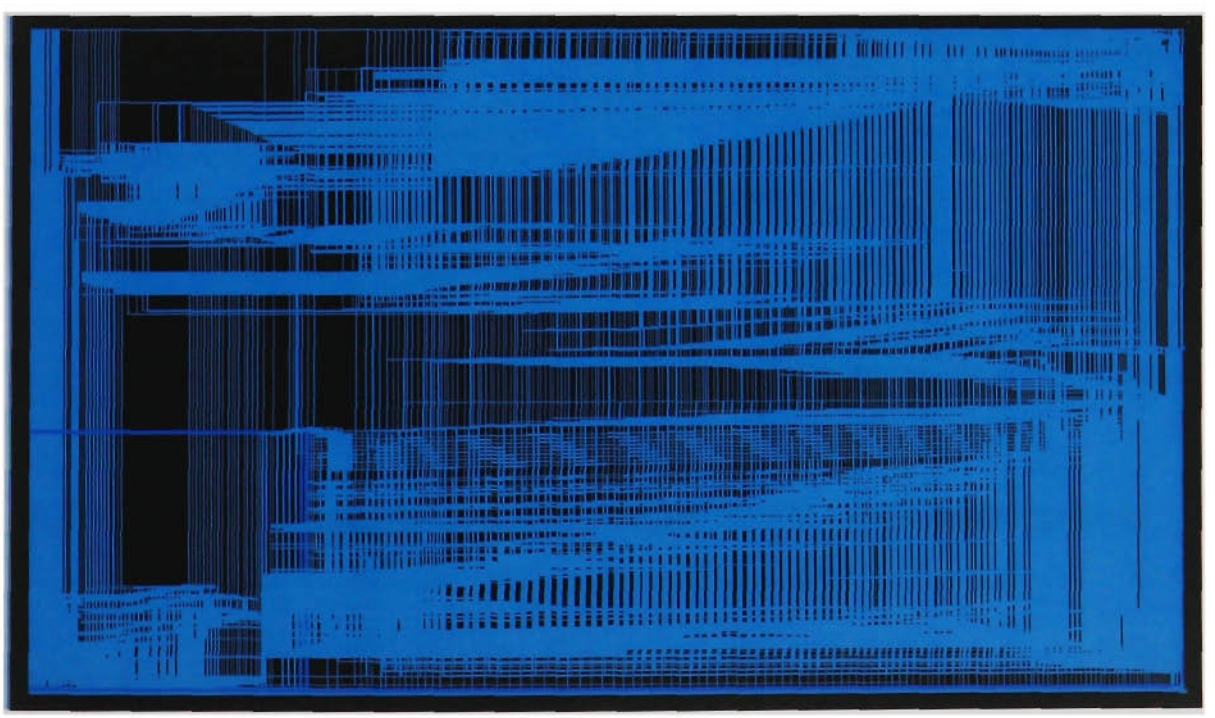


Figure 6.11 The intelligent controller ASIC synthesised schematic diagram.

## 6.4 System Performance Analysis

In this section, performance analysis of the intelligent controller implemented using a semi-custom ASIC approach and the proposed reconfigurable DAQ architecture for biomedical and power system protection applications is presented.

### 6.4.1 Intelligent Controller Performance Analysis

The performance analysis was carried out on the ASIC to ensure that it meets the timing requirement as well as the power requirements. The analysis was carried out at synthesis stage in Synopsys Design Compiler. Table 6.2 presents the simulated attributes of the intelligent controller ASIC at synthesis stage.

Table 6.2 : Semi-custom ASIC implementation of the intelligent controller.

| Property | Result |
|---|---|
| Core Supply Voltage | 2.5 V |
| Critical Path | 10 ns |
| Power consumption | 450 μW |
| Average operating frequency | 26 kHz |
| Area | 1.9 $mm^2$ |
| Synthesis Technology | NEC 0.25μm CMOS process |

### 6.4.2 Reconfigurable DAQ System Performance Analysis

The reconfigurable DAQ architecture has been implemented in the Cadence Analog Design Environment.

Figure 6.12 illustrates the relay tripping time versus the system sampling rate during normal conditions. It is obvious that the lower the system sampling rate, the longer it will take to detect an abnormal condition and then locate the fault on the transmission line. To provide sufficient time to locate the fault and to trip the relay [121, 122], the DAQ system is required to operate at 10 kilo-samples per second (kS/s) during normal conditions.

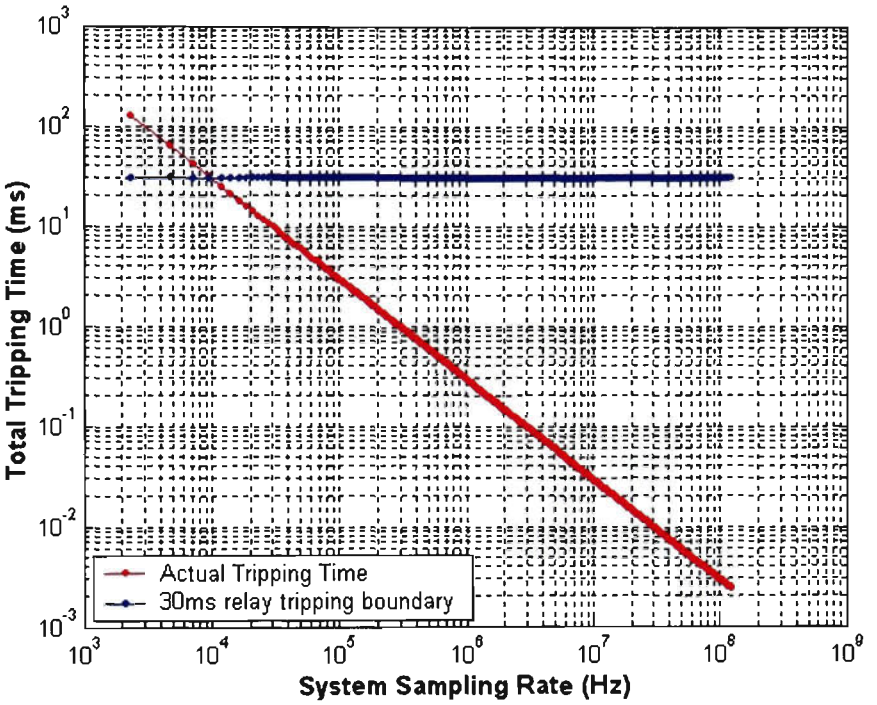



Figure 6.12 System detection time versus system sampling rate during normal conditions.

Figure 6.13 presents the relation between the average system data throughput and system sampling speed during normal conditions. The figure demonstrates that a slower system sampling speed during normal conditions will enable a larger reduction of system data throughput. Therefore, using the reconfigurable approach will reduce the normal condition system sampling speed, which reduces system need for storage and complexity.

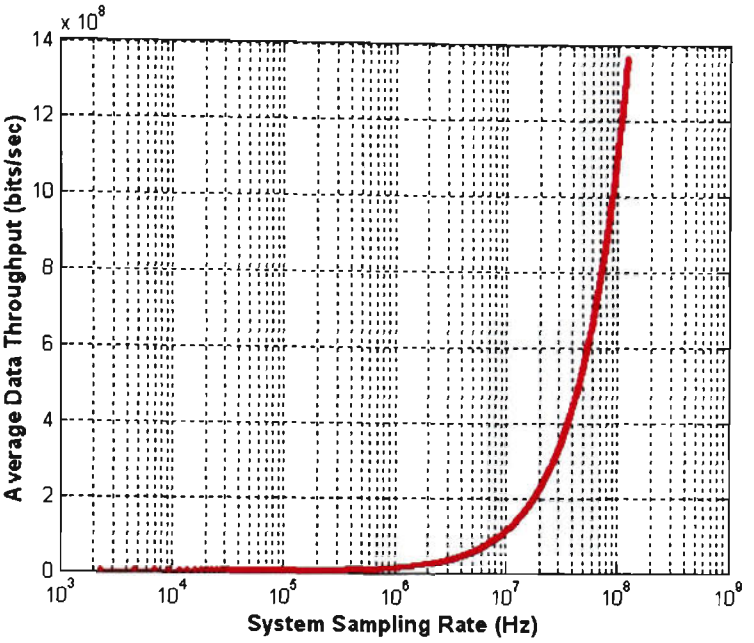



Figure 6.13 System average data throughput versus system sampling rate during normal conditions.

Table 6.3 summaries the performance of the novel reconfigurable DAQ architecture, the non-reconfigurable DAQ system using a modified flash ADC, implemented in Chapter 5, and a non-reconfigurable DAQ system employing a traditional flash ADC. The objective is to carry out the comparison of the three DAQ approaches and to demonstrate the superiority of the reconfigurable architecture.

Results reveal that a 33% power saving is obtained and 31% of the total number of transistors could be minimised when the new modified flash ADC is used instead of a full flash ADC. A 63% average data throughput is obtained, the total sampled data is reduced by 63% and a further 62% reduction of power consumption is achieved when the reconfigurable property was applied to the DAQ system. This significantly reduces the system need for data storage, and hence correspondingly reduces the system complexity, and also enables an increase of system detection speed and accuracy.

Table 6.3 : Comparison results of the three DAQ architecture performance.

| | **Using traditional flash ADC** | **Using modified flash ADC** | **Using modified flash ADC** |
|---|---|---|---|
| **Reconfigurable Property** | ***No*** | ***No*** | ***Yes*** |
| **Device delay** | | | |
| Total delay | 8ns | 8ns | 8ns |
| Max master clock speed | 1GHz | 1GHz | 1GHz |
| Max system data rate | 125MS/s | 125MS/s | 125MS/s |
| Average system data rate | 70kS/s | 70kS/s | 26kS/s |
| **System power consumption** | | | |
| @ max sampling speed | 97.9mW | 65.6mW | 66.1mW |
| Average power consumption | 7.24mW | 4.85mW | 1.84mW |
| **Number of Devices** | | | |
| PMOS | 1172 | 860 | 860 |
| NMOS | 1211 | 926 | 926 |
| Resistors | 87 | 87 | 87 |
| Capacitor | 10 | 10 | 10 |
| **Other Parameters** | | | |
| DNL | ±0.5 LSB | +0.6/-0.5 LSB | +0.6/-0.5 LSB |
| INL | ±0.5 LSB | ±0.5 LSB | ±0.5 LSB |
| Technology | 0.18µm CMOS | 0.18µm CMOS | 0.18µm CMOS |
| Resolutions | 12 bits | 12 bits | 12 bits |
| Supply Voltage | 2.5V | 2.5V | 2.5V |

## 6.5 Conclusion

This chapter has presented the implementation of a novel reconfigurable DAQ architecture for power system protection application. The reconfigurable DAQ architecture is highly efficient for power system protection application. At the normal operating conditions, the proposed reconfigurable DAQ architecture operates at a low sampling speed and the anti-aliasing filter cut-off frequency is adjusted accordingly. This approach leads to a low data throughput and a host CPU processing time saving, enabling a reduction of the system need for data storage and hence accordingly reducing the system complexity. The reconfigurable DAQ architecture is capable of

reconfiguring its characteristics, such as increasing its sampling rate, depending on the occurrence of a fault in the network. High-speed sampling permits the system to not only accurately detect and locate the fault but also capture sufficient information for further analysis.

This chapter has also presented the semi-custom ASIC implementation of an intelligent controller that performs the proposed control algorithm power system protection application. A novel approach to determine the line impedance angle has been proposed. This approach eliminates the square-root and arc-tan operations to reduce the cost of the semi-custom ASIC implementation of the intelligent controller. Analysis revealed that the intelligent controller achieved a maximum operating frequency of 100MHz, with 10ns critical path delay. The result indicates that it meets the timing requirements of the reconfigurable DAQ architecture when it operates at its normal sampling rate of 10kS/s. The controller core utilises an area of 1.9mm$^2$.

A performance analysis of the proposed reconfigurable DAQ architecture for power system protection application has been performed. Results reveal that a 33% power saving is obtained and 31% of the total number of transistors could be minimised when the new modified flash ADC is used instead of a full flash ADC. The analysis also indicated that for the power system protection application, a 63% average data throughput reduction is obtained, the total sampled data is reduced by 63% when the reconfigurable property was implemented to the DAQ system. The reconfigurable DAQ architecture provides an efficient approach to enhance the system performance and power system protection application. It significantly reduces the system need for

data storage and power consumption, hence accordingly reducing the system complexity and cost, and increasing the system speed and accuracy.

# Chapter 7

# Biomedical Application

## 7.1 Introduction

In this chapter, the data acquisition (DAQ) system, implemented in Chapter 5, is proposed for biomedical instrumentation application. The initial DAQ system has been modified and a novel reconfigurable DAQ architecture approach will be proposed and implemented to enhance the system efficiency for this application.

In biomedical instrumentation, it is usually required to acquire, analyse and display biosignals obtained from sensors, which convert a physical measureand from a human body to an electric signal. The biosignals normally have different frequencies and amplitude ranges. The DAQ system, implemented in Chapter 5, however, only provides a fix sampling rate throughout input channels. Therefore, this DAQ system will be

inefficient for biomedical application where channels containing biosignals with different amplitudes and frequencies should be treated differently. That will improve the system performance and efficiency. A novel reconfigurable DAQ architecture is proposed to overcome the limitations of the traditional DAQ system, for multi-rate biomedical application. In this new DAQ system design, different frequency input channels will be conditioned and sampled at different rates, so that data storage and power consumption will be optimised, while maintaining system accuracy and improve the system performance.

This chapter also focuses on the implementation of a semi-custom application specific integrated circuit (ASIC) of an intelligent controller that will perform the proposed control algorithms for biomedical application. Advantages of implementing the controller on ASIC over using a Digital Signal Processing (DSP) core includes: high speed, low cost, high reliability and low power consumption. In addition, the ASIC is specific to a certain application, therefore, providing maximum efficiency. With the employment of the ASIC approach, it is possible to implement both the intelligent control unit and the DAQ system on a single integrated circuit (IC).

This chapter is structured as follows: Section 7.2 presents the implementation of a reconfigurable DAQ architecture for biomedical application. Section 7.3 describes the hardware realisation issues and solutions of the implementation of the intelligent controller on ASIC. The reconfigurable DAQ architecture performance analysis is described in Section 7.4. Conclusions of this chapter are presented in Section 7.5.

## 7.2 Biomedical Application

In early 19th century, medical diagnosis was based on the physical examination and treatment was only to heal the structural abnormality. In late 19th century, diagnosis was based on laboratory tests and treatment was designed to remove causes of disorder. The 20th century has witnessed the emergence of biology and medicine as disciplines of technological innovations. The development of personal computers (PCs) and electronic devices has allowed biomedical technology to achieve a great advancement. It has allowed the generation of computerised patient monitoring, and enabled automation and instant analysis of medical events for modern medical diagnoses and treatments [79, 80].

In biomedical instrumentation, it is usually required to obtain, analyse and display analog signals obtained from sensors, which converts a physical measureand from human body to an electrical signal. These analog signals are variable amplitude and frequency waveforms, and continuous in time. Initially these signals are acquired, extracted and analysed using analog technology. However, since the digital signal processor has developed rapidly due to integrated circuit technology over the past 20 years, engineers have turned to digital signal processing as a more advanced and convenient method. A DAQ system is, therefore, enviably necessary as it will acquire, amplify, filter and digitise analog signals for further analysis using the advanced digital signal processing technique [78, 79].

An overview of biomedical instrumentation is presented in Section 7.2.1. The current DAQ system limitations are outlined in Section 7.2.2 to emphasise the necessity of a new DAQ design for biomedical application. The design and implementation of the reconfigurable DAQ architecture is presented in Section 7.2.3.

### 7.2.1 Overview of Biomedical Instrumentation

Biomedical signals are frequently complex waveforms that occur in a very noisy environment. Advanced signal processing techniques have proven to be invaluable to the analysis of biomedical signals. With the increased capability of PCs, the acquisition and analysis of biomedical signals is becoming practical at the individual physician level. [80].

Figure 7.1 illustrates a block diagram of a multi-channel physiological monitoring system. It accepts several biomedical signals related to the function of several parts of a human body, including the heart system, the brain, the eye, the body temperature, etc. The signals are acquired, analysed and displayed to monitor the patient health and/or to provide information about the patient for diagnosis and treatment. The DAQ section of the system in Figure 7.1 comprises of input buffers, an analog multiplexer (MUX), a Programmable Gain Amplifier (PGA) for signal conditioning and an Analog-to-Digital Converter (ADC) with an internal Sample-and-Hold Circuit (SHC) for signal digitisation. The acquired and digitised data is, then, fed to a PC or a microprocessor through opto isolation for inspection, display and analysis [79].

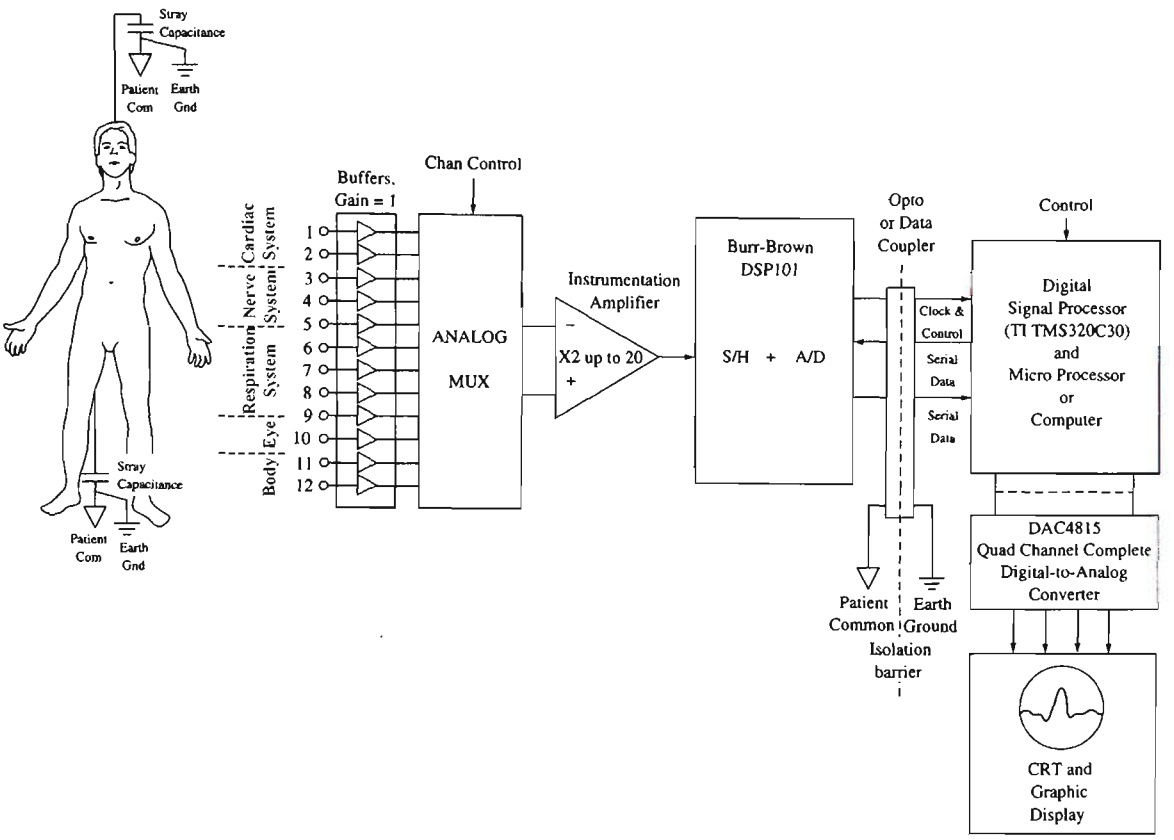



Figure 7.1 A traditional multi-channel physiological monitoring system [79].

The most popular biopotential signals typically include electrocardiogram (ECG), electroencephalogram (EEG), electroneurogram (ENG), electromyogram (EMG) and electroretinogram (ERG), which are related to different measuring and analytical processes. Different signal types have different requirements on signal acquisition and conditioning, and therefore a suitable DAQ system should be implemented for each signal type. Detailed information of these signals are discussed as follows:

- **The ECG** signals are used to monitor and detect the abnormal function of the heart. Clinically obtained ECG signals are often contaminated with different types of noise and baseline drifting commonly occurs. In order to facilitate automated ECG analysis, signal conditioning is undoubtedly a necessity [81]. A modified

morphological filtering (MMF) technique, proposed in [82], can be used for signal conditioning in order to accomplish baseline correction and noise suppression with minimum signal distortion. ECG signals typically have the frequency range of 0.05-250 Hz and the signal range of ±8mV.

- **The EEG** consists of a set of signals measured with electrodes on the scalp. The pattern of changes in the signals reflects some large-scale brain activity. In addition to brain activity, the EEG also reflects activation of the head musculature, eye movements, interference from nearby electric devices, and changing conductivity in the electrodes due to the movements of the subject or physiochemical reactions at the electrode sites. These voltages are approximately 10-5000 μV with frequency range from 0.5 to 150Hz. These signals are highly dependant on the degree of activity of the cerebral cortex [81].
- **The ERG** is related to the human eye diagnosis. When the retina is stimulated with a brief flash of light, a characteristics temporal sequence of changes of potential can be recorded between an exploring electrode, placed either on the inner surface of the retina or on the cornea, and an indifferent electrode placed elsewhere on the body. These potential changes are collectively known as the ERG. Typical vertebrate (including human) ERG frequency range is of 10-300Hz, with maximum amplitude of 0.7mV [81, 83]
- **The ENG** is related to neural field potential that is elicited from a purely sensory nerve or from sensory components of a mixed nerve. The study of field potentials from sensory nerves in general has been shown to be the considerable value in diagnosing peripheral nerve disorders. Practical shows that the measured ENGs contain frequency up to 10kHz. However, they are on the order of 500 μV

amplitude, thus leading to the need of a high-gain amplifier for signal conditioning [81].

- **The EMG** is related to the recording of the electrical potential generated by the muscle. It yields information concerning the total electrical activity associated with the muscle contraction. Concentric needle electrodes are inserted through the skin into the muscle, to record the muscle fibre action potentials. The recorded action potentials have a duration of about 1ms, with amplitudes of a few millivolts. The bandwidth used to process the EMG signal is 500Hz to 10kHz [81, 84].

Table 7.1 summaries the biosignal characteristics as discussed before. It is clear that different biopotential signals have different sampling rate and conditioning requirements at the DAQ level. A DAQ system should 'condition' or properly 'treat' each signals in a very careful way, to achieve a high precision and high performance biosignal acquisition process.

Table 7.1 : Biopotential signal parameters [81].

| Type of Signal | Amplitude Range | Max Frequency | Standard Sensor or Method |
|---|---|---|---|
| Electrocardiogram (ECG) | 0.5-8mV | 250 Hz | Heart Function |
| Electroencephalogram (EEG) | 0.01-5mV | 150 Hz | Brain-surface |
| Electroretinogram (ERG) | 0.05-0.7mV | 300 Hz | Eye potential |
| Electroneurogram (ENG) | 0.01-0.5mV | 10 kHz | Nerve Potential |
| Electromyogram (EMG) | 0.1-5mV | 10 kHz | Skeletal muscle motor unit |

### 7.2.2 A DAQ System Proposal and Limitation

The main challenges in acquiring biosignals are: signal amplitudes are often very small, unwanted noise is often present or introduced, and desired signals maybe masked by biosignals from other phenomena [82-84]. To overcome these challenge, the DAQ system has to "condition" the signals during acquisition phase. It has to provide some gain to boost up input signals. In addition, it has to filter the input signals to remove high-frequency noise and also to eliminate aliasing noise when sampling. Moreover, biomedical instruments require low power consumption and low complexity to reduce the size and cost of the devices and to enable the generation of portable biomedical instrument devices to monitor and/or assist patients inside and outside hospitals.

The DAQ system, proposed and implemented in Chapter 5, has several aspects that are appropriate for some of the requirements of biomedical application. A PGA and an anti-aliasing filter has been included on-chip, enabling a flexible conditioning of input signals. Furthermore, the proposed system employed the modified flash ADC, which enable a significant reduction of system power consumption and complexity. Its high-speed conversion allows several channels to be processed at a high-speed using a single DAQ chip.

The proposed and implemented DAQ system in Chapter 5, however, has specific limitations. It only provides a fix sampling rate for all input channels. This will be inefficient for biomedical application since real biosignals, which are generated from sensors or transducers, will be at different frequency range. For example, the EEG

signals, measured with electrodes on the scalp for brain activity, typically lie in the rage of 0 Hz and 150 Hz, while the EMG signals, recording muscle fibre action potentials, could contains frequency up to 10kHz. It is clear that different biopotential signals, as summarised in Section 7.2.1, have different sampling rate and conditioning requirements at the DAQ level. For example, low frequency input signals require a low sampling rate. Decreasing the sampling speed will reduce system complexity, data storage and power consumption, and hence correspondingly reduce system cost and increase the system operating time for portable biomedical devices. These biomedical instruments will require a reconfigurable DAQ architecture with multi-rate acquisition and programmable signal conditioning.

### 7.2.3 A Reconfigurable DAQ Architecture for Biomedical Application

In this section, a novel low cost low power reconfigurable DAQ architecture is proposes and implemented to overcome the limitations of the traditional DAQ system for biomedical application.

#### *7.2.3.1 Implementation of Reconfigurable DAQ Architecture*

Real biosignals, which are derived from biological processes observed in medicine, usually contain unwanted noise or unwanted signals with frequencies that are higher than the useful data. If the high-frequency components are not correctly filtered (or band limited, they will 'fold down' into the original signal and show up as aliases, and

thus causing error. The best approach to eliminate these alias signals is to use an anti-aliasing filter (low-pass filter). It can block these alias signals by limiting the input signal bandwidth to below half the sample rate. The filter, when applied to each input channel being sampled, eliminates unwanted high frequency noise and interference introduced prior to the sampling [123].

The traditional DAQ systems are typically designed to cover the worst-case sampling scenario based on the fastest input channels. It, however, will be inefficient technique because it is possible to decrease the sampling rate for slower input channels to reduce system complexity and data storage. A DAQ system with variable sampling rate, therefore, will provide a more effective solution with certain system performance specifications. However, reducing channel-sampling speed without a proper signal conditioning (signal filtering) will introduce more aliasing errors, because the frequency components above half the system sampling rate will "fold over" into the lower frequency spectrum and appear as false information that can not be distinguished from valid sampled data [123].

A reconfigurable DAQ architecture with an intelligent control unit, therefore, is required to respond to all above-mentioned requirements of multi-rate biomedical instrument. The reconfigurable DAQ architecture is proposed and illustrated in Figure 7.2. An intelligent control unit will be implemented to correspondingly adjust the filter cut-off frequency, PGA gain and system sampling speed based on which input channel is selected for processing.

In biomedical application, it is possible to previously identify the maximum data frequency of each input channel. Therefore, it is feasible to decide the suitable filter cut-off frequency for each channel. It will allow input channels, containing lower frequency components, to be sampled at lower rate while still achieving a given accuracy. Therefore, depending on which channel is selected for processing, a suitable filter cut-off frequency and sampling rate will be setup. Moreover, biopotential signals typically could have many different amplitude levels, it will be efficient to assign different PGA gains to different input channels to increase the precision of the data conversion process. The proposed DAQ architecture, therefore, is highly efficient for biomedical application as well as other multi-rate applications, such as process control application. It automatically selects the optimum method to 'condition' the input signals, depending the input channel requirements, so that high accuracy signal acquisition is achieved. Moreover, it correspondingly selects an optimal sampling speed for each input channel to reduce the system data storage, complexity and cost.

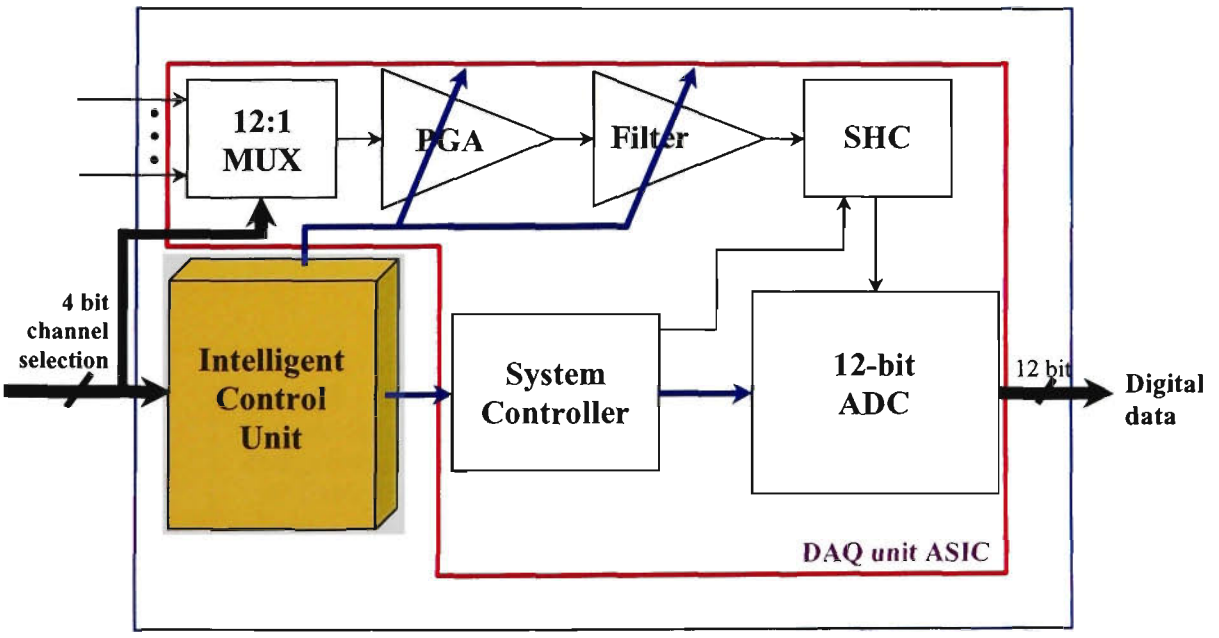



Figure 7.2 A Reconfigurable DAQ Architecture.

### 7.2.3.2 *Control Unit Implementation*

The control unit is the brain of the reconfigurable DAQ architecture and provides an intelligent interface between the host processor (PC) and the processing DAQ unit. Figure 7.3 shows the flow chart of the control unit's operation. The control unit continuously monitors the channel selection signals ($D_3D_2D_1D_0$). Once a 'different' channel from the current one is selected for processing, it will look up a required filter cut-off frequency, PGA gain and DAQ sampling rate from a look-up table (LUT). The LUT is stored in a re-writable memory so that it can be re-programmed to suit changes in the input channel requirements.

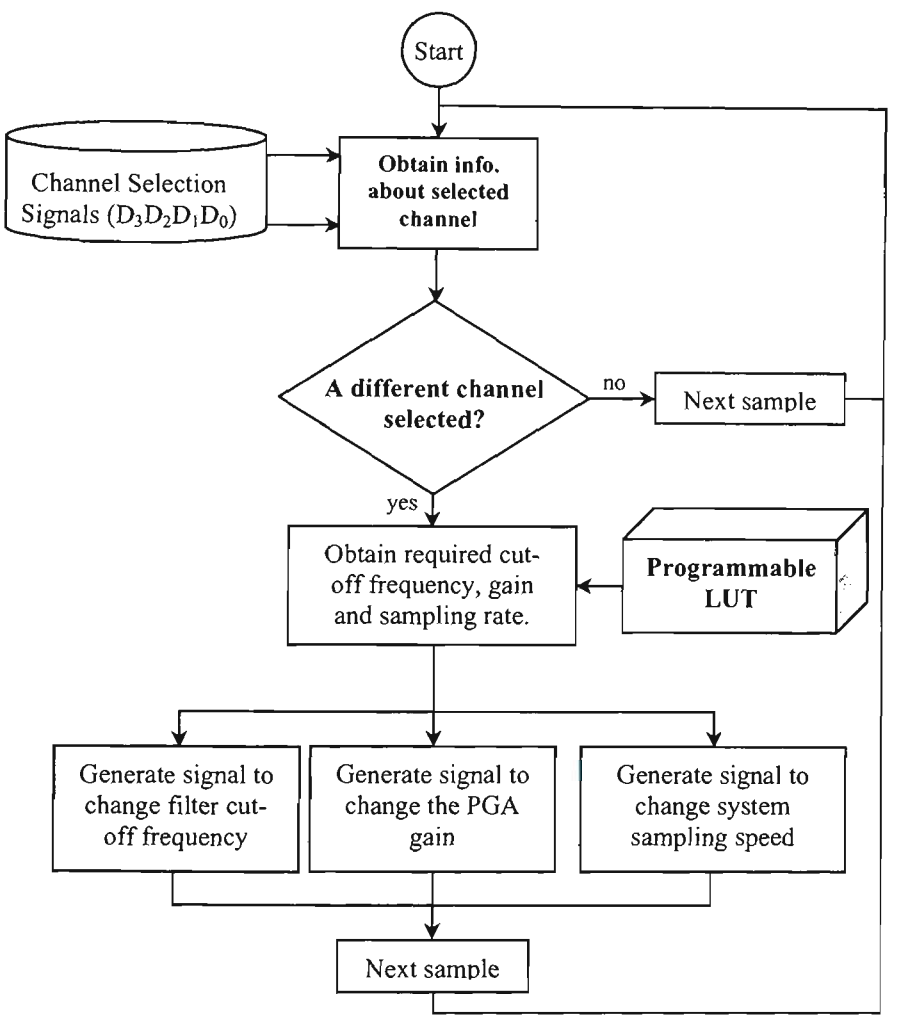



Figure 7.3 Control unit implementation.

## 7.3 ASIC Implementation of the Intelligent Control Algorithm

The intelligent control unit, developed in Section 7.2.3.2, has been implemented on a DSP core, which drastically increases system complexity, size, power consumption and cost. In order to reduce the system complexity and power as well as increase the system performance and efficiency, the intelligent control unit has been implemented on ASIC.

### 7.3.1 Algorithm Implementation Considerations

The proposed reconfigurable DAQ system should be flexible in the sense that it can change its operating characteristics to properly acquire different biosignals. To achieve such realisation, the controller was hardware partitioned so that the signal conditioning and acquiring requirements of the input channels are programmable. Based on the channel requirements, the reconfigurable DAQ system enters a real-time reconfigurable mode, where it continuously monitors the operating conditions and reconfigures the parameters of the system. When the reconfigurable DAQ architecture is employed in another biomedical instrumentation, it can be re-programmed so suit the new operating conditions. Such reconfigurable DAQ architecture is highly appropriate for not only biomedical application, but also all other multi-rate applications, such as process control application, where the DAQ architecture characteristics can be reconfigured to suit any changes of the input signal requirements.

In order to achieve the flexibility, the system characteristics are stored in an electrically erasable programmable read-only memory (EEPROM), allowing users to re-program the signal conditioning and implementing requirements at the DAQ level. In addition, proper hardware partitioning for the implementation of the intelligent controller is considered to achieve high speed with reduced complexity, small size and minimal power dissipation.

## 7.3.2 Design Considerations and Implementation

This section discusses the hardware considerations and implementation of the intelligent controller for biomedical instrument and other multi-rate applications. To achieve such universal reconfigurable DAQ system, the intelligent control unit has been hardware partitioned for an ASIC implementation, as illustrated in Figure 7.4.

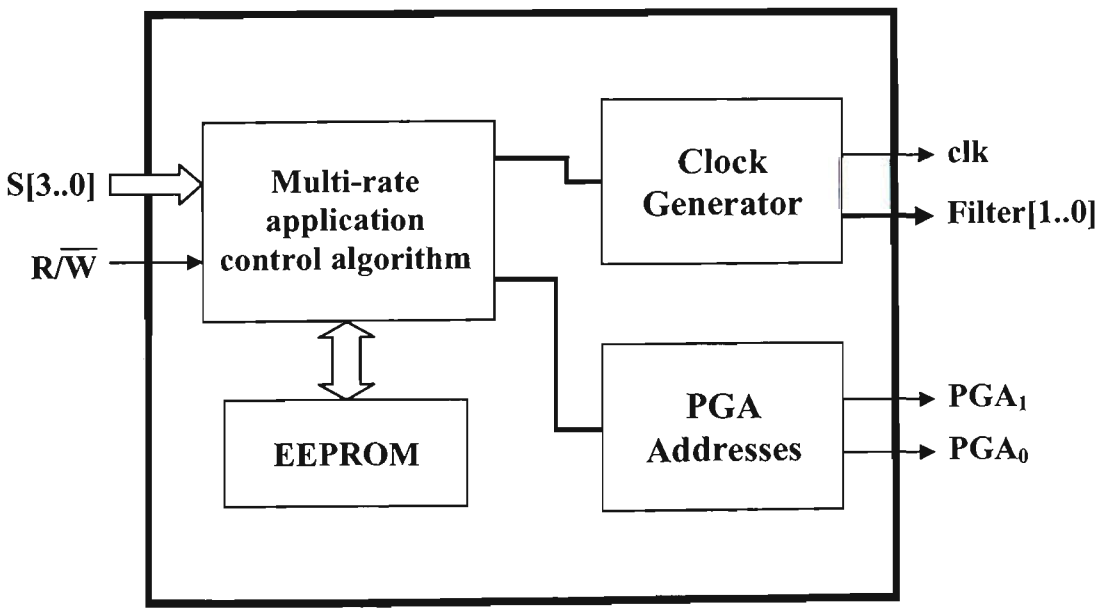



Figure 7.4 Hardware partition diagram of the intelligent controller.

The control algorithm was realised in VHDL - RTL and synthesised using a standard cell NEC 0.25-micron CMOS process in Synopsys Design Compiler. Figure 7.5 presents the top-level entity of the ASIC and the corresponding synthesised schematic is presented in Figure 7.6.

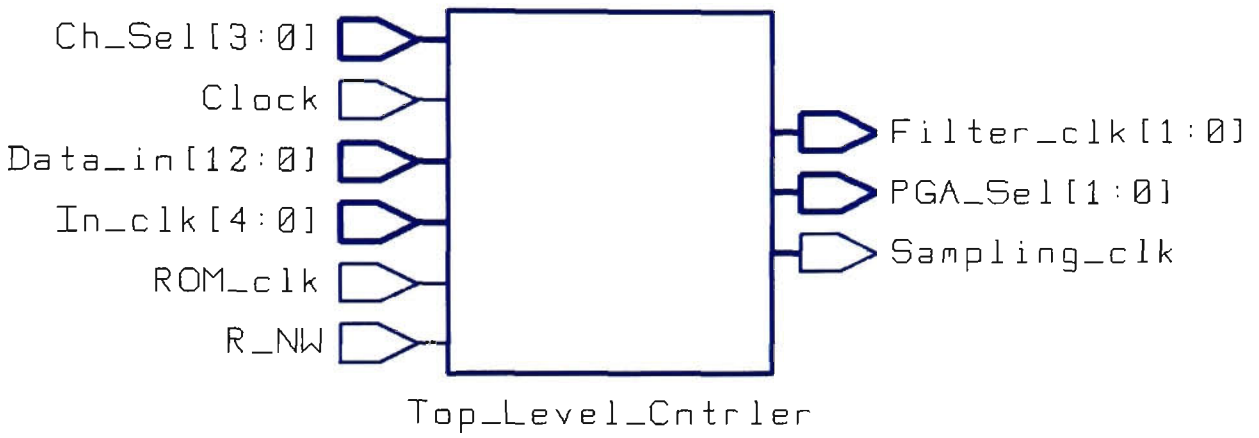



Figure 7.5 The intelligent controller ASIC top-level entity.

The Input-Output (I/O) signals of the implemented control unit are as follows:

A word length of 4 bits is used for the Ch_Sel signal to select the input channel for processing. The R_NW input signal is required to address the DAQ system to read data from the EEPROM or write a new data to the EEPROM. The Clock signal is the system clock. The output Sampling_clk will control the DAQ system master clock to change its sampling rate. Filter_clk signal will be sent to the on-chip filter while PGA_Sel signal will decide the gain of the PGA. ROM_clk is the clock of the internal EPPROM of the controller. Data_in, having a word length of 13 bits, is the input data to re-program the EPPROM. In_clk signal is required so that the clock generator in the controller is able to generate the Sampling_clk and Filter_clk signals.

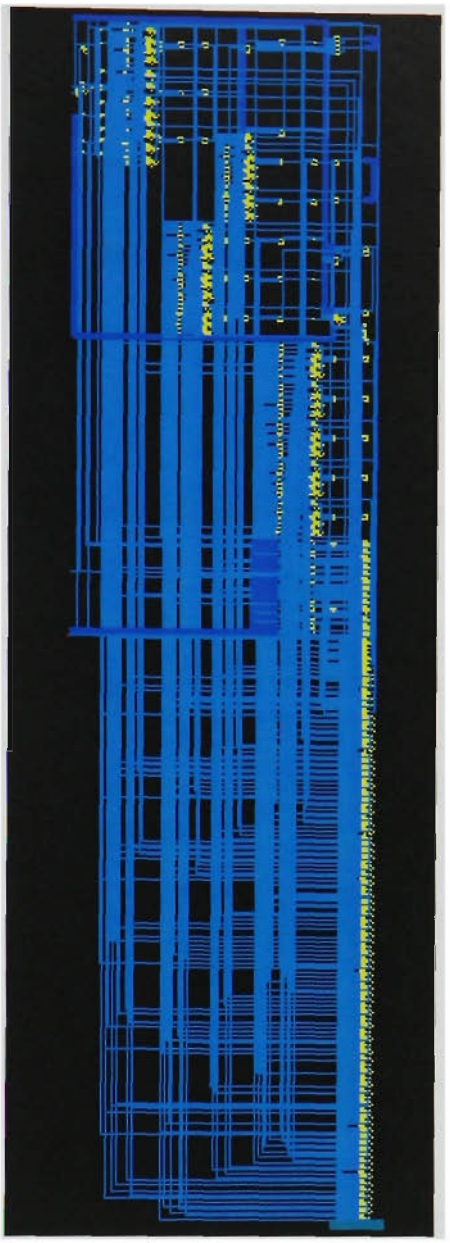


Figure 7.6 The intelligent controller ASIC synthesised schematic diagram.

## 7.4 System Performance Analysis

In this section, performance analysis of the intelligent controller implemented using a semi-custom ASIC approach and the proposed reconfigurable DAQ architecture for biomedical application is presented.

### 7.4.1 Intelligent Controller Performance Analysis

The performance analysis was carried out on the ASIC to ensure that it meets the timing requirement as well as the power requirements. The analysis was carried out at synthesis stage in Synopsys Design Compiler and is presented in Table 7.2.

Table 7.2 : Simulated results of the intelligent controller.

| *Property* | *Result* |
|---|---|
| Core Supply Voltage | 2.5 V |
| Critical Path | 0.42 ns |
| Power consumption | 300 µW |
| Average operating frequency | 120 kHz |
| Area | 0.027 $mm^2$ |
| Synthesis Technology | NEC 0.25µm CMOS process |

### 7.4.2 Reconfigurable DAQ System Performance Analysis

A traditional fix-rate DAQ system and the reconfigurable DAQ architecture have both been implemented using Cadence Analog Design Environment (Analog Artist). The objective is to carry out comparison of the two DAQ approaches and to demonstrate the superiority of the reconfigurable architecture. Table 7.3 shows the comparisons between the traditional fix-rate system and the designed reconfigurable DAQ architecture.

Results indicate that a 99% average data throughput reduction is obtained, 98% power consumption will be saved and the aliasing error is reduced by 76% when the

reconfigurable architecture is used instead of traditional DAQ system without anti-aliasing filter.

Table 7.3 : Comparison results of the two ADC circuit performance.

| **Property** | **Traditional fix-rate DAQ systems** | | **Proposed reconfigurable DAQ architecture** |
|---|---|---|---|
| | **Without anti-aliasing LPF** | **With anti-aliasing LPF** | |
| **Average system data throughput** | 125MS/s | 240kS/s | 120kS/s |
| **Average system Power Consumption** | 56.1mW | 6.36mW | 3.25mW |
| **Total Error** | 2.79% | 0.96% | 0.66% |
| **Master clock frequency** | 1GHz | 1GHz | 1GHz |
| **Max data throughput** | 125MS/s | 125MS/s | 125MS/s |
| **Power Consumption @ max rate** | 56.1mW | 65.6mW | 65.9mW |
| **Resolutions** | 12 bits | 12 bits | 12 bits |
| **Technology** | 0.18μm CMOS | 0.18μm CMOS | 0.18μm CMOS |
| **Supply Voltage** | 2.5V | 2.5V | 2.5V |

Results also reveals that a 50% average data throughput reduction is obtained, 47% power consumption will be saved and the aliasing error is reduced by 31% when the reconfigurable architecture is used instead of traditional fix-rate DAQ system with anti-aliasing filter. This reconfigurable DAQ system is well-suited for multi-rate biomedical application, where several channels are assessed using different sampling rate and amplification gain. Decreasing the sampling speed will reduce system power consumption and average data throughput, and hence correspondingly decrease system need for data storage and system complexity.

## 7.5 Conclusion

This chapter has presented the implementation of a novel reconfigurable DAQ architecture for biomedical instrumentation. The DAQ architecture is highly efficient for the biomedical application, in a sense that it automatically adjusts its signal conditioning function, including filtering condition and amplification gain, to suit the selected input channel for processing. In addition, it correspondingly varies its sampling frequency, depending on the input channel requirements. This allows input channels, containing lower-frequency components, to be sampled at lower rate to attain a given accuracy. Such reconfigurable DAQ architecture is appropriate for not only biomedical application, but also all other multi-rate applications, such as process control application, where the DAQ architecture characteristics can be reconfigured to suit any changes of the input signal requirements.

This chapter has also presented the semi-custom ASIC implementation of an intelligent controller that performs the proposed control algorithm for biomedical application and other multi-rate applications. In order to achieve a high flexibility, the system characteristics are stored in an EEPROM, allowing users to re-program the signal conditioning and acquiring requirements at DAQ level. In addition, proper hardware partitioning is considered for the implementation of the intelligent controller to achieve high speed with reduced complexity and size and minimal power dissipation. Analysis revealed that the intelligent controller achieved a maximum operating frequency of 2.3GHz, with 0.42ns critical path delay. The result indicates that it meets the timing requirements of the reconfigurable DAQ architecture when it operates at its typical

sampling rate of 120kS/s. The controller consumes only 301μW and utilises an area of 0.027 $mm^2$.

A performance analysis of the proposed reconfigurable DAQ architecture for biomedical application has been performed. The analysis showed that for the biomedical application, 50% average data throughput reduction is obtained, 47% power consumption will be saved and the aliasing error is reduced by 31% when the designed architecture is used instead of traditional fix-rate DAQ system with anti-aliasing filter. The reconfigurable DAQ architecture provides an efficient approach to enhance the system performance for the biomedical application and other multi-rate applications. In addition, it significantly reduces the system need for data storage and power consumption, hence accordingly reducing the system complexity and cost.

# Chapter 8

# Conclusions and Future Developments

## 8.1 Introduction

This chapter details the major findings of this work and how the work has addressed the aims proposed in Chapter 1. Also, it presents the conclusions that are drawn from the findings as well as the limitations and assumptions in this work. Future research options are also outlined in this chapter.

## 8.2 Major Findings

In this thesis, research on the design and implementation of a reconfigurable Data Acquisition (DAQ) System on a single IC has been presented. The thesis has addressed

major challenges and several critical issues related to electronic circuit design and integration of the new DAQ system on a single chip. New design techniques and circuit structures have been developed to reduce the DAQ system complexity and power dissipations as well as increase its speed and enhance its performance. In this work, a novel reconfigurable DAQ architecture has been proposed and implemented. The reconfigurable DAQ chip continuously monitors the operating requirements and automatically adjusts its characteristics, such as increasing its sampling rate or changing its amplification factor, to adapt the changes in the input conditions. Such reconfigurable property optimises the system function by reducing the system power consumption and complexity as well as increasing the system efficiency and performance. The reconfigurable DAQ chip is highly efficient and presents an important development for present and future applications.

Major findings of this thesis, results and novel ideas have been reported in related publications in 'List of Publications' section of this thesis. The findings in this thesis have addressed the aims, outlined in Chapter 1, and the following conclusions are drawn:

- **Design and implement the constituent components of a DAQ system**

DAQ system overview in Chapter 2 highlights that, there are several topologies to implement each building-block component. Each topology comprises of some advantages and disadvantages. Thus, the DAQ system performance can be greatly improved by selecting, modifying and optimising the device architectures. In this thesis several new component architectures are proposed to achieve a DAQ system with high

performance, high-speed, low power consumption, low complexity and low cost for specific applications. The proposed DAQ system contains an analog Multiplexer (MUX), a Programmable Gain Amplifier (PGA), a Switched-Capacitor (SC) anti-aliasing filter, a Sample and Hold circuit (SHC) and an Analog-to-Digital converter (ADC).

A 12:1 analog MUX has been designed using only one stage of CMOS transmission gate (TG) switches from input to output in order to reduce the device delay and also increase its accuracy. In this design, CMOS TG is selected to implement the switches due to its superior characteristics including high dynamic analog range and clock feedthrough error elimination.

The PGA has been designed and implemented in Chapter 3. It employs linear resistors in the feedback network to achieve high linearity, permitting the device to achieve a THD of -80dB. This chapter also presents the design and implementation of a SHC employing feedback loop and a compensation capacitor. The main advantage of this architecture is that the charge injection error and the clock feedthrough error are effectively removed, providing a very high-accuracy.

A programmable SC filter employing both inverting and non-inverting integrators to improve device accuracy and stability level is implemented. In this filter design, additional feedback capacitors have been included to compensate the offset voltage and DC gain error of the operational amplifiers (OPAMs). The filter provided the DAQ system an attractive feature of programmable cut-off frequency.

ADC is the most critical and the most area and power consuming device in a DAQ system. In Chapter 3, a new modified flash ADC has been proposed and implemented to reduce the system complexity and power consumption. It requires only $(2^{n-2} + 2)$ comparators to implement an n-bit modified flash ADC, compared to $2^n$-1 comparators required for a traditional n-bit flash ADC. This greatly reduces the complexity of the flash ADC approach. The modified flash ADC development is based on the implementation of an optimised comparator that offers an attractive combination of high-speed, low-power and high accuracy. To achieve a high resolution system, three four-bit modified flash ADC modules has been cascaded in pipeline ADC architecture. Results indicate that 40% power saving is obtained and 60% of comparators could be saved when the modified flash ADC is used instead of a full flash ADC to design a pipeline ADC. This enables a realisation of a high-speed, high-accuracy DAQ chip with reduced power and complexity.

In order to improve the DAQ system performance, a mathematical model has been developed and presented in Chapter 4 to represent noise generated within all of its constituent components, including the proposed 12-bit pipeline ADC architecture, 12:1 MUX, PGA, anti-aliasing filter and SHC. The developed model provides a good estimation of the noise generated by the circuit and gives an accurate prediction on the circuit noise performance.

- **Develop the DAQ chip using the proposed building block components**

A multi-channel 12-bit DAQ system on a single IC has been implemented by integrating the design recommendations of the building block components, using the

0.18-micron full custom CMOS technology. In order to control and synchronise constituent components of the DAQ system, a system controller, which is the intelligence behind the DAQ architecture, has been implemented. In addition, the controller receives control signals from outside environment and generates output signals, representing the progress of the data conversion procedure to the outside world.

The system controller has been designed to be compatible with the parallel Peripheral Component Interconnect (PCI) bus standard, so that the proposed DAQ system is able to communicate with and transfer data to and from a host Personal Computer (PC) or a Microprocessor. The communication interface of the controller consists all of the standard signals required for the PCI bus standard, as presented in Table 5.1. The controller also generates an REQ signal as an interrupt to the PC, so that the PC will no longer waste processing time by waiting for the completion of the data conversion process.

Performance analysis of the implemented DAQ system shows that the final DAQ design can obtain 125MS/s sampling rate. It dissipates only 65.6mW of power when a modified flash ADC architecture as compared to 97.9mW power consumption when the traditional flash ADC was used. Results yields that 31% of die size could be saved and 33% power saving is obtained with the employment of the modified flash ADC architecture. This greatly reduces the system complexity, power consumption and cost.

- **Develop a novel reconfigurable DAQ architecture to improve the system performance and efficiency for power system protection application**

A novel reconfigurable DAQ architecture for power system protection application has been proposed and implemented. At the normal operating conditions, the proposed reconfigurable DAQ architecture operates at a low sampling speed and the anti-aliasing filter cut-off frequency is reduced. This approach leads to a low data throughput and a host CPU processing time saving, enabling a reduction of the system need for data storage and hence accordingly reducing the system complexity. The reconfigurable DAQ architecture is capable of reconfiguring its characteristics, such as adjusting its conditioning circuit and increasing its sampling rate, depending on the occurrence of a fault in the network. High-speed sampling permits the system to not only accurately detect and locate the fault but also capture sufficient information for further analysis.

This chapter has also presented the semi-custom application specific integrated circuit (ASIC) implementation of an intelligent controller that performs the proposed control algorithm power system protection application. A novel approach to determine the line impedance angle has been proposed. This approach eliminates the square-root and arc-tan operations to reduce the cost of the semi-custom ASIC implementation. Analysis revealed that the intelligent controller achieved a maximum operating frequency of 100MHz, with 10ns critical path delay. The result indicates that it meets the timing requirements of the reconfigurable DAQ architecture. The controller core occupies an area of 1.9mm$^2$.

A performance analysis of the proposed reconfigurable DAQ architecture for power system protection application has been performed. Results reveal that a 33% power saving is obtained and 31% of the total number of transistors could be minimised when

the new modified flash ADC is used instead of a full flash ADC. The analysis also indicated that for the power system protection application, a 63% average data throughput reduction is obtained, the total sampled data is reduced by 63% when the reconfigurable property was implemented to the DAQ system. The reconfigurable DAQ architecture provides an efficient approach to enhance the system performance and power system protection application. It significantly reduces the system need for data storage and power consumption, hence accordingly reducing the system complexity and cost, and increasing the system speed and accuracy.

- **Develop a novel reconfigurable DAQ architecture to improve the system performance and efficiency for biomedical application**

A novel reconfigurable DAQ architecture, which has been developed in Chapter 7, is highly efficient for not only biomedical application, but also all other multi-rate applications, such as process control application, where the DAQ architecture characteristics can be reconfigured to suit any changes of the input signal requirements. It automatically adjusts its signal conditioning function, including filter characteristics and amplifier gain, to satisfy the requirements of the selected input channel for processing. In addition, it correspondingly varies its sampling frequency, depending on the input channel requirements. This allows input channels, containing lower-frequency components, to be sampled at lower rate to attain a given accuracy.

This chapter has also presented the semi-custom ASIC implementation of an intelligent controller that performs the proposed control algorithm for biomedical application and multi-rate applications. In order to achieve a high flexibility, the system characteristics

are stored in an EEPROM, allowing users to re-program the signal conditioning and acquiring requirements for the data acquisition process. In addition, proper hardware partitioning is considered for the implementation of the intelligent controller to achieve high speed with reduced complexity and minimal power dissipation. Analysis revealed that the intelligent controller achieved a maximum operating frequency of 2.3GHz, with 0.42ns critical path delay. The result indicates that it meets the timing requirements of the reconfigurable DAQ architecture for biomedical application. The controller utilises and area of $0.027mm^2$.

A performance analysis of the proposed reconfigurable DAQ architecture for biomedical application has been performed. The analysis showed that for the biomedical application, 50% average data throughput reduction is obtained, 47% power consumption will be saved and the aliasing error is reduced by 31% when the designed architecture is used instead of traditional fix-rate DAQ system with anti-aliasing filter. The reconfigurable DAQ architecture provides an efficient approach to enhance the system performance for the biomedical application and other multi-rate applications. In addition, it significantly reduces the system need for data storage and power consumption, hence accordingly reducing the system complexity and cost.

## 8.3 Limitations and Assumptions

The results and analysis presented in this thesis are based on a series of mathematical models, circuit and system simulation and circuit implementation. The limitations and assumptions made in this thesis are discussed in this sub-section.

The ASIC implementation of the intelligent controllers, that performs the reconfigurable control algorithms for the preferred applications, is synthesised in Synopsys Design Compiler. The results do not include the power consumption of the complete controller ICs, only the core circuitry. Implementing the controller on chip will slightly increase the power consumptions of the controllers.

The development of a reconfigurable DAQ architecture and its performance analysis for power system protection application are based on a power system mathematical model, developed and simulated in MATLAB. The developed model has accurately simulated the signals travelling on transmission lines before and after the occurrence of a fault. However, the model has not considered the random noise in the transmission system. This possibly will result in a slight increase the sampling rate of the proposed reconfigurable DAQ system during normal conditions to compensate the error introduced by the noise floor. In addition, transmission line signals can be affected by environment attributes, such as temperature, moisture, wind speed, etc. For these reasons, it will be beneficial to obtain measured data of the line signals in a real transmission system during fault and normal conditions, since a re-simulation of the proposed DAQ architecture with the protected line measured values will provide results with better accuracy.

The noise performance analysis and the noise model development of critical components in the proposed reconfigurable DAQ architecture, introduced in Chapter 4, are based on noiseless input signals. In another word, the total input noise power to the device is assumed to be zero, which could slightly affect the total device output noise

power. However, the noise analysis presented in Chapter 4 is concentrated on the total noise generated within the circuits themselves in order to improve the device performance as well as to represent the lower limit to the size of electrical signals that can be read by the devices without significant deterioration in signal quality. For this reason, it is practicable to assume that the input signals to the devices are noiseless and does not influence the results.

## 8.4 Future Work

The following are some of the issues related to the future research into reconfigurable DAQ system design and implementation:

Future work can involve system simulation with measured results of a real transmission system during fault and normal conditions. It will be motivating to analyse the results, as it will provide a more precise approach to demonstrate the effect of the reconfigurable architecture on the power systems. Using the practical approach, the DAQ system sampling speed requirement may be increased to compensate noise and environment effects in the transmission lines. This may result in minor amendments so that the reconfigurable DAQ architecture is well-suited for realistic power transmission systems.

The function of the proposed reconfigurable DAQ chip for microprocessor-based relays can be further improved by incorporating memory circuits on the chip. This will result in greater device flexibility and efficiency, where the DAQ system can continuously

sample the protected line signals (voltages and currents) at its maximum speed when a fault occurs and place the sampled data in the on-chip memory. The host PC will access the data when it is ready. This approach prevents possible missing data in situations where the PC is overloaded and/or data is congested when the PC needs to handle too many interrupts.

Future work can include the full implementation of the intelligent controllers and testing the final chip. Before the full implementation can be fabricated, some further optimisation of the layout is required to improve the overall system performance and efficiency.

Future work can involve an extension of the proposed DAQ scheme to Multiple Input Multiple Output (MIMO) Systems for Wireless Communications. In communication theory, MIMO refers to radio links with multiple antennas at the transmitter and the receiver side. Given multiple antennas, the spatial dimension can be exploited to improve the performance of the wireless link. However, each channel at the receiver side requires a separate data conversion system, and thus inducing high cost. The proposed DAQ scheme, featuring a high-speed characteristic, enables savings since multiple channels can be served using only one DAQ chip. In addition, the employment of the modified flash ADC architecture within the DAQ system permits a large reduction in the system power consumption, complexity and cost. This approach, thus, could be highly beneficial in MIMO receivers.

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# Appendix A

# MOS FET Noise Analysis

In order to provide supplement information in regards to the integrated circuit (IC) noise analysis in Chapter 4, the detailed noise model of a Metal-Oxide Semiconductor (MOS) Field Effect Transistor (FET) is presented in this appendix. The information in this appendix is directly taken from [93], [103] and [104].

## A.1 Noise Sources in a MOS Transistor

In this section, a detailed overview of all noise sources in a MOS FET is considered. Each type of noise sources is associated with a different phenomenon in a transistor and has a different degree of effect on the transistor noise performance.

## A.1.1 Short Noise

Short noise is associated with a direct-current flow and is present in MOS transistors. When a MOS transistor is forward-biased, an electrical filed exists in the depletion region and creates a potential difference between the n-type and p-type regions, thus inducing a forward current in a MOS. The current is composed of holes from the p-region and electrons from the n-region, which have sufficient energy to overcome the potential barrier at the junction. Once these carriers have crossed the junction, they diffuse away as minority carriers. Thus, the current, which appears to be steady, is, in fact, composed of a large number of random independent current pulses. The fluctuation in this current, $I$, is termed short noise, and is generally specified by [93]:

$$\overline{i_{short}^2} = \lim_{T\to\infty} \frac{1}{T} \int_0^T (I - I_{AV})^2 \, dt \tag{A.1}$$

where $I_{AV}$ is the average current value.

It can be shown that if a current $I$ is composed of a serries of random independence pulses with average value $I_{AV}$, then the resulting noise current has a mean-square value of [93]:

$$\overline{i_{short}^2} = 2q_e \cdot I_{AV} \cdot \Delta f \tag{A.2}$$

where $q_e$ is the electron charge and $\Delta f$ is the bandwidth is Hertz.

Equation (A.2) shows that the noise current has a mean-square value that is directly proportional to the bandwidth. Thus, the noise current spectral density ($\overline{i^2}/\Delta f$) is a

constant function of frequency. This type of noise is called *white noise* [93].

## A.1.2 Thermal Noise

Thermal noise is due to the random thermal motion of electrons (Johnson effect) since the typical electron drift velocities in a semiconductor are much less than electron thermal noise. This type of noise is unaffected by the presence or absence of a direct current. Since this source of noise is the thermal motion of electrons, it is related to temperature and is independent of frequency [93]:

$$\overline{i_{thermal}^2} = 4kT\frac{2}{3}g_m\Delta f \tag{A.3}$$

where $k$ is the Boltzmann's constant and $T$ is the absolute temperature, $g_m$ is the MOS FET transconductance and $\Delta f$ is the bandwidth (in Hertz).

Equation (A.3) implies that this type of noise is independent of frequency, thus, it is another source of white noise. This type of noise is a fundamental physical phenomenon and is present in any resistive devices. This is the major noise source in a MOS transistor [103].

## A.1.3 Flicker Noise

The origin of flicker noise is associated with traps that are related to device contamination and crystal defects. These traps capture and release charge carriers in a

random fashion and the time constants associated with the process give rise to a noise signal with energy concentrated at low frequencies. Flicker noise, whish is always associated with a flow of direct current, displays a spectral density of the form [93]:

$$\overline{i_{flicker}^2} = K_1 \frac{I^a}{f^b} \Delta f \tag{A.4}$$

where $I$ is the direct current, $K_1$ is a constant for a particular device, $a$ is a constant in the range of 0.5 to 2 and $b$ is a constant about unity.

Since $b$ is approximately equal to zero, the noise spectral density has a $1/f$ frequency dependence (hence the alternative name of 1/f noise). It is apparent that flicker noise is most significant at low frequencies. However, in devices exhibiting high flicker noise levels, this noise may dominate the device noise at frequencies into the megahertz range. In addition, the mean-square value of a flicker noise signal as given in equation (A.4) contains an unknown constant $K_1$. This constant not only varies by orders of magnitude from one device type to another, but also varies widely for different transistors from the same process wafer. However, experiments have shown that a typical value of $K_1$ can be determined and then can be used to predict average or typical flicker noise performance for ICs from that process [104].

### A.1.4 Burst Noise

This is another type of low-frequency noise found in MOS transistors. The source of this noise is not fully understood, although it has been shown to be related to the presence of heavy-metal ion contamination. Burst noise is so named because of an

oscilloscope trace of this type of noise shows bursts of noise on a number of discrete levels. The repetition rate of the noise pulse is usually in the audio frequency range (a few kilohertz or less) and produces a popping sound when played through a loud speaker. This has led to the name of popcorn noise for this phenomenon. The spectral density of burst noise can be determined by [93]:

$$\overline{i_{burst}^2} = K_2 \frac{I^c}{1+\left(\frac{f}{f_c}\right)^2} \Delta f \tag{A.5}$$

where $K_2$ is a constant for a particular device, $c$ is a constant in the range of 0.5 to 2 and $f_c$ is a particular frequency for a given noise process. Equation (A.5) shows that this type of noise is insignificant at medium and high frequency ranges. Therefore, it is typically not considered in the noise analysis of the MOS transistors [93].

## A.2 Noise Model of a MOS Transistor

As summarised in the previous section, there are several noise sources in a MOS transistor. Since the channel material is resistive, it exhibits thermal noise. This noise source can be represented by a noise-current generator, $\overline{i_d^2}$, from drain-to-source in the small signal equivalent circuit of Figure A.1 [93].

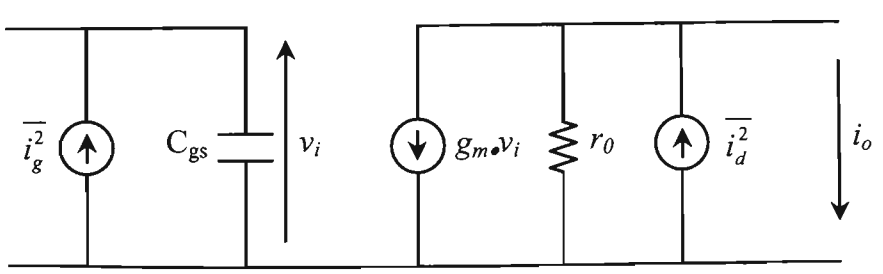


Figure A.1 MOS FET small-signal equivalent circuit with noise sources [93].

Another source of noise in MOS transistors is flicker noise. Because MOS transistors conduct current near the surface of the silicon where surface states acts as traps that capture and release carriers. The flicker noise is found experimentally to be represented by a drain-source current generator, and the flicker noise and thermal noise can be lumped into one noise generator, as illustrated in Figure A.1, where [93]:

$$\overline{i_d^2} = \overline{i_{thermal}^2} + \overline{i_{flicker}^2} = 4kT\left(\frac{2}{3}g_m\right)\Delta f + K_1\frac{I^a}{f}\Delta f \qquad \text{(A.6)}$$

Another source of noise in the MOS transistors is short noise generated by the gate leakage current. This noise can be represented by $\overline{i_g^2}$, as shown in Figure A.1, where:

$$\overline{i_g^2} = 2q_e \cdot I_G \cdot \Delta f \qquad \text{(A.7)}$$

This type of noise, however, is usually very small since the DC gate current $I_G$ is typically less than $10^{-15}$ A. Thus, it is negligible in calculating the noise performance of a MOS transistor [93].

## A.3 MOS Transistor Input Noise Generator

From the noise analysis in section B.2, an equivalent input noise generator for a MOS FET can be calculated using a circuit, as illustrated in Figure A.2. This circuit is equivalent to that of Figure A.1. If the inputs of both the circuits, in Figure A1 and Figure A2, are short circuited and resulting output noise current, $i_o$, are equated, we obtain [93]:

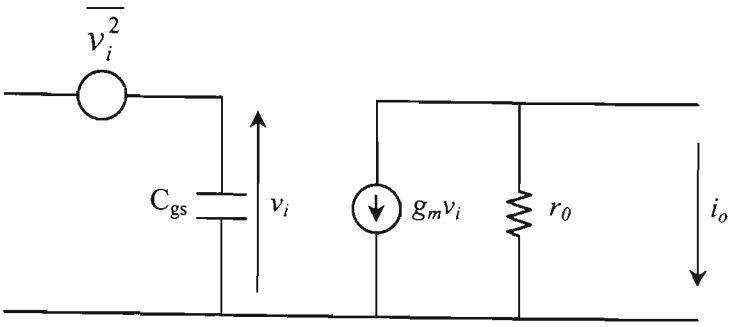


Figure A.2 MOS FET small-signal circuit with equivalent input noise generator [93].

$$i_d = g_m v_i \tag{A.8}$$

and thus,

$$\overline{v_i^2} = \frac{g_m}{\overline{i_d^2}} \tag{A.9}$$

Substituting equation (A.6) into equation (A.9) gives [93]:

$$\frac{\overline{v_i^2}}{\Delta f} = 4kT\frac{2}{3g_m} + K_1\frac{I^a}{g_m^2 f}\Delta f \tag{A.10}$$

The input-referred flicker noise component in equation (A.10) is typically larger than the thermal noise component for frequencies below 10kHz. Thus, an accurate representation of the input-referred flicker noise component is important for the optimisation of the noise performance of MOS analog circuits. The physical mechanisms giving rise to the flicker noise have received extensive study [104]. The exact dependence of the magnitude of the input-referred flicker noise is dependent on the details of the device fabrication process. In most cases, the magnitude of the input-referred flicker noise component is approximately independent of bias current and voltage and is inversely proportional to the active gate area of the transistors. It is also

observed practically that the input-referred flicker noise is an inverse function of the gate-oxide capacitance per unit area. Therefore, the equivalent input noise generator of a MOS transistor can be written as [93]:

$$\overline{v_i^2} = \frac{8kT}{3g_m}\Delta f + \frac{K_f}{WLC_{ox}f}\Delta f \qquad \text{(A.11)}$$

Measurements show that the typical value for constant $K_f$ is $3 \times 10^{-24}$ ($V^2F$) [93].

# Appendix B

# ASIC Design Methodology

An application specific integrated circuit (ASIC) is an integrated circuit (IC) designed for a specific application. ASICs are used in a wide-range of applications. It can be pre-manufactured for an application or can be custom manufactured for a particular customer application [124]. There are basically two approaches to implement an ASIC, a semi-custom ASIC design methodology and a full-custom ASIC design methodology. The two methodologies, which have been used in this thesis for the implementation of the reconfigurable data acquisition (DAQ) system, are presented in this appendix.

## B.1 Full-Custom ASIC Design Methodology

A full custom ASIC contains customised logic cells (gates etc.) as well as customised mask layers. A microprocessor is an example of an IC that is 'full custom' – designers

spend a lot of time squeezing the most out of every last square micron of chip space by hand. In a full custom ASIC, the engineer designs and optimises all the logic cells, circuits and layout specifically for one ASIC. Full-custom ASICs, thus, obtain advantages of better performance and lower power consumption than its semi-custom ASIC counterparts. The full-custom ASIC design methodology is presented in Figure B.1 [124-126].

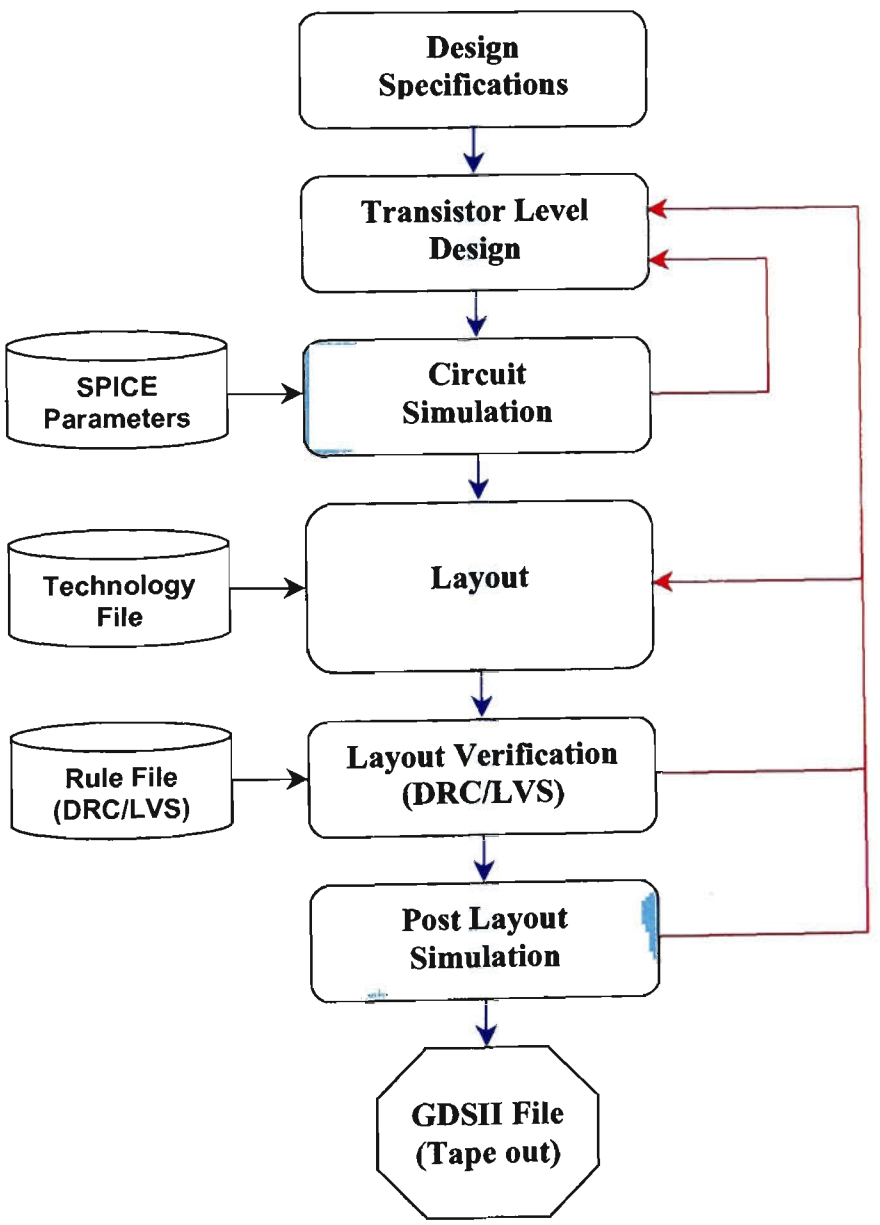


Figure B.1 Full-custom ASIC design methodology [124].

The full-custom AISC design flow is as follows [124-126]:

Firstly, the engineer obtains a set of design specifications for the ASIC and performs the design entry. The design entry is typically a schematic entry at transistor level. The design is then simulated, using the SPICE model for transistors, with a certain test bench. Recurrence circuit design and simulation are performed to ensure that all of the design constrains are met.

The layout creation phase is a critical process in ASIC implementation. It typically involves floor planning and place and route process. Floor planing involves setting the parameters of the chip layout, such as core utilisation, input-output (I/O) pad placement, as well as allocating chip space for voltage routing. Place and route involves placing all components of the design (combinational logic, gates, memories, etc) in the core provided by the floor planing and then routing all the connections between the components.

Layout verification is then performed to verify the circuit layout creation. At this stage, design rule check (DRC) and layout versus schematic check (LVS) is carried out to verify the design. Design rules are the restrictions of the mask patterns that are used for the fabrication of the IC circuit. Subsequently, post layout simulation is performed to verify if timing constraints are met. The layout parasitic extraction is performed to *extract* the exact values of parasitic capacitances and resistances from the layout data. The extracted circuit is then re-simulated to find out how parasitic capacitances and resistances affect the circuit behaviour. The final stage in the design flow is the tape out

where the engineer generates a file (GDSII) to send to the manufacturer foundry for fabrication.

## B.2 Semi-Custom ASIC Design Methodology

A semi-custom ASIC, also known as a 'cell-based' ASIC, uses predesigned logic cells (AND gates, OR gates, Multiplexers, Flip-flops etc.) known as standard cells. The ASIC designer defines only the placement of the standard cells and the interconnect in a semi-custom ASIC. However, the standard cells can be placed anywhere on the silicon die. The advantage of semi-custom ASICs is that the designer saves time & money and reduces risk of design errors by using a predesigned, pretested and precharacterised standard-cell library. The semi-custom ASIC design methodology is presented in Figure B.2.

The semi-custom ASIC design flow is as follows [124-126]:

Firstly, the engineer obtains a set of design specifications for the ASIC and performs the design entry. The design entry is typically register transfer level (RTL) – hardware description language (HDL), such as Very High Speed Integrated Circuit HDL (VHDL) or Verilog. A certain set of timing constrains is considered in the design and the design is simulated with a certain test bench.

Synthesis is the process of mapping the logic in the RTL to a certain set of building blocks from a synthesis library to produce a schematic of the design and the engineer

can also perform test insertion. After that, several analyses is performed at the gate-level to verify the design. Static timing analysis can be performed to estimate the critical path delays and maximum clock frequency of the ASIC. Power consumption analysis will provide the engineer with an estimation of the core circuitry power consumption (static and dynamic).

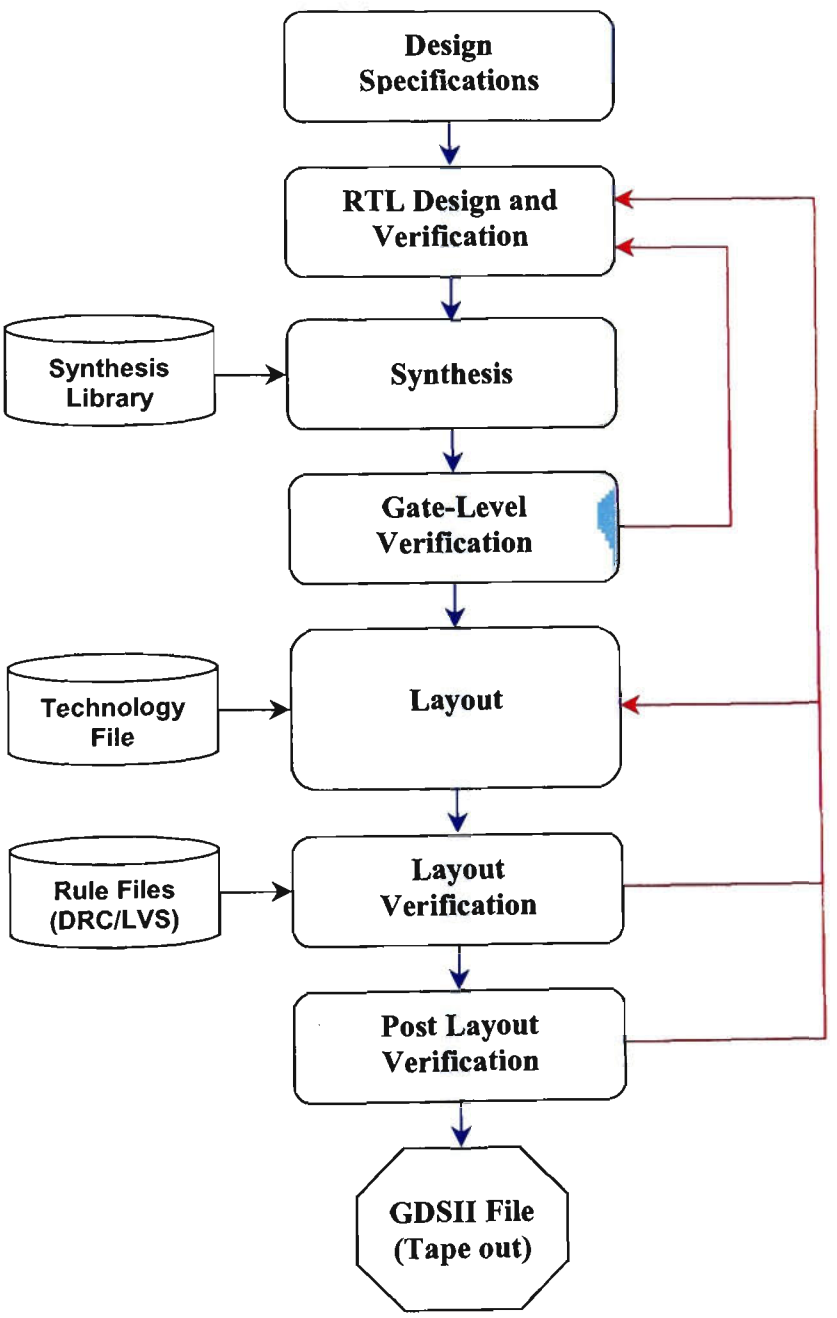


Figure B.2 Semi-custom ASIC design methodology [124].

The layout creation phase is divided into the following steps: Floor planning (which is also part of the pre-layout design process), clock tree generation and place and route. Floor planing involves setting the parameters of the chip layout, such as core utilisation, input-output (I/O) pad placement, as well as allocating chip space for voltage routing. When the ASIC complexity (gate count) increases, the clock signal may require an even timed distribution throughout the layout. A large chip may contain hundreds of clocked elements (e.g. flip-flops), therefore a great deal of buffering is required and care is taken in the layout to ensure all clocked elements switch at the same time. Clock tree generation is the process of achieving the even clock distribution. Place and route involves placing all components of the design (combinational logic, gates, memories, etc) in the core provided by the floor planing and then routing all the connections between the components.

The latter concludes the layout creation process, and then followed by layout verification, which includes geometrical DRC, LVS and a parasitic extraction. Post layout verification is performed to allow the engineer to perform static timing analysis to verify if timing constraints are met. After successful completion of all layout verification steps to confirm that the design complies with the timing specification, based on post-layout timing verification, the final stage in the design flow is the tape out where the engineer generates a file (GDSII) to send to the manufacturer foundry for fabrication.