Power Management Schemes for Ultra Low Power Biomedical Devices

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"Never look down on anybody unless you are helping them up."

--Jesse Jackson

"Everyone who works have some burdens to bear in their lives. Not just you. Still everyone continues working. That's what it means to work for a living."

--Bambino

"People who don't focus on the job in front of them have no right to talk of their dreams."

--Bambino

"The greatest danger for most of us is not that our aim is too high and we miss it, but that is too low and we reach it."

--Michelangelo

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Declaration of Originality

"I, David Fitrio, declare that the PhD thesis entitled "Power Management Schemes for Ultra Low Power Biomedical Devices" is no more than 100,000 words in length, exclusive of tables, figures, appendices, references and footnotes. This thesis contains no material that has been submitted previously, in whole or in part, for the award of any other academic degree or diploma. Except where otherwise indicated, this thesis is my own work".

Signature Date

David Fitrio

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List of Figures

Note to the reader: *Many of the design and simulation packages used in this thesis do not permit the use of super-scripts and sub-scripts in the production of the figures. As a result many symbols appear in a standard format.*

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List of Abbreviations

AC	Alternating Current
ADC	Analog to Digital Converter
ADSL	Asymmetric Digital Subscriber Line
ALU	Arithmetic Logic Unit
ASIC	Application Specific Integrated Circuit
BAN	Body Area Network
BL	Bit Lines
BSIM	Berkeley Short-Channel IGFET Model
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
CV	Capacitance-Voltage
DAC	Digital to Analog Converter
DC	Direct Current
DFT	Discrete Fourier Transform
DIF	Decimation in Frequency
DIT	Decimation in Time
DNL	Differential Non-Linearity
DR	Dynamic Range
DRAM	Dynamic Random Access Memory
DSP	Digital Signal Processor
DVS	Dynamic Voltage Scaling
DVFS	Dynamic Voltage and Frequency Scaling
EDA	Electronic Design Automation
EDP	Energy Delay Product
ESR	Equivalent Series Resistance
FET	Field Effect Transistor

FFT	Fast Fourier Transform
FPGA	Field Programmable Gate Array
FSM	Finite State Machine
IC	Integrated Circuit
ICT	Information and Communication Technology
INL	Integral Non-Linearity
IV	Current-Voltage
ISDN	Integrated Services Digital Network
LCM	Leakage Current Monitor
Li-Ion	Lithium Ion
LLUL	Low Leakage, Ultra Low Leakage
LPF	Low Pass Filter
LSB	Least Significant Bit
MEMS	Micro-Electro-Mechanical Systems
MOS	Metal-Oxide-Semiconductor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
MSB	Most Significant Bit
MTCMOS	Multi-Threshold Complementary Metal Oxide Semiconductor
MUX	Multiplexers
NMOS	Negative-Channel Metal Oxide Semiconductor
NiCD	Nickel-Cadmium
NiMH	Nickel-Metal Hydride
NML	Noise Margin
PAN	Personal Area Network
PDP	Power Delay Product
PFD	Phase Frequency Detector
PFM	Pulse Frequency Modulation
PLL	Phase Locked Loop
PMOS	Positive-Channel Metal Oxide Semiconductor
PWM	Pulse Width Modulation
R-2R	Resistor to Two Resistor Weighted Network

RDD	Responsive Drug Delivery
RAM	Random Access Memory
RF	Radio Frequency
RTL	Register Transfer Logic
SOC	System on Chip
SR	Slew Ratio
SRAM	Static Random Access Memory
VCO	Voltage Controlled Oscillator
VLSI	Very Large Scale Integration
VTC	Voltage Transfer Characteristics
VTCMOS	Variable Threshold Complementary Metal Oxide Semiconductor
W-2W	Width to two Width Transistor Ratio
WBAN	Wide Body Area Network
WL	Width and Length

List of Publications

1. D.Fitrio, J.Singh, A.Stojcevski, “Dynamic Voltage Scaling for Power Aware Fast Fourier (FFT) Transform,” *Lecture Notes on Computer Science*, Springer-Verlag ACSAC, pp. 52-64, 2005.

2. D.Fitrio, A.Stojcevski, J.Singh, “Leakage Current Reduction Techniques for Subthreshold Circuit in a Simulation Environment,” Published in *Best of Book, AMSE Journal Press*, 2004.

3. D.Fitrio, A.Stojcevski, J.Singh, “Ultra Low Power Weak Inversion Current Steered Ditital to Analog Converter,” *2006 IEEE Asia Pacific Conference on Circuits and Systems.* Ed(s). Y P Yang. IEEE, pp.1545-1548, 2006.

4. D.Fitrio, J.Singh, A.Stojcevski, “Energy Efficient Low Power Shared-Memory Fast Fourier Transform (FFT) Processor with Dynamic Voltage Scaling,” *SPIE International Symposium on Microelectronics: Design, Technology and Packaging II*, Vol. 6035, pp.69-79, 2006.

5. D.Fitrio, J.Singh, A.Stojcevski, “Dynamic Voltage Scaling Implementation for Power Management,” *IFIP WG 10.5 Conference on Very Large Scale Integration-System On a Chip*, pp.459-464, 2005.

6. D.Fitrio, J.Singh, A.Stojcevski, “Energy Efficient Shared-Memory Fast Fourier Transform (FFT) Processor,” *ATcrc Telecommunications and Networking Conference*, 2005.

7. A.Stojcevski, V.Soundararaman, D.Fitrio, A.Zayegh, “Analog to Digital Converter for Dual-Standard Mobile Receiver,” *IEEE International Conference on Modelling and Simulation (ICMS)*, 2005.

8. A.Stojcevski, K.Y. Law, D.Fitrio, A.Zayegh, “Modelling and Simulation of a Data Conversion Architecture for a Bluetooth Device,” *IEEE International Conference on Modelling and Simulation (ICMS)*, 2005.

9. D.Fitrio, A. Stojcevski, J. Singh, “Subthreshold Leakage Current Reduction Techniques for Static Random Access Memory,” *SPIE International Symposium on Smart Materials, Nano and Micro-Smart Systems*, Vol. 5649. pp. 673-683, 2004.

10. D.Fitrio, A. Stojcevski, J. Singh, “Leakage Current Reduction Techniques for Subthreshold Circuit in a Simulation Environment,” *International Conference on Modelling and Simulation (ICMS 04).* Ed(s). Y. Municio Y and Angle M Qento. Association for Modelling and Simulation in Enterprise (AMSE), Palemcia, Espana, pp. 61-62, 2004.

12. V. Vibhute, D. Fitrio, J. Singh, A. Zayegh, A.Stojcevski, “A Tunable VCO for Multistandard Mobile Receiver,” *IEEE International Workshop on Electronic Design Test and Application (DELTA)*, 2003.

13. V. Vibhute, D. Fitrio, J. Singh, A. Zayegh, A.Stojcevski, “MEMS components for front end of Direct Conversion Receiver Architecture*,” SPIE’s International Symposium on Microelectronics, MEMS and Nanotechnology*, Vol. 5276, pp. 515-523, 2003.

Abstract

Device power dissipation has grown exponentially due to the rapid transistor technology scaling and increased circuit complexity. Motivated by the ultra low power requirements of emerging implantable and wearable biomedical devices, novel power management schemes are presented in this thesis to increase device run-time. The schemes involve several techniques suitable for ultra low power biomedical integrated circuit design.

This thesis presents a combination of two novel power reduction schemes to reduce the total device power comprising of dynamic and static power dissipation. One of the schemes used is the supply voltage (V_{dd}) scaling, also known as Dynamic Voltage Scaling (DVS). DVS is an effective scheme to reduce dynamic power ($P_{dynamic}$) dissipation. The DVS architecture primarily consists of a DC-DC power regulator which is customised to handle scaling variability of the V_{dd}. The implemented DVS can dynamically vary the V_{dd} from 300 mV to 1.2 V.

The second scheme presented in this thesis to reduce static power (P_{static}) dissipation is threshold voltage scaling. The variable threshold keeper technique is used to perform threshold voltage scaling, which comprises of a keeper transistor whose threshold voltage is scaled by a body bias generator. The use of the keeper transistor increases the device noise immunity.

This combination of supply and threshold voltage scaling techniques offers a further reduction in the overall device power dissipation and enhances reliability without degrading circuit speed. A power reduction of 23% to 31% is achievable with up to 90% efficiency. The thesis discusses the primary design challenges of ultra low power biomedical devices. System and circuit levels design techniques are described which help meeting the stringent requirements imposed by the biomedical environment. This thesis presents a new DVS architecture and investigates the effect of lowering the supply voltage combined with threshold voltage scaling on dynamic power dissipation using 0.13 μm ST-Microelectronic® 6-metal layer CMOS dual-process technology.

Chapter One:
Introduction

1.1 Background of This Research

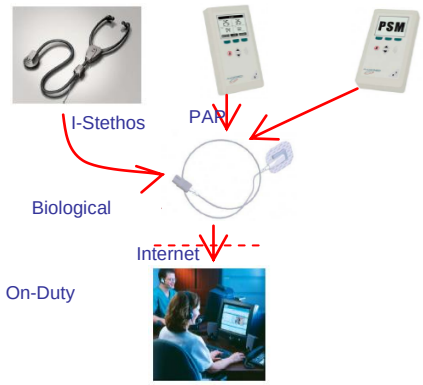
Australia, as the world's smallest continent, is located in the southern hemisphere of the world. Demographically, Australia comprises of 5% of the world's land area, at 7,692,024 km^2 of world's total 149, 450,000 km^2, and is the sixth largest country after Russia, Canada, China, USA, and Brazil. However, Australia is 30 times smaller in population when compared with Europe having a population density of just 2.5 people per km^2. The majority of Australia's population and cities are spread along the coastal areas [1]. As a consequence, primary infrastructure such as medical facilities are located in coastal areas [2]. The infrastructure overlay makes it difficult for people living in rural area to get medical attention.

Although, Australia is known to have adequate medical knowledge and technology, the number of hospitals and medical practitioners are not sufficient to satisfy all patients needs. The Australian government has tried to solve this problem by: increasing the number of hospitals and medical professionals, by making improvements to medical facilities, introduction of flying doctors for rural patients, and increasing research activity in medical fields. However, all of these developments have an impact on medical care cost. Australia needs a cheaper solution to this problem. Therefore, the Australian government have encouraged medical research activity in the field of biomedical engineering [3]. Biomedical Engineering is defined as the application of engineering principles to the field of biology and medical chemistry, as for example in the development of aids or replacements for defective of missing body organs which cause problems to human health. Engineering in this

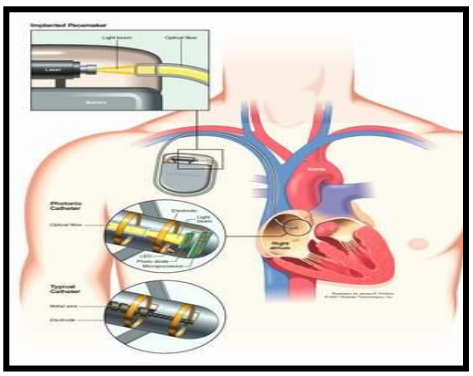
context is the application of scientific and mathematical principles to the design, manufacturing and operation of the practical devices.

One of the emerging fields in Australian engineering is Microelectronic engineering. Microelectronic engineering, particularly Complementary Metal Oxide Semiconductor (CMOS) integrated circuits, has shown its wide application in many key consumer products from computers, automobiles, consumer electronics and telecommunications equipment. Its wide use in our daily life, has enabled low production and material cost. The Australian government has recognised CMOS technology as the solution for the missing link in the medical field, and is encouraging researchers to investigate CMOS biomedical portable devices [4, 5].

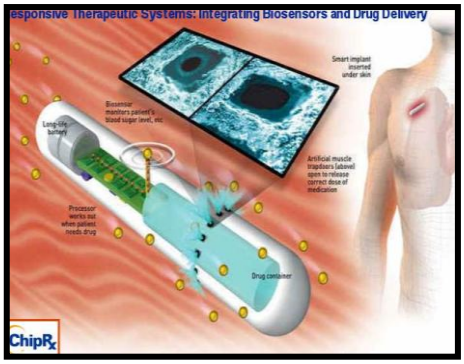
Some of the enhancements in biomedical technology due to CMOS implementation are shown in Figure 1.1. A Home tele-monitoring system as shown in Figure 1.1a; it is a personal home health monitoring system, which is capable of measuring heart rate, pulmonary arterial pressure and breathing regularity [6]. The collected measurements are then packaged and sent via an internet connection to the hospital and further diagnosed by medical professionals. The medical professionals would then directly provide, as appropriate, a prescription from the diagnosis or dispatch a medical team for a critical patient. This medical system would be very beneficial for patients residing in rural areas, and could potentially reduce general medical costs. Implantable medical devices have improved in size, function and comfortableness. Electrical pacemakers have replaced the mechanical pacemaker which was very bulky and introduced an unpleasant experience to recipients, as shown in Figure 1.1b) [7, 8]. Another example, shown in Figure 1.1c), is a Response Drug Delivery (RDD) system [9], which is implanted under the skin and is capable of detecting human's blood chemical inadequacy which then releases appropriate medication. The response drug delivery system, or Smart-drug, has proven to be very efficient for diabetes sufferers where constant medication is required. CMOS technology and Micro-Electro-Mechanical systems (MEMS) have resulted in an implantable CMOS retina sensor for sight impaired patients in Figure 1.1d) [10].



a) Home tele-monitoring



b) Electrical Pacemaker



c) Response drug delivery system

d) Implantable CMOS image sensors

Figure 1.1: Examples of Biomedical enhancements through CMOS technology.

1.2 Motivation

The motivation behind this research comes from the interest of the candidate in the area of pervasive computing healthcare technologies and wearable biomedical devices. Most of the applications proposed in these areas consist of a sensor, data collecting and communication infrastructure for data transfer.

A biomedical portable device primarily functions as a personal aid device. As the name ‘portable’ indicates, it needs to be small in dimensions, battery operated and preferably to have wireless capabilities for mobile use. The fact that the nature of usage is either attached to or implanted in the human’s body, requires the device to have very low power consumption in order to be efficient [7].

Very low power consumption is the primary criteria in biomedical devices and is the driving motivation for this research. This research involves the design of circuits that enable dynamic power management and dynamic leakage current management or schemes, combined with low power logic design techniques at processor logic core level, for CMOS biomedical devices.

1.3 Research Objectives and Aims

The objective of this research is to design and implement power management schemes that will minimise power usage for application in biomedical devices. The specific aims of this research are:

- To investigate CMOS transistor behaviour in the ultra low operating region for biomedical devices,
- To develop ultra low power logic techniques,
- To design and implement dynamic voltage supply (V_{dd}) scaling to reduce dynamic power dissipation,
- To design and implement dynamic threshold voltage (V_t) scaling to reduce static power dissipation, and
- To analyse the performance of the combined power management schemes on a Fast Fourier Transform processor core.

1.4 Research Design Methodologies and Techniques

The proposed research methodology and techniques to accomplish the afore mentioned aims are as follow:

- Investigate transistor behavior in the low operating region (subthreshold).

Since minimisation of power is the primary aim of this research, the starting point for ultra low power design is to investigate transistor behaviour and characteristics in the low operating region (subthreshold). An extensive literature review regarding the source of power dissipation has been undertaken prior to proceeding with the design step. The CMOS transistor's power dissipation characteristics, behaviour analysis and performance limitations in subthreshold region were investigated by applying different biasing techniques. The design and implementation was performed using Electronic Design Automation (EDA) tool sets from the Cadence Corporation.

- Develop and investigate low power logic techniques

Ultra low power logic techniques were developed to reduce power dissipation as well leakage current. The analysis of biasing techniques in the subthreshold region was used to develop ultra low power logic schemes. The first step was to investigate and combine several structures, power reduction techniques and range of power reduction values achievable. The most suitable structure combinations were chosen, developed and analysed for their use in the core design of biomedical applications. This step was repeated to develop a small component library using a combination of material parameters together with a range of values in the CMOS fabrication process. The designs and their implementation were performed using Electronic Design Automation (EDA) tool sets from the Cadence Corporation.

- Design and implementation of dynamic supply voltage scaling

A dynamic supply voltage (V_{dd}) scaling module makes use of a clock frequency signal from the processor block. The module scales the power supply up or down, based on the clock signal. In designing dynamic V_{dd} scaling, initially a virtual clock is given to the input and an observed stable analog voltage output must be maintained. Since the

dynamic V_{dd} scaling circuit controls the power supply of the whole core circuitry, careful attention must be given to the current driving capability of the design. The dynamic V_{dd} scaling was designed to respond at different frequencies and the performance was analysed. The selected design was optimised for performance in terms of minimizing power consumption and reducing physical area of the circuit.

- Design and implementation of dynamic threshold voltage scaling.

Designing a dynamic threshold voltage (V_t) scaling block is critical, as the leakage current is the main factor in static power consumption. Firstly, an appropriate transistor technology model library must be used. Secondly, the V_t scaling itself acts as a leakage current monitor (LCM) block, so preferably the same transistor technology model as the core logic is needed. The selected design was optimised for performance in terms of minimizing power consumption and reducing physical area of the circuit.

- Performance analysis of the dynamic power management scheme.

The performance of the power management chip was analysed with the respective FFT core logic, and compared in terms of reliability, speed, and power dissipation reduction.

1.5 Originality of the Thesis

In this dissertation the design and implementation of a low cost, low power, power management schemes for biomedical devices has been addressed. This research therefore represents a contribution of knowledge to integrated circuit power management in following key areas:

Power: Power reduction in dynamic and static power domains is the main topic in this thesis. Improved power management reduces the power dissipated in the biomedical device.

Performance: Bigger computation tasks require the processor to work harder, whilst smaller tasks do not require the processor to work at the same performance levels. The

performance of any particular device can now be varied according to the computation tasks, thereby improving the efficiency.

Weight: Portability of biomedical devices is one of the issues being addressed in this thesis. Improvement in transistor technology used for the development of biomedical devices reduces the physical size and weight of the device.

Functionality: Power management schemes allow a reduction in the power and heat generated by the device. As a result more functionality can be added onto the chip which reduces the risk of overheating.

Cost: A biomedical device designed using CMOS technology has the potential advantage of lower production costs.

1.6 Thesis Organisation

The Thesis is organised into 9 chapters. Chapter 2 introduces the literature review and the background of this research. Several approaches to low power design are reviewed. In Chapter 3, low-voltage CMOS implementations of the three basic switching regulator topologies - buck, boost, and buck-boost - are introduced. A mathematical model is developed to estimate the overall battery run-time enhancements that can be effected by DC-DC converters. The requirements imposed on these regulators by the portable environment are described. Design equations and closed-form expressions for losses are presented for both pulse-width and pulse-frequency modulation schemes. Alternative regulator topologies which may find use in ultra-low-power applications where voltage conversion or regulation is required are introduced. Chapter 4 and 5 discuss the design techniques of each module involved in DC-DC conversion technique and voltage scaling, respectively. Mathematical models and simulation results of the optimized modules are presented. Chapter 6 discusses the possibility of applying threshold scaling in conjunction with voltage supply scaling for better performance, while Chapter 7 discusses the implementation aspect of the designed threshold scaling scheme to reduce static power dissipation. Chapter 8 discusses the integration results and layout implementation of the schemes in a FFT system. Chapter 9 is a conclusion which include of discussion of possible further work.

1.7 Conclusion

This research dissertation is an exploration of transistor, circuit, architectural and system-level considerations of a power management chip for energy reduction. Many concepts described here are specifically targeted to Biomedical device applications or processor systems, where the key metric is energy-efficient computation and other traditional metrics such as clock frequency or performance, latency and device physical area may need to be traded in order to achieve energy efficiency.

Chapter Two:

Motivation and Defining Parameters

2.1 Home Care System

2.1.1 Introduction

The world's future demographic indicates two major phenomena, an aging population due to increased life expectancy, and Baby Boomers demographic peak. According to the U.S Bureau of Census statistic alone, life expectancy has significantly increased from 49 years in 1901 to 77.6 years in 2003, and the number of people aged 65 and older is expected to increase from 35 million to 70 million by 2025. This projects that the worldwide population of people aged 65 and over, will rise from 357 million in 1990 to nearly 761 million by 2025.

The demand for healthcare in Australia is escalating; patients and government continue to be frustrated by the long waiting lists due to lack of medical professionals or infrastructure [5, 11]. This is an ongoing problem despite significant injections of government funds into the health industry.

2.1.2 Medical monitoring Systems

For a long time, humans have dreamed of monitoring body functions and performing surgical procedures with tiny electronic systems. Monitoring body functionality has become a vital tool for medical diagnosis. For example, the conventional process of

repeated mandatory measurement of blood pressure at short intervals increases the stress level of patients and consequently may falsify the results.

The key enabling factor in the monitoring system is the personal wearable health monitoring system. Wearable health monitoring systems integrated into tele-medical systems enable early detection of abnormal health conditions and the prevention of serious consequences [12-15]. Patients benefit from continuous real time monitoring as part of the diagnostic process, optimal monitoring those with chronic conditions or during their recovery from post acute surgical treatment.

2.1.3 What is being Monitored?

In general, medical monitoring systems have been used for the following applications:

- Vital health signs monitoring is the main priority such as the patient's temperature, respiration, pulse, and blood pressure.
- Falling/Accident monitoring is another important detection for the elderly. This type of monitoring is essential as many elderly patients may suffer tremendously from a fall, which is caused by increasing instability due to age or other health conditions.
- Patients located at home, or at health care facility, need to be monitored for emergency events.
- Monitoring patients with cardiac disease, hypertension, diabetes, asthma, post stroke pain management, obesity, post surgical care and surveillance.

Traditionally, personal wearable medical monitoring systems have been implemented to collect data for offline processing. These systems incorporate multiple wired electrodes attached on a patient's body being connected to the monitoring system, which limit the patient's activity, mobility and level of comfort, thereby negatively influencing the measured results [16]. The development of the Personal Area Network (PAN) or Body Area Network (BAN) enables the possibility of integrating wearable health-monitoring devices into a patient's clothing [17]. However, the system is not

robust enough for lengthy, continuous monitoring during normal physical activity [18], intensive training or computer-assisted rehabilitation [19].

Recent technological breakthroughs in microelectronic fabrication [20], wireless networking [21] together with integration of physical sensors, processors and radio interfaces/protocol on a single chip, promise a new generation of wearable wireless sensors suitable for many applications [22]. New generation wearable wireless systems are the primary area of application in this research, where many optimisation techniques and issues need to be addressed.

2.1.4 Home Tele-care System

The evolvement of healthcare industry is triggered by advances in pervasive computing and Information and Communication Technologies (ICT), supported by technology advancement and miniaturisation of health care devices. The combination of these fields establishes potential for the development of a product which allows patients to have greater control of their personal health via delivery of health care at home (tele-care). This increasingly popular system architecture is applied for tele-care delivery by using pervasive computing at home. The key components in the architecture are: an intelligent health sensor, home healthcare servers, health care service providers (healthcare centres), telecommunication technology and devices, as depicted in Figure 2.1.

The figure shows the relationship between different technologies which not only need to be integrated together under strict health regulations and specifications, but also to maintain high quality delivery of service to patients.

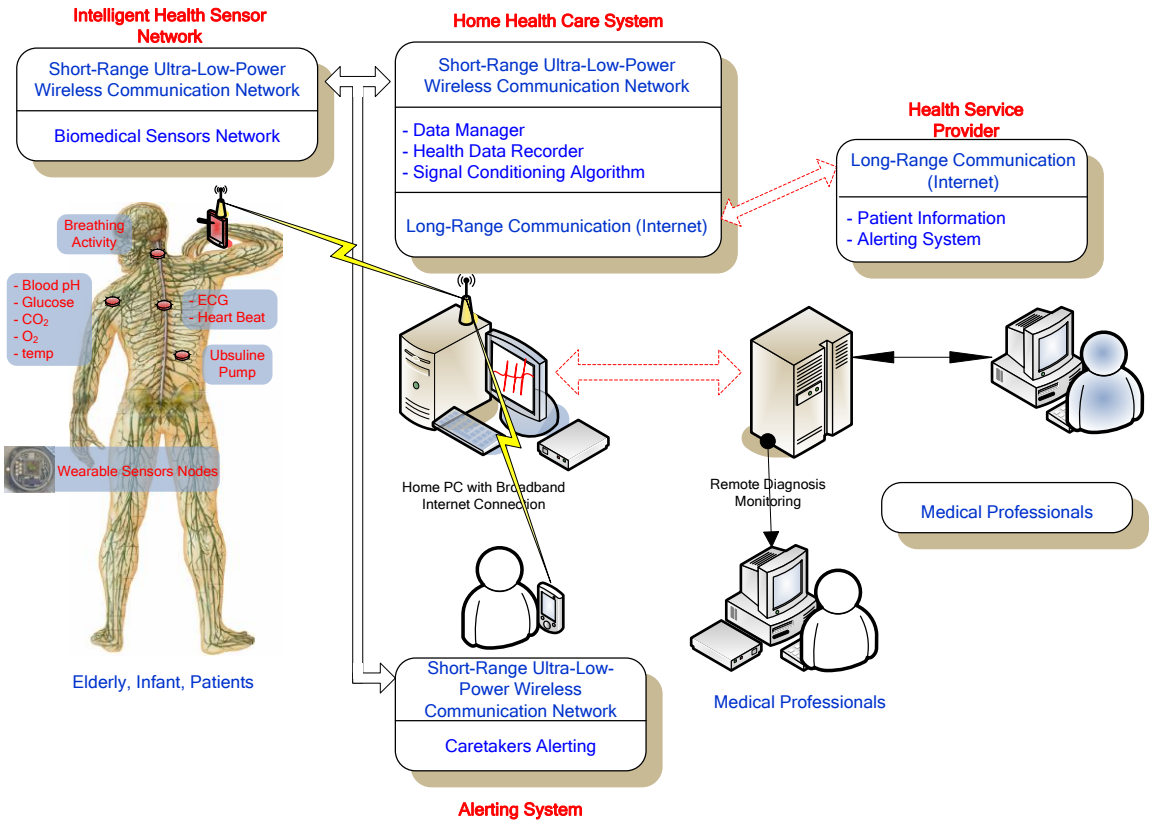


Figure 2.1: Home healthcare system showing a personal network attached to a patient body, together with its supporting system and connection to a health service provider.

2.1.5 Essential Home Health Care System Building Blocks

2.1.5.1 Health Sensory and Personal Server

A Wireless Body Area Network (WBAN) consists of a number of health sensors, which are combined to obtain the required patient information. Examples of such health sensors may include the following:

- Sensors for electrocardiogram, monitoring heart activity
- Sensors for electromyography, monitoring muscle activity
- Sensors for electroencephalography, monitoring brain electrical activity
- Blood pressure sensor
- Tilt sensor, monitoring trunk position

- Breathing sensor
- Movement sensors for analysing patient's activity

These sensors generate analog signals, which are continuously sampled, processed and delivered via a wireless network for further computation or storage. Furthermore, the health sensors are interfaced to a pre-processing/sampling module, whose task is to provide on-sensor processing capability and wireless communication protocols, so a single wireless network can be shared by multiple health sensor nodes. These wireless sensor nodes can be implemented as tiny external patches or embedded into the patient's attire. Therefore, these wireless sensor nodes should have minimal weight, size and power dissipation to prolong the continuous monitoring operation of the system. The current wireless sensor node continuously collects and processes a patient's body information, store them locally, and send them to the personal server. However, the sensor node should be able to vary the sampling, processing, transmitting capability according to the nature of the healthcare application in order to significantly reduce power consumption, thus extending battery life.

The information collected by the sensor node is further processed by the personal server. The personal server's other tasks are to synchronise and configure the WBAN nodes, monitor functionality of the nodes, and to act as the communication gateway to a remote healthcare provider.

2.1.5.2 Telecommunications

There are two types of telecommunication networks required in a wireless homecare system, an external and an internal network. The external network is responsible for transmitting the processed health information of the patient from home to the health care provider. In general, the current telecommunication technology available for home tele-care systems include, public switched telephone networks, Integrated Services Digital Network (ISDN), satellite, wireless networks, leased line, cable and Asymmetric Digital Subscriber Line (ADSL). Currently in Australia, ADSL and cable, which are marketed as broadband connection, are the most viable options for a home

tele-care system. In remote areas where broadband connection is not available, satellite connection can be used.

The internal network enables intercommunication between the connected wireless nodes and the personal server. The existing telemetric devices use wireless communication channels exclusively to transfer data from the sensors to the monitoring station (personal server). They either transmit raw data or use more advanced protocols such as Bluetooth® that are too complex, power demanding and prone to interference by other devices operating in the same frequency range. These characteristics limit the prolonged use of the wireless wearable health device in terms of battery life [23, 24].

2.1.5.3 Medical Service Providers

The healthcare provider collects data from individual patients, integrates the data into patient's medical record, processes them, and if necessary gives advice to the patients. If the received patient's health information indicates an imminent medical situation an emergency service can be notified. Storing patient's medical history in electronic medical form for future analysis must also be made available by the healthcare providers. Security and privacy of data is a significant issue in this area.

2.1.5.4 System Design Issues

A home tele-care system integrates various aspects of technology with physical behavioural patterns which creates an inherently complex system. As WBAN and sensor nodes are the heart of the system, it is very important to analyse the technical aspects required and issues that might arise in the system design.

The main system design issues to enable the collection and delivery of patient's data in the system are:

- Advanced telecommunications, to ensure rapid and secure transmission of medical information

- Very low power radio frequency (RF) schemes
- Very low power data acquisition or personal health monitoring sensor network.
- Advanced or alternative power supply/source for the system
- Miniaturisation

Currently technology advances in Integrated Circuits (IC) allow designers to develop systems with low power and small system size, which fit well with the demands of wireless sensor networks. Recent developments in low power sensor communication networks, such as Zigbee®, have improved the bandwidth and data rate performance for sensor node networks.

Like other mobile devices, mobile biomedical devices use a portable battery. Although there are other sources of energy, they are expensive and unsuitable for commercial purpose, thus batteries are still the most economical, widely available and safest energy source. However, the progress in improving battery life and size has been relatively slow and the most popular type of battery currently used, Lithium-Ion battery, has limited battery performance and life due to degradation of energy storing capability after repetitive charging. The characteristics of commonly used batteries are shown in Table 1. An in depth look of the power – physical size characteristics of different battery types from Table 1.1, suggests that there is no major improvements in battery technology. Therefore, there is a need for alternative ways to reduce power dissipation in a semiconductor system to extend battery life.

Table.1.1: Performance characteristics of commonly used batteries

Battery Type	**Nominal Cell Supply Voltage** (V)	**Energy / Weight** (MJ/kg)	**Energy/ Size** (Wh/L)	**Power/weight** (W/kg)
Wet Lead-Acid	2.1 - 2.2	0.11-0.14	60-75	180
Nickel-Iron	1.2	0.18	175	100
Nickel-Cadmium	1.2	0.14-0.22	50-150	150
Nickel Metal Hydride	1.2	0.11-0.29	140-300	250-1000
Lithium Ion	3.6	0.58	270	1800

2.2 Conclusion

Home tele-care systems are health care systems, whose implementation is focused at the patient's home. The system involves continuous monitoring of the patient's health data via wearable sensor devices. These data are then sent to a medical facility via an existing telecommunication channel. The system also has the capability for the patient to have a face to face video conferencing facility with a medical professional, which will help in reducing health-care response time. The major benefits of home tele-care systems particularly for the remote areas are better access to healthcare, improved communication, reduce healthcare cost, reduce waiting time, and increased healthcare standards. The home tele-care systems involves the use of many key technologies, such as pervasive computing, telecommunications, internet and networking, semiconductors, smart medical sensors, and electronic health recording. The primary focus of this dissertation is power reduction in portable and battery operated biomedical sensor devices.

Chapter Three:
Source of Power Dissipations

3.1 Introduction

Power dissipation in CMOS devices has grown exponentially due to the fast technology scaling and the increase in complexity. Power dissipation has become a major concern in CMOS devices, primarily for battery operated portable systems where energy consumption is heavily constrained. A portable system with a microprocessor generally has a power management scheduling inside the kernel, which is responsible for adjusting clock frequency and operating the voltage in a low power sleep mode. Some of the recently introduced microprocessors, such as the StrongARM® processor, support external dynamic voltage scaling (DVS) and internal operation frequency scheduling [25]. Typically in a dynamic voltage scaling processor based system, supply voltage and the clock frequency can be dynamically varied according to the required throughput so as to significantly extend the battery life. Therefore it is important to understand the sources of power dissipation in CMOS circuits, in order to optimise the design for low power consumption.

Fundamentally, the two main sources of power dissipation in CMOS circuits are dynamic and static power dissipation. The total power dissipation is the accumulation of dynamic and static power dissipation, as shown in Equation 3.1 [26].

$$P = \underbrace{\frac{1}{2} \cdot C \cdot V_{dd}^2 \cdot f \cdot N + Q_{SC} \cdot V_{dd} \cdot f \cdot f_{0\to1}}_{P_{dynamic}} + \underbrace{I_{leak} \cdot V_{dd} + I_{static} \cdot V_{dd}}_{P_{static}} \qquad \text{Eq. 3.1}$$

Where,

P = total power

C = circuit capacitance

V_{dd} = supply voltage

f = clock frequency

N = switching gate transition/cycle ($F_{0\to1}, F_{1\to0}$)

Q_{sc} = short circuit charge quantity

I_{leak} = leakage current

I_{static} = static current

Dynamic power dissipation ($P_{dynamic}$) is more dominant in the majority of digital CMOS applications. However, CMOS transistor is progressing towards submicron sizes and static power dissipation is becoming more dominant. In order to calculate the total power dissipations, both types of power dissipations must be considered. The $P_{dynamic}$, due to its nature, has a direct relationship between the switching frequency and the supply voltage (V_{dd}).

$$P_{dynamic} = f_{0\to1}.f_{clk}.V_{dd}^{2}.C_L \qquad \text{Eq. 3.2}$$

where, $f_{0\to1}$ is the half switching frequency, f_{clk} is the clock frequency and C_L is the capacitance on a node.

As seen in Equation 3.2, dynamic power dissipation can be effectively reduced by lowering V_{dd} due to its quadratic dependence. However, an effective V_{dd} reduction could be achieved together with reduction in total load capacitance, which means smaller transistor size. Clock frequency depends on the target device application. A higher clock frequency is still preferable for processor based devices.

Short circuit charge (Q_{sc}) is another element in dynamic power dissipation which can not be neglected, as seen from Equation 3.1. This thesis refers to Q_{sc} rather than short circuit current, due to the fact that there are two components involved in CMOS short circuit. A general understanding of short circuit current is when a direct path from the power supply to ground is established, due to the transistor leaving the cut-off region

into saturation and vice-versa. However, the reverse charge to the gate to drain coupling capacitance also has an influence in the total short circuit power. Therefore, it is more accurate to represent the total short circuit power in terms of Q_{sc}.

The second part of the total power dissipation shown in Equation 3.1 is derived from the total static power equation (P_{static}). P_{static} is formed of two components, the more dominant subthreshold leakage power, due to the small subthreshold leakage current (I_{leak}) flowing between the source and drain, and the static leakage power, from reverse bias pn-junction leakage current (I_{static}) between the source/drain and substrate, or commonly known as the substrate leakage current.
The detailed subthreshold leakage current, which is known to have an exponential characteristic, can be expressed as,

$$P_{static} = V_{dd} \cdot I_{subthreshold} \cdot e^{\frac{(V_{gs} - V_t)}{nV_{TH}}} \qquad \text{Eq. 3.3}$$

where n is the process parameter, V_{gs} is the gate to source voltage, V_t is the threshold voltage and V_{TH} is the thermal voltage at room temperature [27].

The exponential increase of subthreshold leakage drain current with decreasing V_t for a given V_{gs} may be understood from Equation 3.3. In other words, a transistor with a higher threshold voltage has a lower leakage current. However, one must be careful in choosing V_t as a slight increase in threshold voltage means a larger delay [26]. Another important factor is to use a transistor with a steep slope characteristic or transfer characteristic. The slope is measured by plotting of the drain current in semi-logarithmic scale against V_{gs}, which is linear in the subthreshold region. The larger the slope means the closer the transistor's behaviour is to an ideal switch.

As CMOS technology transistors scale down to provide a smaller surface dimension and better performance, subthreshold leakage current grows exponentially and consequently has become an increasingly large component in total power dissipation. Scaling down the transistor size has added a further 60% to the clock frequency and has brought about a reduction in the delay within a certain die area. However, the

growing complexity of the system has also increased the energy consumption, power dissipation and power requirements. A discussion of various commonly used voltage scaling techniques, having the purpose of reducing the dynamic power dissipation, is presented in Section 3.2. In Section 3.3, a brief review of the Metal Oxide Semiconductor (MOS) transistor modelling is presented; the leakage current is analysed in Section 3.4.

3.2 Dynamic Power Reduction through Voltage Scaling

As has already been observed from Equation 3.2, that a reduction of the power supply voltage, V_{dd}, yields a quadratic saving in energy dissipation per computational event. However, there is a drawback of reduction in computational throughput, since the propagation delay of a digital CMOS gate increases with decreasing V_{dd}. There is a fundamental trade-off between energy consumed and the switching speed, as depicted in Figure 3.1.

Carrier velocity saturation, in a short channel MOS device under a high electric field produces a reduction in current drive. However, at a sufficiently high voltage there is little delay, which provides potential for power reduction from supply voltage scaling.

In Figure 3.1, as V_{dd} approaches the MOS device threshold voltage (below 1 V), there is a large amount of circuit delay with insignificant energy saving. Therefore, the shaded region in Figure 3.1 is the optimum area where performance and energy consumption is readily traded for voltage scaling application. Two of the most appropriate techniques of voltage supply scaling are presented below.

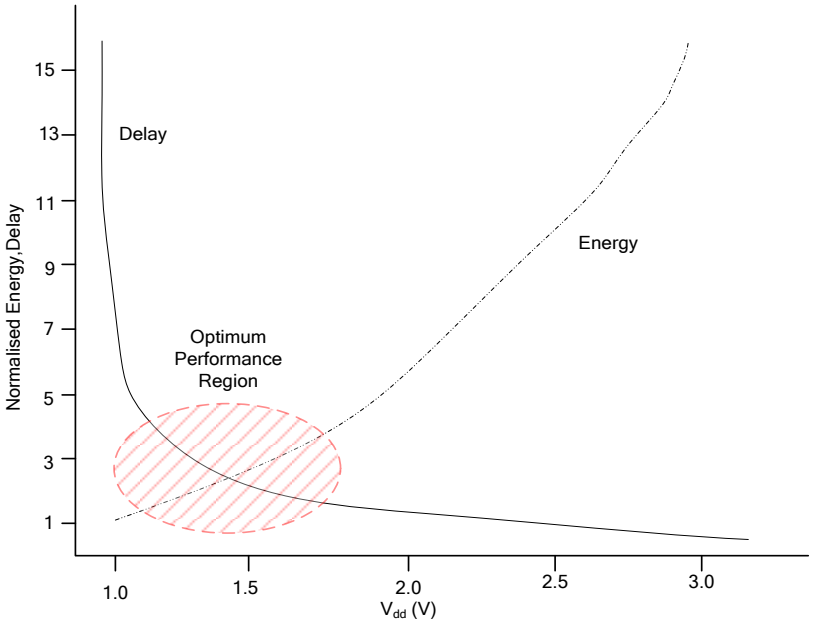


Figure 3.1: Energy and Propagation Delay Trade-off for a 0.13 μm CMOS, the energy dissipated is shown as a dashed line, whilst the delay is shown by the solid line.

3.2.1 Multiple Supply Voltage Scaling

The multiple supply voltage Scaling technique, often called clustered voltage scaling, is illustrated in Figure 3.2 [28]. This technique has been demonstrated to achieve power reduction without sacrificing computational throughput. The circuit with the longest delay, or critical path of the chip, is separated from the other circuits, and a higher supply voltage, V_{ddH}, is applied to the critical path to obtain a faster performing circuitry. A reduced supply voltage, V_{ddL}, is applied to non critical path circuits [29-32]. Since the output of the circuit outside the critical path has a lower voltage swing, a level converter is required to bring the output swing back to V_{ddH}. The limitation of this approach, from an energy usage perspective is that the level converter will contribute to the total power dissipation and usually the number of level converters increases for a large system.

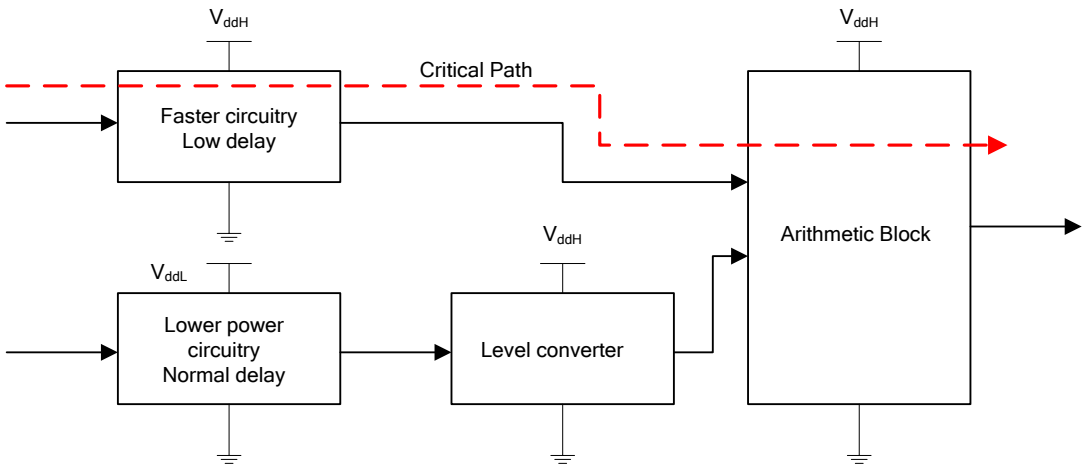


Figure 3.2: Illustration of Multiple Supply Voltage Scaling. Two supply voltages are provided being V_{ddH} (high) and V_{ddL} (low).The optimised critical path of the circuit is shown by the red dashed line.

3.2.2 Architectural Voltage Scaling

There are two techniques commonly used in architectural voltage scaling: parallel and pipeline. In the parallel technique some hardware blocks are duplicated to reduce the clock frequency of each block so as to compensate for computational throughput loss. This approach allows supply voltage to be scaled and results in a power reduction.

Consider a simple datapath circuit such as that shown in Figure 3.3, the datapath circuit block has three input vectors, A, B, and C [33]. The input vectors are latched into the datapath with the same clock frequency, f_{clk}. As the maximum clock frequency is determined by the propagation delay of the adder and the comparator block, the output throughput of (A+B) > C is generated based on the clock frequency of f_{clk}. At this clock frequency, the circuit dissipates power based on the switching of the adder, comparator, and the three latches.

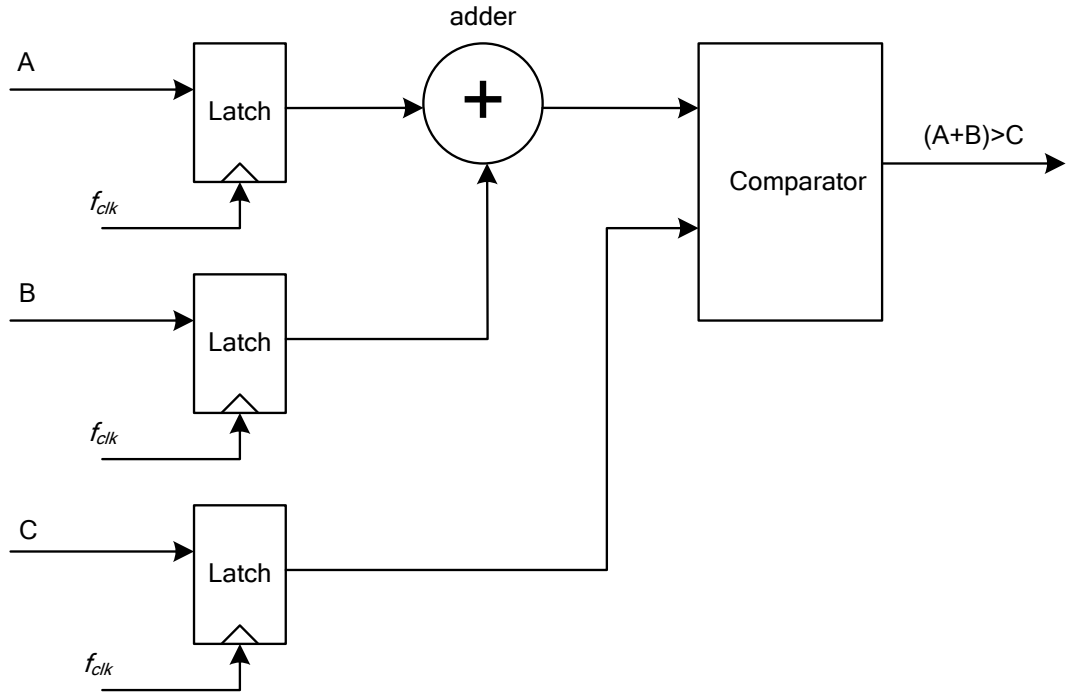


Figure 3.3: A Simple Datapath Block Diagram.

If architectural parallelisation is implemented in the datapath, the entire structure is duplicated and as a result the clock frequency can be reduced to half, $f_{clk/2}$, as shown in Figure 3.4. The parallelisation enables the clock frequency to be reduced as well as the power supply, thus the power dissipation will be redued. However, this approach increases the chip area due to the additional latches, adder, comparator and a multiplexer. As consequence it does add some additional overhead power.

Another technique of voltage scaling is pipelining the datapath, as depicted in Figure 3.5. In this technique the circuit operates at the maximum clock frequency, f_{clk}, which is set to be the maximum delay of either the adder or the comparator. However, the main disadvantage of architectural voltage scaling is the additional power introduced by duplicated hardware. As a result more leakage current is introduced.

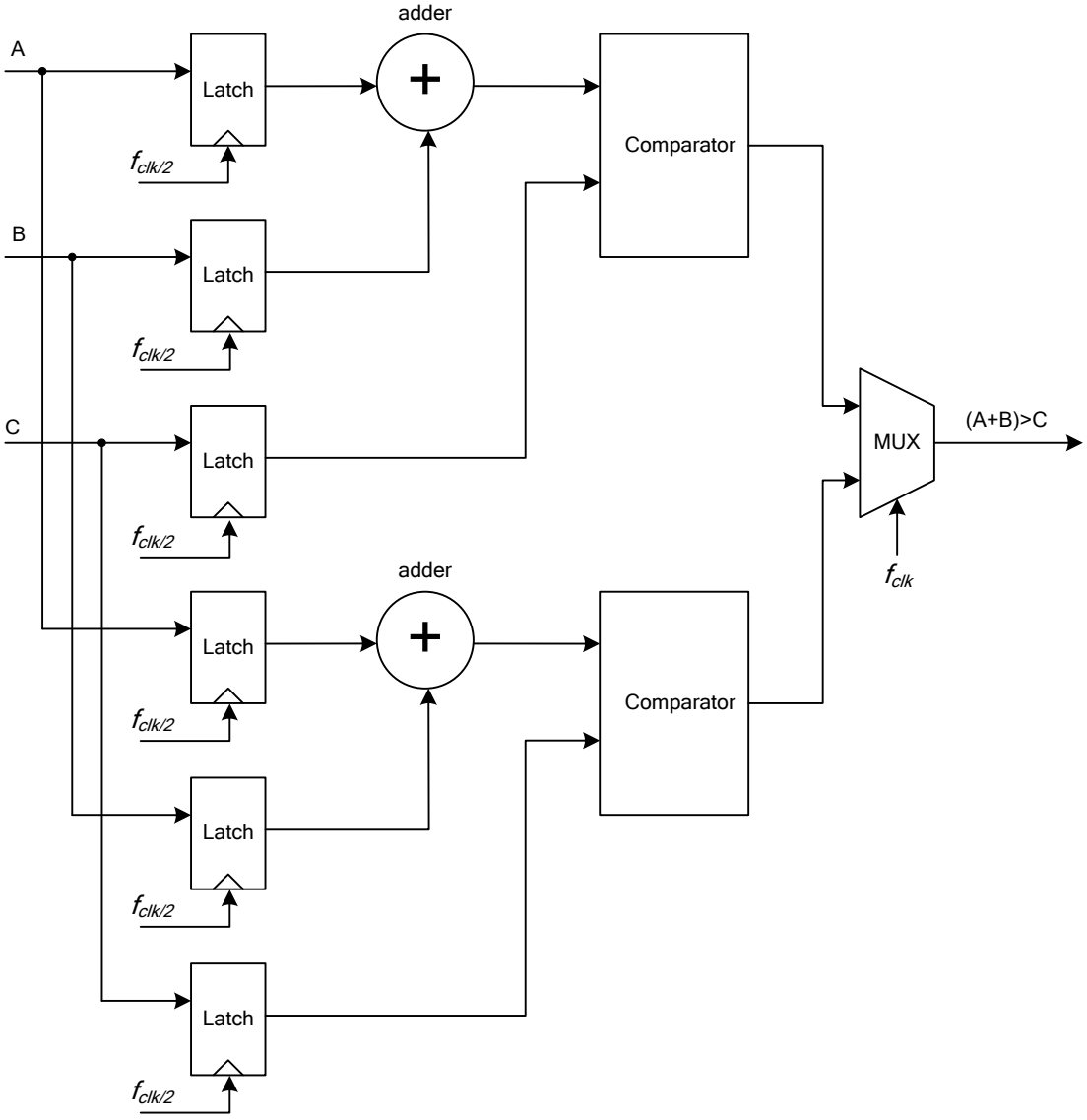


Figure 3.4: Parallel Architecture Implementation of the Datapath.

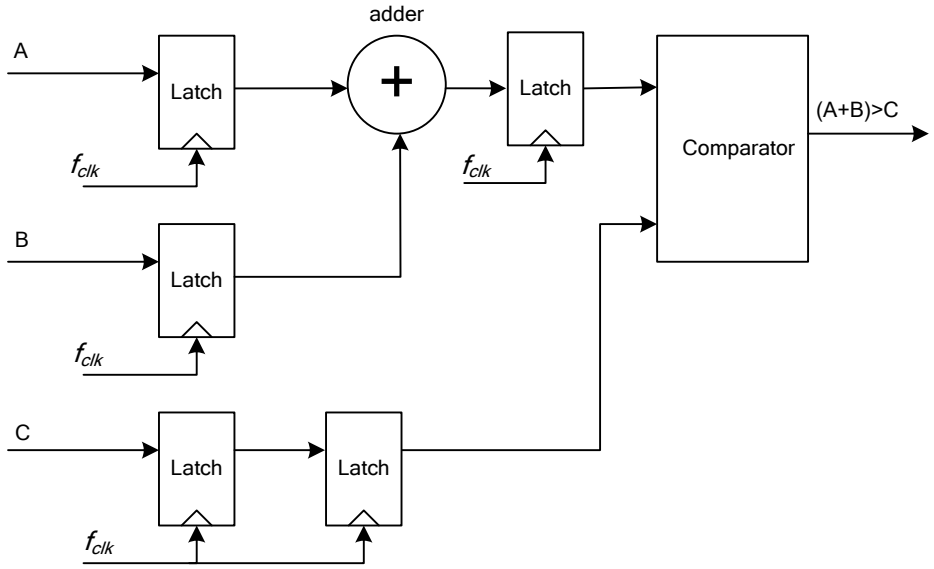


Figure 3.5: Pipelined Architecture Implementation of the datapath

3.3 MOS Drain Current Modelling

Previously, subthreshold leakage current had been a negligible component of the total power consumption. However, as the size of a MOS transistor continues to scale deep into the sub-micron, the subthreshold leakage current has become a major component of the total power dissipation and can no longer be ignored for low power design. Therefore, accurate MOS transistor drain current modelling is required to predict the leakage current in subthreshold region. There have been a number of models developed for transistors operating in the subthreshold region. The key parameters in modelling are the threshold voltage, and the pre-exponential constant, I_O. The general model equations describing the drain current above threshold are:

$$I_{ds} = \begin{cases} S\beta\left[\left(V_{gs} - V_t\right)V_{ds} - \dfrac{{V_{ds}}^2}{2}\right], \text{ linear region} \\ \dfrac{S\beta}{2}\left[\left(V_{gs} - V_t\right)^2\left(1 + \lambda V_{ds}\right)\right], \text{strong inversion region} \end{cases} \qquad \text{Eq. 3.4}$$

where *S* is the channel width to length ratio (W/L), $\beta = \mu\varepsilon / t_{ox}$ ($\mu\varepsilon$ is the carrier mobility in the permittivity of the gate insulator and t_{ox} is the thickness of the gate insulator),

and V_{ds} is the drain to source voltage, λ is the linear channel length modulation factor. In the subthreshold region, the drain current has an exponential characteristic, which is described as:

$$I_{ds} = I_0 \left(\frac{kT}{q} \right)^2 e^{\frac{-q\kappa V_g}{kT}} \left(e^{\frac{qV_s}{kT}} - e^{\frac{qV_d}{kT}} \right) + g_d V_{ds} \qquad \text{Eq. 3.5}$$

where I_o is the pre-exponential constant, κ is the transistor body effect, k is Boltzmann's constant, q is the electron charge and g_d is the subthreshold coefficient for the channel length modulation effect. The difficulty is in deriving the continuous relationship of the different coefficient of channel length modulation factor in the square law regions (linear and strong inversion), λ, and the exponential subthreshold region, g_d. The early drain current approximation above shows a discontinuity of current changing from the subthreshold region into linear-strong region. Since representation of I_{ds} as described in Equation 3.5, other researchers have derived improved approximation for subthreshold drain current. However, the approximation is still derived from the strong region counterpart [34].

Some of the MOS transistor models have been unofficially adopted as industry standard, such as the BSIM family. Berkeley Short-Channel IGFET Model, known as BSIM, is a model approximation based on the device physics of small geometry MOS [35]. It is an advanced empirical model and normally referred to as level 4 transistors. There have been 4 different BSIM generations. The first generation, BSIM1, tried to solve the discontinuity of the drain current expression by summing the current obtained in both regions. The approximation leads to a constant current offset in the strong inversion region. The offset current introduces a significant error in simulation when the MOS operates under low current. BSIM2, realised that the threshold voltage effect in BSIM1 is a technology dependent parameter, which varies between processes and also as a function of the device dimensions. The third successor BSIM3 is the first model that fully eliminates the discontinuity in the approximation of IV (Current-Voltage) and CV (Capacitance-Voltage) characteristics by deriving a single representation for device characteristics such as current across all operation regions. The BSIM3V3.2 has demonstrated an accurate approximation of 0.18 μm MOS

transistors. The most recent model of MOS transistors, BSIM4, was introduced in year 2000. It has made improvements compared to BSIM3 in terms of the IV approximation, noise and parasitic modelling. Other than the BSIM family models, there are several other models of industry standard transistors, such as MOS model 9 from Phillips Semiconductor®, which is derived from BSIM1 transistors. A summary of the evolution of MOS transistor models can be seen in Figure 3.6.

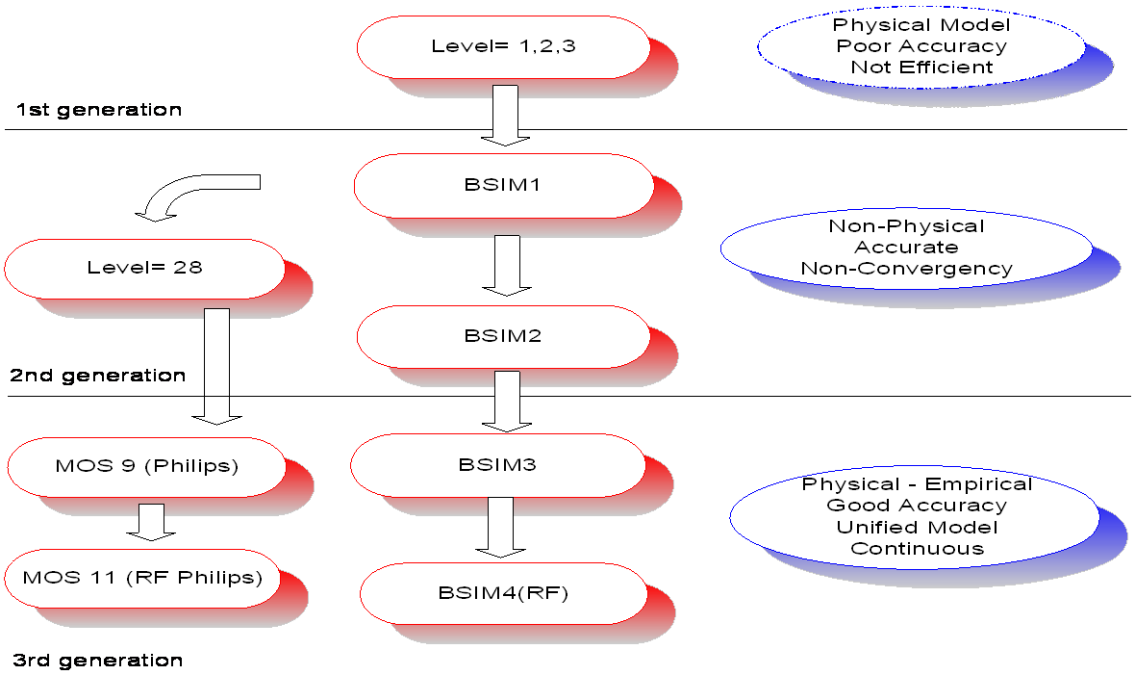


Figure 3.6: Evolution of MOS transistor models.

The designs in Section 3.4 were simulated by using 0.18 μm TSMC transistors with BSIM3V3 models. Figure 3.7, shows the simulation results of the basic characteristics of the BSIM3V3 model which was analysed due to its suitability for use in the research project.

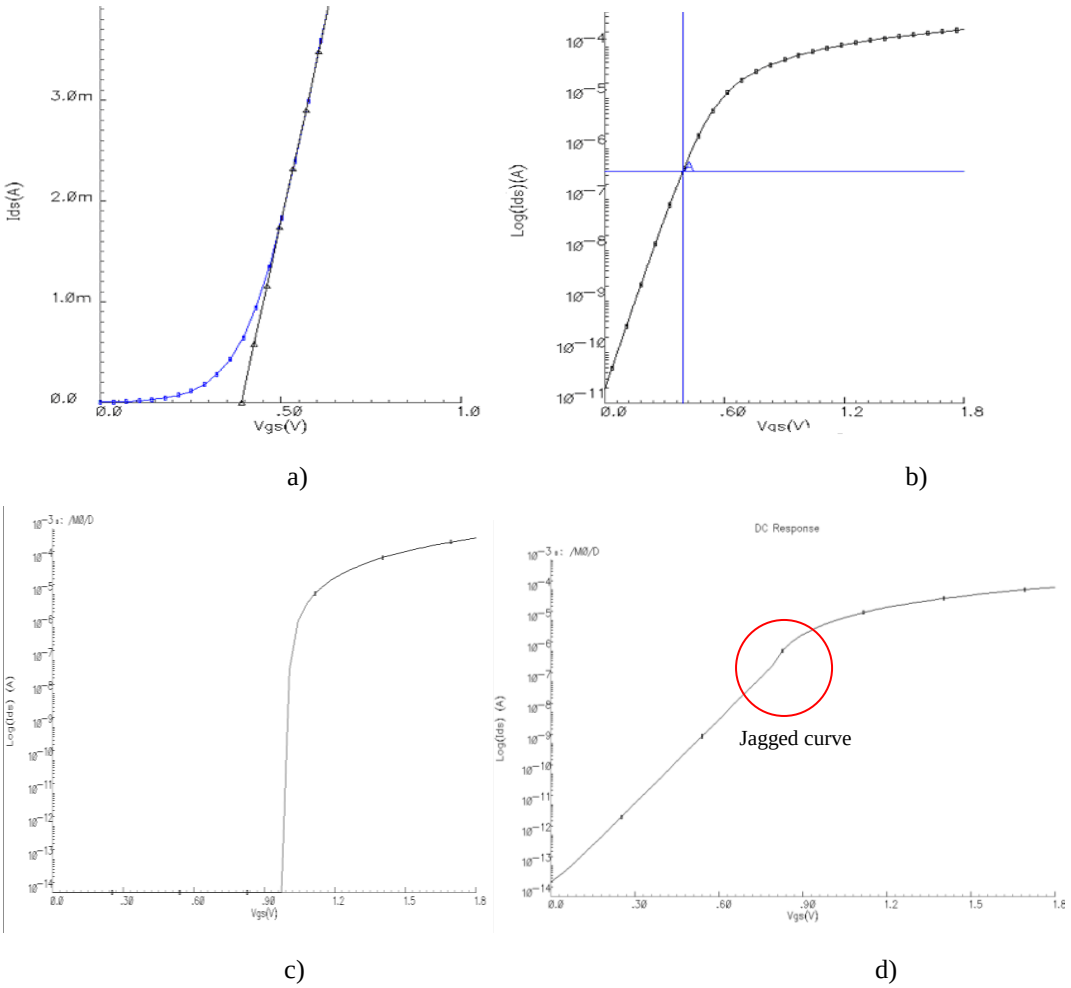


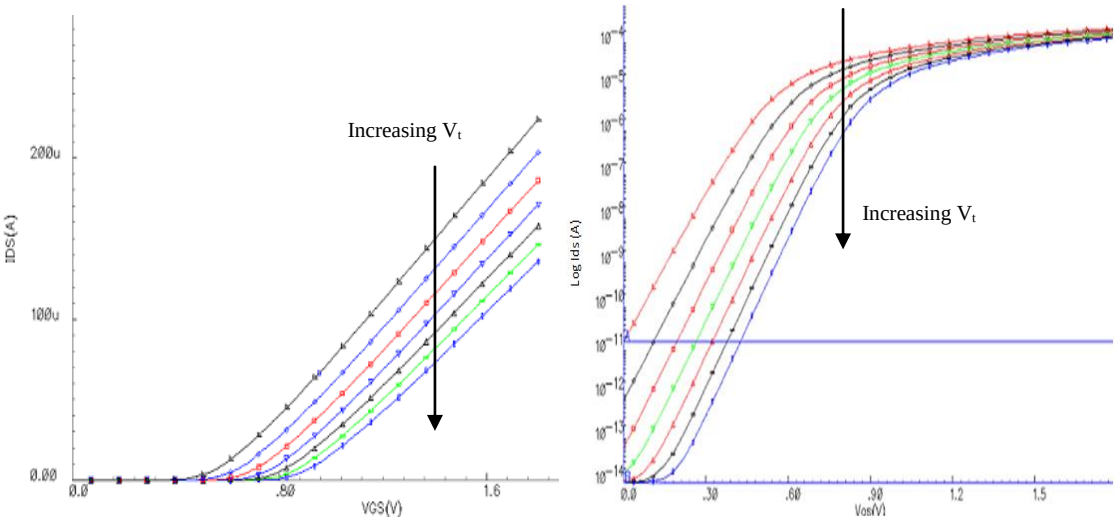
Figure 3.7: a) Threshold Voltage Plot, b) Smooth transitional of Log (I_{ds}) current for BSIM3, c) Subthreshold leakage current unavailability for Level-1 MOS, d) Rough transitions in Level-3 MOS

Figure 3.7a and b, show a threshold plot of a transistor and a smooth transitional curve of Log (I_{ds}) current between weak inversion and strong inversion for the BSIM3V3 transistor model, respectively. The simulation result shown in Figure 3.7b, is compared with an older transistor model simulation shown in Figure 3.7c and 3.7d. Figure 3.7c was simulated using a Level-1 transistor model, where there was no subthreshold leakage current derivation for the model. Figure 3.7d on other hand, is taken from a Level-3 transistor model, which has a drain current derivation in subthreshold region, however with discontinuity as shown as the rough line seen in the curve. The simulations were taken by finding the appropriate threshold voltage for a particular transistor. The IV curve was then plotted in the logarithmic scale, to check for any discontinuity in the weak/strong transitional region.

3.4 Effects on Leakage Current

Subthreshold leakage current occurs during both active and standby periods. Standby leakage current occurs when circuits are in idle mode where no circuit activity takes place. It is recommended to switch off the leakage current when performance is not required, however it is not always possible to shut off the leakage current completely during this period. In general, subthreshold leakage current is exponentially dependent on temperature, process variations and the threshold voltage (V_t).

Figure 3.8a shows how a change in the bulk/substrate source voltage (V_{bs}) will vary the threshold voltage of the device. As the substrate voltage increases, so does the threshold voltage. However, the device leakage current during standby mode is not clearly represented in this plot. Plotting the drain source current (I_{ds}) using logarithmic scale will reveal its true characteristics, as shown in Figure 3.8b.



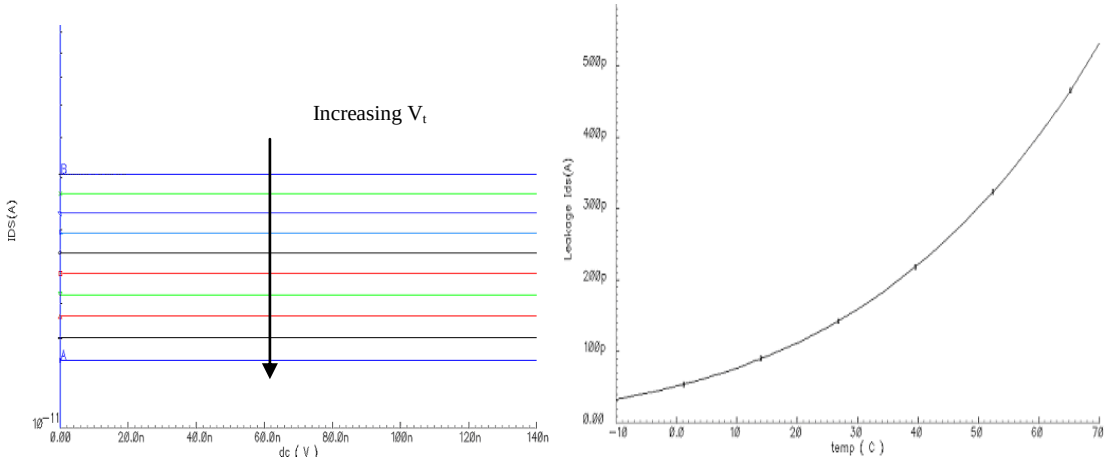
a) b)

Figure 3.8: a) Effects of substrate voltage variation on threshold voltage (V_t), b) Log (I_{ds}), leakage current plot of Figure a).

As the threshold voltage increases, the leakage current reduces from tens of pico-amperes (pA) to a few femto-amperes (fA). This demonstrates the exponential dependency of drain current on threshold voltage. The plots in Figure 3.9 show that a

variation of 3 volts in V_{bs} will indirectly vary V_t, which in turn will affect leakage current by tens of pico amperes, which result in a difference in current of almost a thousand times compared to leakage current in normal working temperature of 27°C.

Temperature is known to have impact on all aspects of MOS devices. Process parameters and adjustment of the component's layout location in the wafer can control temperature effects. As seen on Figure 3.9b, variation of the temperature from –10°C to 50°C will increase leakage current from 30 pA to 300 pA, a gradient of 0.438 pA/° C.



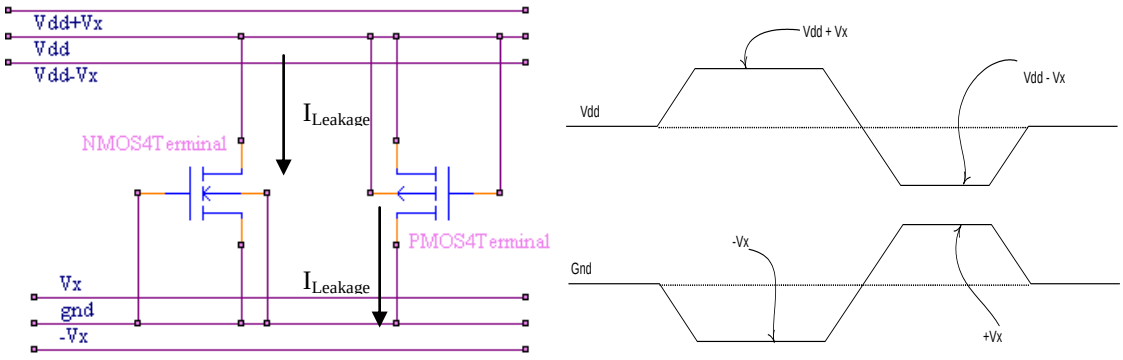
a) b)

Figure 3.9: a) I_{ds} current in cut-off region from Figure 3.8 a) enlarged in view, b) I_{ds} Leakage versus Temperature.

3.4.1 Effective higher threshold voltage biasing schemes to reduce leakage current

Subthreshold leakage current depends on threshold voltage; therefore transistors with accurate models of subthreshold leakage current must be used for low power design. Principally, as the MOS transistor goes into the deep submicron, the transistor's gate begins to loose control over the drain current [36]. This behaviour is due to the barrier effects induced as the channel length becomes shorter. Unlike gate leakage, which can be solved by using high-k material as the channel, subthreshold leakage cannot be

solved entirely by MOS structures nor by introducing new material. One of the feasible solutions is the combine use of Low- V_t transistors for its high-speed capability and High- V_t transistors for smaller leakage current, but with a drawback being that more delay results in slower transistors. Figure 3.10a, shows normal 4 terminal MOS transistors connection with the direction of the subthreshold leakage current drawn with an arrow flowing from the drain to substrate for N-type and substrate to drain for P-type MOS. Three power rails and ground rails were prepared for different levels of biasing in the simulation. V_x and $-V_x$ are offset voltages weighted in the positive and negative direction, respectively. The three voltage levels can be clearly distinguished in Figure 3.10b.



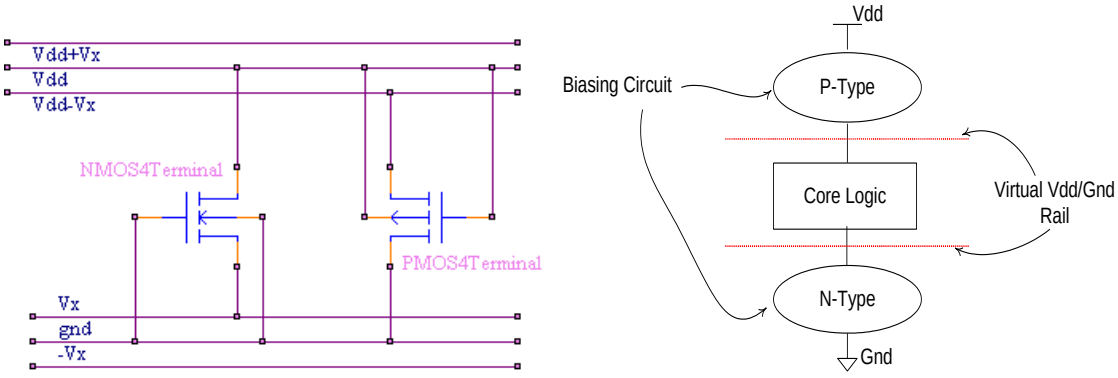
a) b)

Figure 3.10: a) MOS under normal biasing scheme, b) Voltage control level of the biasing scheme

3.4.2 Source voltage reverse biasing scheme

The source voltage, V_s, reverse biasing scheme [37] is obtained by keeping the gate voltage fixed over a controlled source voltage, as shown in Figure 3.11a. The configuration requires the MOS device under biasing to act as a MOS power switch, working as a source impedance turning on and off the core logic circuitry during active and standby mode respectively [38]. The advantage of this type of biasing is that the High- V_t device can be stacked between V_{dd} to core logic and/or core logic to *gnd* level to reduce the subthreshold leakage current, lowering the device P_{static} without sacrificing speed. As shown on Figure 3.11b, actual implementation of this scheme

does not require an additional power or ground rail, as the stacking effect of the transistors automatically provide a reverse biasing resulting in a lower V_{dd} level (V_{dd} - V_x) for the core logic. In other words, the current inside the block is effectively reduced. The effect of this biasing scheme is normally combined with V_{ds} reduction technique, resulting in even lower subthreshold leakage current flow.

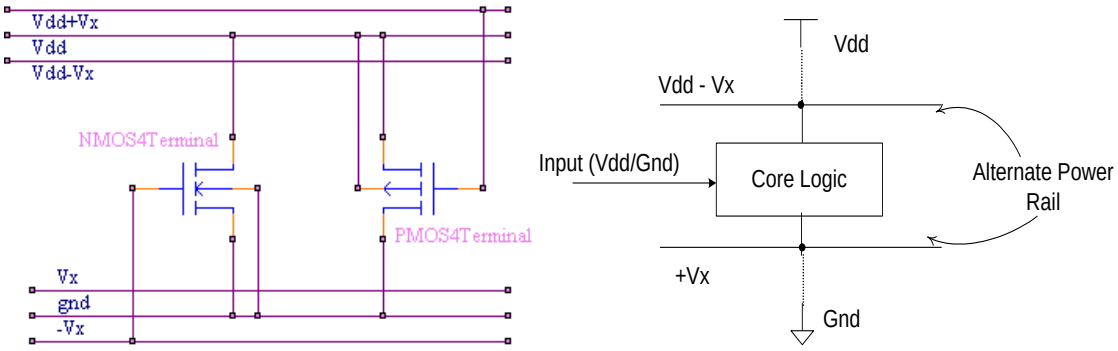


a) b)

Figure 3.11: a) MOS under V_s reverse biasing scheme, b) Circuit implementation.

3.4.3 Gate voltage reverse biasing scheme

Another type of biasing scheme is to reverse bias [39-41] the gate voltage, V_g, by applying a higher gate offset voltage, as shown in Figure 3.12a. Implementation of this type of biasing circuit will result in a reduction of the overall output swing to V_{dd} - V_x and V_x, due to the alternate power rail, as shown in Figure 3.12b. However, a problem may arise in driving the next cascaded logic cells, as the required output swing must be smaller than the input gate level. Therefore, this type of biasing is very useful for reducing leakage current in the bus driver with low logic swings [42].

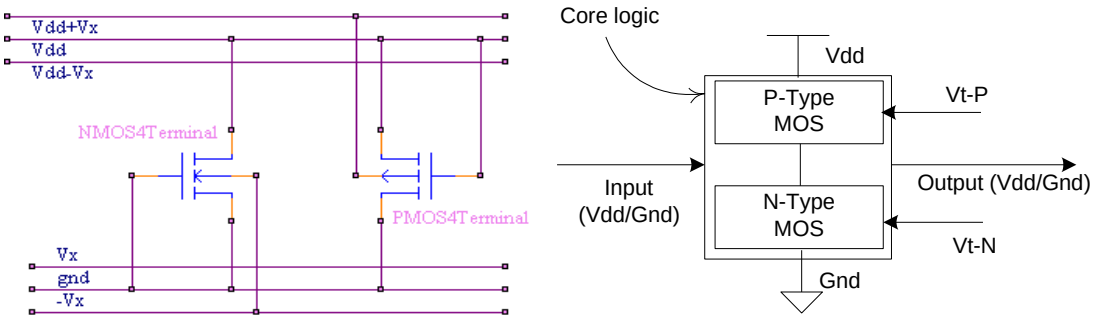


a) b)

Figure 3.12: a) MOS under gate voltage reverse biasing scheme, b) Circuit implementation.

3.4.4 Bulk/Substrate biasing scheme

This scheme involves a fixed source voltage over a controlled substrate voltage, as shown in Figure 3.13a. The advantage of this scheme is the manipulation of the threshold level of the device can be performed directly inside the logic core itself as shown in Figure 3.13b. Threshold voltage adjustment of power switches for alternate power lines can also be realised by this scheme to reduce leakage current [43].

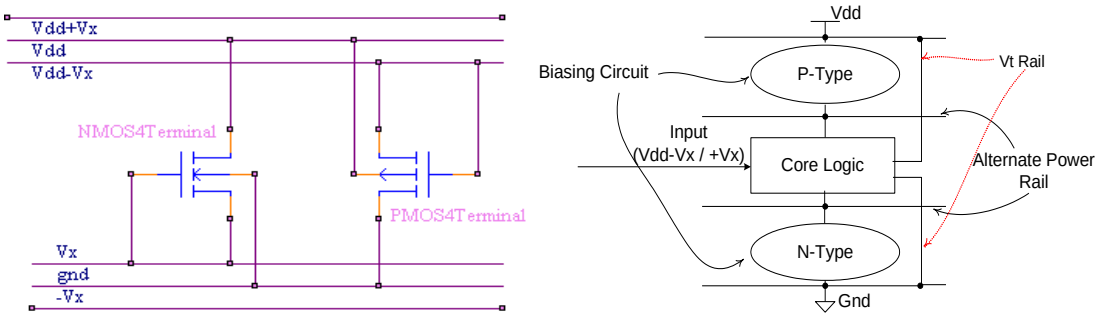


a) b)

Figure 3.13: a) MOS under substrate biasing scheme, b) Circuit implementation.

3.4.5 Source-gate voltage offset biasing scheme

A source-gate voltage offset biasing scheme can be achieved by controlling the source and gate voltage with a fixed substrate voltage, as shown on Figure 3.14a. The output of this scheme swings from V_{dd} - V_x to V_x, due to the alternate power rail [44, 45].

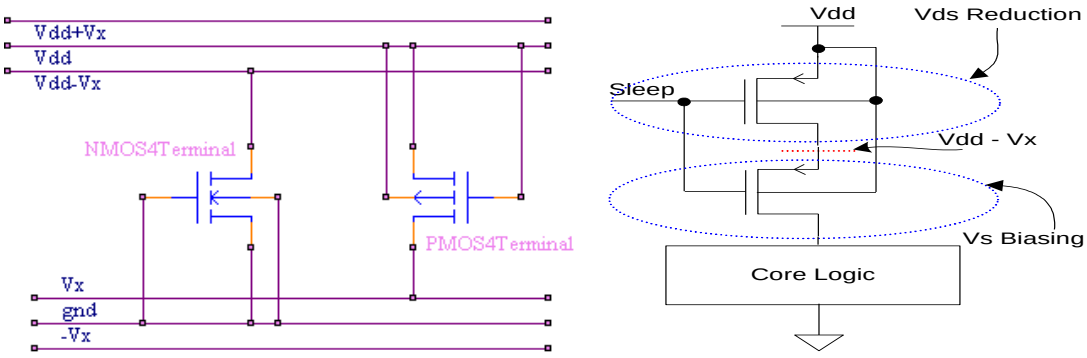


a) b)

Figure 3.14: a) MOS under source-gate voltage offset biasing scheme, b) Circuit Implementation.

3.4.6 Source-drain voltage reduction scheme

A source-drain voltage, V_{ds}, reduction scheme, shown in Figure 3.15a. It involves reduction in the drain terminal and normally does not work in isolation. This scheme requires another biasing technique to satisfy the required effect. A combination of circuit topologies, such as a source voltage biasing scheme, could satisfy leakage current reduction, as shown in Figure 3.15b. The additional transistor functions as a sleep transistor, which isolates the core logic from the supply voltage during standby mode.

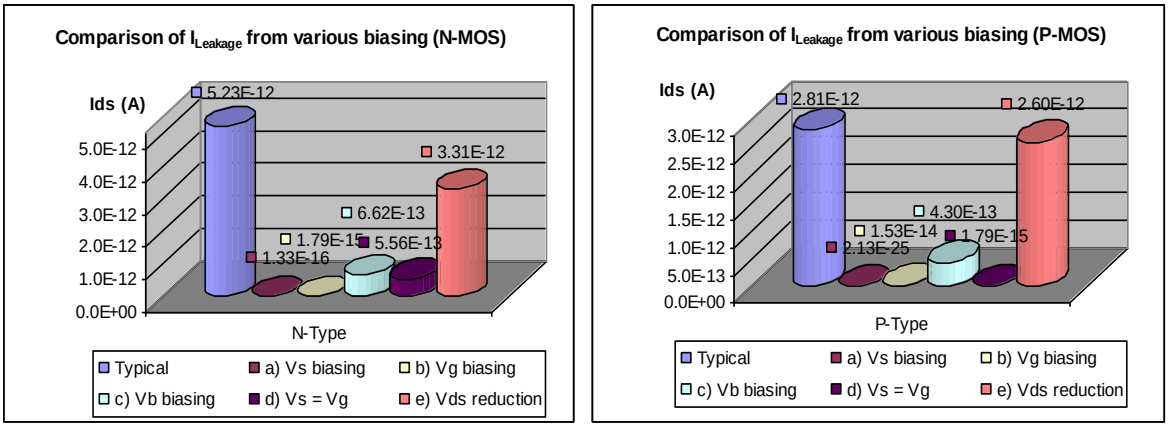


a) b)

Figure 3.15: a) MOS under V_{ds} reduction scheme, b) Stacking Effect

3.4.7 Comparison of simulated results for different biasing schemes

Figure 3.16, shows the subthreshold leakage current reduction ($I_{Leakage}$) comparison for the two types of MOS. The simulations were performed by applying 1.8 V as the nominal supply voltage, and offset voltage, V_x, as 300 mV. Subthreshold leakage current measurements were performed for each of the transistors under different biasing.

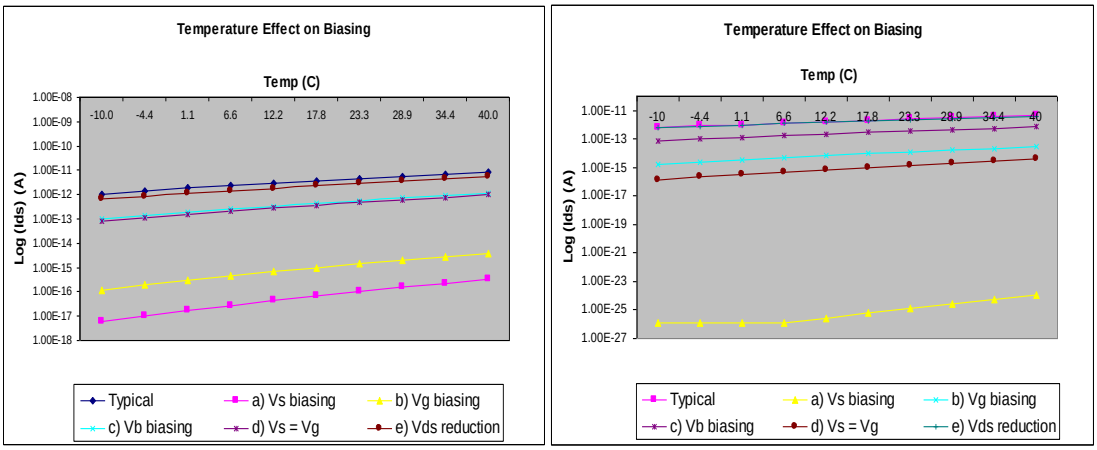


a) b)

Figure 3.16: Comparisons of the simulated leakage current result of a) N-type, b) P-type MOS under different biasing scheme

The results of the simulations indicate V_s reverse biasing to be the most effective in reducing subthreshold leakage current during standby mode. V_{ds} reduction gives the least reduction out of the five types of biasing, however there is a possibility to combine this scheme with V_s reverse biasing (stacking effect) to achieve optimum total power reduction. In another application, Substrate/bulk (V_b) biasing shows an attractive prospect as the possibility exists for the direct V_t manipulation of the leakage current. However, this might suffer a poorer recovery time, as usually a large voltage swing to control V_t is required.

Another important factor to consider is the effectiveness of the bias techniques against an increase in temperature. Simulating the transistor under bias with increasing temperature shows that there is a constant increase in the subthreshold leakage current as seen in the Log(I_{ds}) curve, shown in Figure 3.17.



a) b)

Figure 3.17: a) N-MOS, b) P-MOS biasing techniques against temperature for the various biasing schemes as described in the text.

3.4.8 Circuit application techniques of high threshold voltage circuit biasing schemes

A large number of biasing techniques have been presented above focusing on the reduction in leakage current with threshold voltage manipulation. Popular techniques such as, MTCMOS and VTCMOS and dynamic-V_t scaling use a combination of the biasing schemes to reduce standby leakage current, while dynamic- V_{dd} scaling are used to reduce dynamic power dissipation. This diversity implies that careful design is required to optimise the CMOS circuit for particular low power consumption applications.

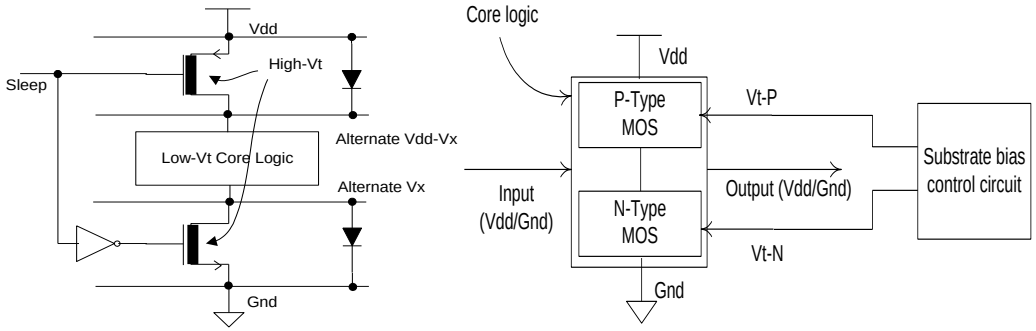
3.4.8.1 Multi-Threshold CMOS

Multi-Threshold CMOS (MTCMOS) is a circuit technique that uses two combinations of transistors. Low-V_t transistors for the high-speed core logic and high-V_t transistors as a power switch to reduce leakage current. The main principle of MTCMOS is shown in Figure 3.18a. MTCMOS has been a popular technique because of the simplicity of its design. Ideally the larger the threshold level the lower the leakage

current, however, one must decide the optimum value of the threshold level between the power switch (High-V_t devices) and (Low-V_t devices), as recovery delay tends to increase for the higher threshold level [46]. A thicker oxide layer, t_{ox}, must be considered to prevent transistor meltdown and to completely block the current flow in source-drain channel.

3.4.8.2 Variable-Threshold CMOS

Variable-Threshold CMOS (VTCMOS) is another way of reducing subthreshold leakage current [47]. The reduction can be achieved by directly manipulating the threshold level in the core logic. The general circuit diagram of a VTCMOS can be seen in Figure 3.18b. The manipulation has to be performed carefully to avoid the core logic exhibiting unstable behaviour from the sleep state to the active state, due to rigorous threshold scaling. The ideal way for determining the appropriate threshold level is to have two different levels of threshold, one for standby and another for the active mode. VTCMOS uses a different principle with dynamic-V_t scaling. Dynamic-V_t scaling is where the threshold level of the core logic is actively scaled according to input and clock requirements and is effective in reducing P_{static}.



a) b)

Figure 3.18 a) MTCMOS circuit architecture, b) VTCMOS circuit architecture.

3.5 Conclusion

This chapter presented the challenges in designing low power CMOS circuits for portable biomedical devices. The sources of power dissipation are categorised as dynamic and static dissipation. Both sources play their own part in total power dissipation. The technology scaling to the nano-meter scale has resulted in an increase of static power dissipation, mainly through the transistor's leakage current. This chapter discussed subthreshold leakage current reduction design techniques through a combination of analysed biasing schemes. Dynamic power dissipation, which was a well known problem in the past, has continued to increase due to increases in the circuit and chip complexity. Therefore, a solution must be obtained to reduce the overall power dissipation by considering these two elements. Chapter 4 discusses the importance of DC-DC converter as the dynamic power reduction enabler, and Chapter 5 discusses the detailed design and implementation of the dynamic voltage scaling scheme.

Chapter Four:
DC-DC Converter as a Dynamic Power Reduction Enabler

4.1 DC-DC Conversion

4.1.1 Introduction

As was discussed in Chapter 3, recent trends in portable electronics demand progressively ultra-low power circuitry to maximise battery life. An effective way to reduce power dissipation and maintain computational functionality in such systems is to operate digital CMOS circuits at the lowest possible supply voltage with architectural modification, applications of appropriate logic styles, and technology optimisation to compensate for any reduction in performance [48-51]. In portable electronic systems, an efficient low voltage DC-DC conversion is required to generate low voltage supply from a single battery source. This chapter discusses the role of DC-DC converters in conjunction with the dynamic voltage scaling technique.

4.1.2 Types and Challenges of Low Voltage DC-DC Conversion

This research work focuses on applications for ultra low power hand held biomedical devices where high energy efficiency (to ensure maximum savings) and small physical size are of critical importance. Therefore with such priorities in mind, low voltage DC-DC conversion architectures can be classified into two types: high-current and low-current converters.

4.1.2.1 Low-Voltage High-Current DC-DC Conversion

As CMOS technology scales down to nanometre size, a greater number of smaller geometry transistors can be integrated on a single chip. This reduction in transistor size also results in a reduction of supply voltage required to power the circuit, which is rapidly approaching 1.3 V and below. However, there is a consequent increase in system current with decreasing voltage, due to a greater system operating frequency and an increase in the overall system capacitance as a result of diminishing feature sizes. The low voltage, high current DC-DC converters are used specifically to meet this trend in processor based systems.

If a Pentium Pro® processor with current and voltage demand of 13 A at 2.4 V is scaled to 0.18 μm technology, it would require as much as 40 A at 1.0 V with an effective impedance of 25 mΩ [52]. If the converter supplying this current had an effective series impedance of 10 mΩ, considering all the resistance of wire bonding and packaging, the efficiency of DC-DC converter would be at best 60%. Further to this, powering up a processor from standby mode would require a current as high as 40 A from the DC-DC converter. This would require careful design, interconnect and a great amount of bypass capacitance to ensure a stable voltage. The bypass capacitance required would thereby increase from a few millifarads (mF) to more than 10 mF [53].

4.1.2.2 Low-Voltage Low-Current DC-DC Converter

The low voltage low current DC-DC converter is suitable for Application Specific Integrated Circuit (ASIC) digital signal processing circuits for portable device applications. In an ASIC implementation, the circuits are designed to meet a certain throughput requirement, and the current consumption has to scale according to the voltage supply, to obtain lower power dissipation and extended battery life. The biggest challenge in designing a DC-DC converter for this application is that it must dissipate far less power than its load to be effective in reducing power consumption. The converter's efficiency perhaps has become the most important design consideration for low voltage, low current DC-DC converters [50, 53-57]. Another

limiting factor is the device size, as portable applications demand minimum form factor of the DC-DC converter for portability.

4.1.3 The Importance of Voltage Regulation

A system can be designed to work at its optimum operating voltage to minimise power consumption without a DC-DC converter. This however makes the circuit design more challenging due to the non-linearity of the battery cell discharge characteristic, which results in the circuit consuming more power throughout the majority of the discharge period. The application of DC-DC converters between the power cell and the circuit load has been demonstrated to extend digital CMOS system life-time by up to 50%, running from a single Lithium Ion battery cell [58]. Since battery capacity is very limited in hand held portable electronics, DC-DC converters must dissipate minimal energy to be beneficial. Figure 4.1 depicts the typical discharge graph of three commercially available rechargeable AA-battery sources; Nickel Cadmium (NiCd), Nickel Metal Hydride (NiMH), and Lithium Ion (Li-Ion) [58].

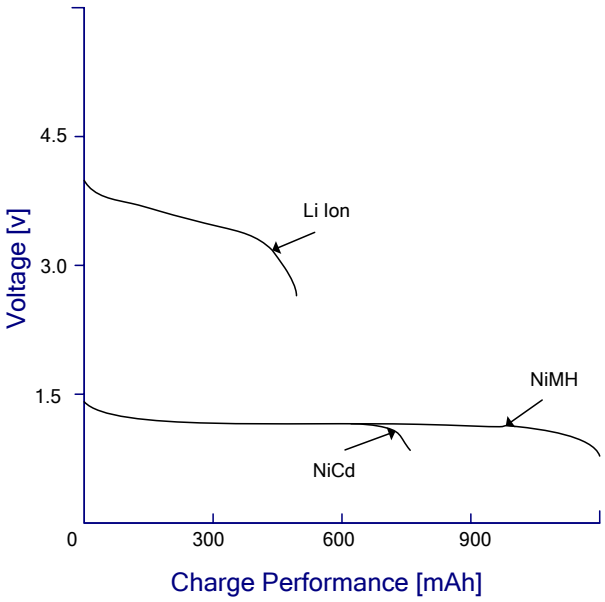


Figure 4.1: Typical discharge characteristics for AA-type Nickel Cadmium (NiCd), Nickel Metal Hydride (NiMH), and Lithium Ion (Li-Ion) cells [55].

By considering maximum battery life as the primary factor, a designer must ensure that the designed circuit will operate at the minimum possible supply voltage. Consider an integrated circuit block which uses a NiMh battery directly as its energy source. By observing the graph in Figure 4.1, the minimum possible voltage which the cell can deliver is 1.2 V. For a circuit designed using 90 nm transistor technology, the minimum possible supply voltage required to ensure a proper operation is roughly 80% (0.8 V) of its optimum supply (1 V). If the majority of the core logic power dissipation originated from dynamic dissipation, and the circuit is operating at 80% of optimum frequency to meet stable throughput requirements of the minimum logic voltage, *v(q)*, would be 0.8 V, then the circuitry will have the least amount of power dissipation at end of the battery usable life (minimum supply voltage);

$$P_{L(\min)} = f_{0.8}.C_{eff}.0.8^2 \qquad \text{Eq 4.1}$$

Equation 4.1 is derived from the dynamic power term of Eq 3.2, where C_{eff} is the effective switching capacitance of the overall circuit at a certain activity factor. However, at any other charge points along the NiMh discharge curve, the power dissipation of the circuit is given by:

$$P_{L(q)} = f_{0.8}.C_{eff}.v(q)^2 = P_{L(\min)}.\frac{v(q)^2}{0.8^2} \qquad \text{Eq 4.2}$$

By substituting *v(q)* equal to 1.5 V when the battery cell is fully charged, the ratio of maximum power to $P_{L(min)}$ is 2.4, while at nominal battery cell voltage, the ratio is 1.9. Thus, the load is seen to dissipate greater power with the same throughput. However, for a DC-DC converter placed between the battery source and the load with zero drop out and having efficiency η (equated in Eq 4.3), the output of the converter is regulated to match the battery's minimum voltage with power dissipation independent of $P_{L(min)}$.

$$\eta = \frac{P_{out}}{P_{in}} \qquad \text{Eq 4.3}$$

Thus, the power drawn at any point in the battery cell's discharge characteristic is constant and equal to:

$$P_{L(q)} = \frac{P_{L(\min)}}{\eta} \qquad \text{Eq 4.4}$$

The benefits of the DC-DC converter efficiency to a particular integrated circuit are to enhance system life time. This can be estimated by equating the approximation of battery energy usage and the circuit load. Consider the same battery source (NiMh) in Figure 4.1, at the end of usable life, the battery has delivered an amount of charge, Q_{eol}, and at total energy, E_{eol}. Therefore, the average voltage delivered over the delivered charge by the battery cell is equal to:

$$\overline{v(q)} = \frac{E_{eol}}{Q_{eol}} \qquad \text{Eq. 4.5}$$

The system life time, t_{eol}, can be approximated as the derivation of the area under the discharge curve, which represents E_{eol} at any point of time of current charge, $i(q)$. Thus, the approximation of the t_{eol} becomes:

$$t_{eol} = \int_0^{Q_{eol}} \frac{dq}{i(q)} \qquad \text{Eq 4.6}$$

To approximate the efficiency of voltage regulation to the battery life time, which discharge characteristic was depicted in Figure 4.1, the voltage source, $v(q)$, is applied to three different load models, constant current (I_{DC}), resistive load (R), and a constant power load (P_L), as depicted in Figure 4.2.

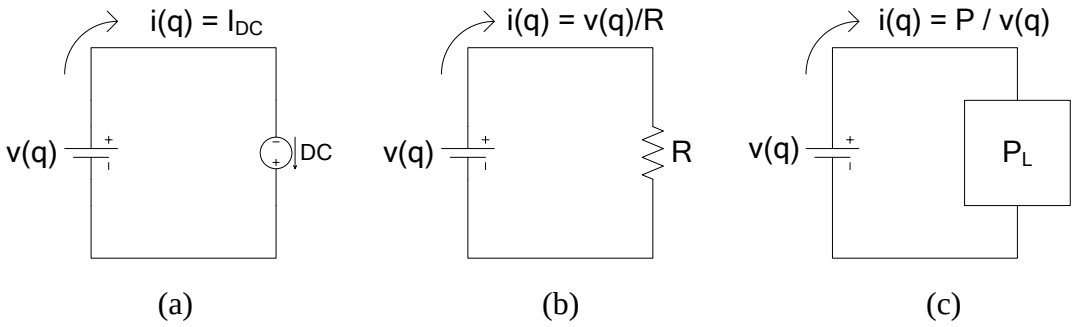


Figure 4.2: Three different loads applied to the battery model, (a) constant current, (b) resistive load, (c) power load.

Figure 4.2 (a), depicts the constant current, I_{DC}, drawn from the battery, thus the I_{DC} term will be generalised to I, which yields battery life, $t_{eol,}$ of:

$$t_{eol} = \frac{Q_{eol}}{I} \qquad \text{Eq 4.7}$$

However, if the battery's discharge characteristic is applied to a resistive load, shown in Figure 4.2 (b), with respect to average voltage over a period of time, the average delivered load current would be:

$$\overline{i(t)} = \overline{i(q)} = \frac{\overline{v(q)}}{R} \qquad \text{Eq. 4.8}$$

Thus, when Equation 4.8 is applied to Equation 4.6, it will give an expression of time for end of battery life as:

$$t_{eol} = \frac{Q_{eol}.R}{\overline{v(q)}} \qquad \text{Eq 4.9}$$

In the case of load model that draws a constant power, P_L, from the battery cell, as depicted in Figure 4.2 (c), the battery life is a ratio of the total energy delivered by the battery at the end of the life cycle, over the total power consumed, thus:

$$t_{eol} = \frac{E_{eol}}{P} = \frac{Q_{eol}.\overline{v(q)}}{P} \qquad \text{Eq 4.10}$$

The three battery loads and connections are then applied to analog or digital circuitry to observe the advantages of using a regulated power source.

4.1.3.1 Circuit connected directly to the battery cell

Consider an analog circuit with an ideal supply and independent biasing, which draws a current, *I*, independent of the voltage across its terminal, which gives a baseline system run-time, $t_{BL(eol)}$:

$$t_{BL(eol)} = \frac{Q_{eol}}{I} \qquad \text{Eq 4.11}$$

In digital CMOS circuitry, power dissipation is largely dominated by its dynamic components, which are: minimum voltage frequency, $f_{V(min),}$ to ensure the throughput requirements, and the effective switching capacitance, C_{eff}. Therefore, an effective resistance value is modelled to include the dynamic components mentioned above for equating the baseline system run-time. This is shown in Equation 4.12.

$$R_{eff} = \frac{1}{f_{V(\min)}.C_{eff}} \qquad \text{Eq 4.12}$$

Thus, by substituting R_{eff} into Equation 4.9, the baseline system run-time for a digital circuit running directly from a battery cell is obtained as:

$$t_{BL(eol)} = \frac{Q_{eol}.R_{eff}}{\overline{v(q)}} \qquad \text{Eq 4.13}$$

4.1.3.2 Circuits connected to a linear regulator

An ideal linear regulator has a zero dropout output voltage and consumes a negligible current with respect to the constant current as described in Equation 4.11. Therefore, it is valid to assume that the supply is regulated at the minimum operating voltage and by neglecting the quiescent current of the regulator, as shown in Equation 4.14.

$$\frac{t_{eol}}{t_{BL(eol)}} = 1 \qquad \text{Eq 4.14}$$

Equation 4.14 indicates that the system run-time is neither diminished nor enhanced, in other words there are no additional benefits gained by applying a regulator in an analog circuit to extend battery life.

However, in a digital circuit, where the load with effective resistance, R_{eff}, modelled in Equation 4.12 is run at the minimum throughput required, and at a minimum voltage of V_{min}, the circuit dissipates the following minimum current:

$$I_{\min} = \frac{V_{\min}}{R_{eff}} \qquad \text{Eq 4.15}$$

Substituting this minimum operating load current into I in Equation 4.7, and normalising it to baseline system time, $t_{BL(eol)}$, yields:

$$\frac{t_{eol}}{t_{BL(eol)}} = \frac{E_{eol}}{V_{\min}.Q_{eol}} = \frac{\overline{v(q)}}{V_{\min}} \qquad \text{Eq 4.16}$$

4.1.3.3 Circuits connected to a switching regulator

In an analog circuit connected to a switching regulator with efficiency η, and output voltage regulated to a minimum voltage, the load dissipates a constant and minimum power, which is equal to:

$$P = \frac{P_{L(\min)}}{\eta} = \frac{I.V_{\min}}{\eta} \qquad \text{Eq 4.17}$$

Substituting the constant power drawn, P, by the circuit into Equation 3.10 and normalising with $t_{BL(eol)}$, yields:

$$\frac{t_{eol}}{t_{BL(eol)}} = \frac{\eta.E_{eol}}{V_{\min}.Q_{eol}} = \frac{\eta.\overline{v(q)}}{V_{\min}} \qquad \text{Eq 4.18}$$

However, in digital circuitry, dynamic components contribute to the overall power dissipation and therefore the average power drawn by the circuit from the battery cell through the switching regulator is modified from Equation 4.17 to:

$$P = \frac{V^2_{\min}}{\eta.\mathrm{R}_{eff}} \qquad \text{Eq 4.19}$$

Thus, substituting Equation 4.19 into Equation 4.10 and normalising the equation with $t_{BL(eol)}$, yields:

$$\frac{t_{eol}}{t_{BL(eol)}} = \frac{\eta.E^2_{eol}}{(V_{\min}.Q_{eol})^2} = \frac{\eta.\overline{v(q)}^2}{V^2_{\min}} \qquad \text{Eq 4.20}$$

4.1.3.4 Comparisons of the system run-time

A comparison of system run-time can be drawn from the normalised baseline equations, $t_{BL(eol)}$, consisting of different load connections to battery cells, regulators and load circuits. In the comparison a factor of β is used to describe the ratio of the averaged delivered charge of the mean cell voltage to the minimum voltage required by the load:

$$\beta \approx \frac{\overline{v(q)}}{V_{\min}} \qquad \text{Eq 4.21}$$

A symbol K is used to denote the enhancement factor of the run-time, t_{eol}, relative to the baseline run-time, $t_{BL(eol)}$, when the load is directly connected to battery cell, as shown in Equation 4.22. The comparison of the different system run-times in terms of K is tabulated in Table 4.1.

$$K = \frac{t_{eol}}{t_{BL(eol)}} \qquad \text{Eq 4.22}$$

Table 4.1: Comparison of system run-time

Type of Regulation	Analog Load (constant current)	Digital CMOS Load (constant throughput)
Linear	K=1	K= β
Switching with η efficiency	K= $\eta\,\beta$	K= $\eta\,\beta^2$

Table 4.1 can be used to predict the advantage of different regulation schemes for a variety of loads. Incorporating linear regulation in an analog circuit does not give any benefit to the overall power dissipation, as many of the circuits draw constant current.

A linear regulator can be used in analog circuitry only if regulating the supply voltage improves the performance of the load circuit. The linear regulation improves system run-time by a factor of β for a digital CMOS load. However, if a switching regulator is used, regardless of the load type, then there is an additional factor $\eta\beta$ multiplied to the output which is produced by the corresponding linear regulator. Therefore, if an efficient switching regulator is applied to the circuit, which gives a total factor of $\eta\beta$ of more than 1, then it can be concluded that adding the switching regulator improves the overall system run-time.

4.2 Switching Regulators Converter Topologies

The operational principle of a switching regulator is illustrated in Figure 4.3. The circuit converts unregulated battery DC voltage source, V_{in}, to the desired regulated DC output voltage level, V_{out}.

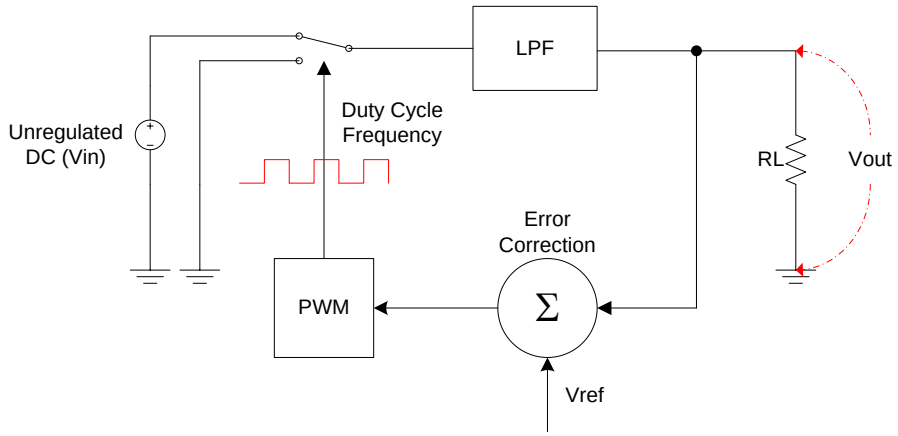


Figure 4.3: DC-DC converters driven by a PWM switching circuit.

The circuit mainly consists of a switch, a Pulse Width Modulator (PWM) circuit, a low pass filter (LPF), and an Error correction circuit. The switch, driven by a PWM circuit, switches between V_{in} and ground, producing a series of rectangular waves that averages out to the desired output voltage level. The series of rectangular waves are rectified by a LPF to an acceptable AC ripple value. The error correction circuit compares the regulated output voltage to a reference voltage, V_{ref}, which produces an

error voltage level to the PWM circuit. The correction voltage level adjusts the fraction of the duty cycle for which the switch is connected to V_{in}. The PWM generates an average voltage value of the clipped V_{in} and thus controls the output voltage. This type of switching regulator has an efficiency that approaches 100%, if ideal components are used in the circuit. Practically an efficiencies up to 90% are attainable with this circuit topology.

Generally, there are three basic topologies of pulse width/frequency controlled switching regulators. These are buck, boost, and buck-boost regulators [59-61]. Each one has different properties and switching filter components, which produce a smaller or higher output voltage than the input voltage. However, they each have an inductor and are derived from the same basic switching cell, by two power transistors.

4.2.1 Buck Converter

A buck converter can produce any arbitrary output voltage ranging from $0 \leq V_{out} \leq V_{in}$, and is depicted in Figure 4.4. The buck converter achieves its rectifying operation by switching the two power transistors, PMOS and NMOS, clipping the input voltage, V_{in}, to reduce the average voltage. The operation produces square waves with variable duty cycle, $d(t)$, at a constant period at the PMOS-NMOS inverter topology output.

The second order low pass filter, L and load capacitor, C_L, passes the desired DC component of the chopped signal, while attenuating the AC to an acceptable value. Ideally, the output voltage, V_{out}, is a result of the product of the input voltage and the duty cycle, as described in Equation 4.23.

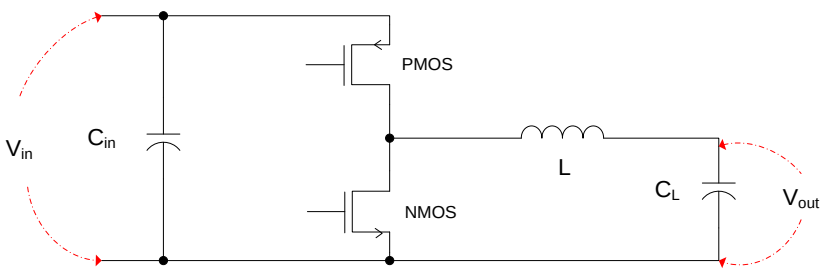


Figure 4.4: CMOS Buck converter circuit diagram.

The power transistors are driven by a pulse width modulates of square wave to adjust the duty cycle which depends on the input and load variations. The output voltage of the buck converter is described in Figure 4.5.

$$V_{out} \cong V_{in}.d(t) \qquad \text{Eq 4.23}$$

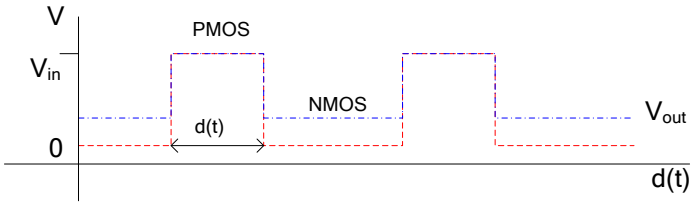


Figure 4.5: Power Transistors Periodic Output Voltage Waveform of the buck converter.

4.2.2 Boost Converter

The boost converter, as depicted in Figure 4.6 is considered to be a variation of the buck converter. A boost converter has a property of producing a greater output voltage than the input voltage, hence the name, thus $V_{out} \geq V_{in}$. The operational steady state waveform is shown in Figure 4.7. During the NMOS operation period (NMOS device is on), the input voltage applied across the inductor, *L*, builds up current in the inductor. When the NMOS device is turned off, there is a sudden change in the current flow across the inductor, hence causing the voltage across the drain and source of the NMOS device (V_{ds}) to increase rapidly.

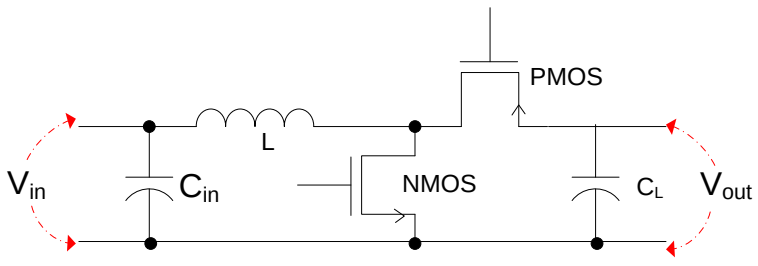


Figure 4.6: CMOS Boost Converter Circuit diagram.

At the same time, the PMOS transistor is switched ‘on’ to limit the voltage produced by the inductor to the load capacitor, C_L. This brief period of voltage release when the PMOS conducts some of the energy stored in the inductor, is transferred to the output with the additional current from input voltage. The cycle repeats over a period of time until a stable higher output voltage is reached.

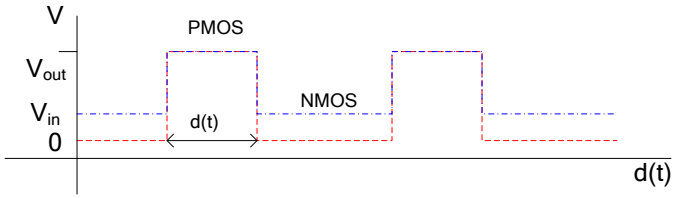


Figure 4.7: Periodic output voltage steady state diagram of a boost converter.

Thus the input-output voltage relationship in a boost converter can be described as the same as for buck converter, but with input and output terminals reversed, as can be seen in Equation 4.24.

$$V_{in} \cong V_{out}.d(t) \qquad \text{Eq 4.24}$$

4.2.3 Buck-Boost Converter

Another variation of the converters is the buck-boost converter, as shown in Figure 4.8. Buck-boost converters can produce output voltages of smaller or larger magnitude as compared to the input voltage.

The operation of a buck-boost converter starts when the PMOS device is turned ‘on’, which applies input voltage across the inductor, *L*, for a duration of *d(t)*. The next phase starts when the PMOS transistor is switched ‘off’, and NMOS transistor is ‘on’, and in this phase the voltage across the inductor drops having a polarity opposite to the input, as can be seen in Figure 4.9.

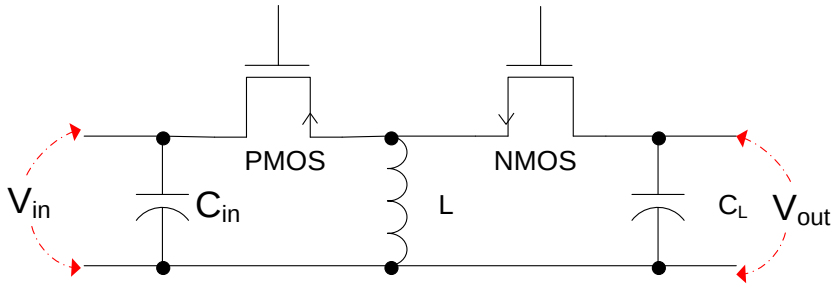


Figure 4.8: Buck-Boost Converter Circuit Diagram

However, the current flow differs from the boost converter, this time only energy stored in the inductor flows to the load capacitor, C_L. Therefore, if we assume the voltage across the inductor is equal to zero, the conversion ratio can be equated as:

$$V_{out} \cong V_{in}.\frac{d(t)_{on}}{d(t)_{off}} \qquad \text{Eq 4.25}$$

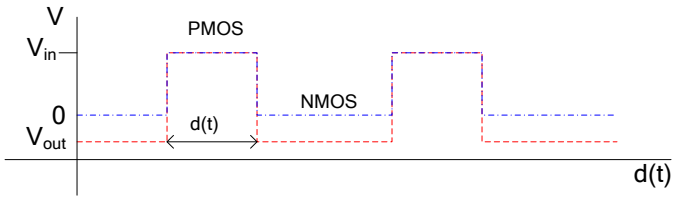


Figure 4.9: Periodical Steady-State Waveform of a Buck-Boost Converter.

4.2.4 Converter choice for a low power battery operated system

The three main converter constraints to meet the usage requirement in a battery operated portable system are:

- Low voltage support with high efficiency,
- Small size and low cost, and,
- Low noise emission.

Since the battery capacity, which can be fitted into a portable device, is limited, power minimisation is crucial, and the selected DC-DC converter must dissipate minimum energy to extend the overall system run-time. The device size form factors have reduced significantly. This is due to portable devices becoming increasingly sophisticated with various new technologies incorporated into a single system. Device cost is also an important factor in the consumer electronics industry. A high-end DC-DC converter chip with additional components could increase manufacturing costs of a system by up to $10. Therefore, an embedded integration of the DC-DC converter on to the core chip is a significant challenge for low power portable devices. The inductor used in the DC-DC converter is usually implemented as an external component. However, a minimum inductor design can be implemented by considering wire bonding inductive properties as a trade off for the inductor cost.

Noise emission is a major problem for DC-DC converters, since they are well known to be among the noisiest components in electronic circuits, due to their switching property. However, the high frequency noise emission can be controlled by careful design, isolation of noisy components in layout implementation and the use of soft switching techniques.

4.3 Conclusion

This chapter discusses various types of DC-DC converters and the effects of these converters on various loads. The benefits of implementing a switching DC-DC converter to a digital system, with the exception of a very short run-time system, will enhance overall system life-time. The small increase in the system area introduced by the application of the DC-DC converter is insignificant as compared to the increase in the battery volume. The simplicity and the step down output voltage property of a DC-DC buck converter are most desired for battery operated biomedical devices. The detailed description and application of the DC-DC buck converter in a dynamic voltage scaling scheme is described in Chapter 5.

Chapter Five:
Design Considerations in Dynamic Voltage Scaling for Dynamic Power Management

5.1 Introduction

This chapter describes the novel design techniques and the circuit implementation of dynamic voltage scaling (DVS) management for portable biomedical devices. DVS consists mainly of four major blocks: a pulse width modulator, a digital to analog converter (DAC), a voltage controlled oscillator and a DC-DC converter. In Section 5.1, the fundamental operating principle of a DVS system is presented. The concept of dynamically scaling the supply voltage to realise the speed versus power trade-off for systems with variable throughput requirements is also discussed. Section 5.2 describes the functionality of each DVS module. Section 5.3 explains design techniques, and circuit level implementation of the DAC, pulse modulator block, voltage controlled oscillator and DC-DC converter.

5.2 Dynamic Voltage Scaling Definition

Theoretical and experimental procedures show that lowering V_{dd} directly reduces the power consumption, as discussed in Chapter 3. However, the drawback in lowering V_{dd} is a longer delay signifying slower performance or slower processing speed in the integrated circuits. For instance, Intel® has developed a power dissipation solution for laptop/notebook computer users. The technique is named “Speed-Step Technology”

and can be found in Intel's mobile processors [52]. "Speed-Step Technology" presents dual power supply scaling management and frequency scaling. The dual power supply scaling management enables the processor to operate in two power domains, the battery mode and the external adapter mode. It steps up or down the processing speed according to the power source. Thus a reduction of power dissipation is obtained by slowing down the processing speed while in battery mode, resulting in longer battery life. However, "Speed-Step Technology" could not be applied to battery only sourced portable devices where a single power source is used.

One of the solutions to lower power dissipation is to use dynamic V_{dd} scaling technique. Dynamic V_{dd} scaling enables power supply scaling into different supply voltage levels. It is known that lowering the supply voltage means less charge or current flowing inside the circuit, which result in larger delay [62-65]. The concept behind the V_{dd} scaling is that, if the speed of a logic core can be adjusted according to the input throughput load or amount of the processor's computation required, then the processor can run at "just enough" operation frequency to meet the requirement, as shown in Figure 5.1.

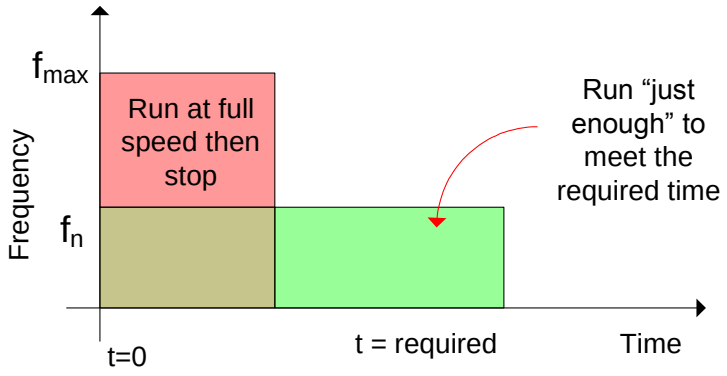


Figure 5.1: "Just enough" operation in dynamic V_{dd} scaling.

The voltage supply and frequency can be reduced for processes which do not require maximum throughput thus minimising power consumption. The primary factors involving power reduction in DVS are:

- A system is not always required to work at 100% performance.
- The total power dissipation for the device is dominated by dynamic power.
- The performance level is reduced during low utilisation periods in such a way that the processor finishes its task "just in time" by reducing the working frequency.

As the most effective way to manage power dissipation is highly dependent on the particular application, the current DVS implementation is focused at the algorithm level power scheduling which resides in the kernel system of the operating system rather than in hardware implementation. The portability of the DVS system to support multiple platforms with different requirements is the main concern for many DVS designers. These considerations cause DVS designers to depend on DVS at the algorithm level power scheduling. However, optimisation in DVS architecture can further reduce the algorithm used in process kernel by realising some of the modules in hardware, which will result in a more effective power management scheme. The focus of the research present in this thesis is on the application of DVS to portable biomedical devices. There are significant advantages in considering hardware elements to obtain optimum device performance.

5.3 Dynamic Voltage Scaling Architectural Design

This section discusses the modules required for a processor based DVS system. The power management blocks discussed in the DVS architecture include a DAC, a tuneable ring oscillator, a pulse width modulator, a phase frequency detector, a current driver and a loop filter [66].

Generally, there are three key considerations in the implementation of DVS in a system with a central processing unit (CPU), namely:

- An operating system capable of varying the processor speed.
- A regulator which generates a minimum voltage for a particular frequency.
- A main processing unit which is capable of working across a wide operating voltage.

As mentioned earlier, hardware implementation alone would not be possible. The processor speed is controlled by the operating system, where its task is to gather the load requirements of the process from a power profiler module. In order to minimise power dissipation, the supply voltage must vary as the processor frequency varies. However, the operating system is not capable of controlling the required minimum supply voltage for a given frequency. Hardware implementation is required to provide this functionality. The overall architecture of the designed DVS system is presented in Figure 5.2.

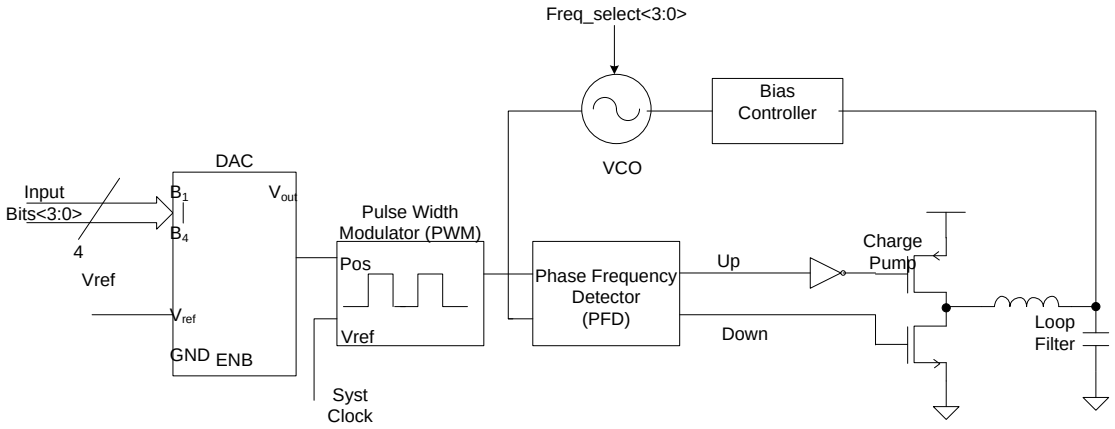


Figure 5.2: DVS Implementation System Architecture

The digital-to-analog (DAC) converter in the DVS system converts the quantised digital bits from the CPU's load to an analog voltage. The represented analog voltage is then used by the Pulse Width Modulator (PWM) as a voltage reference together with reference external clock pulses to generate a series of train pulses. The pulses vary in period, depending upon the voltage level from DAC.

The DAC used in the designed system is a weighted transistor voltage biased current DAC [67]. The transistor network configuration used in this DAC is based on resistor ladder (R-2R) architecture. By replacing the resistors with transistor pairs of width and

length (W) and twice the width (2W), the same R-2R characteristic can be obtained. The implementation of a transistor-only W-2W DAC will reduce the power dissipation of the DVS system, as no passive components are used.

PWM is a common modulation technique in signal processing. PWM generates a series of pulses where the pulse width varies depending upon the weighted input binary scalar. The PWM module used in the DVS system described in the thesis has the same functionality as a conventional system. The module generates a series of weighted pulses from the comparison of V_{ref}, as the reference voltage, and the oscillation frequency from the clock reference. The series of pulses from PWM is then compared by a Phase and Frequency Detector (PFD) with a tuneable oscillator frequency.

PFD is commonly used as phase detector in frequency lock in Phase Locked Loop (PLL) systems. As the phase difference of the two input signals: the reference clock, Ref-Clk (coming from PWM output) and the clock, Clk (the actual VCO clock), change so do the two output signals: Up and Down. The bigger the phase difference, the larger is the pulse width produced at the Up and Down terminals. The output signal DOWN is high when Clk leads the Ref-Clk signal, and output signal UP is high when Clk lags the Ref-Clk. These series of small pulses control the charge current injected by the charge pump circuit.

The purpose of a DC-DC buck converter is to transform time domain train pulses into continuous steady voltage for the VCO, depending on the signals from the PFD. If the reference clock signal lags the VCO signal, the PFD will discharge the charge pump and lower the output voltage, and vice-versa. The loop filter removes jitters and smoothes out the continuous steady voltage from the charge pump into an analog voltage to control the VCO frequency.

The VCO used in this DVS architecture is a current-starved ring oscillator which consists of transmission gate switches. A wide frequency range can be achieved by changing the VCO bit selection switch configuration. The minimum oscillation

frequency is obtained by using all the inverter stages. The ring oscillator also includes a current controlled inverter connected in parallel with a conventional inverter for gain control and for different inverter frequency stages. The output frequency of the VCO can be programmed to 330 KHz, 500 KHz and 1 MHz.

5.4 DVS Modules Power Consideration

Minimisation of power usage is a key objective of this thesis. Therefore it is important that each of the selected modules dissipate minimum energy to extend overall system run-time. Metal Oxide Semiconductor (MOS) transistor scaling has made it feasible to improve circuit performance and transistor density. However, as the dimensions of a MOS device are continuously scaled down to sub-micron, approaching the physical limit of fabrication processes, new problems arise. One of the major problems is the exponential increase in leakage current with oxide scaling. For this reason the MOS transistor becomes increasingly sensitive to process and temperature variations [27]. For example, temperature variation effects electron migration within the MOS, particularly the drain current in the subthreshold region. Hardware implementation of a DVS system on a very large scale digital system creates a mixed-signal circuit environment. Mixed-signal integrated circuits usually consist of the same cell placed adjacently in two dimensional arrays for parallel processing, with additional analog peripheries. The effect of variations in a mixed-signal environment will jeopardize the linearity of the analog circuitry, which will in turn affect the overall system performance. One way to prevent the system from malfunctioning is to design the analog circuitry to be highly immune to these variations and hence maintain linearity.

5.5 DVS Modules Circuit Implementation

5.5.1 Digital to Analog Converter

This thesis proposes a MOS DAC scheme with improved circuit linearity and a voltage reference biasing circuit which is insensitive to variations. The MOS DAC described is based on a current splitting technique with additional circuitry to compensate for transistor mismatch.

5.5.1.1 DAC Types

This sub-chapter compares different types of DAC configurations considered for the work to determine that with the lowest-power, and most linear and stable operation for portable biomedical application.

5.5.1.1.1 Typical R-2R Resistor Ladder DAC

Generally, a DAC is implemented by using the R-2R technique. This technique involves splitting the voltage reference using a binary weighted resistor ladder network. The ladder network is arranged in a particular manner so that current flowing inside the R-2R ladder network causes a division of the voltage reference (V_{REF}) by a binary representation to analog voltage. The R-2R technique can be classified into two sub categories: voltage mode R-2R DAC and current mode R-2R DAC.

5.5.1.1.2 Voltage Mode Resistor Ladder DAC

In the voltage mode DAC, the binary weighted switches are connected before the R-2R ladder, as shown in Figure 5.3. Therefore the current distribution is performed before the current-splitting. The voltage level on the non-inverting input of the operational amplifier is the potential difference of the two voltage references (V_{REF+} and V_{REF-}), which in general can be written as

$$V_{+} = \sum_{bits=1}^{TN_{bits}} \frac{N_{bits} \cdot V_{REF+} + \overline{N_{bits}} \cdot V_{REF-}}{2^{bits}} + V_{REF-} \qquad \text{Eq 5.1}$$

Equation 4.1 indicates that the output voltage swings from V_{REF+} to V_{REF-} with N_{bits} as the number of active bits, $\overline{N_{bits}}$ as the number of non-active bits and TN_{bits} as total number of bits. However, the non-inverting operational amplifier connection to the R-2R ladder will introduce a linearity problem.

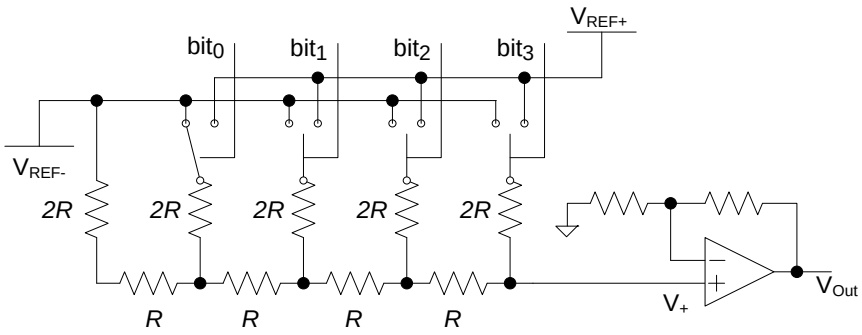


Figure 5.3: 4 bits R-2R Voltage Mode Resistor Ladder DAC.

5.5.1.1.3 Current Mode Resistor Ladder DAC

In typical current mode R-2R DAC, the voltage references are scaled statically with the resistor weight, which results in a constant current flowing through the various branches of the resister ladder network, as shown in Figure 5.4.

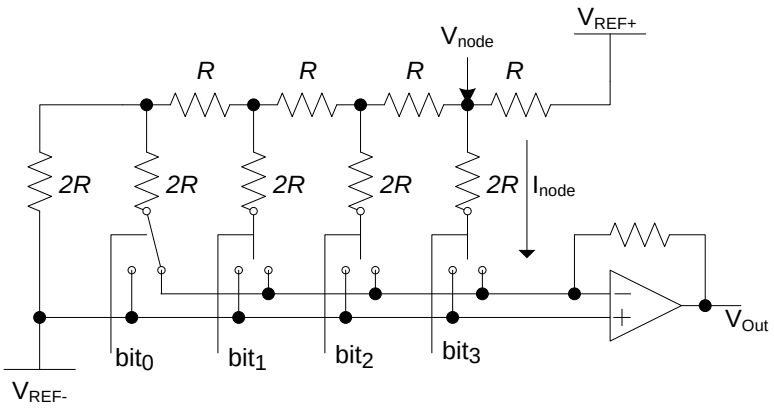


Figure 5.4: 4 bits R-2R Current Mode Resistor Ladder DAC.

The branch currents flowing through the R-2R ladder network are diverted, either to a feedback resistor inverting input of the operational amplifier or to the negative voltage reference (V_{REF-}), which is connected to the non-inverting input of the operational amplifier by binary weighted input switches. The final output of the DAC is the addition of the current on each ladder branch, which can be written as

$$I_{node} = \frac{V_{node} - V_{REF-}}{2R} = \frac{1}{2R} \cdot \frac{2^{node}}{2^{bits}} \left(V_{REF+} - V_{REF-} \right) \qquad \text{Eq 5.2}$$

where *node* is the number of reference point nodes for calculation purpose with total number of input *bits*.

The DAC's output voltage is determined by the subtraction of the current from the voltage references and the total current on each branch, which results in lower output swings. However, it is beneficial to have a wide output swing as was the case for the voltage mode DAC and to have a fixed common mode input, as in the current mode DAC. Both properties can be achieved by:

- Re-arranging the bits selector and the resistor ladder.
- Keeping the common mode voltage of the op-amp fixed.

As a result, the modified *wide swing current mode DAC* can be seen in Figure 5.5. The total current flowing through the inverting input from each branch of the operational amplifier can be described in Equation 5.3.

$$I_{-} = -\frac{V_{REF+} - V_{REF-}}{2R} + \frac{V_{REF+} - V_{REF-}}{2R} \cdot \left[1 \cdot \overline{N_{bits}} + \sum_{bits=1}^{TN_{bits}} \frac{1}{2^{N_{bits}-1}} \cdot \overline{bits} \right] \qquad \text{Eq 5.3}$$

Assuming the feedback resistor is equal to *R* in the ladder network, the output voltage of the DAC is equal to

$$V_{out} = V_{REF-} + \frac{V_{REF+} - V_{REF-}}{2} + I_{-} \cdot R \qquad \text{Eq 5.4}$$

Application of Equation 5.4 will reveal that the output of the DAC changes from V_{REF+} to $V_{REF-}+1$ LSB in steps of 1 least significant bit (LSB) or $(V_{REF+}-V_{REF-})/2^{Nbits}$. The rail to rail swing can be obtained by replacing V_{REF+} and V_{REF-} with V_{dd} and *Gnd* respectively.

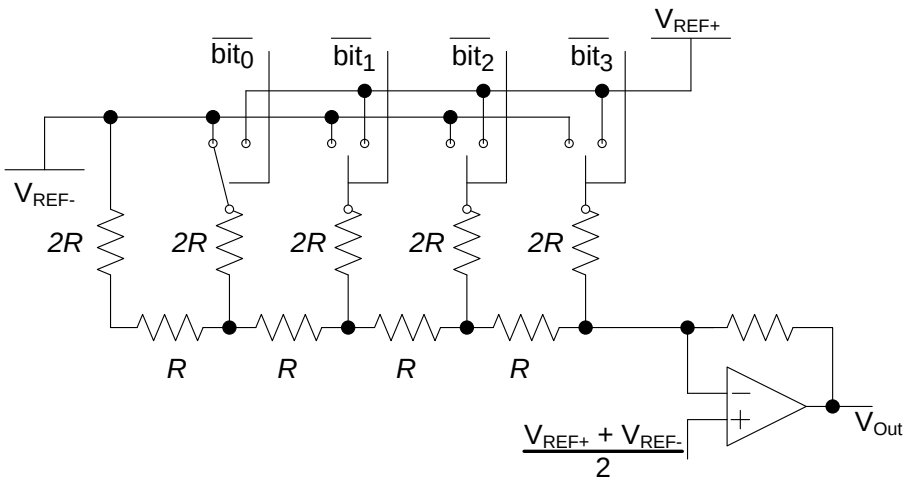


Figure 5.5: 4 bits R-2R Wide Swing Current Mode Resistor Ladder DAC.

5.5.1.1.4 MOS Transistor DAC

The MOS current splitting method was first introduced by Bult and Geelen in 1992, and is an alternative implementation of the traditional resistor ladder which utilises transistors in the ladder network [67]. The currents are divided in the similar fashion to the resistor ladder, so that the currents are binary weighted in each branch, as shown in Equation 5.5.

$$I_i = I_{REF} / 2^i \qquad \text{Eq 5.5}$$

The W-2W network, shown in Figure 5.6, splits the current depending on the bias voltage (V_{Bias}) conditions of the transistors, which mean the transistors can either operate in weak or strong inversion mode, in other words in their triode or ohmic region. One can easily observe the similarity of the way current splits in W-2W and R-2R, by the arrangement of two 2W transistors in series is equivalent to a single W transistor, and the combination of two W transistors in parallel is equivalent to a single 2W transistor [68].

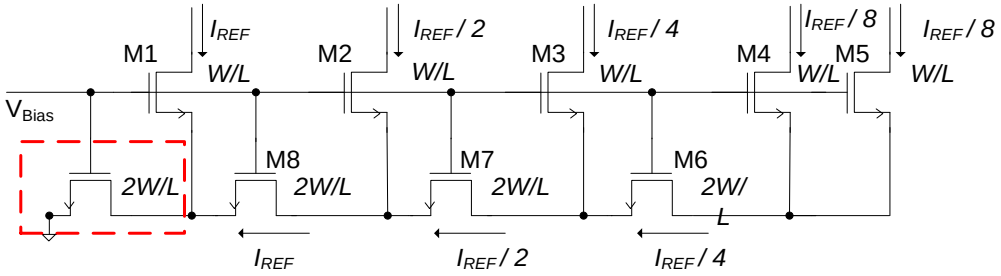


Figure 5.6: Current Splitting Principle in NMOS DAC, with reference current (I_{REF}) flow through in each W-2W transistor branch with intercorrelation mismatch correction transistor shown in the dashed box.

5.5.1.2 Improving Linearity in Low Power Weak Inversion DAC

The intercorrelation mismatch in N-type MOSFET-only DAC is related to the ladder arrangement of the transistors. Consider the top section of Figure 5.6, it can be seen that the mismatch current I_{REF}, is due only to the mismatch in transistor M1 of size W/L. However, the mismatch current $I_{REF/2}$ is due to mismatch in transistor M1 and M2, and the current mismatch $I_{REF/4}$ is related to M1, M2, and M3, and similarly for $I_{REF/8}$. In general, the last transistor M5 in the ladder is experiencing serious current mismatch carried over from the previous transistors' current mismatch which will affect the DAC linearity.

5.5.1.2.1 Intercorrelation Mismatch Correction Transistor

The intercorrelation mismatch can be reduced by averaging the DAC current with the output from a few exact replicas of the DAC [69]. By placing a few DACs adjacent to each other in the mask layout, the random mismatch effects will be averaged and linearity improved. The disadvantage in using this averaging method is that the total output current is four times the current in a single DAC, hence resulting in a higher power dissipation. Other alternative ways to reduce the effect of the intercorrelation mismatch is to directly reduce the current flowing through the DAC, either by adding another 2W/L transistor in series to ground (V_{REF-}) path (lowering the bias current applied to V_{Bias}) or by selecting larger transistor dimensions (W/L). An additional transistor, shown inside the dashed box in Figure 5.6, which is referred to as the

intercorrelation mismatch correction transistor, reduces the current flowing inside the ladder to ground, hence reducing the mismatch. The effect of the intercorrelation transistor mismatch is to increase the overall linearity, by changing the 1 LSB step value, as can be seen in Figure 5.7. The graph in Figure 5.7 shows an improved linear step increment with a intercorrelation mismatch correction transistor (black line), as compared to the DAC without a correction transistor (dashed red line).

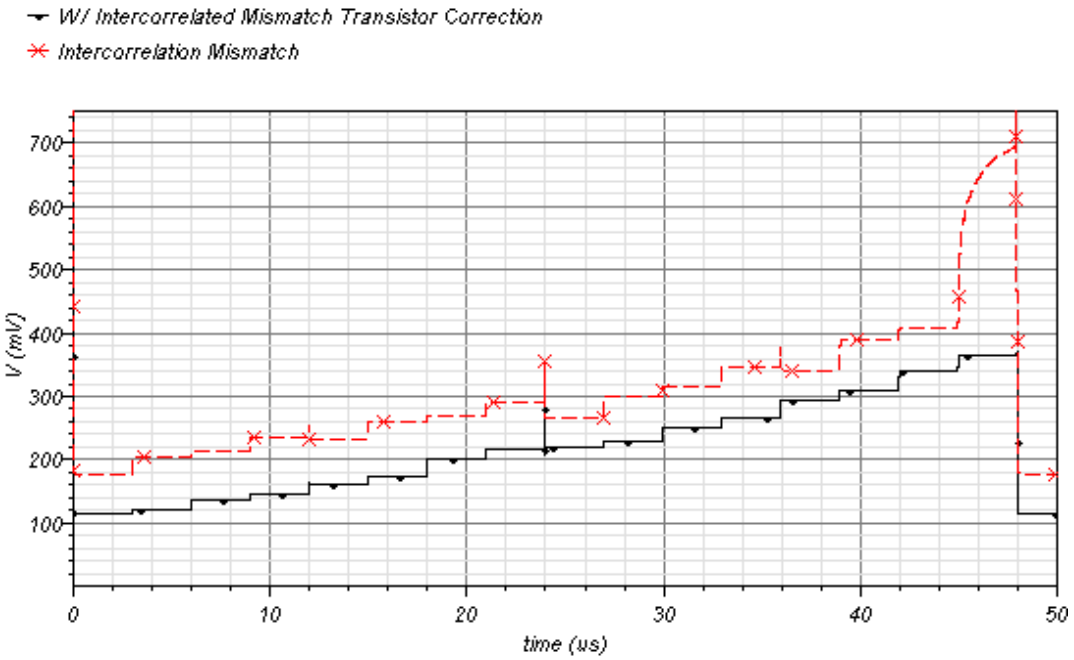


Figure 5.7: Simulation Results of the effect of Intercorrelation Mismatch in transistor-only DAC with the application of the correction transistor. The linearity of the DAC is improved by using the correction transistor as shown by line in black.

5.5.1.2.2 Voltage Bias

As discussed above, the voltage bias, V_{Bias}, manages the MOS transistor DAC so that it may operate in either strong or weak inversion mode, whilst the splitting method still works the same way. As far as linearity is concerned, lowering the V_{Bias} has a beneficial impact on linearity. Lowering V_{Bias} reduces the transistor operating region, hence reducing the mismatch current in the ladder, as depicted in Figure 5.8. Four bias voltages were simulated, from 100% bias voltage to 50% bias voltage. At 100% the

bias voltage is equal to V_{dd} or in other words the transistors are operating in the fully saturated mode. In general, the simulation shows better linearity for a transistor with biasing near the threshold voltage level, which is 0.4 Volt. Any biasing lower than the threshold voltage would significantly reduce the step size, which in turn would require a very large gain and more sensitive amplifier to increase the output level. As variation in biasing voltage has a significant impact on the performance of a transistor DAC, it is critical to have a stable voltage reference circuit insensitive to process variations for the DAC's biasing. The process variations insensitive biasing voltage circuit is shown in the dashed box in Figure 5.9. The biasing voltage circuit is a modification of the work of Vittoz [70]. The circuit has no bulky resistive dividers and works in the weak inversion region, which is known to have better immunity to variations. The desired bias output voltage can be obtained by appropriate sizing of the transistors W_1 and W_2 using the following equation:

$$V_{BIAS} = \frac{kT}{q} \log\left(\frac{W_1}{W_2}\right) \qquad \text{Eq 5.6}$$

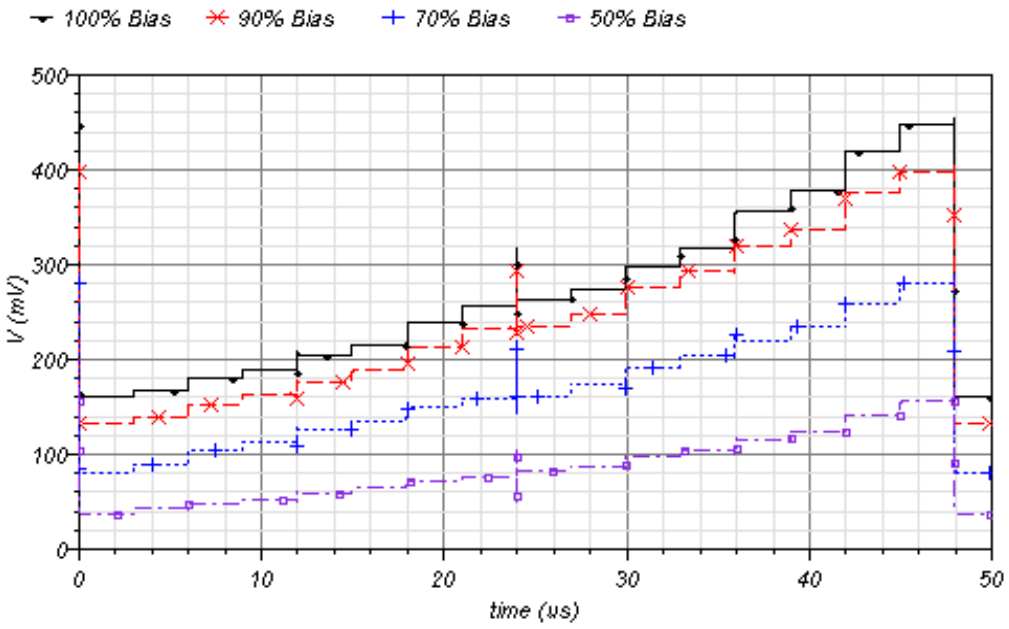


Figure 5.8: The Comparison of four different Voltage Biases (100%, 90%, 70% and 50%) on transistor only DAC, which directly effect the DAC linearity.

5.5.1.2.3 Transistors Dimension

Transistor dimension (W/L) has an important role in DAC intercorrelation mismatch, as the transistor size directly modifies the current under a particular biasing voltage. Figure 5.10 provides an indication of how the linearity of the current biased DAC relates to the transistor size. Transistors with four different geometries, with the largest width size of 10 µm to the smallest width size of 0.2 µm, were simulated. The simulation shows that the bigger transistor size has a noticeable negative impact on linearity, which is mainly due to excessive current present in the circuit. This verifies that the intercorrelation mismatch increases as more current is introduced in the circuit. On the other hand, a very small transistor size induces large deviations in the transistor electrical parameters, which would adversely affect the dynamic range of the DAC due to large random variations. Therefore, a careful selection of transistor size is required, which is referred in [71]. In this research, transistors with width size of 5 µm were selected for the MOS-only current steered DAC circuit to minimise power and limit random variations.

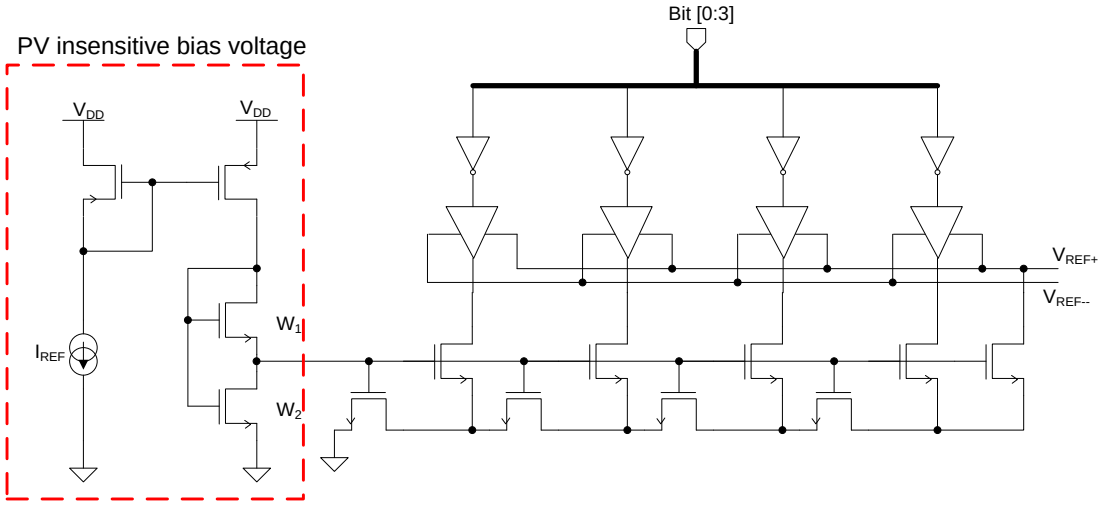


Figure 5.9: The MOS Current Steered DAC with the process insensitive bias voltage shown in the dashed box.

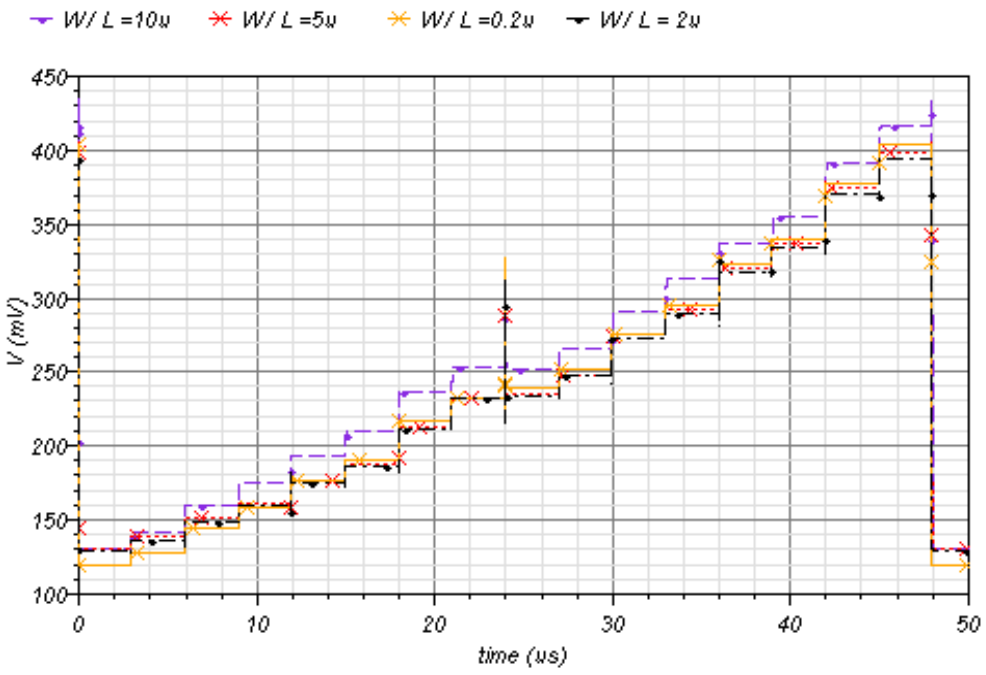


Figure 5.10: The comparison of different transistor size on linearity in the MOS only transistor DAC. Four different transistor width were simulated; 10 µm, 5 µm, 2 µm and 0.2 µm

5.5.1.3 DAC performance

The DAC produces reasonable linearity of ± 0.55 LSB at a moderate application frequency. However as frequency increases, capacitive effects of the scaling transistors on linearity become more apparent, as depicted in Figure 5.11.

The effective methods of increasing linearity in a MOSFET-only current steered DAC, by transistor correction and process variation insensitive voltage reference, have been presented. The mismatch of the output current in the DAC's ladder network depends on the mismatch of all the devices in the structure, except in the first transistor current in the first branch of the ladder.

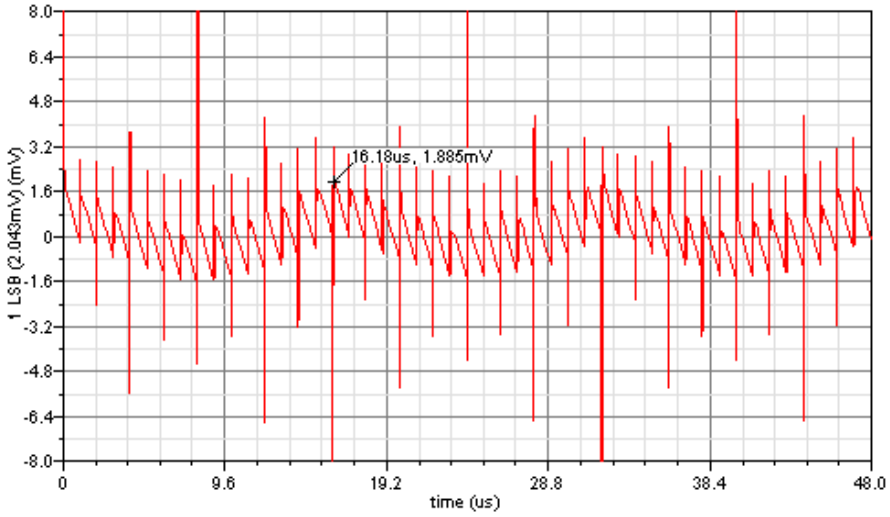


Figure 5.11: An INL @ 150 MHz plot of the MOS only transistor DAC.

5.5.2 Pulse Width Modulator

Pulse Width Modulation (PWM) is a common modulation technique in signal processing. PWM generates a series of pulses where the pulse width varies depending upon the weighted input binary scalar. The PWM circuit used consists of a comparator with a two stage fast pull-up and pull-down amplifier, as depicted in Figure 5.12. The comparator amplifies the difference between the two input reference (negative, Neg and positive, Pos) signals. The result is propagated to the pull-down and pull-up stage to generate a series of pulses in different width sizes, as shown in Figure 5.13. This type of amplifier is very beneficial for low-voltage design, as it increases the input swings coming from the previous module being the ultra-low power DAC.

5.5.2.1 PWM Design Specifics

The PWM circuit was designed to compare the input from the DAC to the reference clock. The DAC produces output references ranging from 120 mV to 420 mV. In other words, a 300 mV output signal must be resolved by the comparator. The power supply rails are 1.2 V for V_{dd} and 0 V for V_{ss}. Thus, the output will swing by 1 V peak (from 0 V to 1 V) for the resistor ladder output signal swing of 300 mV (from 120 mV

to 420 mV). Therefore the comparator gain must be at least 3.333 to have a full scale voltage output. The following specifications were used in designing the comparator in Pwell material transistor process; V_{dd} = 1.2 V, voltage gain > 3.333, Output voltage $0 < V_o < 1$, and with slew rate (SR) of 10 V/µs.

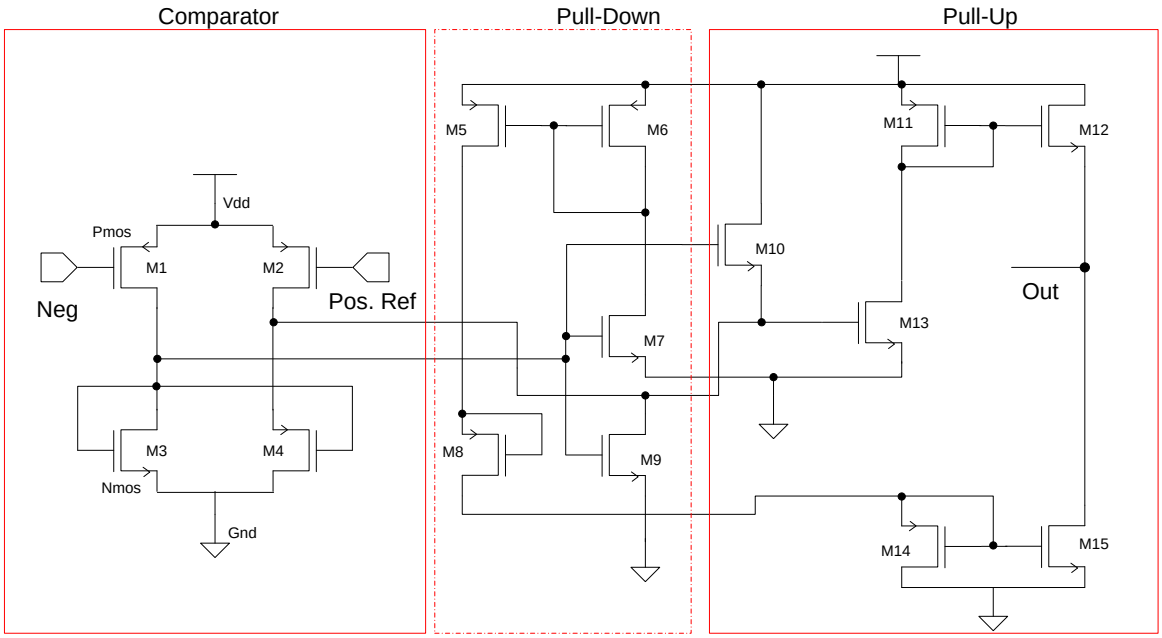


Figure 5.12: Two Stage Comparator Functioning as Pulse Width Modulator, with the pull-down and pull-up circuit for faster output response.

The first calculation involves the drive current requirement of the circuit to satisfy the SR specification. By estimating the load capacitance (C_L) induced by the PFD circuit to be 20 pF, the drain current required by transistor M15 is estimated by the following equation,

$$I_{drain} = C_L\left(\frac{dV}{dt}\right) \qquad \text{Eq 5.7}$$

where the rate of voltage change over time (dV/dT), is the required SR output signal. The estimated output current required to drive the load is 200 µA.

The size of transistor M12 and M15 can be calculated by applying Equation 5.8, with the transistor saturation value ($V_{ds12(sat)}$) at 1 V, to satisfy the output voltage swing requirement.

$$V_{ds12(sat)} = \sqrt{\frac{2I_{ds12}}{K_p\left(W/L\right)_{12}}} \qquad \text{Eq 5.8}$$

Similarly with transistor M15;

$$V_{ds15(sat)} = \sqrt{\frac{2I_{ds15}}{K_N\left(W/L\right)_{15}}} \qquad \text{Eq 5.9}$$

The calculated transistor M15 and M12 size determine the second stage gain of the circuit.

$$A_{v2} = -\left(\frac{g_{m12}}{g_{ds12}+g_{ds15}}\right) = -\frac{\sqrt{2K_N I_{ds12}\left(W/L\right)_{12}}}{I_{ds12}\left(\lambda_N+\lambda_P\right)} \qquad \text{Eq 5.10}$$

The second-stage gain equation is then used to estimate the gain for the first stage, by applying Equation 5.11

$$A_v = A_{v1}A_{v2} \qquad \text{Eq 5.11}$$

The output current that flows through M15 is approximately equal to the current flowing in M13, which is in current mirror topology to transistor M4.

$$I_{ds13} \approx I_{ds15} \qquad \text{Eq 5.12}$$

Therefore, the first stage biasing current can be designed by using a minimum transistor size so as to minimise output offset voltage. The current I_{ds4} flowing in M4 which mirrors with M15, can be approximated using Equation 5.13.

$$I_{ds4} = \frac{\left(W/L\right)_4}{\left(W/L\right)_{15}} I_{ds15} \qquad \text{Eq 5.13}$$

Since the current that flows in M4 is equal to M3, the width and length of transistor M1 required can be approximated using the remaining gain required for stage one to produce the total gain of 3.333. Estimation for transistor M1 device parameter is equated in Equation 5.14

$$A_{v1} = -\left(\frac{g_{m1}}{g_{ds2} + g_{ds4}}\right) = -\frac{\sqrt{2K_P I_{ds1}(W/L)_1}}{I_{ds1}(\lambda_N + \lambda_P)} \qquad \text{Eq 5.14}$$

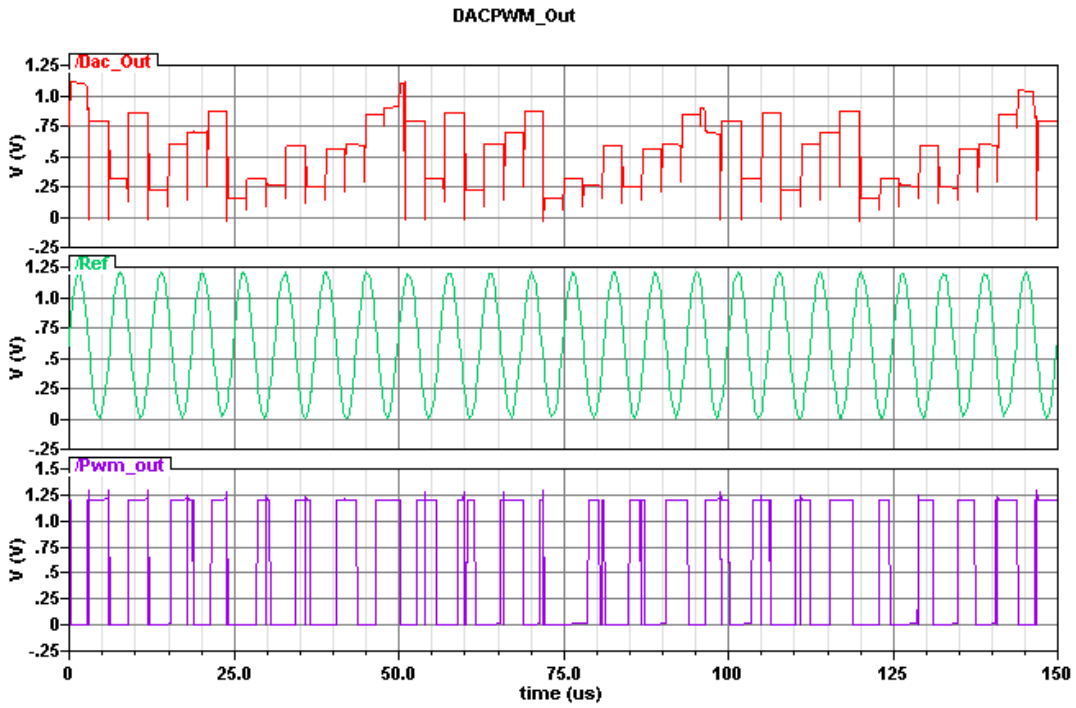


Figure 5.13: Pulse Width Modulator Circuit Output Waveforms (Pwm_OUT), which compares the DAC circuit output (Dac_Out) to the reference clock signal (Ref).

The equations are used to approximate each transistor's parameters for the PWM circuit. The transistors are further optimised using Cadence Analog Artist® to meet the power and pulse width requirements. The final voltage gain magnitude and phase margin bode plot centred at 500 KHz is shown in Figure 5.14. The bode diagram shows a steady gain magnitude at centre frequency, with phase margin of approximately -30 deg at its peak.

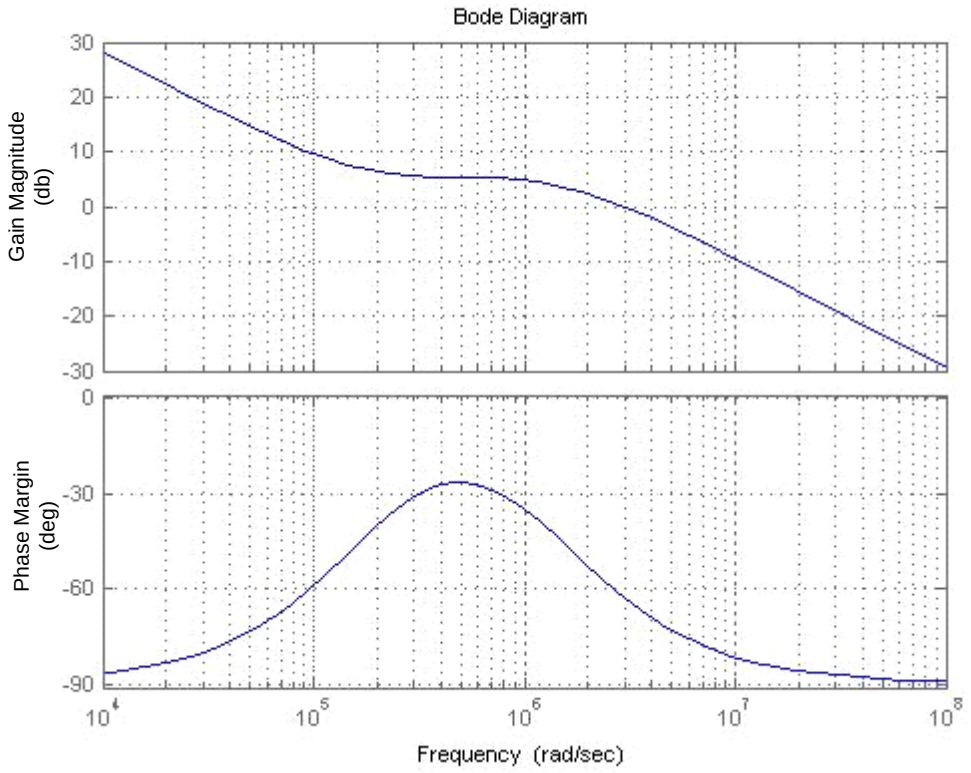


Figure 5.14 Pulse Width Modulator Circuit Gain Magnitude (db) and Phase Margin (deg) Bode Diagram.

5.5.3 Current-Starved Voltage Controlled Oscillator

The Voltage Controlled Oscillator (VCO) used in the research is a current-starved-based ring-oscillator with selectable frequency bits. CMOS Current-starved VCO circuit designs are known to be commonly integrated due to: their feasible implementation, their linear response over a wide range of input voltages ranging from threshold to V_{dd}, and their ability to allow a design that can be specified across a wide frequency range.

5.5.3.1 Current Starved VCO with selectable frequency

The implemented VCO contains cascaded ring oscillators. Ring oscillators are known for their linear response over a wide range of input bias voltages and may be varied from NMOS's V_{th} to V_{dd}, which are suitable for many integrated circuits applications. The implemented ring oscillator is partitioned with transmission gates to achieve a wide range of frequency selection. The ring oscillator circuit with frequency selector and bias control circuit is shown in Figure 5.15. The oscillator contains a voltage-to-current converter to generate a bias current for each inverter for fine frequency tuning.

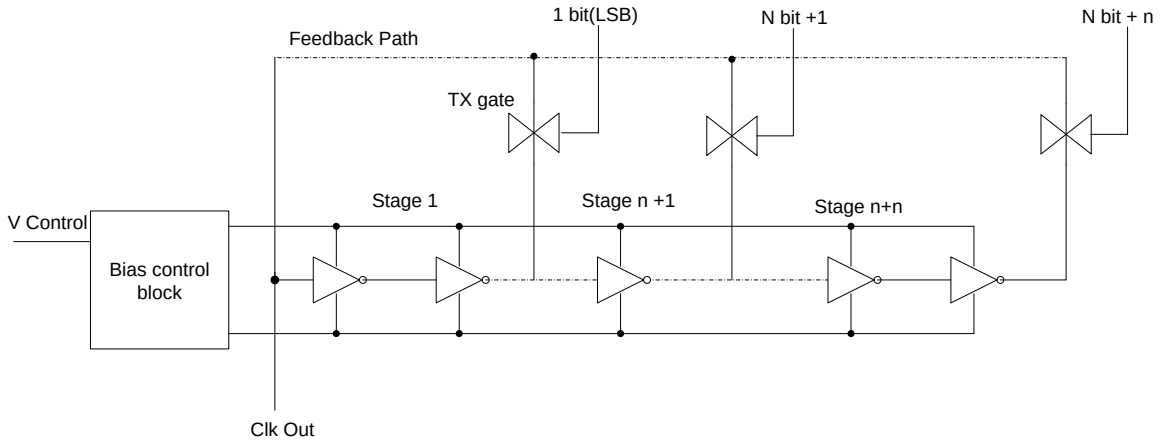


Figure 5.15: The designed ring oscillator partitioned with transmission gates to allow frequency selection and bias control for frequency fine tuning.

Each ring oscillator stage consists of an odd number of serially connected inverters. The operational frequency and power requirement for the design and for biomedical applications in particular, determine the total number of inverters used in the oscillator chain. The oscillator chain is divided into a smaller group of odd numbered inverter stages to enable frequency scaling for the DVS application. The inverter stages are separated from each other by a transmission gate circuit, so as to vary the length of the inverter chain. The transmission gate acts as a short circuit path, sending the generated pulses into the feedback path. Generally, a slower output frequency for the oscillator can be achieved by enabling more inverter stages, as greater delay is introduced in the oscillator chain. The bias control block, as seen in Figure 5.16, consists of six transistors arranged in a current mirror topology.

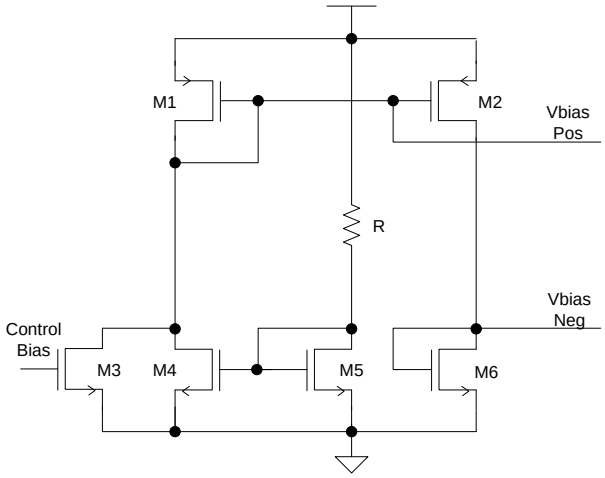


Figure 5.16: Bias Control Block of the ring oscillator which generates positive and negative voltage bias to the inverter stages.

The input transistors, M3 and M4, generate current pull to transistor M1, which in turn drives bias transistors M2 and M6. This circuit represents a current mirror which determines the maximum current that can flow in the circuit limited by the resistor, *R*. The output bias voltages, V_{bias}-*Pos* and V_{bias}-*Neg*, are equal in their relative voltage magnitude but in opposite sign. The magnitude of the output bias voltage swing is determined by the control bias voltage applied to transistor M3, as shown in Figure 5.17.

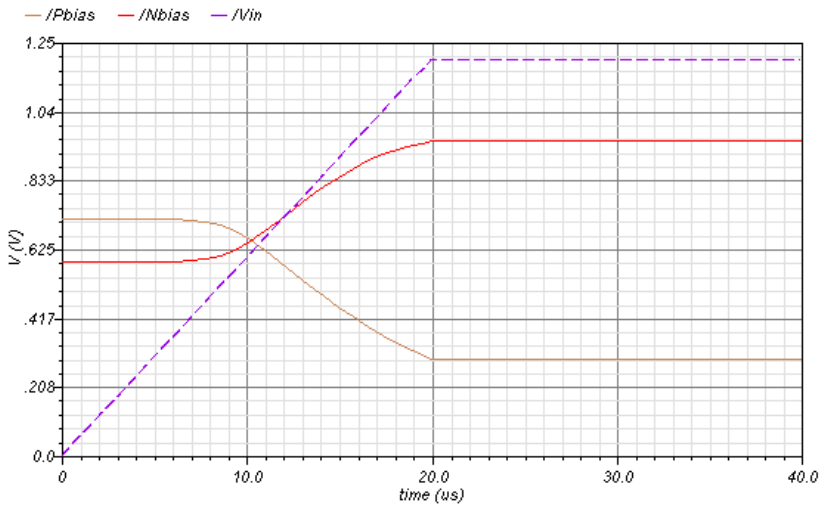


Figure 5.17: The output magnitude of V_{bias}-*Pos* (Pbias) and V_{bias}-*Neg* (Nbias) of the control bias with input control bias voltage (Vin).

The outputs of the bias control block are connected to the inverter bias transistors M7 and M10 of the current starved inverter stages, as shown in Figure 5.18. This circuit configuration enables an adjustment to the drive current available to the inverter chain. Therefore, a precisely controlled oscillation frequency can be achieved by controlling the sink and source current of each inverter, which acts as fine tuning. Each of the inverter stages consist of six transistors, as can be seen in Figure 5.18.

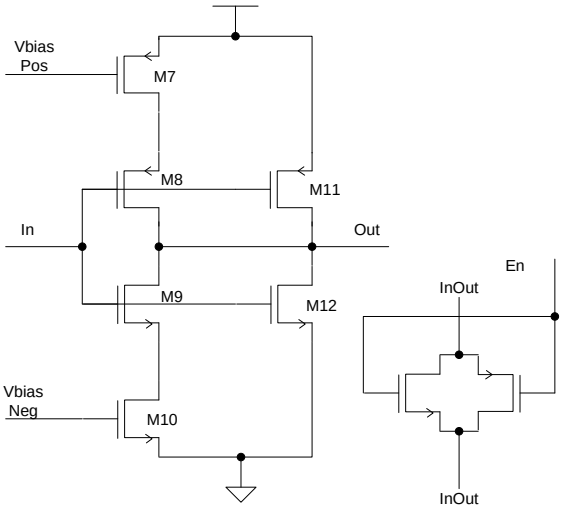


Figure 5.18: Current-Starved VCO Inverter and Transmission Stage Schematic.

The current controlled inverter comprising the four transistors, M7 trough to M10, and a conventional inverter are connected in parallel, so that the VCO oscillation frequency can be sufficiently tuned without sacrificing the inverter driving capability. The transistor size optimisation of the inverter circuit is straight forward, with PMOS being twice the width of the NMOS circuit in general.

5.5.3.2 VCO design specifics

Each of the VCO circuit share the same overall topology and exhibit similar design properties within their specific requirements for frequency range. Each of the oscillator stages are designed to oscillate at a central frequency, F_c, or close to the centre of the possible oscillation frequency range, $(F_{min} + F_{max})/2$, when a bias of half V_{dd} ($V_{dd}/2$) is applied to the input bias voltage. This is to ensure that a symmetric range of linear

operational frequencies can be obtained, and to reduce nonlinearity when the operational frequency approaches the corners of the gain characteristic. Figure 5.19 illustrates the importance of F_c in VCO design when using the topology showed in Figure 5.15.

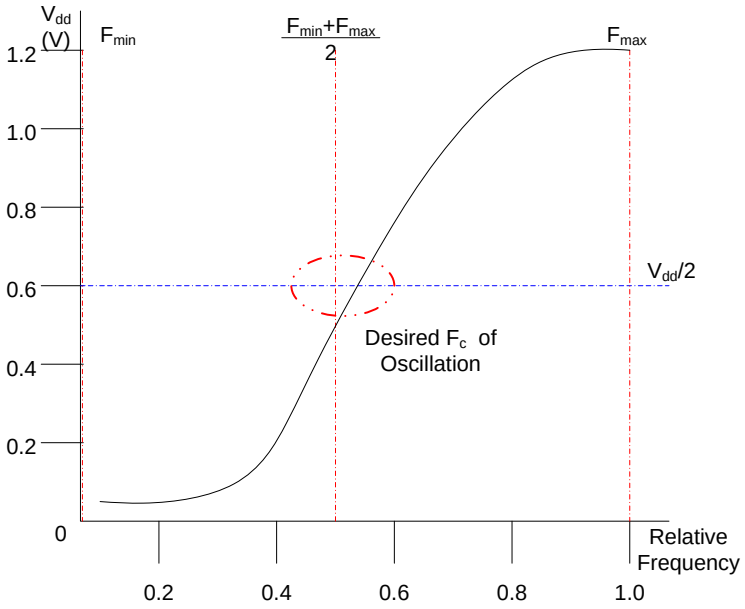


Figure 5.19: Desired oscillator circuit centre frequency performance as compared to the ideal centre frequency from the average of F_{min} and F_{max}.

The oscillation quality of the VCO design can be determined by the relative close proximity of the VCO output transfer function graph with the crossing point of the two ideal characteristic points, half V_{dd} and the $(F_{min} + F_{max})/2$ lines. The VCO transfer function shows that the design is very close to achieving the ideal slope of $(F_{min} + F_{max})/(V_{dd}-V_{th})$. The transfer function curve has its characteristic points, $V_{dd}/2$ and $(F_{min} + F_{max})/2$ close to the ideal crossing point and shows a wide linear range slope, where VCO is very responsive with a near constant slope and where the device saturation is limited to corners. These characteristics demonstrate an excellent fine tuning range of the VCO to a desired oscillating frequency by the bias control, which means from the linear slope shown in Figure 5.19, the voltage to frequency conversion can achieve a high resolution.

5.5.3.3 Transistor parameter sizing

The design equations for the current-starved VCO are derived from the total capacitance of the drains of the *current-starved* path of transistors M8 and M9, combined with driving path of the transistors M11 and M12, as can be seen in Figure 5.20.

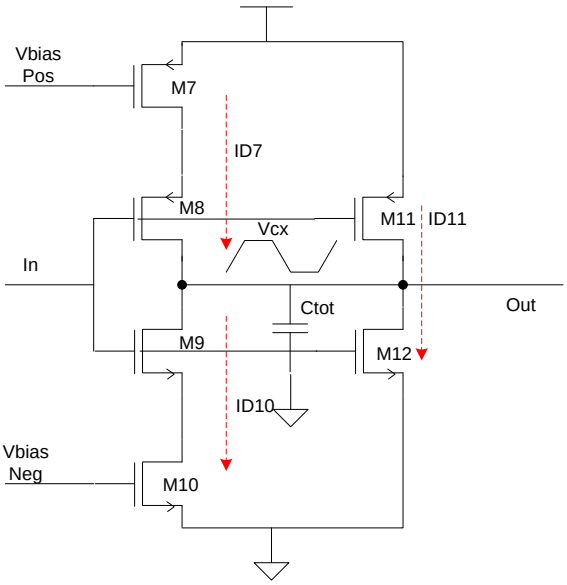


Figure 5.20: The two current paths of the oscillator inverter stage. The current starve paths of ID7 and ID10 and the driving current path of ID11.

The total capacitance of the current limited path is given by

$$C_{tot} = C_{out} + C_{in} = C'_{ox}\left(W_p L_p + W_n L_n\right) + \frac{3}{2} C'_{ox}\left(W_p L_p + W_n L_n\right) \qquad \text{Eq. 5.15}$$

Which comprises the output and input capacitances (C_{out} and C_{in}) of the inverter. The total capacitance equation can be rewritten as

$$C_{tot} = \frac{5}{2} C'_{ox}\left(W_p L_p + W_n L_n\right) \qquad \text{Eq. 5.16}$$

The time required to charge up the capacitance from zero to V_{cx}, with constant current I_{D7} is given by

$$t_1 = C_{tot} . \frac{V_{cx}}{I_{D7}} \qquad \text{Eq. 5.17}$$

While the time it takes to discharge from V_{dd} to V_{sp} is given by

$$t_2 = C_{tot}.\frac{V_{dd} - V_{cx}}{I_{D10}} \qquad \text{Eq. 5.18}$$

If the current I_{D7} is set to be equal to I_{D10}, renamed as I_D, then when $V_{control}$ is equal to $V_{dd}/2$, then the sum of t_1 and t_2 is

$$t_1 + t_2 = \frac{C_{tot}.V_{dd}}{I_D} \qquad \text{Eq. 5.19}$$

The oscillation of the *current-starved* inverter, f_{CSosc}, for N odd number of stages is

$$f_{CSosc} = \frac{1}{N\left(t_1 + t_2\right)} = \frac{I_D}{N.C_{tot}.V_{dd}} \qquad \text{Eq. 5.20}$$

The same set equations from Equation 5.15 and Equation 5.16 can be used to approximate the transistor size for the driving inverter stage (M11 and M12). Thus the average oscillation frequency, f_{avrg}, for the whole circuit is given by

$$f_{avrg} = \frac{f_{CSosc} + f_{osc}}{2} \qquad \text{Eq. 5.21}$$

The associated total centre drain current, derived from Equation 5.22, is given by

$$I_{Dcentre} = f_{avrg}.N.\left(2.C_{tot}\right).V_{dd} \qquad \text{Eq. 5.22}$$

The centre drain current can be used to compute the width and length of transistors M8 and M9 or M11 and M12. As shown in Equation 5.23

$$I_{Dcentre} = \frac{\beta}{2}\left(V_{GS} - V_{THN}\right)^2 \qquad \text{Eq. 5.23}$$

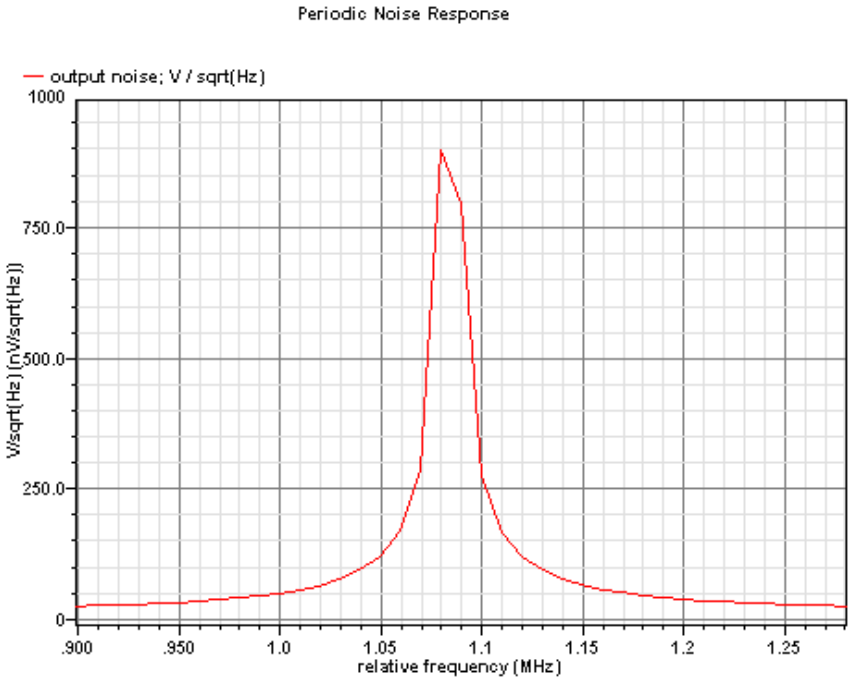


Figure 5.21: VCOs Centre Frequency Response.

The ring oscillator was implemented in 0.13 µm CMOS process by ST-Microelectronics®. A total of 150 ring stages were used to meet the required clock median frequency of 1.1 MHz. The oscillator was designed to operate with 1.2 V power supply with 0.2% voltage variation and to be insensitive to process variations using the bias control circuit.

5.5.4 Phase and Frequency Detector

A phase and frequency detector (PFD) is commonly used in a clock generator circuit as simultaneous phase and frequency acquisition. The PFD circuit used comprised of 5 NAND gates, 2 Set-Reset latches, and 8 inverters designed to have a minimum size to reduce internal current spikes, the circuit is shown in Figure 5.22.

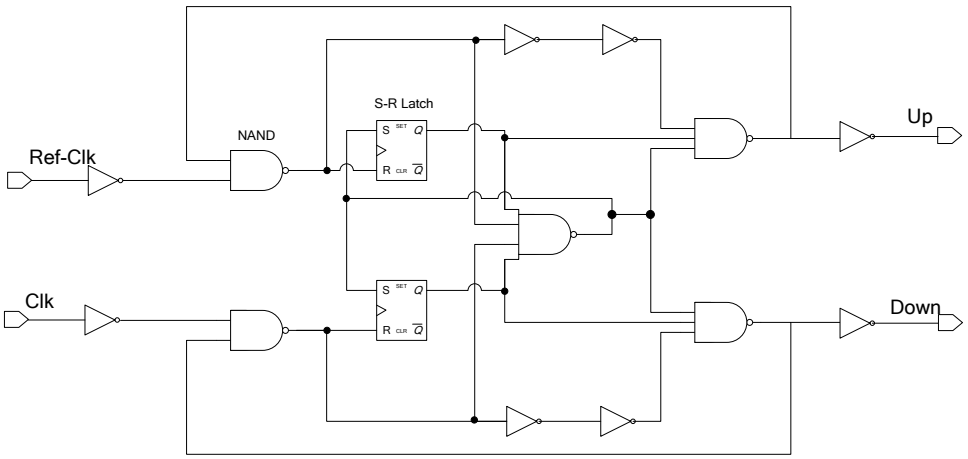


Figure 5.22: Phase and Frequency Detector (PFD) comprises of 5 Nand gates, 8 inverters and 2 latches.

In this DVS design, the PFD monitors the difference between the input reference frequency (Ref-clk) and the input frequency (clk). The PFD generates an up (UP) signals if Ref-Clk leads Clk, and a down (Down) signal if Ref-Clk lags Clk, as shown in Figure 5.23 and 5.24 respectively. In a locked condition, when the frequency into Ref-Clk is equal to Clk, both of the output terminals remain constant, as can be seen in Figure 5.25.

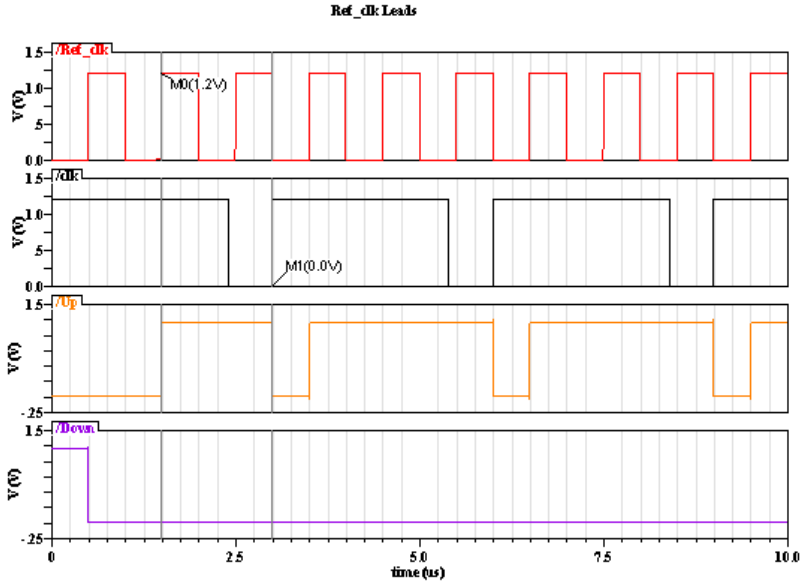


Figure 5.23: The Up signal is generated if the Clk signal lags the Ref_Clk signals. The waveforms shows Ref-Clk signal in the first panel, Clk signal on the second panel, output Up on the third panel and output Down on the last or bottom panel.

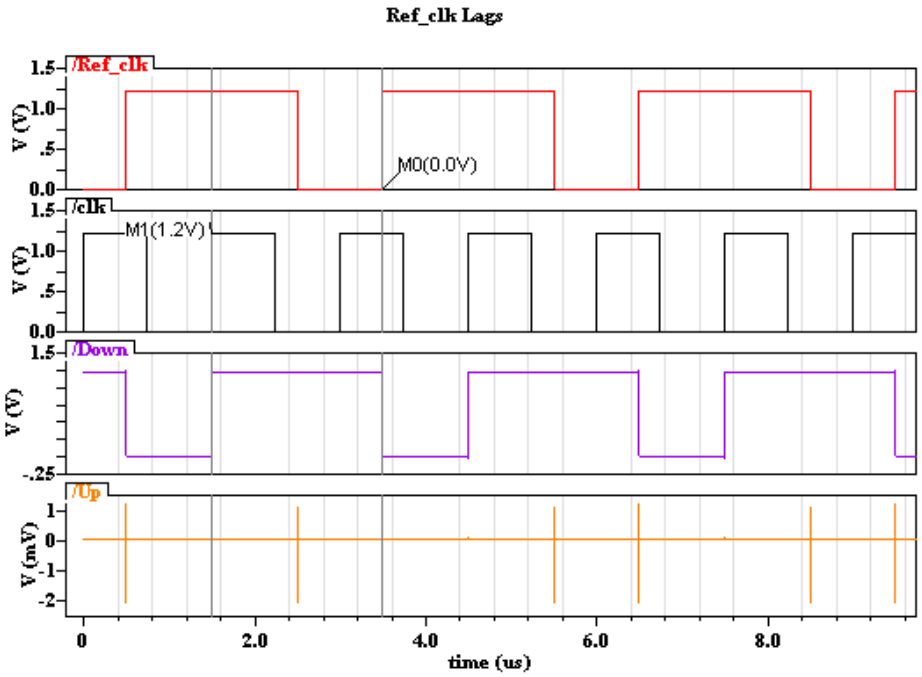


Figure 5.24: The PFD generates Down signals if Clk signal leads the Ref_Clk signal.

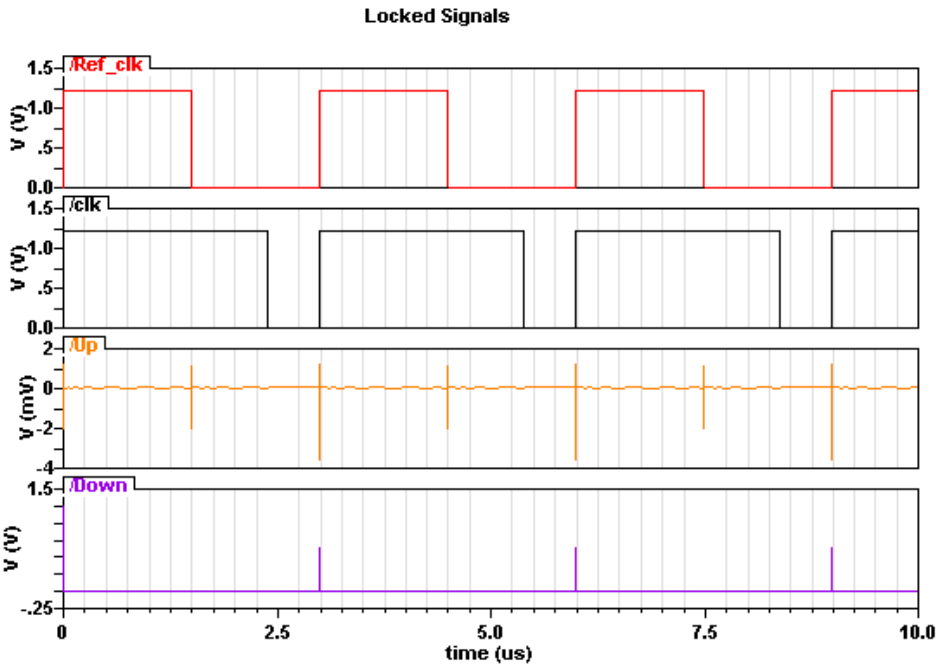


Figure 5.25: The Locked Condition happens when the Clk signal is equal to the Ref_Clk signal.

The operational characteristics of the PFD can be described as:

- A rising edge from the input reference clock and input clock signals must be present when a phase comparison is in progress.
- The width of the input reference clock and the clock pulse is irrelevant.
- The PFD will not lock on a harmonic of the data.
- The Up and Down outputs of the PFD are both logic low when the loop is in lock, eliminating ripple on the output.

The principle of data locking in a PFD circuit can be infered from the phase difference of the two inputs. If the time difference between the rising edge of the input reference clock and the input clock signals is denoted by Δt and the time between successive leading edge of the clock is labelled T_{clk} (or the time difference between the leading edge of the reference clock) then we can write the phase as,

$$\Delta\phi = \frac{\Delta t}{T_{clk}}.2\pi(radians) \qquad \text{Eq. 5.24}$$

The phase difference, $\Delta\phi$, is zero when the loop is in lock. The Zero-zone, or the range when zero difference is detected, occurs when the PFD circuit detects no phase difference when phase error is present. The accuracy of the zero-zone is the most important specification in the PFD design. The circuit zero-lock performance is depicted in Figure 5.26. The output voltage of the PFD is shown in Equation 5.25.

$$V_{PD} = \frac{V_{dd} - 0}{4\pi}.\Delta\phi = K_{PD}.\Delta\phi \qquad \text{Eq. 5.25}$$

Where the gain is,

$$K_{PD} = \frac{V_{dd}}{4\pi}(volts/radians) \qquad \text{Eq. 5.26}$$

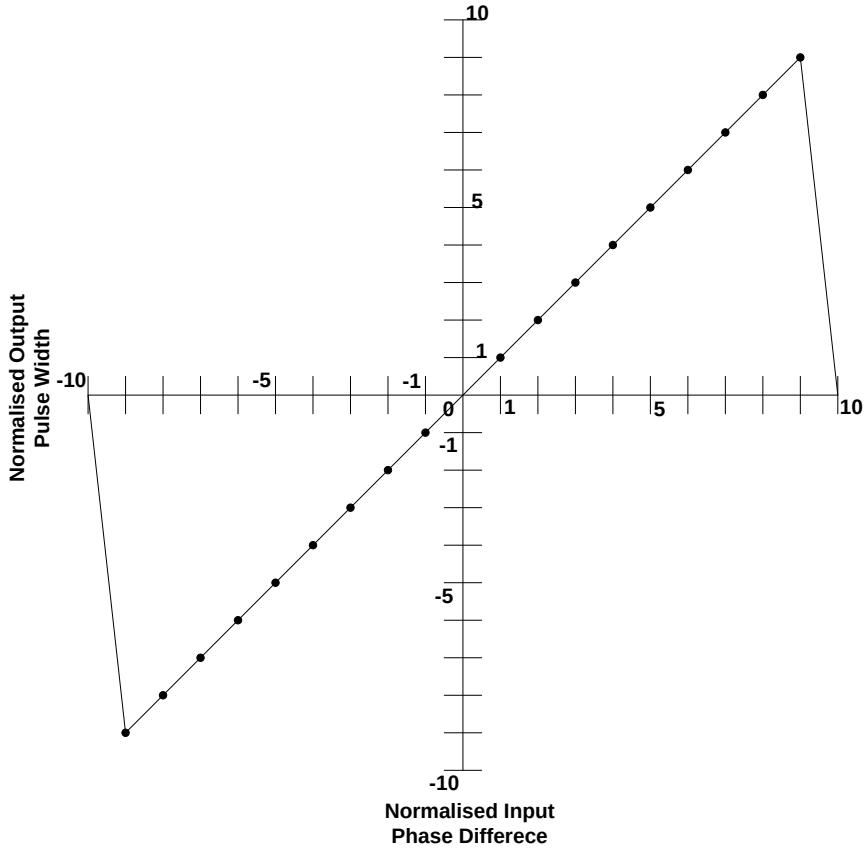


Figure 5.26: The Zero zone transfer characteristics of the PFD from a SpectreS simulation®.

5.5.5 Buck converter

Power supply generation is an important functionality of a DVS system. The primary objective of a DVS is to minimise the system energy consumption by voltage scaling technique. The voltage scaling functionality is achieved by the application of the power supply switching property, as discussed in Chapter 4. The overall buck converter circuit used in this thesis is shown in Figure 5.27.

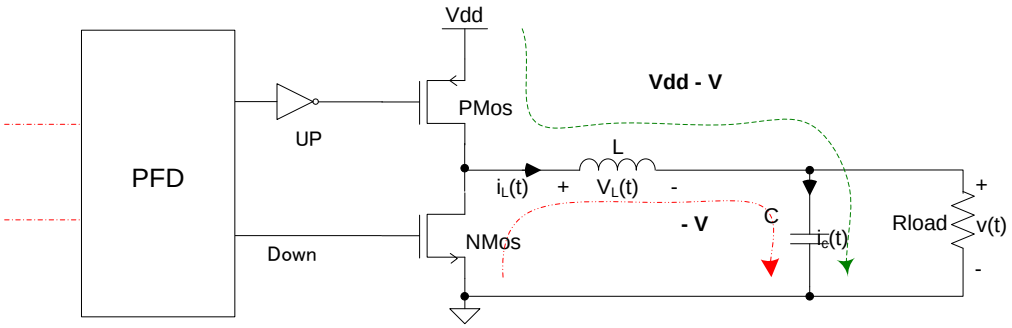


Figure 5.27 The Buck Converter in a DVS system, shown connected to the output of the PFD block. The charging current path (V_{dd}-V) is shown by the green arrow, while the discharging current path (-V) is shown by the red arrow.

5.5.5.1 Buck Converter Design Equations

5.5.5.1.1 Derivations for the Duty Ratio

To determine the duty cycle ratio derivation, the first assumption made was that the converter is in a steady state. In the steady state mode, all the transistor switch components were being treated as ideal, ideal inductor and capacitor with no losses and there are no parasitic resistances considered for the steady state derivation. The green arrow indicated in Figure 5.27, represents the scenario when the PMOS switch conducts the inductor current and the result is a positive voltage (V_{dd} - V) across the inductor in a time frame t_{on} as depicted in Figure 5.28. However, when the NMOS switch is turned on, the current flow is now negative, resulting in a negative voltage (-V) across the inductor, as indicated by the red arrow in Figure 5.27 and depicted in the red time frame, t_{off} in Figure 5.28.

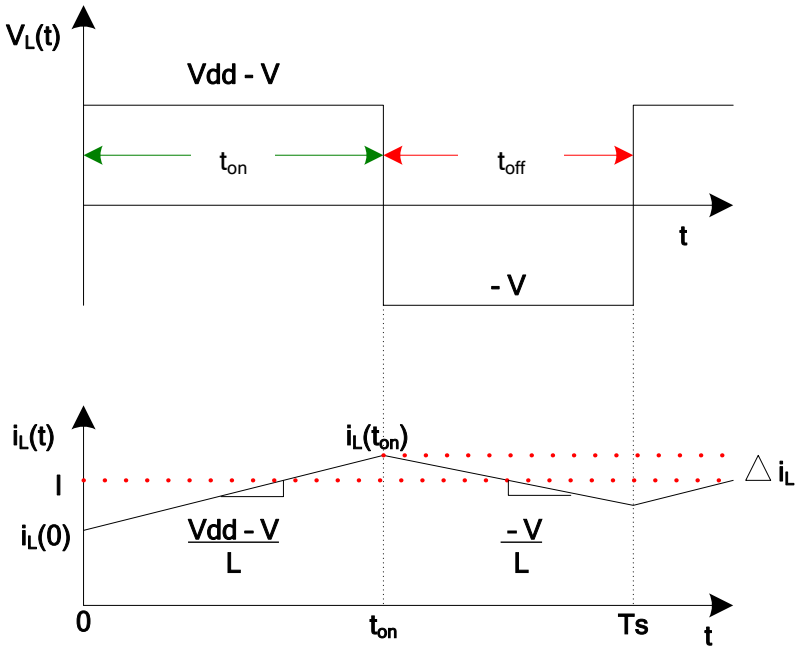


Figure 5.28: Voltage-Current Response of On and Off Pulse Time across the inductor. The inductor voltage (V_L) is shown in the top graph and the inductor current (I_L) is shown in the bottom graph.

In one full cycle of period, *Ts*, the total area during charging can be calculated as; $(V_{dd} - V).t_{on}$ and during discharging period can be calculated as; $(Ts - t_{on}).(-V)$. The total area (λ) of charging and discharging period is shown in Figure 5.29.

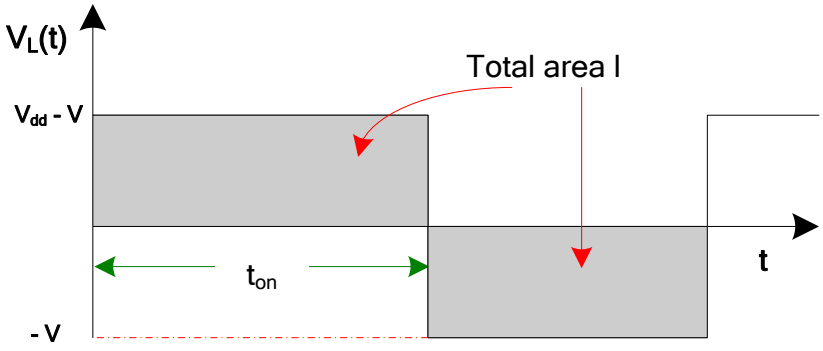


Figure 5.29: Overall On and Off Pulse Area.

Hence, the total area of a duty cycle of the period can be derived as,

$$\frac{1}{T_s}\int_0^{T_s} v_L(t)\,dt = \langle v_L \rangle = 0 \qquad \text{Eq 5.27}$$

The total area (λ) under each rectangle, during t_{on} and t_{off}, is equal in steady state and can by found by taking the integral of the voltage waveform according to each time frame, therefore Equation 5.27 can be written as,

$$\lambda = \int_0^{T_s} v_L(t)\,dt = (V_{dd} - V)(t_{on}) + (-V)(t_{off}) \qquad \text{Eq 5.28}$$

Therefore, the duty cycle ratio calculation can be determined across one period as,

$$(V_{dd} - V).t_{on} = V(Ts - t_{on}) \qquad \text{Eq 5.29}$$

or

$$\frac{V}{V_{dd}} = \frac{t_{on}}{Ts} = D \text{ (duty cycle ratio)} \qquad \text{Eq 5.30}$$

Hence in the steady state, the output voltage varies linearly with the duty cycle ratio of the transistor switch for a given supply voltage.

5.5.5.1.2 Calculation to determine the value of the Inductor

The main function of the inductor within the power supply circuit is to maintain the current flow through the load when there is a variation in the power supply. The inductor acts as a limiter to overcome current overshoot and it acts as a source when the input current falls. In other words, the inductor controls the size of the ripple and maintains a continuous operating mode. A smaller inductor value enables a faster transient response however this also results in larger ripple. This effect is known as conduction loss and to minimise the effect a larger capacitor is required to filter the output voltage ripple. Therefore, careful design steps are required for the two trade-offs.

A simplified differential equation can be formed based on the assumption that the voltage across the load, which is equal to the voltage across the capacitor, is constant in a small ripple approximation.

Therefore, the inductor voltage when the circuit is closed, is shown in Equation 5.31

$$v_L(t) = V_{dd} - v(t) \quad \text{Eq 5.31}$$

can be approximated to

$$v_L \approx V_{dd} - V \quad \text{Eq 5.32}$$

The differential equation for the current through the inductor when charging may then be written as,

$$\frac{di_L(t)}{dt} = \frac{v_L(t)}{L} \approx \frac{V_{dd} - V}{L} \quad \text{Eq 5.33}$$

During the discharging period, i.e. when the circuit is in an open condition, the inductor current flows from the lower side of the NMOS, as depicted as a "red" arrow in Figure 5.27. The inductor voltage $v_L(t)$ during the discharging period is shown in Equation 5.34.

$$v_L(t) = -v(t) \quad \text{Eq 5.34}$$

and using the small ripple approximation, this equation can be rewritten as,

$$v_L(t) \approx -V \quad \text{Eq 5.35}$$

The differential equation for the current through the inductor when discharging may be rewritten as,

$$v_L(t) = L\frac{di_L(t)}{dt} \quad \text{Eq 5.36}$$

or in terms small current approximation as,

$$\frac{di_L(t)}{dt} \approx -\frac{V}{L} \quad \text{Eq 5.37}$$

The inductor current increases linearly to a maximum value while the circuit is in charging mode, therefore Equation 5.33 can be rewritten as follow,

$$i_L(t) = \frac{V_{dd} - V}{L} t_{on} + i_L(0) \quad \text{Eq 5.38}$$

The peak to peak ripple, Δi_L, of the inductor current is defined from its minimum to maximum value. Thus, Equation 5.39 yields the expression for Δi_L as,

$$\Delta i_L = i_L(t) - i_L(0) = \frac{V_{dd} - V}{L} t_{on} \quad \text{Eq 5.39}$$

While $i_L(t)$ is the maximum value of current in the inductor, the inductor current reaches minimum value at $i_L(0)$. Therefore, the inductor current reaches a minimum value in the discharging stage as described by,

$$i_L(0) = -\frac{V}{L} t_{off} + i_L(t) \quad \text{Eq 5.40}$$

The Equation 5.41 yields another expression for peak to peak current ripple as,

$$\Delta i_L = i_L(t) - i_L(0) = \frac{V}{L} t_{off} \quad \text{Eq 5.41}$$

The current flow through the inductor, as described in Equation 5.38 and Equation 5.40 (discharging), is depicted in Figure 5.28. From Figure 5.29, it can be seen that the average current in the inductor must be equal to the DC current that goes through the load. The relationship is described in Equation 5.42, where *R* is the load resistance connected to the buck converter.

$$i_L(avrg) = i_{out} = \frac{V}{R} \quad \text{Eq 5.42}$$

Thus, the expression for minimum and maximum current flows through the inductor can now be expressed as,

$$i_L(t) = i_L(avrg) + \frac{\Delta i_L}{2} = \frac{V}{R} + \frac{V}{2L} t_{off} \quad \text{Eq 5.43}$$

$$i_L(0) = i_L(avrg) - \frac{\Delta i_L}{2} = \frac{V}{R} - \frac{V}{2L} t_{off} \quad \text{Eq 5.44}$$

5.5.5.1.3 Calculation to determine the value of the Capacitor

In the buck converter, the capacitor fulfils the role of filtering out the harmonic currents from the load. The output capacitance is required to minimise the output voltage overshoot and ripple in a step down converter. Insufficient capacitance results in high overshoots whilst lack of capacitance with a high internal resistance (equivalent-series resistance - ESR), in the capacitor creates an under charge effect. Therefore, a careful design for output capacitor with enough capacitance and low ESR is required to meet the ripple specification for a step down converter.

The simplified functional description of the capacitor in a buck converter can be understood when the circuit is in a steady state mode. The magnitude of the current flowing into a capacitor at any time is described as,

$$i_c(t) = C\frac{dv_c(t)}{dt} \qquad \text{Eq 5.45}$$

By integrating Equation 5.45 for one complete switching period (T_s), the voltage measured during the charging and discharging period is shown in Equation 5.46.

$$v_c(T_s) - v_c(0) = \frac{1}{C}\int_0^{T_s} i_c(t)\,dt \qquad \text{Eq 5.46}$$

Therefore, in the steady state period, the net change in the capacitor voltage for a full switching period has to be zero, as shown in Equation 5.47.

$$\frac{1}{T_s}\int_0^{T_s} i_c(t)\,dt = \langle i_c \rangle = 0 \qquad \text{Eq 5.47}$$

However, in the actual buck converter design, the size of ripple in the output voltage needs to be accounted for. The first assumption is that all of the ripple components present in the inductor current, i_L, also flow through the capacitor.

$$\Delta V = \frac{\Delta Q}{C} = \frac{1}{C}\frac{1}{2}\frac{\Delta i_L}{2}\frac{T_s}{2} \qquad \text{Eq 5.48}$$

By substituting the change of inductor current, Δi_L, during the discharging period described in Equation 5.41 into Equation 5.48, the difference in output voltage can be described by,

$$\Delta V = \frac{T_s}{8C}\frac{V}{L}(t_{off}) = \frac{T_s}{8C}\frac{V}{L}(T_s - t_{on}) \qquad \text{Eq 5.49}$$

The comparison of the change of output voltage to the actual output voltage describes the ratio of the output ripple voltage, which can be minimised by choosing a corner frequency, f_c, of the low pass filter at the output, such that $f_c << f_s$, as shown in Equation 5.50.

$$\frac{\Delta V}{V} = \frac{1}{8}\frac{T_s^2}{LC}(1-D) = \frac{\pi^2}{2}\left(\frac{f_c}{f_s}\right)^2(1-D) \qquad \text{Eq 5.50}$$

Where the switching frequency, f_s, and the corner frequency, f_c, are described as,

$$f_s = \frac{1}{T_s}, f_c = \frac{1}{2\pi\sqrt{LC}} \quad \text{Eq 5.51}$$

The analyses shown above assume that ideal components are used in the buck converter. The equations are used to estimate initial values for the components. The equations were then applied in MATLAB®, to optimise values for inductor and capacitor used in the buck converter. The Bode diagram of the buck converter using a cut-off frequency of 500 KHz inculding 1% of ripple in frequency can be seen in Figure 5.30. The MATLAB® program produced a total LC value of $8.333\times10^{-12}\,\Omega$, which determine the inductance value, *L*, of 4.1667 µH and capacitance value, *C*, of 2 µF.

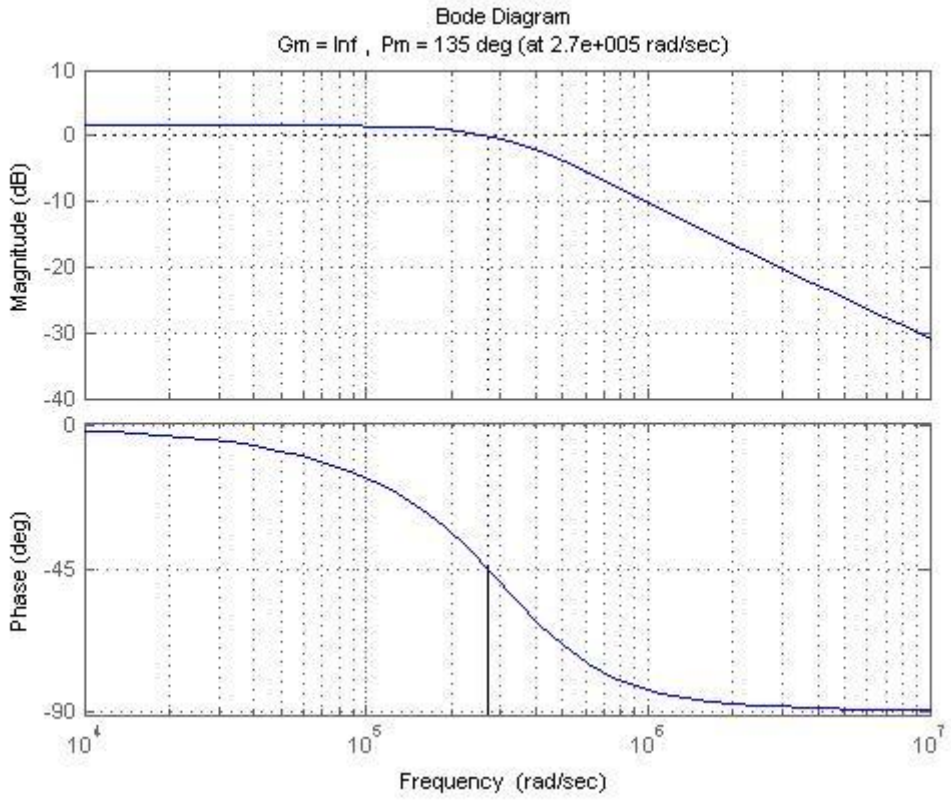


Figure 5.30: Gain Magnitude and Phase Margin Bode Diagram of the Designed Buck Converter.

The Bode plot of the transfer function for the buck converter shows a fixed gain and a minimal phase shift at low frequencies. The gain begins to fall with a slope of 21 dB/decade whilst phase tends toward -90 deg beyond the resonant frequency

($\omega = \sqrt{1/LC}$) of the LC output filter. The ideal Bode plot would show a gain that rolls off at a slope of -20 dB/decade, crossing 0 dB at the desired bandwidth and a phase margin greater than 45 deg for all frequencies below the 0 dB crossing. [12]

5.6 Conclusion

This chapter discussed the design techniques and various circuit implementations for the dynamic voltage scaling scheme. The concept of dynamically scaling the supply voltage to realise the speed versus power trade-off for systems with variable throughput requirements were also discussed. The best strategy for lowering power dissipation is to dynamically adjust the supply voltage as the workload varies with time. The main objective of dynamic voltage scaling is to provide the required maximum throughput when the system workload is high while saving energy during other times by adequately reducing the supply voltage and operating speed of the circuit. The design equations and main characteristics of each module have been discussed in detail. Chapter 6 discusses the energy profiling techniques to be used in static power reduction. Chapter 7 discusses the detailed design and implementation of threshold scaling scheme to reduce static power dissipation.

Chapter Six:

Energy Profiling in Power Management

6.1 Introduction

This chapter describes the design specifications and energy profiling techniques for portable biomedical devices in the strong inversion and weak inversion (subthreshold) regions. Transistor operations in the strong inversion region have been the primary working region for CMOS transistors. Therefore, supply and threshold voltage scaling in the strong inversion region has been extensively studied. In the literature, different metrics are used to study supply and threshold voltage scaling such as energy, delay, power, energy-delay product (EDP), and power-delay product (PDP) [72, 73].

Lowering the supply voltage to the CMOS transistors degrades the speed of the operation due to a reduced transistor current. Therefore, EDP and PDP are more commonly used for measuring the effectiveness of energy saving against delay. In this work, the two metrics of energy and delay performance are focused on, for low power biomedical circuits using a 0.13 μm process [74]. A simple ring oscillator circuit is used to simulate energy dissipation and performance in the operating region of a power supply, between 100 mV to 1 V, whilst varying the threshold voltage. The circuit also enables analysis of the energy dissipation for a variable activity factor. The optimal operating point results in minimum energy dissipation having considered a trade-off between energy and performance. A discussion of the implemented FFT system as a prototype system is also described in this chapter.

6.2 Energy-performance curve for optimal V_{dd} - V_t operation

Exploring the energy usage and delay performance for a wide range of voltage supply (V_{dd}) and for threshold voltage (V_t) provides an understanding into the trade-off between low power and high performance. Threshold voltage reduction for a fixed supply voltage enhances the circuit speed by increasing the transistor's gate overdrive, or in other words realising a reduction in V_{gs}-V_t. The application of threshold voltage reduction together with supply voltage scaling allows overall power reduction without a reduction in the circuit speed.

The energy usage and performance simulations of various activity factors of the circuit for a 0.13 μm process permits an estimate of the optimal V_{dd} and V_t scaling. The ring oscillator circuit under test shows the limits of supply voltage scaling and the benefits of threshold voltage scaling. The ring oscillator circuit used for simulating the various activity factors was shown schematically in Figure 5.15.

The main performance characteristic of the ring oscillator simulated was frequency response. The cascaded inverter stages of the ring oscillator with various depths, were chosen to simulate the delay. The variable activity factor was simulated by enabling or disabling the additional delay chains which were driven by the ring oscillator at the same frequency. The delay chains were enabled or disabled using the selector inputs. When all of the chains are activated the activity factor is 1, since all nodes in the ring oscillator switch once during the clock period. The activity factor (α) is described in Equation 6.1.

$$\alpha = \frac{n(N)}{N} \qquad \text{Eq 6.1}$$

The equation describes the relationship of the total number of nodes switching from low to high, *n(N)*, and the total number of nodes *(N)*. The ring oscillator is a practical way to emulate the variable activity factor of logic gates due to the switching activities of the cells. As expected from the leakage theorem described in Chapter 3, the

switching energy decreases while the leakage current increases when the activity factor decreases.

The simulations of various activity factors for the ring oscillator circuit were modelled using ST-Microelectronics® BSIM3 0.13 μm process. The voltage supply was varied from 0 to 1.2 V and the threshold voltage was varied from 0 to 0.8 V by sweeping the model's threshold voltage parameter, V_{TH0}.

The energy profile in Figure 6.1, shows constant energy curve when α = 1, with minimum energy point at V_{dd} = 1.1 V, and V_t = 340 mV. At the minimum energy point the ring oscillator frequency was 100 KHz. The outer energy curves outside this point indicate higher energy dissipation, with the increased energy magnitude stated on the label.

The energy profile shown in Figure 6.1 demonstrates the relationship between the dynamic and static energy dissipated by the circuit in terms of variations in V_{dd} and V_t. As expected by the energy equation derived in Chapter 2, the switching energy decreases in a quadratic manner until the switching frequency is low enough for the leakage energy to accumulate and increases above the switching energy. The increase in the leakage energy results in a total energy boost in the subthreshold region. However, for a fixed supply voltage, both the energy and the clock frequency of the circuit increase whilst the threshold voltage decreases. This result is due to a reduction in the delay as the threshold voltage decreases, which results in the exponential dependence of subthreshold leakage current to the threshold voltage. As expected, in the region where the threshold voltage is higher than the supply voltage, $V_t >> V_{dd}$, the large leakage energy causes an increase in total energy dissipation usage. Therefore, from the relationship between the two variables of V_{dd} and V_t to energy dissipation, one can allocate an optimal threshold voltage and supply voltage combination that will minimize the total energy dissipation.

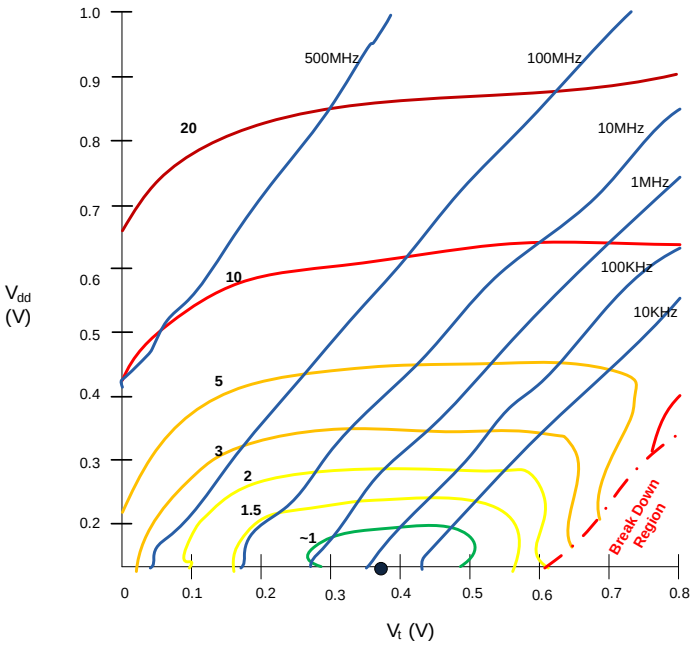


Figure 6.1: Energy-Performance Profile of the Ring Oscillator Circuit with activity factor of one ($\alpha = 1$). The stable operating frequencies are indicated by the straight lines and the curves represent the normalised energy dissipated by the oscillator. The red dot represents the optimum operating point of the circuit.

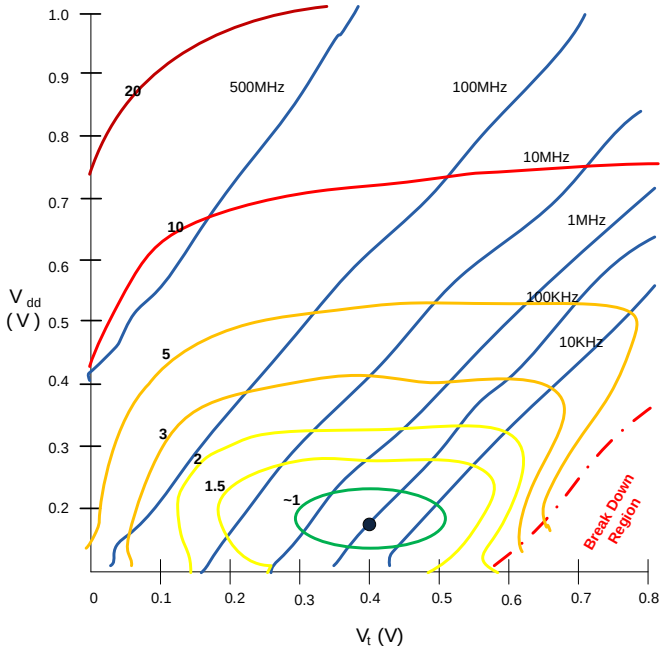


Figure 6.2: Energy-Performance Profile of the Ring Oscillator Circuit with half activity factor ($\alpha = 0.5$).

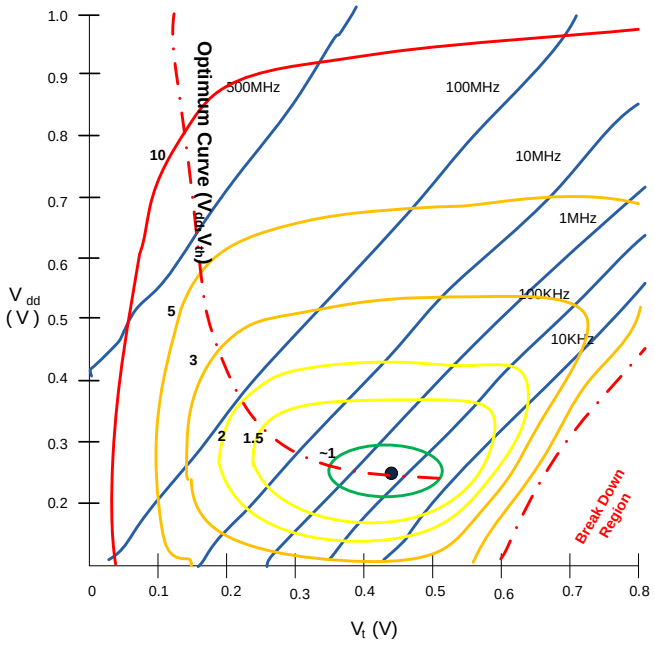


Figure 6.3: Energy-Performance Profile of the Ring Oscillator Circuit with an activity factor of 0.1 ($\alpha = 0.1$) with the Optimal V_{dd} and V_t points.

By using the energy profile figures, the optimal operating frequency of the application can be determined. For applications with frequency performance of 10 MHz and less, the circuit would dissipate minimum energy in the subthreshold region, while for an operating frequency of above 10 MHz minimum energy dissipation will occur in the $V_{dd} > V_t$ region operation.

The optimal V_{dd} and V_t points occur when the performance profile first intersect the energy contour. These are the operating points which give the minimum energy dissipation for a particular clock frequency. The optimal point of operation for this circuit is given by the dashed line in Figure 6.3.

The optimal operating points for a given performance curve enables an understanding of the limits and advantages of scaling the supply and threshold voltages. However, there is a lower limit for the frequency given by the curves, for example, scaling the clock frequency below 110 KHz is not advisable because of the increasing energy dissipation due to leakage current.

The optimal operating points may be extrapolated to a larger system, such as the FFT, to predict the power outcome. The activity factor of the system determines the ratio of the active energy to the leakage energy. By estimating the activity factor of the larger system, one would be able to approximate the energy performance profile for that system by scaling up from the simpler system. This method was used to determine the energy-performance profile of an FFT system to find the optimal supply and threshold voltages that result in the minimum energy dissipation.

6.3 Fast Fourier Transform

The development of FFT algorithms is well established and it is not the intention of the author to fully describe either the development or all of the nomenclature required to understand them. Rather the reader is encouraged to refer to standard text [75].
Fast Fourier Transform is an effective algorithm in processing the Discrete Fourier Transform (DFT). A general N-point DFT is defined by Equation 6.1 [75],

$$X(k) = \sum_{n=0}^{N-1} x(n) W_N^{nk}, \text{ k=0...N-1} \qquad \text{Eq 6.1}$$

where $x(n)$is the DFT sequence and both $x(n)$ and $X(k)$are complex numbers. The coefficient or twiddle factor W_N^{nk}, may be represented as

$$W_N^{nk} = e^{-j\left(\frac{2\pi nk}{N}\right)} = \cos\left(\frac{2\pi nk}{N}\right) - j\sin\left(\frac{2\pi nk}{N}\right) \qquad \text{Eq 6.2}$$

The twiddle factor used to divide the DFT into successively smaller DFTs by using the periodical characteristics of the complex exponential. It is used within the FFT algorithm to increase the computational efficiency. The decomposition of splitting the DFT input sequence $x(n)$ into smaller sub-sequences is called decimation in time (DIT). Inversely, decomposing the output sequence $X(k)$ is called decimation in frequency (DIF).

The basic calculations in FFT are the multiplication of two complex input data with the FFT coefficient W_N^{nk} , at each datapath stage, followed by their summation or subtraction with the associated data, as depicted in Figure 6.4 [75].

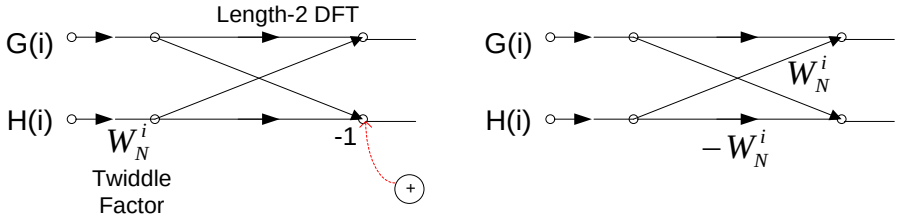


Figure 6.4: Radix 3 DIT Equivalent Butterfly Unit Operation.

The calculation complexity is specified by the $O(N^2)$number of multiplication and $N(N-1)$ number of additions required to perform the transformation. The computational complexity can be reduced to $O(N \log N)$, if the FFT algorithm is applied, as shown in Figure 6.5.

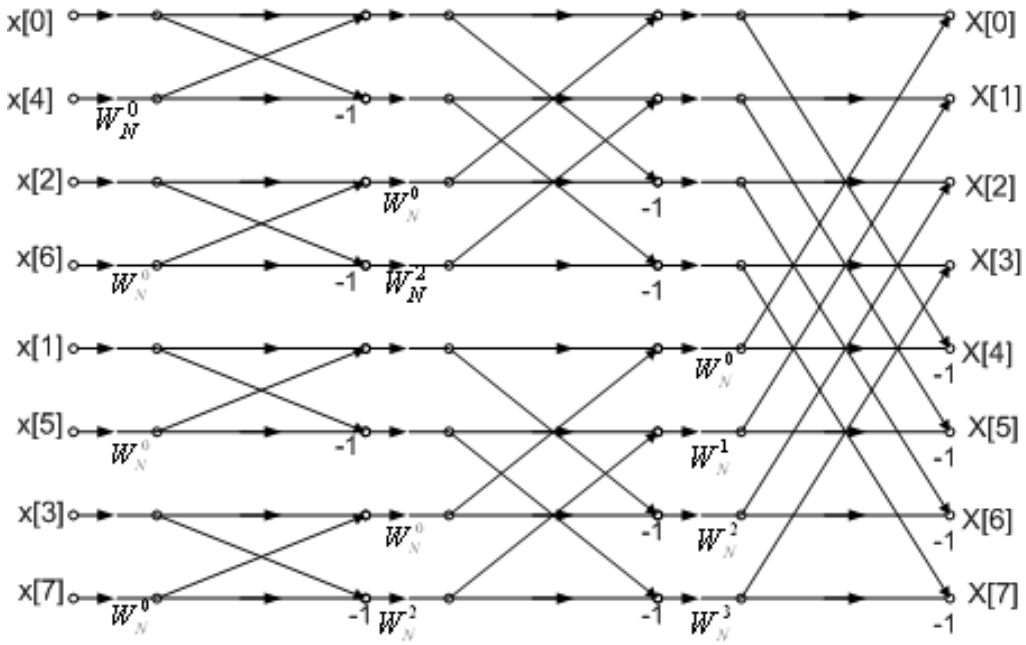


Figure 6.5: N-Point DIT FFT data flow multiplication of the butterfly unit

The number of sampling points required for the calculation is specified by the power of the number of butterfly radix-r in the FFT algorithm. Although, a radix-2 algorithm could cover most of the possible sampling points required, the radix-2 algorithm requires more computation cycles than, for example, radix-4. Contrarily, radix-4 could not handle other sampling points which are not powers of four, such as 128, 512, etc. Therefore, a mixed radix (MR) algorithm that uses both radix-2 and radix-4 to solve FFT which are not powers of four could be used [76]. Generally, N-points of FFT computation requires $(N/r)\times \log_r N$ radix-r butterfly computation. Regardless, the computation could be done by a butterfly unit on each stage (pipelined) or a single recursive butterfly unit (shared memory) depending on the application requirements.

6.3.1 FFT Processor Architectures

Numerous FFT processor architectures have been developed based on a Cooley-Turkey algorithm for different applications. Pipeline architecture, for example, is widely used in high throughput applications [77]. However, the disadvantage of this architecture is the relatively large silicon area required, due to log_rN process elements, where N represents the FFT length and r represents its radix, which are required by pipelined architecture.

A different FFT architecture is the shared memory architecture [78]. The advantages of shared memory architectures are that they are area-efficient and have lower overall power consumption. However, the shared memory architectures cannot achieve high speed operation, due to the fact that more computation cycles are required. The main trade-offs in the FFT processor is hardware overhead and speed requirements.

The low power and low speed characteristics of the shared memory FFT processor architecture make it suitable for a low power application such as in biomedical applications. A FFT algorithm is commonly used in biomedical field such as in data acquisition of biomedical signals [79] , ultrasound image processing [80], heart sound signal monitoring [81] and hearing aid applications [82]. Shared memory FFT

processor architecture generally consists of a Butterfly core datapath, a data storage memory and a twiddle factor look up table, as shown in Figure 6.6.

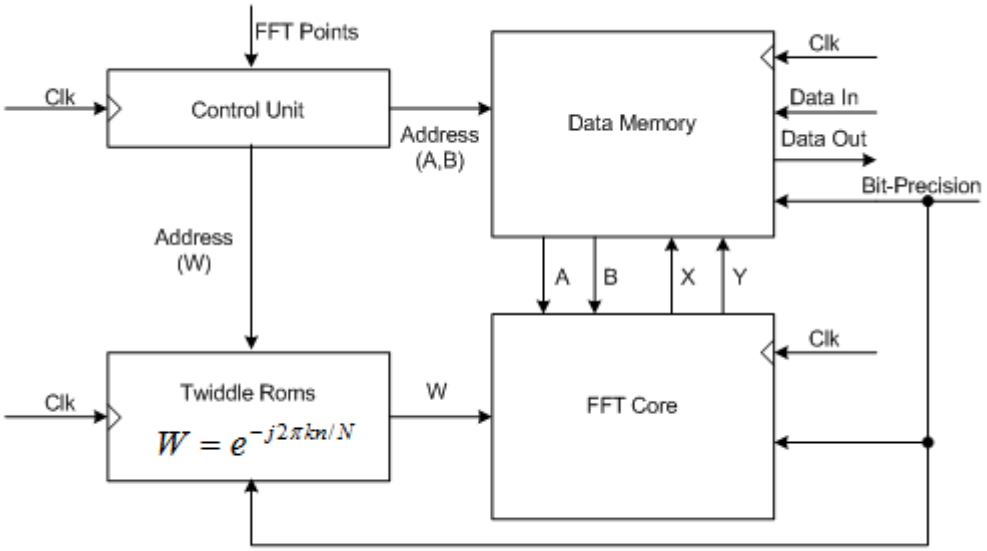


Figure 6.6: The dedicated FFT Processor Architecture used in the thesis.

The main computational core is handled by a Butterfly core radix. Commonly, the computational core in a dedicated FFT processor can range from a single multiplier algorithm logical unit to a high order radix FFT.

6.3.2 Baugh Wooley Multiplier

In this thesis, the FFT core was simulated with the DVS system comprising an 8 bit Baugh Wooley multiplier. A Baugh Wooley Multiplier [83] was used for two's complement multiplication due to its efficiency in handling signed bits. The effectiveness in handling signed bits multiplication makes it a common processing core in FFT processors. Baugh Wooley algorithm was selected for the FFT processor presented in the thesis, due to:

- simplicity, regularity and modularity of the structure, and,
- implementation flexibility on desired length decomposition.

The required function in an FFT butterfly is $X = G(i) + H(i) \times W_N^{nk}$ and $Y = G(i) + H(i) \times W_N^{nk}$, where *G(i), H(i),* and W_N^{nk} are complex inputs, and *X* and *Y* are the complex outputs. This is performed for *log (2N-1)* stages of the N-point real value FFT.

The implementation of the DVS system with a shared memory architecture FFT processor for biomedical application is the main topic in the research. The key characteristic of small area, ultra low power, low throughput whilst maintaining low error rate and efficiency is the challenge in a FFT processor for biomedical applications. Figure 6.7 shows the logic diagram for a 4-bit Baugh Wooley multiplier performing two's complement arithmetic and Figure 6.8 shows the gate level implementation of the multiplier.

$$
\begin{array}{cccccccc}
 & & & A_3 & A_2 & A_1 & A_0 & \text{Multiplicant} \\
 & & & B_3 & B_2 & B_1 & B_0 \times & \text{Multiplier} \\
\hline
 & & & \overline{A_3B_0} & A_2B_0 & A_1B_0 & A_0B_0 & \\
 & & \overline{A_3B_1} & A_2B_1 & A_1B_1 & A_0B_1 & & \\
 & \overline{A_3B_2} & A_2B_2 & A_1B_2 & A_0B_2 & & & \\
A_3B_3 & \overline{A_2B_3} & \overline{A_1B_3} & \overline{A_0B_3} & & & & \\
1 & & & 1 & & & & + \\
\hline
Z_7 & Z_6 & Z_5 & Z_4 & Z_3 & Z_2 & Z_1 & Z_0
\end{array}
$$

Figure 6.7: 4 x 4 bit 2's complement multiplication using the Baugh Wooley Algorithm.

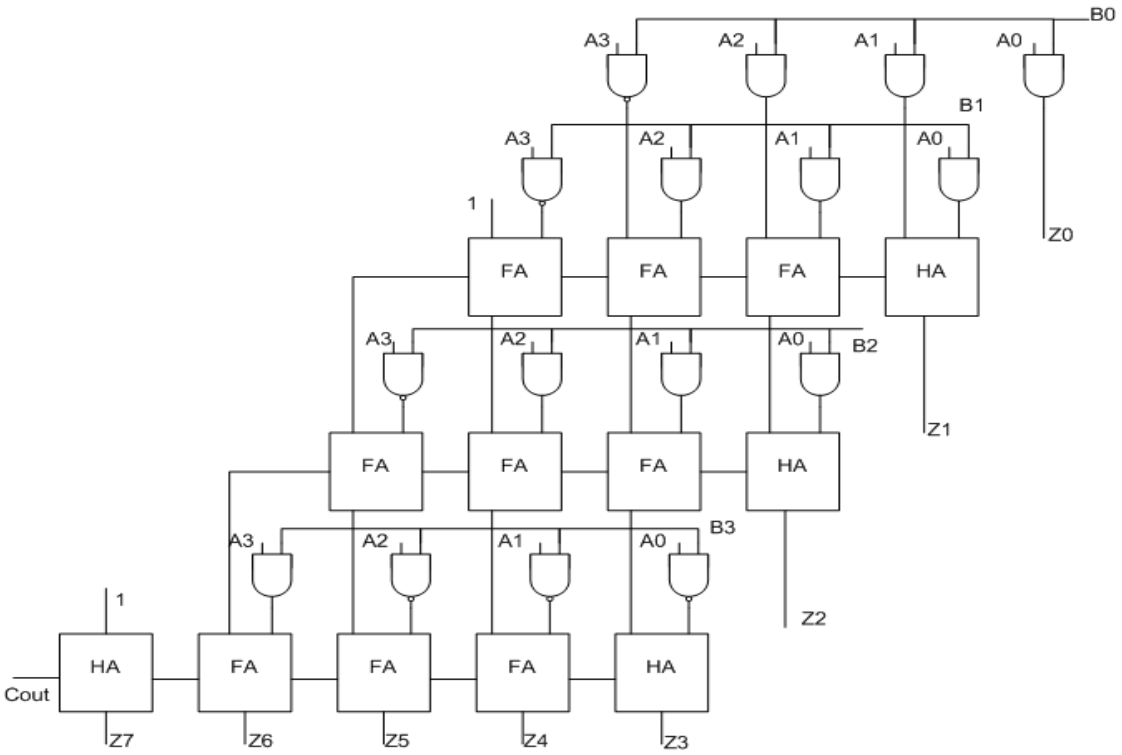


Figure 6.8: Gate level implementation of 4x4 bit Baugh Wooley Multiplier Gates Representation.

Another important component in a shared memory FFT processor architecture is the memory cells. Seventy-five percent of the total power consumption in a FFT processor is associated with memory cell data access and the complex number multiplier operation. It is also understandable that the larger the number of bits in the multipliers or in a long size FFT requires larger word-length for the memory cells. Memory cells require significant chip area with the associated large power consumption. Another aspect that determines power consumption in memory cells is the number of access ports. A single port memory access can be efficient in regard to power dissipation, however it will result in a bottle neck in high speed FFT operation.

6.4 Conclusion

This chapter presented the energy profiling techniques to determine the best operating points for energy efficiency for a maximum and minimum specified supply voltage. It was discussed in Chapter 3 that the best method to overcome an increase in static leakage current, due to the reduction of supply voltage, was to vary the transistor body bias effecting threshold voltage. The operating points were modelled by simulating a simple circuit, in this case a ring oscillator, using various activity factors. The operating points were used for the demonstrated FFT system. One conclusion from the simulations of the operating points conducted, suggest that the performance is suitable for ultra low power biomedical applications.

Chapter Seven:
The Effects of Threshold Scaling and Subthreshold in Low Power Circuit Design

7.1 Introduction

Threshold voltage scaling is used to reduce leakage current, which is becoming more dominant because of technology scaling, with the overall result of reducing the total power dissipation of the system. The application of both threshold voltage scaling together with dynamic voltage scaling provide further speed improvement while maintaining dynamic power consumption to an acceptable level in the CMOS circuit. However, scaling the threshold voltage has been proven to make the circuit more sensitive to noise [84] and threaten the reliable operation of the circuit in deep submicron size circuits [85-87].

It is a common design practice to maintain the circuit operation by introducing a peripheral circuit, or modifications, to reduce coupling noise, charge sharing and subthreshold leakage current. In dynamic circuitry this additional circuit is known as a keeper transistor. The keeper transistor is fully switched on at the beginning of the evaluation or charging phase and will maintain the output to the appropriate discharge output value. The main issue with the keeper transistor is that its application reduces circuit speed and introduces additional power. Therefore, the keeper transistor is typically smaller in size than the rest of the circuit so as to minimise delay. However,

the keeper transistor has to be sized in such way that it's big enough to reduce noise in the circuit. It is apparent that there must be a trade-off between reliability, delay and energy dissipation in the dynamic circuit operation.

This chapter proposes a variable voltage keeper technique which is aimed to simultaneously reduce power dissipation and delay in a clocked dynamic circuit. The threshold voltage of the keeper transistor is modified according to the circuit's activity, thus altering the output current drive. The variable threshold keeper technique has been known to reduce power dissipation by up to 35% compared to standard dynamic circuitry [85, 87, 88]. Moreover, the proposed technique has up to 14% higher noise immunity, with the same power-delay product conditions (PDP) compared to the standard technique [88]. In addition, this chapter discusses the application and integration of subthreshold memory cells in the test system.

7.2 Standard Dynamic Logic Circuits

The clocked dynamic logic circuits used in this thesis are commonly utilised in integrated circuits. This technique offers minimal delay and is generally used to solve a lack of performance in a system's critical path. However, there are issues involved with this technique as technology scales into the submicron. This sub-chapter describes the operational issues and proposed solution for the application of this technique.

7.2.1 General Operation of Dynamic Logic Circuits

A Typical circuit diagram of a dynamic logic circuit is presented in Figure 7.1. The circuit operation starts in the pre-charge phase when the clock signal is low. In this phase, the output node is charged achieving the voltage V_{dd} by the pull-up transistor. The circuit enters the evaluation period when the clock transition is high, and depending on the input combination and logic functionality, the output node is discharged to ground. If the input combination does not produce an answer, i.e. logic

state does not give a result; the keeper transistor is maintained and preserved from noise, charge sharing and leakage current until the next pre-charge phase.

The tail transistor, which is located at the bottom of the pull down network, is a switch in series with the pull down network and helps isolate the operation of the pull down logic transistor into two distinct operational phases. The isolation eases the timing issues that happen between cascaded multi-staged dynamic circuits. In this way, if there are instability occurrences at the input of the pull down logic circuit during pre-charge phase, it will not effect the output node of the circuit as the pull down path to ground is cut-off by the tail transistor.

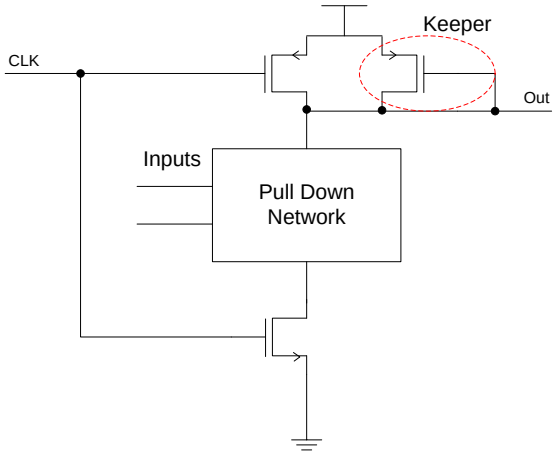


Figure 7.1: A Typical dynamic logic configuration with a keeper circuit.

7.2.2 Design trade-off in dynamic logic circuit

Due to the internal resistance and capacitance of the tail transistor, the transistor is generally sized larger than the pull down network transistors to minimise the speed degradation. However, the larger the size of the tail transistor, the more power will be dissipated since the foot transistor switches in every clock cycle. If the clock signal is managed appropriately, i.e. with an accurate delayed clock signal, the tail transistor can be omitted in the design to reduce power dissipation. The clock signal is delayed from one stage to the next to ensure no short circuit direct current path to ground exists. Although the overall accuracy requirement of the inputs and clock timing signal increases, the overall delay and power requirement of tail-less dynamic logic gates are

enhanced compared to the standard tailed dynamic logic as described by Nowka and Galambos [89]. The combination of the delayed clock signal in the dynamic logic is often called clock-delayed or delayed reset dynamic logic [90].
The trade-off effect of the keeper transistor on noise immunity, delay and power characteristics of the dynamic logic circuits were simulated in this thesis in 0.13 um CMOS technology. The noise margin (NML), which represents noise immunity, is defined as

$$NML = V_{InputLow} - V_{OutputLow} \quad \text{Eq. 7.1}$$

$V_{InputLow}$ is defined as the rate of change of the dynamic output nodal voltage with respect to the change in the input voltage of the voltage transfer characteristic (VTC), and $V_{OutputLow}$ is the output low voltage.

The simulation characteristics of standard two input OR gates are shown in Figure 7.2. The results compare the logic gate in various keeper transistor sizes and without the keeper transistor, while the transistors in the pull down network are sized the same. The results also compare the gate in different input excitation modes to examine the effect on the circuit delay and NML characteristics. The results in group A (the first result in the same keeper size) are based on the assumption that only one input is excited and the other input is either connected to ground or V_{dd}, which is ground for this OR logic gate simulation. The results in group B are simulated from continuous toggling inputs applied to the input signals.

As shown in Figure 7.2, when only one input is applied, while the other is grounded in an OR gate, the addition of a keeper transistor of half the size of the pull down network transistor increases the power and delay by around 15% to 17% respectively as compared to the logic without a keeper transistor. The power, delay and NML characteristics increase by 100%, 97% and 110% respectively as the keeper size increases from 1.3 μm to 2.6 μm. The effect of the keeper current on circuit performance and reliability is reduced when all the input gates are excited with continuous signals. The keeper current effect can be seen when the keeper transistor

size is increased from 1.3 µm to 2.6 µm, with the NML increased only by approximately 19%. The power and delay are increased by 54% and 36% respectively.

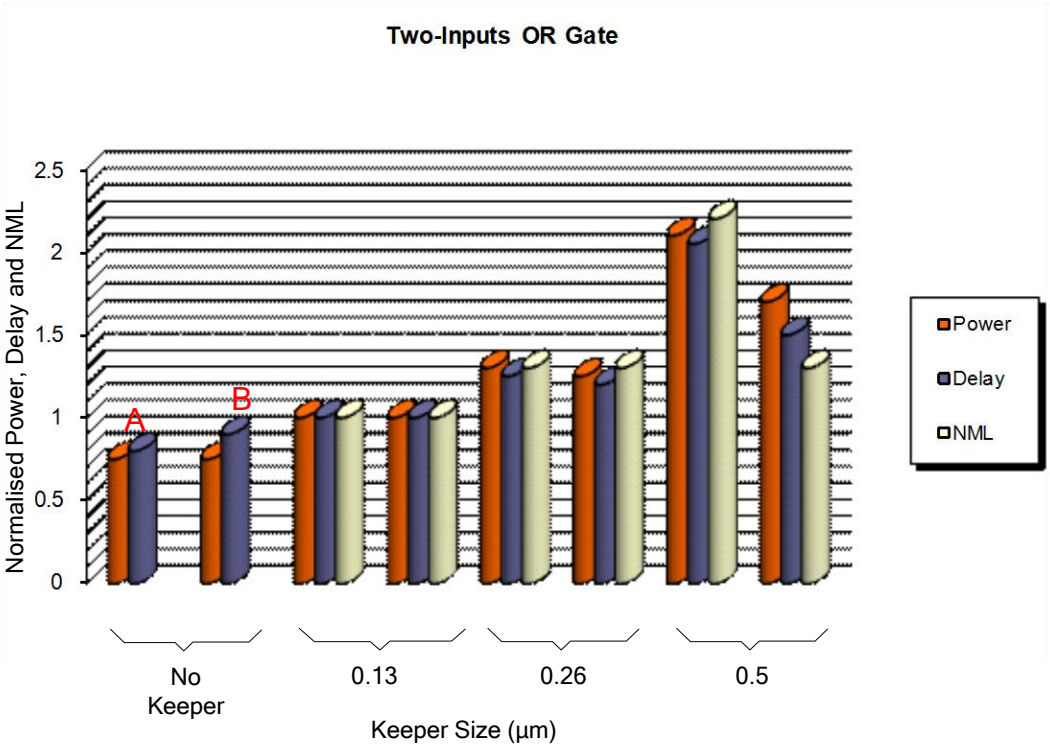


Figure 7.2: Simulation of the effects on power, delay and NML characteristics of a two input OR gate by increasing keeper transistor size of the circuit. Group A: only one input is excited and the other grounded, Group B: all inputs are excited with the same signal.

As illustrated by Figure 7.2, the keeper size should be kept as small as possible in order to enhance circuit performance and energy efficiency. In terms of noise immunity, however, the larger the size of the keeper transistor, the better it performs; this in turn will make sure proper logic functionality is maintained in the worst case scenario of the input. There is therefore an obvious trade-off between noise immunity and delay/energy efficient operation in dynamic logic [84, 91, 92].

There are various techniques to overcome these trade-off issues, one of them is by using two different size of keeper transistor [84] and having the smaller keeper transistor turned-on dependent on the circuit condition. The main drawback of this

approach is the increased area and energy overhead due to the additional keeper transistor compared with the standard keeper method. Another approach uses a similar single keeper transistor as in the standard method, but where the keeper transistor cuts-off at the start of the evaluation phase [85]. This method does not guarantee reliable operation in an increasingly noisy and sensitive chip environment. Both alternative keeper techniques use timing signals that are determined by the worst case evaluation delay. If the worst case delay is underestimated, the keeper can be turned on before the evaluation phase is completed. However, if the delay timing is overestimated, the keeper will be turned off and the circuit will be exposed to noise, therefore degrading circuit's reliability.

This chapter proposes a variable threshold voltage keeper circuit technique to improve noise immunity in dynamic circuits. The threshold voltage of the keeper transistor is modified during circuit operation to reduce the current, however without reducing noise immunity.

7.2.3 Variable Threshold Voltage Keeper

A variable threshold voltage keeper technique on an OR logic gate is shown in Figure 7.3. The technique employs a body bias generator circuit that scales the threshold voltage of the keeper transistor dynamically during the circuit operation. The operational principal of the variable threshold voltage keeper technique may be understood by first considering when the clock is low and the circuit is in the pre-charge phase and the dynamic output is set to V_{dd1}. The substrate of the keeper transistor is set to V_{dd2} by the body bias generator, which means a higher threshold voltage. The amplitude of the high voltage threshold of the keeper is determined by the reverse body bias voltage applied to the source to substrate of the keeper PMOS transistor. At this phase the current delivered by the keeper transistor is lowered due to the high threshold voltage, until the next evaluation phase begins. The current reduction at this phase does not reduce the ability of the circuit to resist noise, as the output voltage is sourced by the pull-up network rather than the logic pull-down network.

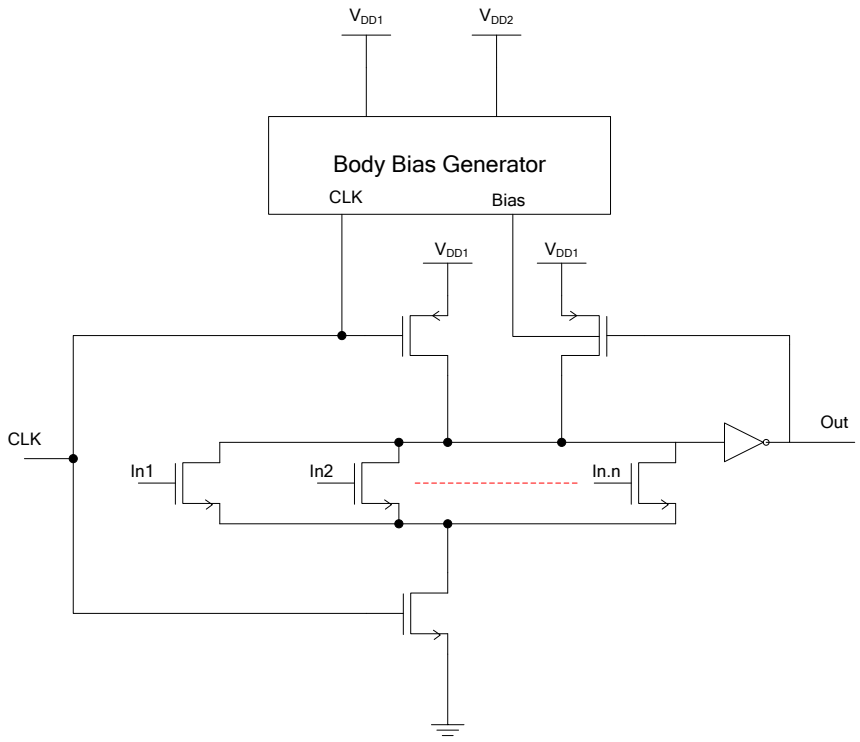


Figure 7.3: An N input dynamic OR logic together with a Body Bias Generator and variable threshold keeper.

In the evaluation phase, or when the clock is high, the pull-up transistor is disconnected and in this phase the keeper transistor is in high threshold mode and prevents the circuit output from noise and charge sharing. Depending on the input combinations that discharge the pull-down network transistor, the high threshold voltage keeper significantly reduces the current dissipation during evaluation phase. During the evaluation phase, the keeper transistor swings down to V_{dd1} according to the time delay estimated by the logic circuit worst case scenario. In this period, the transistor is biased with a low threshold voltage which increases the keeper transistor current source ability. A summary the operational sequence can be seen in Figure 7.4.

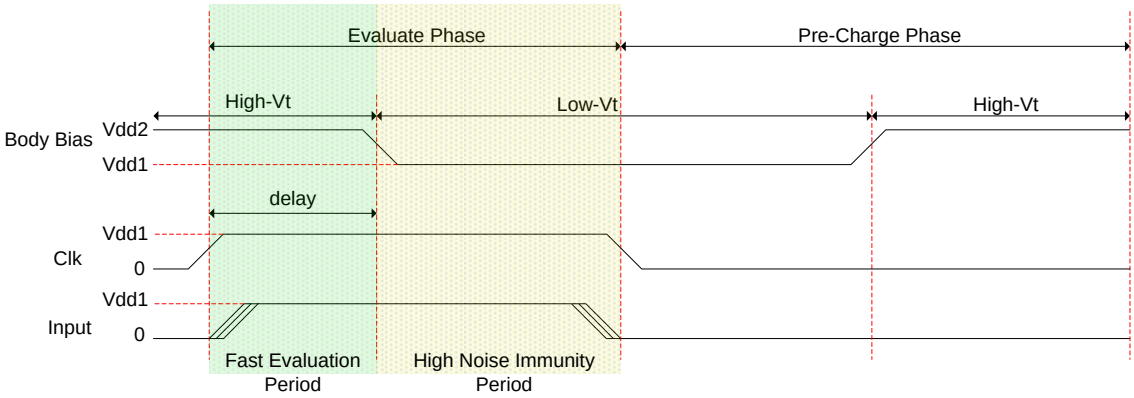


Figure 7.4: Operational waveform sequence of the variable threshold voltage keeper technique. The evaluation and pre-charge phase is separated by the red dashed lines. The High-V_t is shaded in green and Low-V_t in red to differentiate the body bias condition to the keeper.

7.2.4 Dynamic body bias generator

The body bias generator produces an output swing between V_{dd1} and V_{dd2} from a typical input swing from ground to V_{dd1}. The output of the body bias generator is used to adjust the keeper threshold voltage with an appropriate delay. One of the proposed body bias generators is shown in Figure 7.5.

The operation of the body bias generator starts when the clock signal is low and the current through transistors M1 and M4 are cut-off through transistor M5, which will turn on M2 and M3 and the body bias is increased to V_{dd2}. The next cycle starts when the clock signal is high, this will bring the pull down network logic into evaluation phase. During this period M2 and M3 are cut-off turning on M1 and M4, which produces the body bias output to V_{dd1} through M6. The body bias generator must bring the keeper transistor to the low-*Vt* operation level to maintain higher noise immunity. The threshold voltage reduction to V_{dd1} is delayed with a time delay obtained from the worst case scenario simulation, which will increase the keeper transistor current.

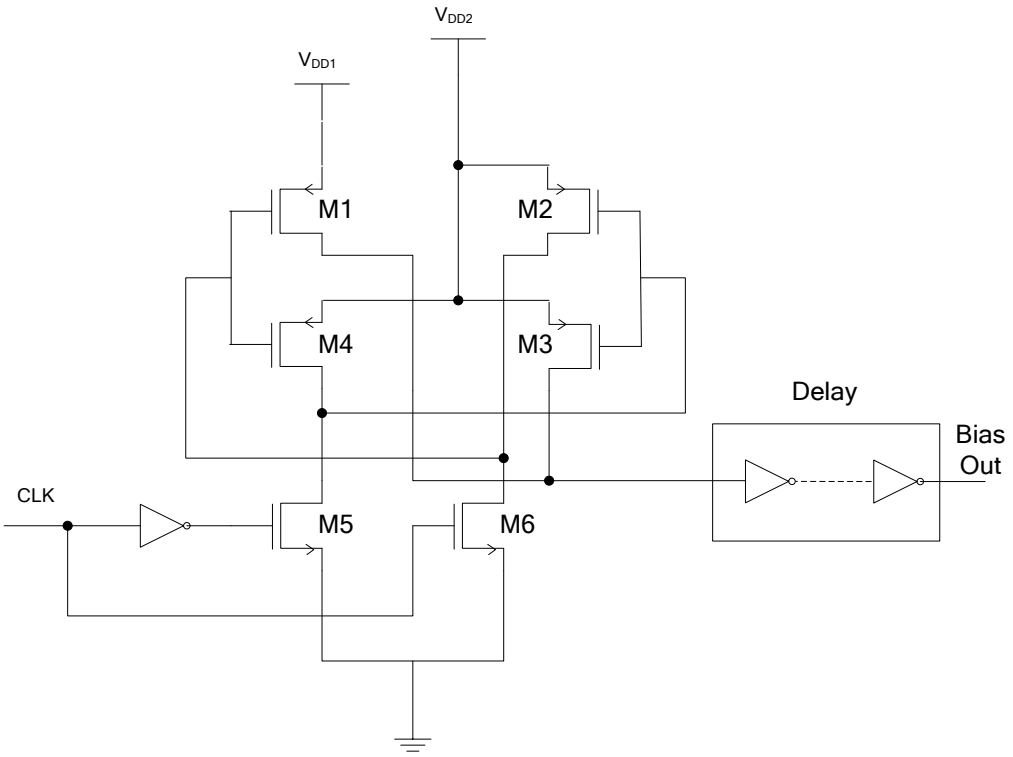


Figure 7.5: Body Bias Generator circuit with the non-inverting worst case delay shown in the box.

The body bias generator assumes two voltage levels, V_{dd1} and V_{dd2}, where $V_{dd1} < V_{dd2}$. The appropriate voltage level for V_{dd2} is determined by target delay and power objectives while satisfying the lowest acceptable noise immunity requirements during the worst case operation of the logic circuit. The threshold voltage trade-offs must be considered to optimise the circuit design in terms of power and delay.

7.2.5 Optimising V_{dd2} for Power Delay Product

As was shown in Figure 7.2, the worst case delay of the logic cells occurs when only one input is excited. This worst case delay scenario determines the logic circuit clock speed which also determines the size of the keeper transistor. The effectiveness of reverse body bias voltage to be applied to the keeper transistor in terms of delay, power, PDP and noise immunity characteristics is simulated by varying the amplitude of V_{dd2} with respect to the body bias generator. The normalised characteristics to the standard dynamic four bit adder logic are shown in Figure 7.6.

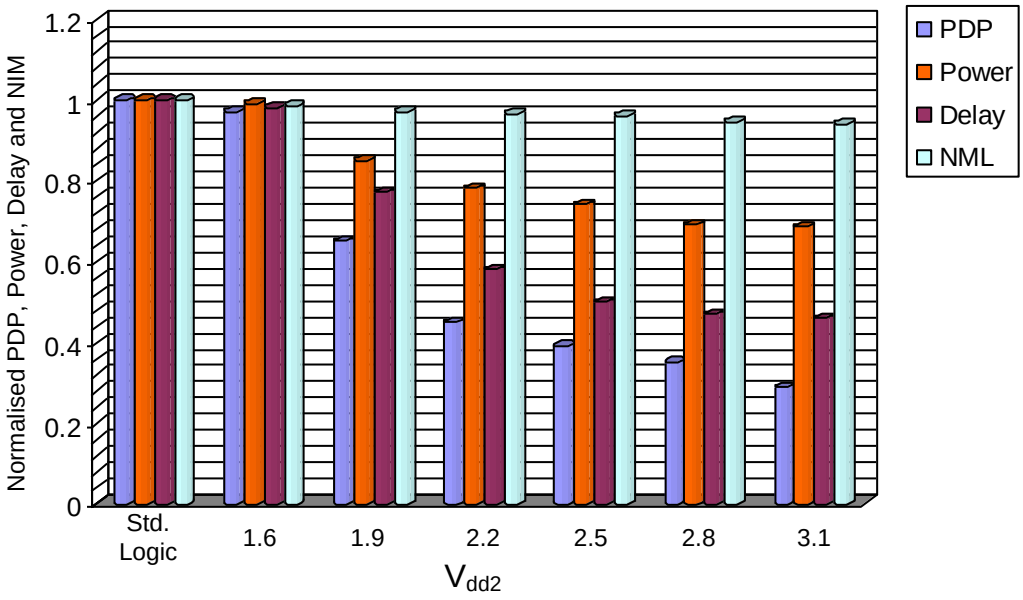


Figure 7.6: The effect of different V_{dd2} amplitude on PDP, power, delay and NML characterisation for the variable threshold keeper technique.

The simulation results show that there is a significant decrease in power dissipation and delay when V_{dd2} is increased. However, this also degrades the noise immunity characteristics of the logic, due to the beginning of the evaluation phase. The reduction of the noise immunity with an increase of 0.3 V in the reverse body bias is around 1.8%. Increasing the reverse body bias to 0.3 V also reduces the system delay to about 3.4% and 0.9% on total power. The delay and power reduction are 58% and 33% respectively, when the V_{dd2} amplitude is changed to 3.1 V.

Simulation results show a significant improvement of the circuit characteristic, therefore it can be concluded that increasing the size of the keeper circuit does improve power dissipation and delay without sacrificing NML as compared to the standard logic cell.

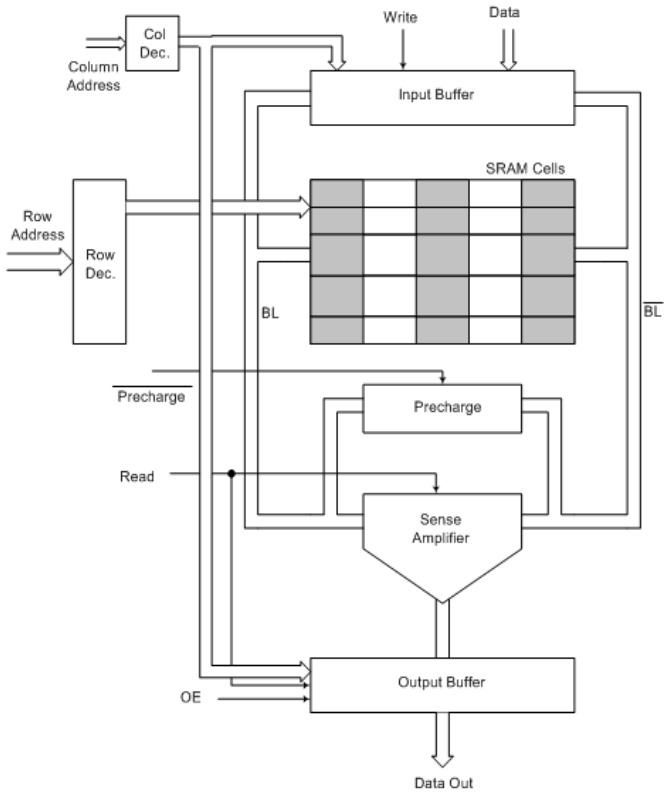
The voltage keeper technique was used in an FFT and Microprocessor test circuit, which incorporate a significant memory size. This requires a low power technique suitable for Static Random Access Memory (SRAM) operation.

7.3 Static Random Access Memory

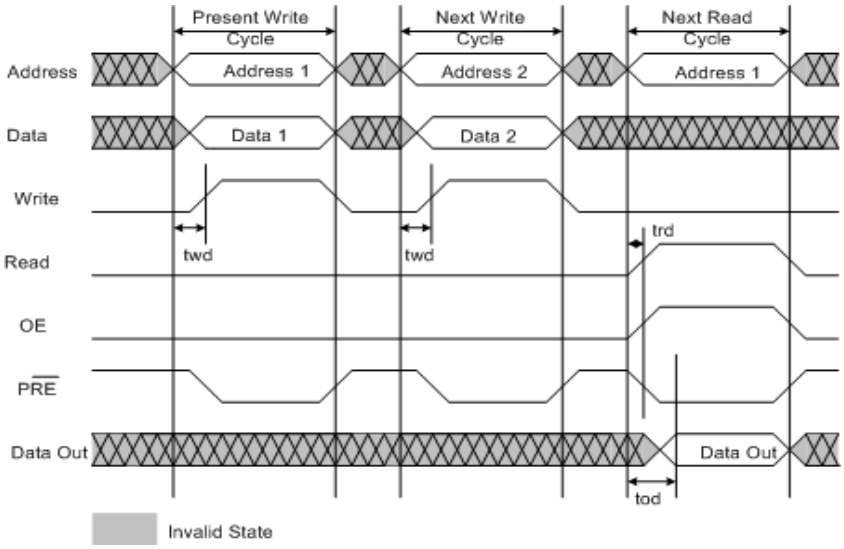
Memory cells have not only reached large-scale integration but also must meet demands for increasing high-speed operation [93]. As transistor sizes are scaling down further into the submicron, the voltage supply level and threshold level have to be reduced to reduce power dissipation. However, the reduction of threshold voltage of a MOS transistor results in an exponential increase the subthreshold leakage current; a slight change of the threshold voltage results in higher delay, as discussed in Chapter 3 and 4. Therefore, a careful choice in the design of the threshold voltage is necessary in memory cell circuit operation.

As can be seen in Figure 7.7a) [94], the conventional SRAM structure consists of: the SRAM core memory cells including column and row address decoders, input buffers for data writing purpose, sense amplifiers for charged data amplification in the core memory cells, a pre-charge circuit and an output buffer to latch the output data during output operation transitions. Read and write operations use the bit lines (BL) and its complement not-bit lines buses ($\overline{BL}$). The typical read and write cycle operations are shown in Figure 7.7b). During the writing cycle a valid address and data must be present before the write signal is activated. The time write delay (*twd*) depends on the address decoders and input buffers circuitry driving capability. *twd* is negligible compared to the complete writing cycle period and depends directly on the circuit topology. As described in the previous section, there is a tradeoff between power and delay, therefore attention in designing the input buffers for low power SRAM, to limit the excess output current, is required for low power SRAM design.

The read cycle mainly involves sense amplifiers, but also requires an appropriate address signal, pre-charge and the latched output buffer. Time read delay (*trd*), also exists between the read signal and the output enable signal. The *trd* mainly depends on the capacitance of the SRAM memory cells. The total capacitance determines the speed of the bit line voltage rise up to a detectable voltage level by the sense amplifiers. Time output delay (*tod*) is the combination of *trd* and the sense amplifiers speed to generate full swing output signals from the selected cell's bit lines



a)



b)

Figure 7.7: a) Conventional SRAM topology which consists of an input buffers, pre-charge and amplifier circuits, output buffers and bit addressing decoder b) Read and Write cycles of SRAM. The waveforms depict the appropriate control signal level.

Achieving a reduction in the subthreshold leakage current is an important consideration in this thesis, specifically within the three most critical components, SRAM memory cells, pre-charge circuits and sense amplifiers.

7.3.1 Memory Cells

The most popular memory cell type for the SRAM consists of two cross-coupled inverters (latch) and two access transistors, which are arranged in a matrix structure. This type of SRAM cell has negligible static current, which is suitable for low-power design and high stored data reliability [95]. The conventional way of connecting the memory cells to form a matrix arrangement is by sharing the BL and $\overline{BL}$ for cells in the same column and word line (WL) for cells in the same row. In other words, the writing and reading operation of a particular memory cell is done by selecting a specific WL for row selections and column address for a particular bit line column.

The transistor sizing in the memory cells does not correspond to the electron/hole mobility ratios. Hence, the access transistors that are controlled by the WL must be smaller in driving capability than the NMOS transistors in the memory cell. Ideally the NMOS driver transistors should be around 1.5 to 2 times larger than the access transistors. The popular 6-T (transistors) cell with the WL access transistors for selection is shown in Figure 7.8.

Basically, leakage current occurs when the transistor is in the off condition, but there is a node to source connection to the off transistor. In the 6-T cells particularly, there are two leakage current paths through the two cross-coupled inverters in conventional SRAM cell, as shown in Figure 7.8.

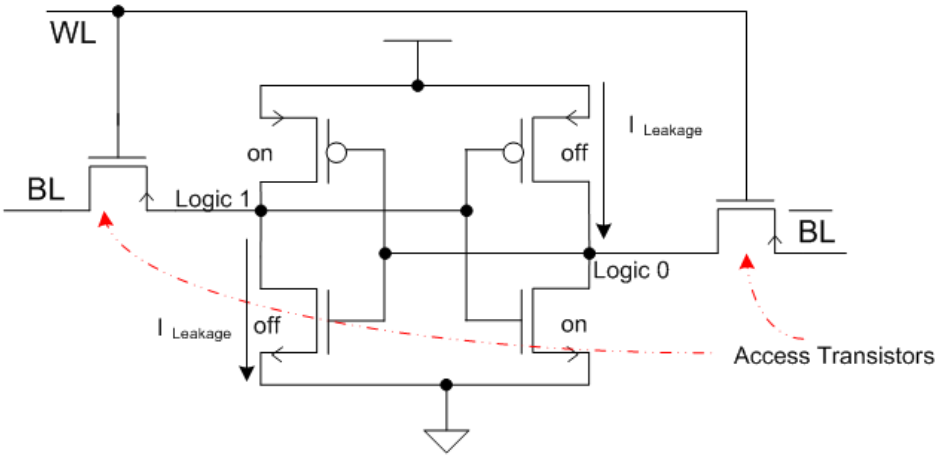


Figure 7.8: 1-Bit of SRAM memory cell circuit with access transistors bit lines (BL) and write line access.

The off transistors leakage current is dominated by the weak inversion current, which can be modeled as [96]:

$$I_D = I_{s0} e^{V_{gs} - V_t / (nkT/q)} (1 - e^{-V_{ds} / (nkT/q)})(1 + \lambda V_{ds}) \qquad \text{Eq. 7.2}$$

where λ is a parameter modeling the pre-saturation region in weak inversion and the other parameters have been defined in Chapter 3. The on transistors are in a strong inversion region and only present a negligible serial resistance, which can be ignored. Hence the total leakage current is the aggregate of the off transistors in the cross coupled inverters. Therefore the total leakage current in the SRAM cell may be modeled as

$$I_L = \left[(I_{SN} + I_{SP}) + (I_{SN}\lambda_N + I_{SP}\lambda_P) V_{DD} \right] \times \left(1 - e^{V_{DD} / (nkT/q)}\right) \qquad \text{Eq. 7.3}$$

where I_{SN} and I_{SP} are the off transistor current factors independent of V_{DS}, shown in Equation 7.3, for NMOS and PMOS respectively. As may be appreciated from Equation 7.3, there is a direct relationship between V_{dd} and the leakage current. Hence, the reduction in leakage power can be obtained by applying sleep mode, as in the MTCMOS circuit.

7.3.2 Sense Amplifier and Pre-charge Circuit

Sense amplifiers play a major role in memory architecture to amplify the output charge from a selected memory cell while having power dissipation in mind. The use of sense amplifiers has become even more critical for low voltage operation, because of the low voltage level of bit lines, static noise margin and the propagation delay of the voltage amplifiers. The sense amplifiers are used to detect the small voltage difference (approximately one tenth of V_{dd}) in the bit line resulting in reduced power dissipation without reduction in the overall performance. The voltage difference is then amplified to the intended voltage level of logic 1 & 0. As shown in Figure 7.9, the popular structure of a sense amplifier in low power design is the cross coupled inverter latch, due to negligible static power dissipation.

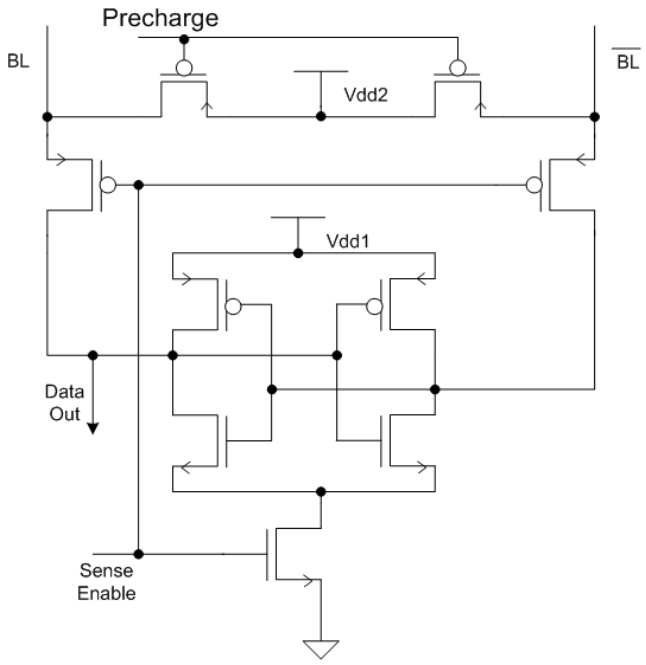


Figure 7.9: The CMOS inverter latch topology in the conventional sense amplifier circuit.

The CMOS inverter latch has a high gain in the transient operation region, and the gain of the sense amplifier itself depends on the sizing of the inverters. During the read operation the pre-charge signal is pulled high and either BL or $\overline{BL}$ discharge. The respective bit lines will continue to discharge producing a voltage small enough to be

detected by the sense amplifier. Once the bit line voltage falls within the sensing range, the sense enable is pulled high. The activation of sense enable signal will discard the internal nodes voltage of the sense amplifier from the bit lines and allow the internal node to reach the rail to rail swing. The V_{dd} level of the pre-charge circuit is increased so as to improve the sense amplifier performance.

7.3.3 SRAM Leakage Current Reduction Techniques

A great number of circuit topologies have been introduced to lower the sub threshold current such as: the inclusion of a switched source impedance circuit, a switched power supply with level holder, and multiple threshold level [97, 98]. In Chapter 3 five biasing techniques were studied and analysed in order to reduce the subthreshold leakage current in particular for Static Random Access Memory (SRAM) design. However, all of the techniques were not found to be suitable for the SRAM design [27]. The SRAM circuit proposed in this thesis adapts the variations of V_t level topology [99-101]. The threshold voltage variation is particularly useful in SRAM architecture assuming the control circuitry knows when particular memory cells are not required, in other words when a memory cell can be switched down to sleep mode. A MOS transistor with higher threshold voltage is used during the sleep period to prevent the leakage current from a particular node to channel through the ground line. However, introducing additional sleep functionality introduces additional number of transistors, either as switches or control circuitry. An attempt to reduce circuit area (i.e. using a less number of transistors in the core memory cell) is a major problem in SRAM, unlike Dynamic Random Access Memory (DRAM) where the smaller cell area is the better. The major concern in SRAM area reduction is the random data access problem and maintaining the charge level of the non-active cells. Therefore, the number of additional transistors in the leakage current control circuit must be kept as low as possible. The two most popular reduction techniques MTCMOS and VTCMOS are described in the following sub-chapters.

7.3.3.1 Multi-Threshold CMOS

Multi-Threshold CMOS (MTCMOS) is a circuit technique that uses two different combinations of transistors type. Low- V_t transistors for the high-speed core logic and High- V_t transistors as a power switch to reduce the leakage current wasted in the circuit. The main principle of MTCMOS is shown in Figure 7.10. MTCMOS has been a popular technique because of its simplicity of design. Ideally the larger the threshold level the lower the leakage current, however, one must decide the optimum value of the threshold level between the power switch (High- V_t devices) and (Low- V_t devices), as recovery delay tends to increase when a higher threshold level is used [46, 85, 94, 99]. A power switch with thicker gate oxide, t_{ox}, must be considered in order to prevent current blow up in source-drain channel.

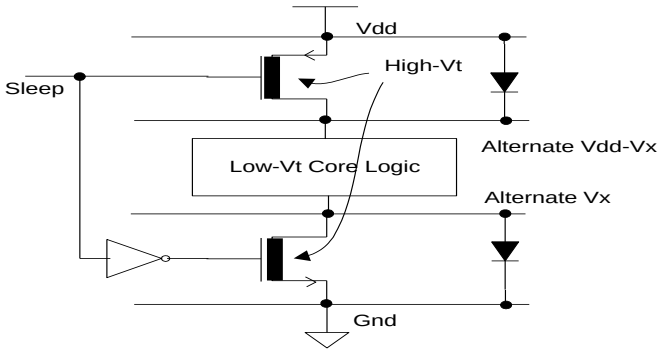
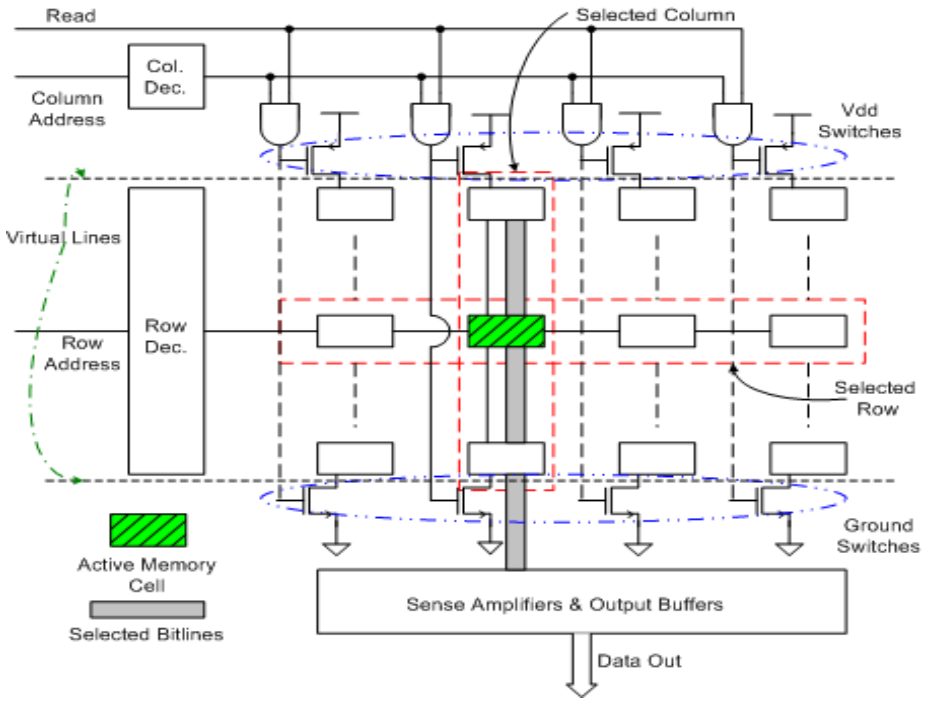


Figure 7.10: MTCMOS circuit architecture principal.

Initially, the MTCMOS principal was applied in the design of SRAM to reduce the power dissipation of the peripheral circuits such as the row decoders and the input/output buffers. However, the application of the MTCMOS technique was not be able to be implemented in the memory cell array, as the power switch cut-off the power supply destroying the data stored in the memory cells.

The MTCMOS SRAM, shown in Figure 7.11, was designed by using the conventional gated-V_{dd} and *Gnd* structure, which was introduced in [102]. This technique reduces the leakage current by using the conventional method of high-V_t transistors between V_{dd} and *Gnd* to cut-off the power supply of the low-V_t memory cell, when the cell is in

sleep mode. However, a slight modification was made by applying an addition virtual V_{dd} and virtual *Gnd* lines for data loss prevention, as shown in Figure 7.11a).



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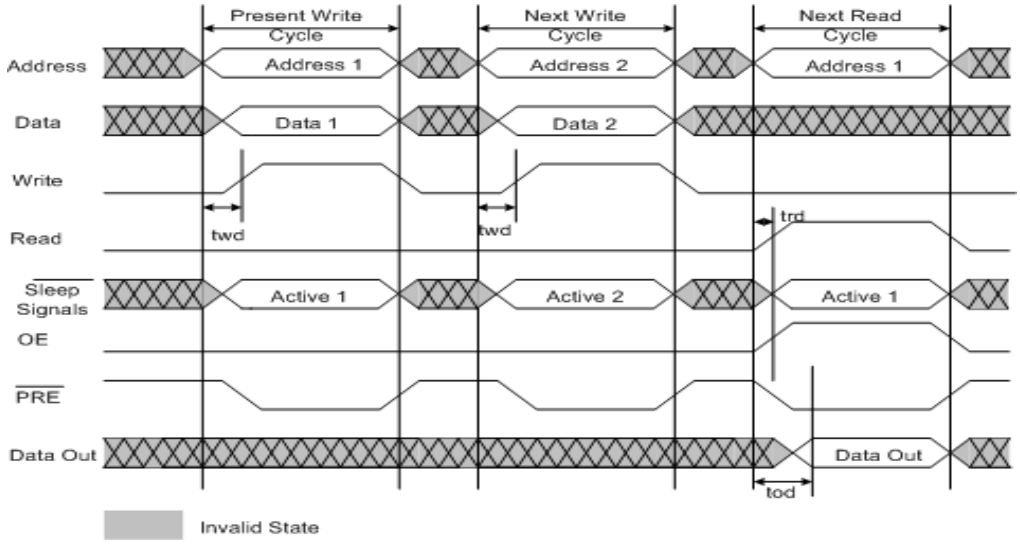


b)

Figure 7.11: MTCMOS a) Memory cells array structure with the active cell shaded in green. The structure consists of switches to reduce the current in the in-active cells, b) Operation signals in read and write cycles with additional set-up time for the active cell to avoid data error due to a different voltage level during the transition from an active to a non-active cell.

The two virtual lines will maintain the stored charge of the memory cells while the power lines are cut-off. Thus the technique introduces a slight delay in *twd* and *trd* due to activation of the sleep transistors. The delay is necessary for the charge of the memory cells to recover from sleep mode to active mode. The read and write operation signals of the MTCMOS SRAM are shown in Figure 7.11b).

7.3.3.2 Variable-Threshold CMOS

Variable-Threshold CMOS (VTCMOS) is another way of reducing the subthreshold leakage current [17]. The reduction can be achieved by directly manipulating the threshold level in the core logic, as can be seen in Figure 7.12. The manipulation has to be performed carefully to avoid the core logic exhibiting unstable behavior due to rigorous threshold scaling. An ideal way to determining the appropriate threshold level is to have two different levels of threshold, one for standby and another for active. VTCMOS uses a different principle to dynamic-V_{dd} scaling which was described in Chapter 3. Dynamic-V_{dd} scaling is where the power supply of the core logic is actively scaled according to the input and clock requirement and is effective in reducing $P_{dynamic}$.

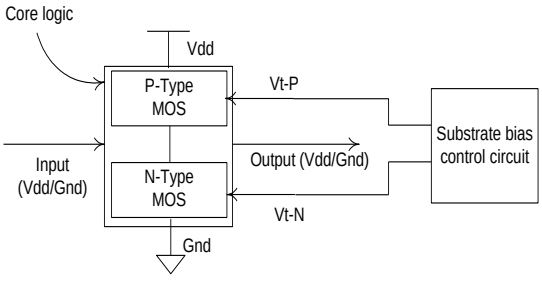
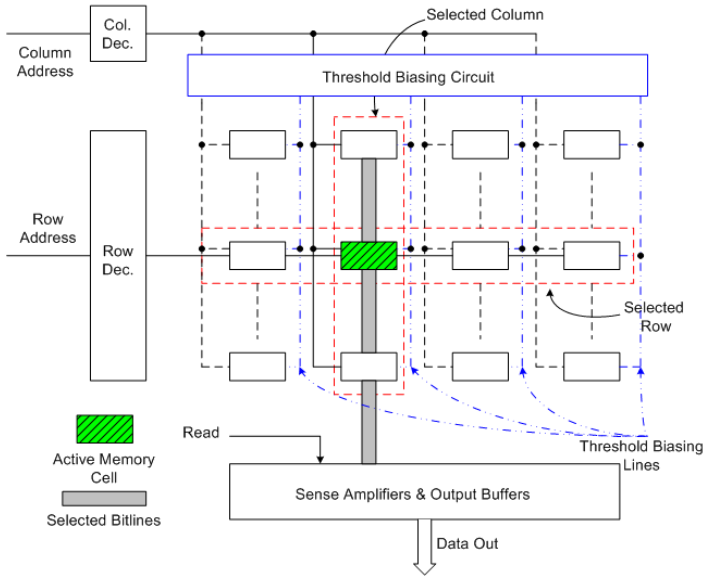


Figure 7.12: VTCMOS circuit architecture

The VTCMOS technique in SRAM is not much different than the original SRAM concept. As seen in Figure 7.13a, there is an extra threshold biasing circuit connected to the SRAM main core. The external biasing circuit is used to change the threshold voltage of an active memory cell depending on the address coming from the decoder. Unlike MTCMOS where the supply voltage changes from V_{dd} to virtual V_{dd} when a particular cell is active, VTCMOS memory cells are still using the same voltage

supply. In VTCMOS, the transistor threshold voltage value changes from 0 to 1.2 V in active mode and -300 mV to 300 mV in sleep mode. Hence, this technique is primarily used to reduce the static current dissipation.



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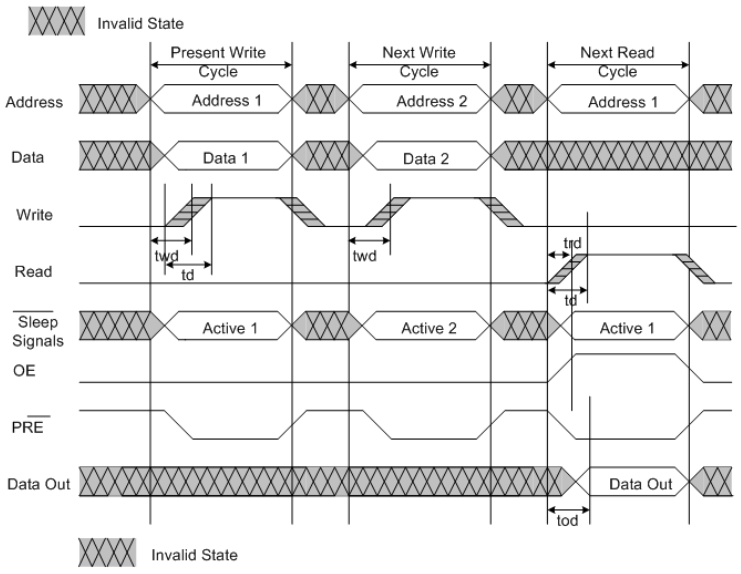


b)

Figure 7.13: VTCMOS. a) Memory cells array structure with the active cell shaded in green. The structure consists of threshold bias generator block. , b) Operation signals in read and write cycles with additional set-up time for the active cell to avoid data error due to a different threshold voltage level during the transition from an active to a non-active cell.

VTCMOS techniques introduce a significant delay in the read and write operation signals, as shown in Figure 7.13b). The delays are required to slowly change the threshold level, as an abrupt change of threshold level in VTCMOS circuit will cause a catastrophic state in the stored data in memory cells.

7.4 Conclusion

The threshold scaling technique, which involves the application of a keeper transistor, has been designed and analysed and are described in this chapter. The circuit technique dynamically changes the threshold voltage of the keeper transistor with a specific delay after the beginning of each operational phase, by changing the body bias voltage of the keeper transistor. The keeper transistor current is reduced by increasing its threshold voltage through the application of a reverse body bias to the beginning of the evaluation phase. Dynamic forward and reverse body biasing of the keeper transistor enhances noise immunity, performance, power dissipation, and PDP characteristics of the dynamic circuit under test. Memory cells not only take up a major part of an FFT system but also dissipate a significant amount of power. Several power reduction techniques for static memory cells have also been discussed and implemented in this chapter. Chapter 8 presents the integration results and layout implementation of the designed FFT core together with the power schemes.

Chapter Eight:
Integration Results and Layout Implementation

8.1 Introduction

The power management modules were integrated together with the FFT core. The FFT ASIC implementation uses a readily available standard cell logic library and memory operating down to 1 V. The simulated energy performance graph on the different variable activity factors shown, in Chapter 5, indicates that operation significantly below 1 V is necessary to minimise energy dissipation. Therefore a combination of standard ST-Microelectronic® library and custom cells were used in the layout implementation of the design. This chapter discusses the integration aspect, layout issues and simulated post layout results of the power management chip.

8.2 Design Flow

The design flow of the low power FFT was modified to use: the standard cell library, the custom Baugh Wooley multiplier and the custom low power memory cell banks. Conventionally in a non-reconfigurable design the BW multiplier core is built as a single block for the largest bandwidth. In this work, a 16-bit multiplier block is used to compute both 8-bit and 16-bit multiplication. However, the implementation of a single large bandwidth multiplier block is not optimal due to the sign bit switching in two's complement boolean computation. The proposed solution is to implement a variety of multiplier bit widths, with the control block deciding the selection of the multiplier block as depicted in Figure 8.1.

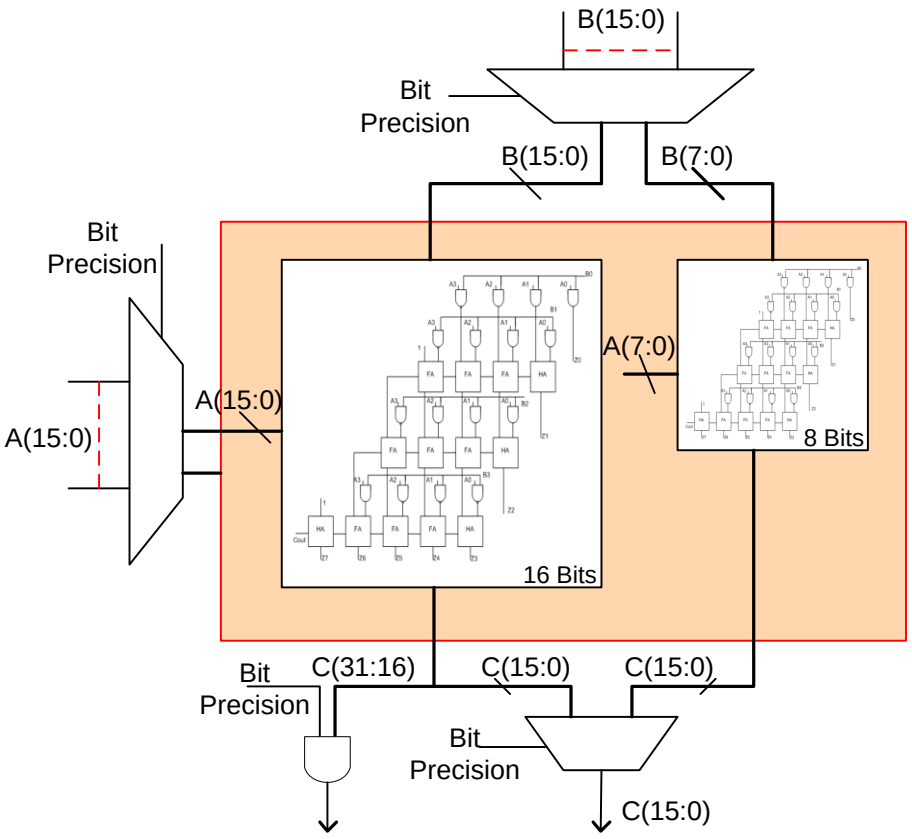


Figure 8.1: 8 bit and 16 bit scalable Baugh Wooley multiplier core with the input addressing Mux and scalable bit precision output to select different output bits, C, size. Both input A and B are processed according to the bit length which enables the appropriate multiplier bit.

The FFT core was first designed in verilog description language and synthesised using Altera® on an FPGA board which then implemented in Synopsis® to verify the semi-custom design functionality. The RTL modules of the design can be seen in Figure 8.2 and the synthesised core layout in Figure 8.3a). Cadence Analog Artist® was used to create the specific additional library which is mainly used in the system control logic (counters, FSMs), data path (two's complement adders and subtractors), and memory blocks.

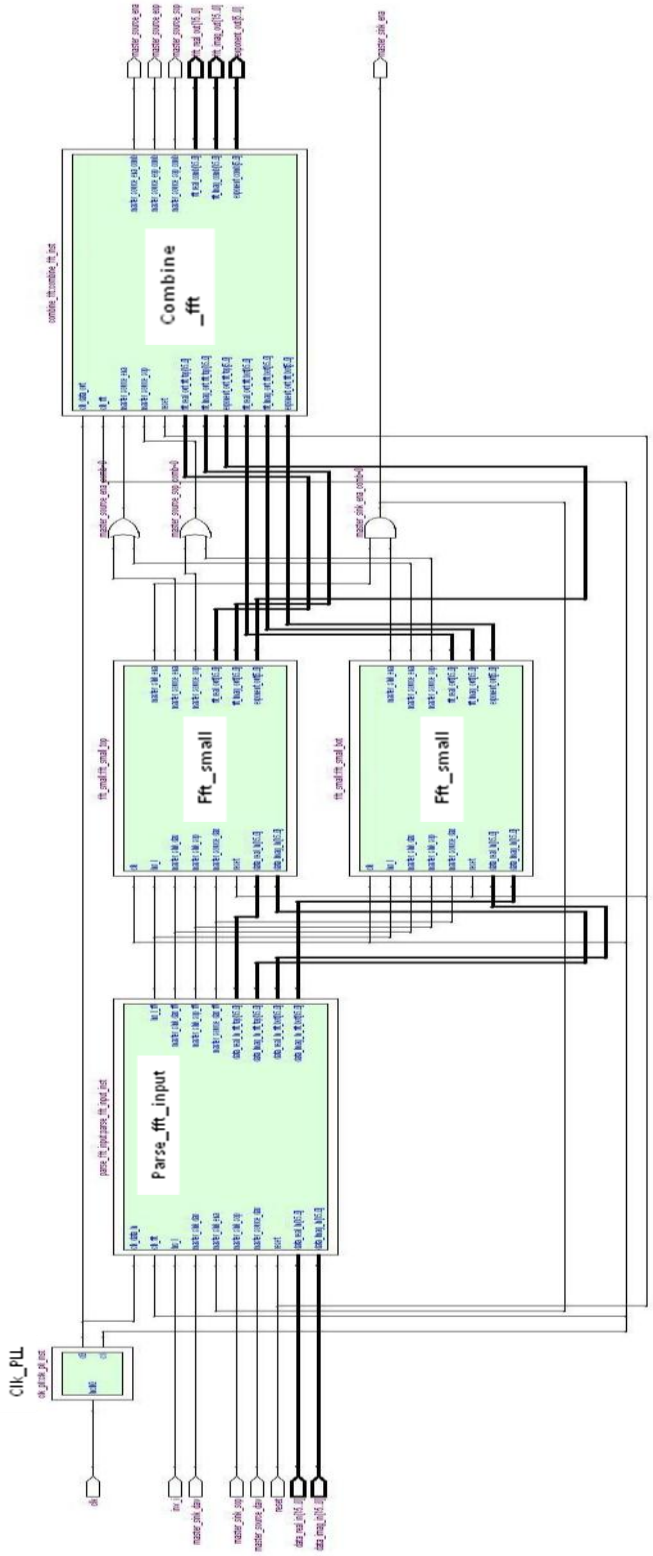
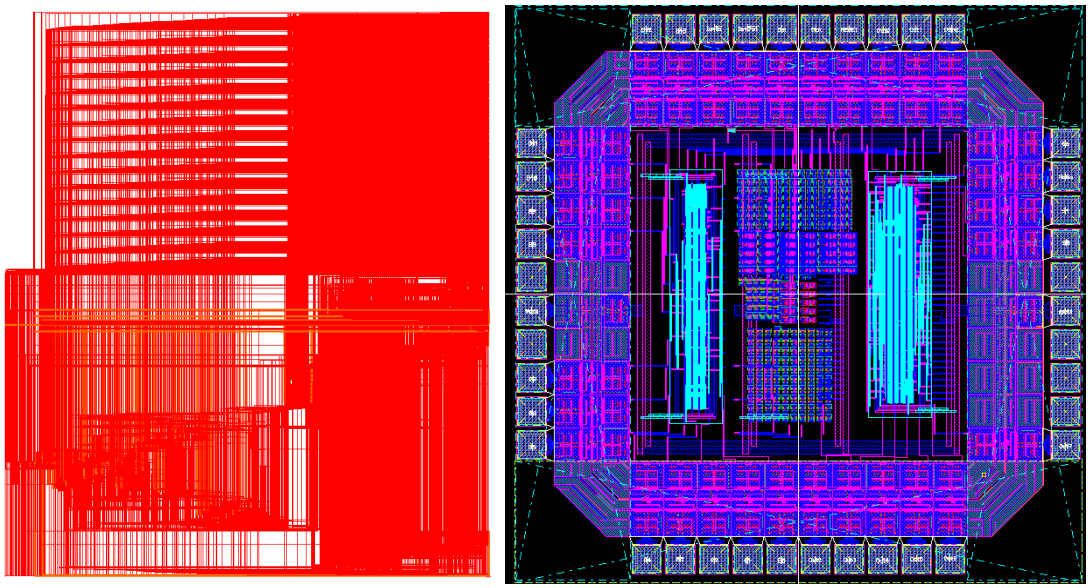


Figure 8.2: Synopsys RTL Synthesis Block View, which consists of the core logic, memory banks for data caching and output latches.

A custom script was used to create the layout for the memory cells and the BW multipliers. Each of the hierarchy library components as well as the custom memory and BW multipliers was verified using Spectra® simulator in Cadence® in the voltage supply range of 300 mV to 1 V for the Typical process corner. The layout of the FFT processor was first tested in analog artist layout editor, as depicted in Figure 8.3b).



a) b)

Figure 8.3: a) Synopsis synthesis RTL View of the FFT design and b) Cadence gates Layout of the FFT cells together with the pads.

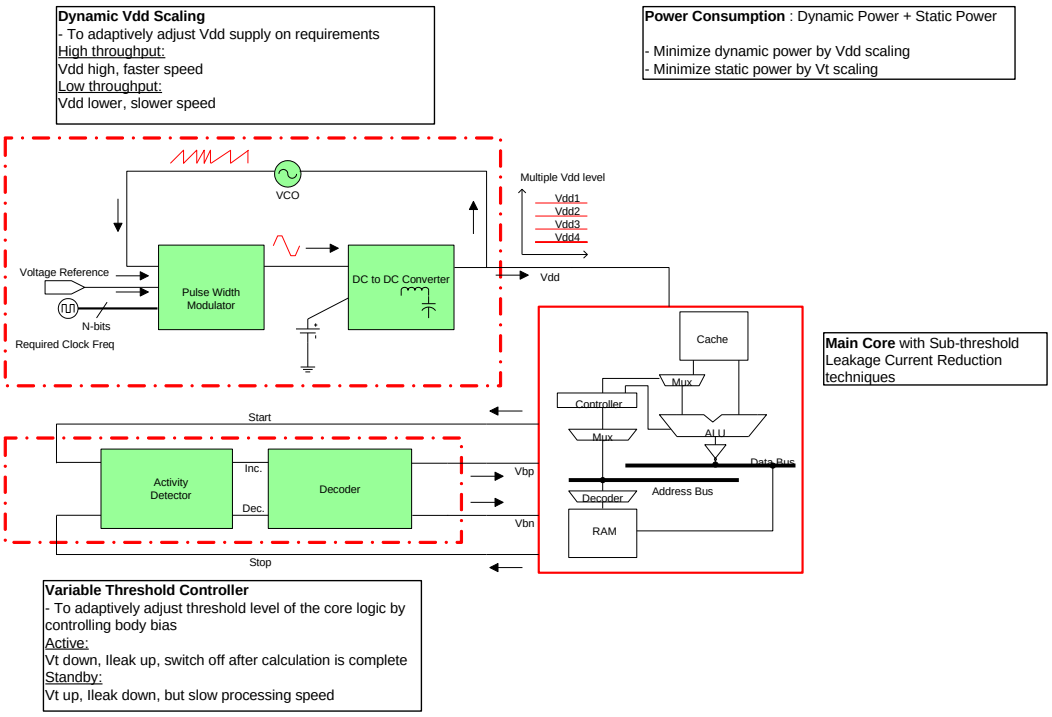


Figure 8.4: Overall Integration blocks, which consists of the dynamic power reduction block and the static power reduction. Both of the power reduction techniques were applied to a FFT main processor core.

8.3 Overall Results

The DVS system, multiplier library and the SRAM were designed and simulated in Cadence Design Framework II Analog Environment® using 0.13 μm low leakage ST-Microelectronic® library. The voltage scaling output characteristics of the DVS system occurs due to the variation of the VCO frequency. The voltage scaling output property of the DVS system is used as the supply voltage of the FFT core. This phenomenon is illustrated in Figure 8.5. The variation of the VCO frequency transpires because of the DAC weighted binary input. The external clock shown in Figure 8.5a, was set to 150 MHz, while the VCO frequency, shown in Figure 8.5e, was adjusted to be slightly greater than 150 MHz. It can be clearly seen in Figure 8.5b, prior to the VCO frequency reaching 1 μs, the DVS output voltage (V_{dd}) ramps up to 1.2 V, as the full set of binary inputs (i.e. Bit<4:0> are all 1) are given. In addition to this, the supply voltage output in Figure 8.5b, only ramps up to 700 mV as the VCO frequency is reduced below the external clock of 150 MHz.

The post layout performance summary of the DVS system is shown in Table 8.1. Overall the DVS system without any load consists of 366 transistors and dissipates 174.1 μW at 150 MHz operation frequency. The effect of temperature in conjunction with DVS on the current performance is also addressed. Figure 8.6, shows the dependence of the system power on the operating temperature for various scaling voltages, V_{dd}, in 0.13 μm technology. The figure shows that total power increases as temperature increases, however, there is an optimum voltage where the temperature effect is minimal on power dissipation.

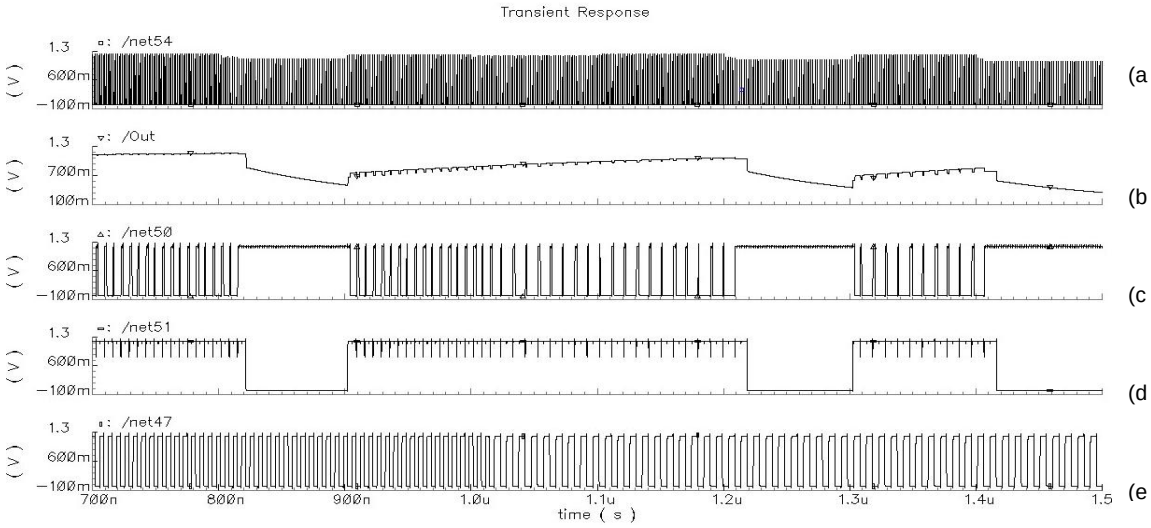


Figure 8.5: V_{dd} Scaling with Frequency Variation Post-Layout Simulation Result. Shown in the panel a) is the reference frequency from the oscillator circuit. Panel e) describes the series of pulse modulated output waveforms. Both of the signals, a) and e), are passed through into the Phase and Frequency Detector which generates Up, shown in d) and Down, shown in c) signals. The output waveform b), is the locked voltage which is used by the FFT processor as power supply, V_{dd}.

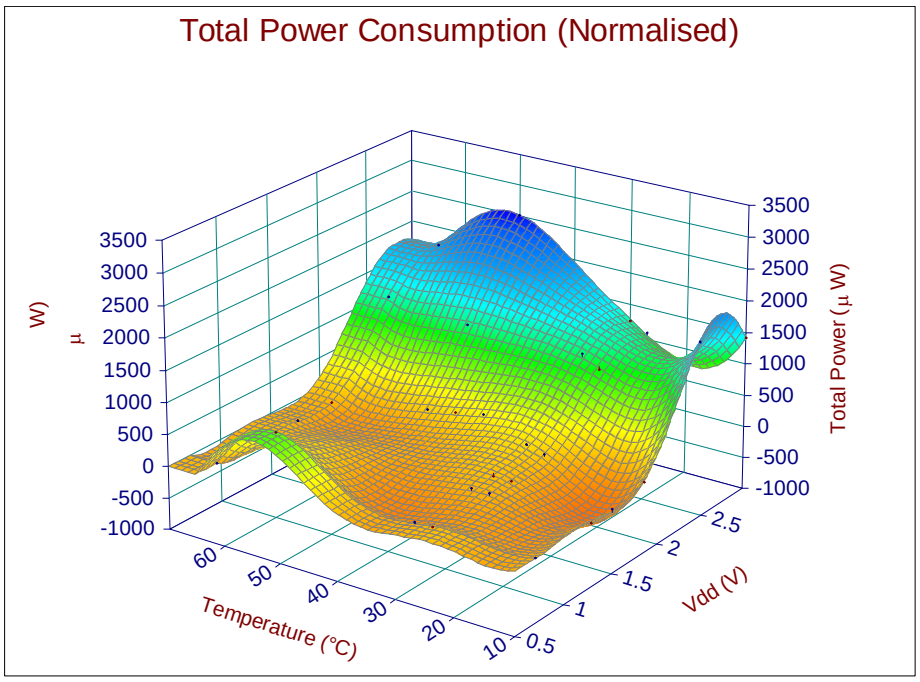


Figure 8.6: Total power consumption versus V_{dd} and Temperature of the Post-Layout System. The system minimum power consumption is optimised at between 1 to 2.25 Volts V_{dd}, as it lies at the lowest power bed scale. There is a power spike shown at 55 degree Celsius together with 3 Volts of operation which is caused by the device breakdown.

The effectiveness of V_{dd} scaling on the FFT multiplier core is presented in Figure 8.7. DVS in a larger multiplier is more effective with an average power reduction of approximately 25%. The synthesized result of the complete system in Cadence SOC Encounter® with medium mapping effort is shown in Figure 8.8. The compiled FFT architecture accommodates 414,360 standard gates cell.

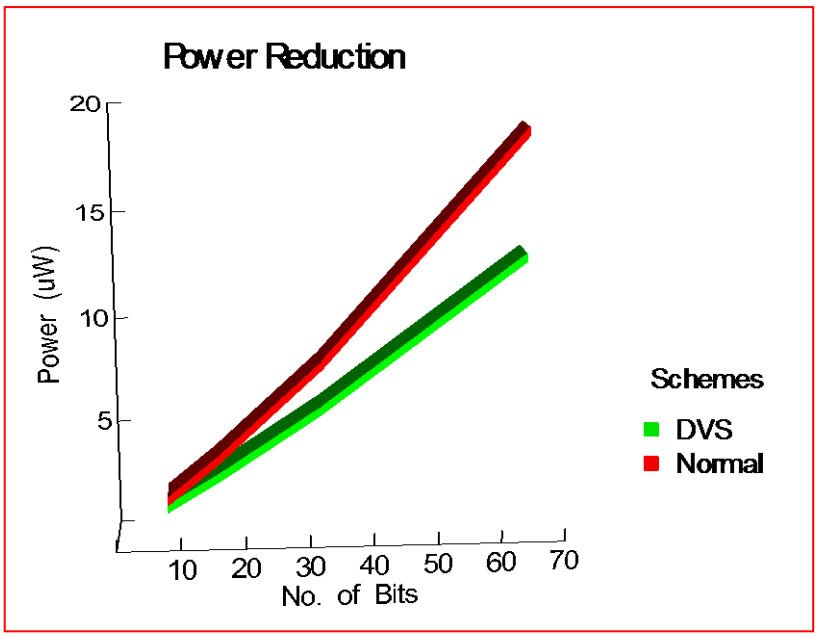


Figure 8.7: The Simulated power comparison plot of normal and DVS scheme, shown in green line, and on the FFT multiplier core, shown in red line.

Table 8.1: Post-Layout simulation result summary of the modeled DVS System.

Fabrication Technology	ST-Microelectronic, 0.13 µm 6-metal layer LLUL library, dual-process CMOS
Number of Transistor	366 transistor
Power Supply	1.2 V
Power Dissipation	174.1 µW @ 150 MHz
Scaling Steps	4 Bits of VCO frequency and 4 Bits of DAC Binary Input. Total Steps of 256 steps

Table 8.2: Power Performance of DVS System in the implemented FFT Core.

Multiplier bits (n)	Power (µW)		Reduction in Power (%)
	Without DVS	With DVS	
8	1.47	1.12	23%
16	3.42	2.55	25%
32	7.81	5.68	27%
64	18.6	12.8	31%

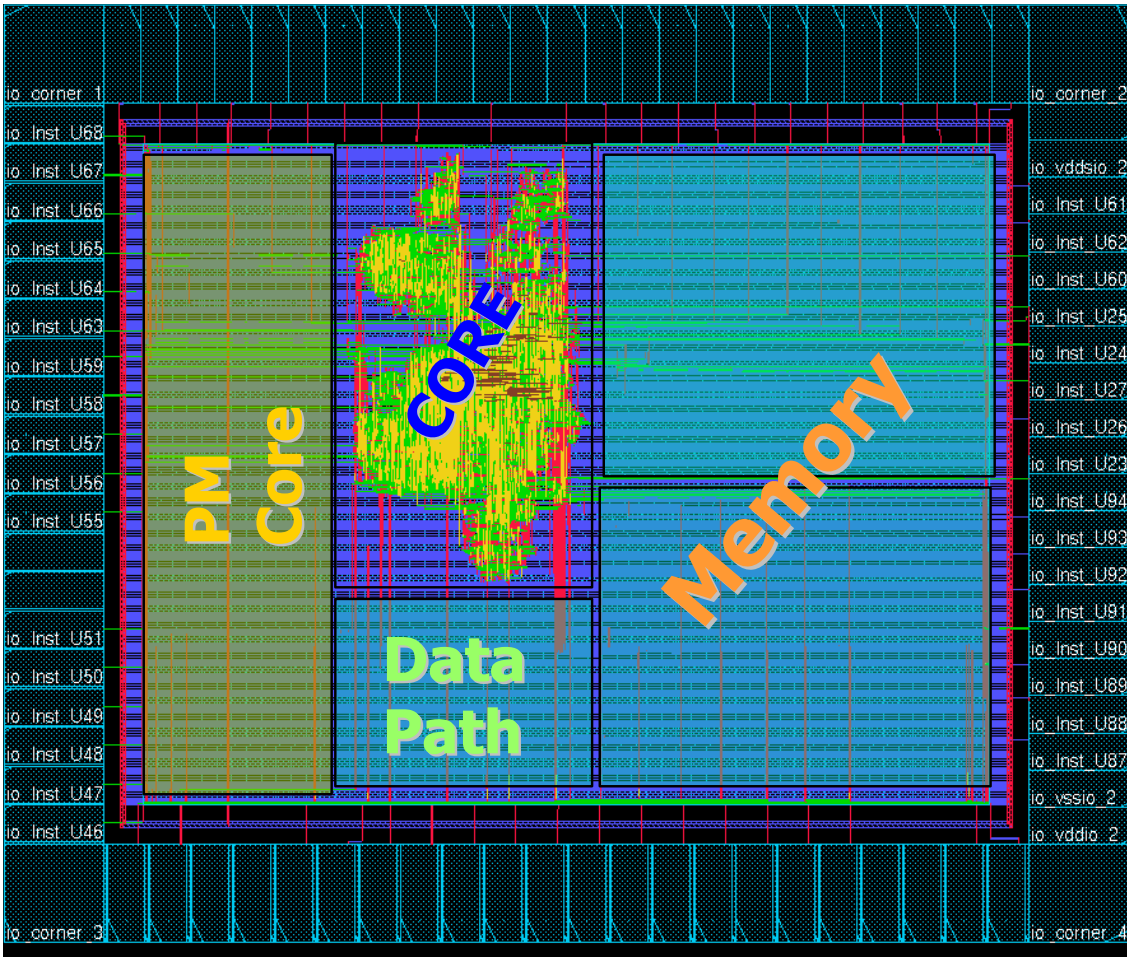


Figure 8.8: Power Management and FFT Core Design Layout.

8.4 Conclusion

Voltage scaling together with threshold keeper scaling achieves a significant level of energy saving. Due to the low frequency clock nature of portable biomedical devices, decreasing the clock frequency together with scaling down the supply voltage, results in a reduction in power dissipation. However, there is a limit to the extent of scaling that can be applied to the supply voltage as a lower clock frequency results in an increase in the static leakage current. In other words there will be a point where static power will exceed dynamic power dissipation. The post-layout simulation result of the DVS system is expected to dissipate 138 μW and 3.4 mW of static power at low throughput and high throughput corners respectively, with the converter consuming the majority of the power drain. The primary dissipating components include the processor, VCO, PWM, DAC and the DC-DC converter. Considering all loses in the processor and the converter operating at full load, the system's nominal energy per operation, at 1 V is expected to be about 1 nJ/instruction at the lowest frequency corner.

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Chapter Nine:
Conclusion and Future Work

A combination of efficient low voltage DC-DC conversion and threshold voltage scaling have been shown to be very beneficial in enabling low power biomedical technology. Recent innovations and improvements in low-power digital CMOS design technology have created an opportunity for scaling of the supply threshold voltage to have little penalty on circuit performance. This thesis has introduced supply and threshold voltage scaling design techniques that take advantage of this opportunity.

Work preceding this thesis demonstrated that highly integrated DC-DC converters custom designed in supply voltage scaling for low power and throughput constraint, for digital biomedical CMOS systems, allow moderate reduction in overall power dissipation compared to more conventional supply designs. Dynamic voltage scaling (DVS) has been demonstrated in this thesis to improve the general system performance for a more energy efficient power management system.

A number of power management and circuit level design techniques have been presented and discussed to reduce the circuit size, cost and energy dissipation. Simulated results on the effectiveness of the prototype have successfully demonstrated these design techniques. The design approach in this thesis is practicable to be used in low voltage low power portable biomedical systems.

9.1 Summary of Research Contribution

In this thesis, DVS and keeper threshold voltage scaling schemes have been designed and simulated as low voltage and low power enablers. This has included the demonstration of a system and circuit level design techniques to enable the usage of power management in portable biomedical applications.

Power management techniques have been previously implemented for applications in Embedded Systems [102-105], Multimedia Systems [106], Field Programmable Gate Array (FPGA) architectures [107] and Dynamic Voltage Frequency Scaling (DVFS) architecture [108]. However to the best of the author's knowledge, there are no existing methodologies for application in the field of Biomedical Electronics. The work in this thesis addresses this shortcoming and proposes a new power management scheme.

A number of design techniques which decrease circuit size, cost and energy dissipation were realised. These include: reduced inductor consideration, dynamic transistor sizing, ultra low power digital to analog converter, low power PWM control; and novel application of existing knowledge in the design of the: current starved ring oscillator, feedback compensation circuit, dynamic logic threshold keeper transistor, moderate to low frequency operation.

The key research contributions are:

- The investigation of CMOS transistor behaviour in the ultra low region (subthreshold), results in different biasing schemes suitable for biomedical devices.
- The development of ultra low power logic techniques resulted from the combinations of the different biasing schemes.
- The development of a novel dynamic voltage scaling technique, which delivers an improvement in the battery run-time for a processor based system. This included the system discussion and circuit level design considerations.

- The development of a dynamic threshold keeper voltage scaling technique used in conjunction with the DVS system. This included the system discussion and circuit level design considerations.
- The simulation of an efficient power management system with 91% efficiency when operating between 175 μW to 1 mW with 23% to 31% power reduction when compared to an FFT processor.

9.2 Future Research directions

This thesis has discussed and simulated the groundwork for various continuing research areas in Low Power CMOS Microelectronics in general and more specifically CMOS Biomedical applications. The research focuses not only on the design techniques to reduce static and dynamic power dissipation, but also to overcome process and temperature variations, for application in portable biomedical electronic systems where battery run-time is to be improved.

The field of microelectronics continues to evolve and change rapidly. One of the areas not considered for this thesis was Micro-Electro-Mechanical Systems (MEMS). Recent advances in MEMS allow the micro-fabrication of magnetic and capacitive components. These can be implemented to introduce a fully integrated power management module together with its individual CMOS load, which would offer further reduction in power system size. The possibility to design the power management module, i.e. DC-DC converters or the threshold voltage bias generator as adds-on macro function blocks for High Description Language or in DSP cores, could be the next low-power enabling technology. Research in the integration of these macros is a logical next step which however requires a breakthrough in computer aided design in order to be implemented.

Further analysis of the optimal operating points for each of the modules is suggested as it is very likely that different system level blocks will have different optimal supply voltages and clock frequencies, which will further complicate the interface between the blocks. The analysis would be enhanced by further fabricating benchmark circuits for variable supply voltage and threshold voltage in various activity factors to verify the energy-performance contours. Multiple threshold CMOS is needed in order to achieve wider range of threshold voltages. A benchmark circuit with multiple instances with back biasing can obtain a large threshold voltage range, however transistor models with triple well process are needed.

New bus interfacing techniques and system level architectures in asynchronous techniques may be developed for multiple clock frequency domains to avoid timing conflicts. Further research possibility in level converting circuits is suggested to interface between two modules with different supply voltage levels. Further analysis is also required to gauge for the effects of process variations, device mismatch, lithography effects and temperature, on the optimal supply and threshold voltage operation, which in turn have a significant impact on energy dissipation and performance, especially in the subthreshold region. Further analysis is required in the area of architectures design for subthreshold circuits. Other interesting research directions which are suggested include the possibility of voltage scaling together with threshold scaling for a subthreshold circuit and the use of pipelining and massively parallel architectures. Massive parallelism and pipeline techniques increase the activity factor for a circuit and require minimum supply voltage operation for minimal power dissipation. The idea of minimum supply voltage design and subthreshold circuit considerations opens up many research possibilities. This will involve further design work in a complete subthreshold standard cell library.

Further research work also could be beneficial in low voltage memory design which operates at low voltage process corners, which will include a subthreshold memory layout generator for SRAMs and ROMs. Simulator tools such as nanosim and hspice are able to simulate a small system in reasonable time, however it will take weeks to

analyse a large system. Due to the large nature of memory cells, a simulator which can verify the functionality of a large subthreshold system is required.

Recent research initiatives made integration of low-voltage operation possible into existing applications [109-112]. However besides the many research ideas listed above, there are many new opportunities for innovation and breakthrough in dynamic power management, subthreshold circuit, scalable architecture and minimal voltage operating circuits.

The research conducted for this thesis fits into a technological context that is rapidly changing and which offers many exciting opportunities for contributions by many researchers. The author trusts that his contribution is appropriate and welcome.

Bibliography

[1] A. B. o. Statistics, 2004.
[2] D. o. I. a. M. a. I. A. D. Australian Government, 2007.
[3] B. Australia, 2000.
[4] G. Rezos, "a presentation in AusBiotech2003 forum," pSividia Limited, 2000.
[5] C. H. I. Kim, H. Soeleman, and K. Roy, "Ultra-low-power DLMS adaptive filter for hearing aid applications," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems,* vol. 11, pp. 1058-1067, 12 2003.
[6] Andromed, France, p. Biomedical Company.
[7] F. Pelletier and S. Morris, "Doing More with Much, Much Less: Ultra Low Power Design for Medical Applications," M. Electronics, Ed., 2003, pp. 73-74.
[8] F. Silveira and D. Flandre, "A 110 nA pacemaker sensing channel in CMOS on silicon-on-insulator," in *2002 IEEE International Symposium on Circuits and Systems. Proceedings*, 2002, pp. V-181-V-V-4 vol.5.
[9] ChipRx.
[10] F. I. B. Technik.
[11] P. M. Brooks, H. M. Lapsley, and D. B. Butt, "Medical workforce issues in Australia: "tomorrow's doctors — too few, too far"," 2003.
[12] C. S. Pattichis, E. Kyriacou, S. Voskarides, M. S. Pattichis, R. Istepanian, and C. N. Schizas, "Wireless telemedicine systems: an overview," *IEEE Antennas and Propagation Magazine,* vol. 44, pp. 143-53, 2002.
[13] X. H. Wang, R. S. H. Istepanian, T. Geake, J. Hayes, M. Desco, G. Kontaxakis, A. Santos, A. Prentza, and S. Pavlopoulos, "A feasibility study of a personalized, Internet-based compliance system for chronic disease management," *Telemedicine Journal and e-Health,* vol. 11, pp. 559-566, 2005.
[14] S. Garawi, R. S. H. Istepanian, and M. A. Abu-Rgheff, "3G wireless communications for mobile robotic tele-ultrasonography systems," *IEEE Communications Magazine,* vol. 44, pp. 91-96, 2006.
[15] R. S. H. Istepanian, E. Kyriacou, S. Pavlopoulos, and D. Koutsouris, "Effect of wavelet compression on data transmission in a multipurpose wireless telemedicine system," *Journal of Telemedicine and Telecare,* vol. 7, pp. 14-16, 2001.
[16] E. Jovanov, A. Milenkovic1, C. Otto, and P. C. Groen, "A wireless body area network of intelligent motion sensors for computer assisted physical rehabilitation," *Journal of NeuroEngineering and Rehabilitation,* vol. 2, p. 6, 1 March 2005 2005.
[17] P. Sungmee and S. Jayaraman, "Enhancing the quality of life through wearable technology," *IEEE Engineering in Medicine and Biology Magazine,* vol. 22, pp. 41-48, 2003.
[18] T. Martin, E. Jovanov, and D. Raskovic, "Issues in wearable computing for medical monitoring applications: a case study of a wearable ECG monitoring

device," in *Wearable Computers, 2000. The Fourth International Symposium on*, 2000, pp. 43-49.

[19] J. M. Winters, W. Yu, and J. M. Winters, "Wearable sensors and telerehabilitation," *IEEE Engineering in Medicine and Biology Magazine,* vol. 22, pp. 56-65, 2003.

[20] M. Ghovanloo, K. Beach, K. D. Wise, and K. Najafi, "A BiCMOS wireless interface chip for micromachined stimulating microprobes," in *Microtechnologies in Medicine & Biology 2nd Annual International IEEE-EMB Special Topic Conference on*, 2002, pp. 277-282.

[21] B. P. Otis and J. M. Rabaey, "A 300- mu W 1.9-GHz CMOS oscillator utilizing micromachined resonators," *IEEE Journal of Solid-State Circuits,* vol. 38, pp. 1271-1274, 2003.

[22] D. Raskovic, T. Martin, and E. Jovanov, "Medical monitoring applications for wearable computing," *Computer Journal,* vol. 47, pp. 495-504, 2004.

[23] M. Scheffler and E. Hirt, "Wearable devices for telemedicine applications," *Journal of Telemedicine and Telecare,* vol. 11, pp. 11-14, 2005 2005.

[24] E. S. Takeuchi and R. A. Leising, "Lithium batteries for biomedical applications," *MRS Bulletin,* vol. 27, pp. 624-627, 08 2002.

[25] J. Pouwelse, K. Langendoen, and H. Sips, "Dynamic Voltage Scaling on a Low Power Microprocessor," *UbiComp-Technical Report,* 2000.

[26] J. M. Rabey, *Digital Integrated Circuits, A Design Perspective, 2nd Edition*: Pearson Education Inc, 2003.

[27] D. Fitrio, A. Stojcevski, and J. Singh, "Leakage Current Reduction Techniques for Subthreshold Circuit in a Simulation Environment," in *Best of Book, AMSE Journal 2004*, 2004.

[28] K. Usami and M. Horowitz, "Clustered voltage scaling technique for low-power design," in *International Symposium on Low Power Electronics and Design Proceedings of the 1995 international symposium on Low power design*, 1995, pp. 3-8.

[29] Q. Gang, D. Kirovski, M. Potkonjak, and M. B. Srivastava, "Energy minimization of system pipelines using multiple voltages," in *Circuits and Systems, 1999. ISCAS '99. Proceedings of the 1999 IEEE International Symposium on*, 1999, pp. 362-5 vol.1.

[30] K. Usami and M. Igarashi, "Low-power design methodology and applications utilizing dual supply voltages," in *Design Automation Conference, 2000. Proceedings of the ASP-DAC 2000. Asia and South Pacific*, 2000, pp. 123-128.

[31] S. Raje and M. Sarrafzadeh, "Variable voltage scheduling," in *International Symposium on Low Power Electronics and Design*, 1995, pp. 9-14.

[32] M. Igarashi, K. Usami, K. Nogami, F. Minami, Y. Kawasaki, T. Aoki, M. Takano, C. Mizuno, T. Ishikawa, M. Ichida, M. Kanazawa, S. Sonoda, and N. Hatanaka, "A low-power design method using multiple supply voltages," *Transactions of the Information Processing Society of Japan,* vol. 40, pp. 1699-1706, 04 1999.

[33] A. P. Chandrakasan, S. Sheng, and R. W. Brodersen, "Low-power CMOS digital design," *IEEE Journal of Solid-State Circuits,* vol. 27, pp. 473-484, 04 1992.

[34] M. D. Godfrey, "CMOS device modeling for subthreshold circuits," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 39, pp. 532-539, 08 1992.

[35] G. Massobrio and P. Antognetti, *Semiconductor Device Modelling with Spice*: McGraw-Hill Inc, 1993.

[36] H. Soeleman, K. Roy, and B. C. Paul, "Robust subthreshold logic for ultra-low power operation," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 9, pp. 90-99, 2001.

[37] T. Kawahara, M. Horiguchi, Y. Kawajiri, G. Kitsukawa, T. Kure, and M. Aoki, "Subthreshold current reduction for decoded-driver by self-reverse biasing [DRAMs]," *IEEE Journal of Solid-State Circuits*, vol. 28, pp. 1136-1144, 1993.

[38] M. Horiguchi, T. Sakata, and K. Itoh, "Switched-source-impedance CMOS circuit for low standby subthreshold current giga-scale LSI's," *IEEE Journal of Solid-State Circuits*, vol. 28, pp. 1131-1135, 1993.

[39] K. Itoh, A. R. Fridi, A. Bellaouar, and M. I. Elmasry, "A deep sub-V, single power-supply SRAM cell with multi-V/sub T/, boosted storage node and dynamic load," in *VLSI Circuits, 1996. Digest of Technical Papers., 1996 Symposium on*, 1996, pp. 132-133.

[40] H. Kawaguchi, K. Nose, and T. Sakurai, "A super cut-off CMOS (SCCMOS) scheme for 0.5-V supply voltage with picoampere stand-by current," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 1498-1501, 2000.

[41] T. Yamagata, S. Tomishima, M. Tsukude, T. Tsuruda, Y. Hashizume, and K. Arimoto, "Low voltage circuit design techniques for battery-operated and/or giga-scale DRAMs," *IEEE Journal of Solid-State Circuits*, vol. 30, pp. 1183-1188, 1995.

[42] Y. Nakagome, K. Itoh, M. Isoda, K. Takeuchi, and M. Aoki, "Sub-1-V swing bus architecture for future low-power ULSIs," in *VLSI Circuits, 1992. Digest of Technical Papers., 1992 Symposium on*, 1992, pp. 82-83.

[43] H. Mizuno, K. Ishibashi, T. Shimura, T. Hattori, S. Narita, K. Shiozawa, S. Ikeda, and K. Uchiyama, "An 18- mu A standby current 1.8-V, 200-MHz microprocessor with self-substrate-biased data-retention mode," *IEEE Journal of Solid-State Circuits*, vol. 34, pp. 1492-1500, 1999.

[44] K. Kumagai, H. Iwaki, H. Yoshida, H. Suzuki, T. Yamada, and S. Kurosawa, "A novel powering-down scheme for low Vt CMOS circuits," in *VLSI Circuits, 1998. Digest of Technical Papers. 1998 Symposium on*, 1998, pp. 44-45.

[45] M. Mizuno, K. Furuta, S. Narita, H. Abiko, I. Sakai, and M. Yamashina, "Elastic-Vt CMOS circuits for multiple on-chip power control," in *Solid-State Circuits Conference, 1996. Digest of Technical Papers. 42nd ISSCC., 1996 IEEE International*, 1996, pp. 300-1, 462.

[46] J. Kao, A. Chandrakasan, and D. Antoniadis, "Transistor sizing issues and tool for multi-threshold CMOS technology," in *Design Automation Conference, 1997. Proceedings of the 34th*, 1997, pp. 409-414.

[47] T. Kobayashi and T. Sakurai, "Self-adjusting threshold-voltage scheme (SATS) for low-voltage high-speed operation," in *Custom Integrated Circuits Conference (CICC)*, 1994, pp. 271-274.

[48] J. Abu-Qahouq, H. Wei, W. Gu, and I. Batarseh, "Analysis and design of soft-switching power factor correction converter," in *ISCAS 2000 Geneva. 2000 IEEE International Symposium on Circuits and Systems. Emerging Technologies for the 21st Century. Proceedings*, Geneva, Switzerland, 2000, pp. 235-8 vol.3.

[49] T. D. Burd and R. W. Brodersen, "Energy efficient CMOS microprocessor design," in *In Proc. of The HICSS Conference*, 1995, pp. 288-97 vol.1.

[50] A. Chandrakasan, V. Gutnik, and T. Xanthopoulos, "Data driven signal processing: an approach for energy efficient computing," in *Low Power Electronics and Design, 1996., International Symposium on*, 1996, pp. 347-352.

[51] T. Kuroda, "Low-power, high-speed CMOS VLSI design," in *IEEE International Conference on Computer Design (ICCD'02)*, 2002, pp. 310-315.

[52] "Pentium II power," *PC Pro*, pp. 80-80-6, 91, 93-2, 104, 114, 10 1997.

[53] B. Arbetter and D. Maksimovic, "DC-DC converter with fast transient response and high efficiency for low-voltage microprocessor loads," in *Applied Power Electronics Conference and Exposition, 1998. APEC apos;98*, 1998, pp. 156-62 vol.1.

[54] W. Li and X. He, "ZVT interleaved boost converters for high-efficiency, high step-up DC-DC conversion," *IET Electric Power Applications*, vol. 1, pp. 284-290, 03 2007.

[55] B. Arbetter, R. Erickson, and D. Maksimovic, "DC-DC converter design for battery-operated systems," 1995, pp. 103-9 vol.1.

[56] S. Janghoon, Y. Gilwon, and K. Chulwoo, "An efficient adaptive digital DC-DC converter with dual loop controls for fast dynamic voltage scaling," in *Conference 2006, IEEE Custom Integrated Circuits*, 2006, pp. 4 pp.-4 pp.

[57] Y. K. Ramadass and A. P. Chandrakasan, "Minimum energy tracking loop with embedded DC-DC converter delivering voltages down to 250mV in 65nm CMOS," in *Solid-State Circuits Conference, 2007. ISSCC 2007. Digest of Technical Papers. IEEE International*, 2007, pp. 64-587.

[58] F. Caruthers, "Battery Technolgy Charges Ahead," Computer Design's OEM Integrations, 1994, pp. 10-14.

[59] S. S. Kelkar and F. C. Lee, "A fast time domain digital simulation technique for power converters: application to a buck converter with feedforward compensation," in *Institute of Electrical and Electronics Engineers, Power Electronics Specialists Conference*, 1984, pp. 397-408.

[60] T. Ninomiya, K. Harada, and M. Nakahara, "Stability analysis of boost and buck-boost converters," *Transactions of the Institute of Electronics and Communication Engineers of Japan, Part C*, vol. J66C, pp. 1-8, 01 1983.

[61] A. K. Panda and K. Aroul, "A novel technique to reduce the switching losses in a synchronous buck converter," in *Power Electronics, Drives and Energy Systems, 2006. PEDES '06. International Conference on*, 2006, pp. 5 pp.-5 pp.

[62] L. Yanbin and A. K. Mok, "An integrated approach for applying dynamic voltage scaling to hard real-time systems," in *Real-Time and Embedded Technology and Applications Symposium, 2003. Proceedings. The 9th IEEE*, 2003, pp. 116-123.

[63] J. Koppanalil, P. Ramrakhyani, S. Desai, A. Vaidyanathan, and E. Rottenberg, "A case for dynamic pipelines scaling," in *International Conference on Compilers, Architecture and Synthesis for Embedded Systems*, Grenoble, France, 2002, pp. 1-8.

[64] T. D. Burd, T. A. Pering, A. J. Stratakos, and R. W. Brodersen, "A dynamic voltage scaled microprocessor system," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 1571-1580, 2000.

[65] B. Mochocki, H. Xiaobo Sharon, and Q. Gang, "A realistic variable voltage scheduling model for real-time applications," in *International Conference on Computer Aided Design*, 2002, pp. 726-731.

[66] D. Fitrio, J. Singh, and A. Stojcevski, "Dynamic voltage scaling implementation for power management," in *IFIP WG 10.5 Conference on VLSI-system on a chip*, 2005, pp. 459-464.

[67] K. Bult and G. J. G. M. Geelen, "An inherently linear and compact MOST-only current division technique," *IEEE Journal of Solid-State Circuits*, vol. 27, pp. 1730-1735, 1992.

[68] R. J. Baker, *CMOS: circuit design, layout, and simulation* vol. 2: IEEE press, Wiley-Interscience, 2002.

[69] E. A. Vittoz and O. Neyroud, "A low-voltage CMOS bandgap reference," *IEEE Journal of Solid-State Circuits*, pp. 573-579, 06 1979.

[70] C. C. Enz and E. A. Vittoz, "CMOS low-power analog circuit design," 1996, pp. 79-133.

[71] B. Linares-Barranco, T. Serrano-Gotarredona, and R. Serrano-Gotarredona, "Compact low-power calibration mini-DACs for neural arrays with programmable weights," *IEEE Transactions on Neural Networks*, vol. 14, pp. 1207-1216, 09 2003.

[72] M. Horowitz, E. Alon, D. Patil, S. Naffziger, K. Rajesh, and K. Bernstein, "Scaling, power, and the future of CMOS," in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, 2005, pp. 7 pp.-7 pp.

[73] R. Gonzalez, B. M. Gordon, and M. A. Horowitz, "Supply and threshold voltage scaling for low power CMOS," *IEEE Journal of Solid-State Circuits*, vol. 32, pp. 1210-1216, 08 1997.

[74] G. Feng, S. Lingling, and L. Jun, "BSIM3v3.2 model parameter extraction and improved model used for RF simulation," in *IET International Conference on Wireless Mobile and Multimedia Networks Proceedings (ICWMMN 2006)*, 2006, pp. 4 pp.-4 pp.

[75] S. W. Smith, *The Scientist and Engineer's Guide to Digital Signal Processing*: California Technical Publishing, 1998.

[76] J. H. Baek, B. S. Son, B. G. Jo, M. H. Sunwoo, and S. K. Oh, "A continuous flow mixed-radix FFT architecture with an in-place algorithm," in *Circuits and Systems, 2003. ISCAS apos;03. Proceedings of the 2003 International Symposium on*, 2003, pp. II-133-II-II-6 vol.2.

[77] J. Lihong, G. Yonghong, I. Jouni, and T. Hannu, "A new VLSI-oriented FFT algorithm and implementation," in *ASIC Conference 1998. Proceedings. Eleventh Annual IEEE International*, 1998, pp. 337-341.

[78] J. Melander, T. Widhe, K. Palmkvist, M. Vesterbacka, and L. Wanhammar, "An FFT processor based on the SIC architecture with asynchronous PE," in

Circuits and Systems, 1996., IEEE 39th Midwest symposium on, 1996, pp. 1313-16 vol.3.

[79] G. R. Kulkarni and V. Udpikar, "An integrated facility for data acquisition and analysis of biomedical signals. Case studies on VEP, IVS," in *Engineering in Medicine and Biology Society, 1995 and 14th Conference of the Biomedical Engineering Society of India. An International Meeting, Proceedings of the First Regional Conference., IEEE*, 1995, pp. 3/67-3/68.

[80] W. Lin, E. Mittra, C. Berman, C. Rubin, and Y. X. Qin, "Measurement of ultrasound phase velocity in trabecular bone using adaptive phase tracking," in *Engineering in Medicine and Biology, 2002. 24th Annual Conference and the Annual Fall Meeting of the Biomedical Engineering Society] EMBS/BMES Conference, 2002. Proceedings of the Second Joint*, 2002, pp. 2583-4 vol.3.

[81] S. Lisha, S. Minfen, and F. H. Y. Chan, "A method for estimating the instantaneous frequency of non-stationary heart sound signals," in *Neural Networks and Signal Processing, 2003. Proceedings of the 2003 International Conference on*, 2003, pp. 798-801 Vol.1.

[82] F. Moller, N. Bisgaard, and J. Melanson, "Algorithm and architecture of a 1 V low power hearing instrument DSP," in *Low Power Electronics and Design, 1999. Proceedings. 1999 International Symposium on*, 1999, pp. 7-11.

[83] C. R. Baugh and B. A. Wooley, "A two's complement parallel array multiplication algorithm," *IEEE Transactions on Computers*, vol. C-22, pp. 1045-1047, 12 1973.

[84] A. Alvandpour, P. Larsson-Edefors, and C. Svensson, "A leakage-tolerant multi-phase keeper for wide domino circuits," in *Electronics, Circuits and Systems, 1999. Proceedings of ICECS '99. The 6th IEEE International Conference on*, 1999, pp. 209-12 vol.1.

[85] M. H. Anis, M. W. Allam, and M. I. Elmasry, "Energy-efficient noise-tolerant dynamic styles for scaled-down CMOS and MTCMOS technologies," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 10, pp. 71-78, 04 2002.

[86] V. Kursun, S. A. Tawfik, and L. Zhiyu, "Leakage-aware design of nanometer SoC," in *Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on*, 2007, pp. 4 pp.-4 pp.

[87] A. Alvandpour, R. K. Krishnamurthy, K. Soumyanath, and S. Y. Borkar, "A sub-130-nm conditional keeper technique," *IEEE Journal of Solid-State Circuits*, vol. 37, pp. 633-638, 05 2002.

[88] V. Kursun and E. G. Friedman, "Domino logic with variable threshold voltage keeper," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 11, pp. 1080-1093, 12 2003.

[89] K. J. Nowka and T. Galambos, "Circuit design techniques for a gigahertz integer microprocessor," in *Computer Design: VLSI in Computers and Processors, 1998. ICCD '98. Proceedings. International Conference on*, 1998, pp. 11-16.

[90] K. Shimizu, T. Shirai, M. Takamura, N. Itazaki, and K. Kinoshita, "Reduction of the target fault list and fault simulation method for crosstalk faults in clock-delayed domino circuits," *IEICE Transactions on Information and Systems*, vol. E85-D, pp. 1526-1533, 10 2002.

[91] G.-q. Hang and Y.-h. Xu, "Novel low-noise current-mode flip-flops for mixed-signal integrated circuits," *Journal of Zhejiang University*, vol. 41, pp. 616-620, 04 2007.

[92] K. Shimazaki, M. Nagata, M. Fukazawa, S. Miyahara, M. Hirata, K. Satoh, and H. Tsujikawa, "An integrated timing and dynamic supply noise verification for multi-10-million gate SoC designs," *IEICE Transactions on Electronics*, vol. E89-C, pp. 1535-1543, 11 2006.

[93] S. Yang, M. D. Powell, B. Falsafi, K. Roy, and T. N. Vijaykumar, "An integrated circuit/architecture approach to reducing leakage in deep-submicron high-performance I-caches," in *High-Performance Computer Architecture, 2001. HPCA. The Seventh International Symposium on*, 2001, pp. 147-157.

[94] D. Fitrio, A. Stojcevski, and J. Singh, "Subthreshold Leakage Current Reduction Techniques for Static RAM," in *SPIE International Symposium on Smart Materials, Nano and Micro-Smart Systems*, 2004, pp. 673-683.

[95] K. Nam Sung, K. Flautner, D. Blaauw, and T. Mudge, "Circuit and microarchitectural techniques for reducing cache leakage power," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 12, pp. 167-184, 2004.

[96] A. Keshavarzi, K. Roy, and C. F. Hawkins, "Intrinsic leakage in low power deep submicron CMOS ICs," in *Proceedings International Test Conference 1997 (ITC'97)*, 1997, pp. 146-155.

[97] N. Shibata, H. Morimura, and M. Harada, "1-V 100-MHz embedded SRAM techniques for battery-operated MTCMOS/SIMOX ASICs," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 1396-1407, 2000.

[98] K. Agawa, H. Hara, T. Takayanagi, and T. Kuroda, "A bitline leakage compensation scheme for low-voltage SRAMs," *IEEE Journal of Solid-State Circuits*, vol. 36, pp. 726-734, 2001.

[99] T. Douseki, N. Shibata, and J. Yamada, "A 0.5-1 V MTCMOS/SIMOX ROM macro with low-V/sub th/ memory cells," in *SOI Conference, 2001 IEEE International*, 2001, pp. 143-144.

[100] M. Ketkar and S. S. Sapatnekar, "Standby power optimization via transistor sizing and dual threshold voltage assignment," in *2002 International Conference on Computer-Aided Design (ICCAD '02)*, 2002, pp. 375-378.

[101] J. T. Kao and A. P. Chandrakasan, "Dual-threshold voltage techniques for low-power digital circuits," *IEEE Journal of Solid-State Circuits*, vol. 35, pp. 1009-1018, 2000.

[102] M. Powell, Y. Se-Hyun, B. Falsafi, K. Roy, and T. N. Vijaykumar, "Gated-V/sub dd/: a circuit technique to reduce leakage in deep-submicron cache memories," in *Low Power Electronics and Design, 2000. ISLPED apos;00. Proceedings of the 2000 International Symposium on*, 2000, pp. 90-95.

[103] T. Chen, J. Huang, Qianjie, and Liangxiao, "Using dynamic and approach static with compiler-assisted power management for DVS-enabled embedded system," *WSEAS Transactions on Computers*, vol. 6, pp. 967-972, 06 2007.

[104] K. Kyong Hoon and K. Jong, "An adaptive DVS checkpointing scheme for fixed-priority tasks with reliability constraints in dependable real-time embedded systems," in *International Conference on Embedded Software and Systems*, 2007, pp. 560-571.

[105] C. Yongseok, C. Naehyuck, and K. Taewhan, "DC-DC converter-aware power management for low-power embedded systems," *IEEE Transactions on Computer-Aided Design of Integrated Circuits*, vol. 26, pp. 1367-1381, 08 2007.

[106] L. Jaejeong, A. Byoungchul, L. Dong Ha, and L. Sang Heon, "A design and implementation of low power management for personal multimedia systems," in *Communications, Computers and Signal Processing, 2007. PacRim 2007. IEEE Pacific Rim Conference on*, 2007, pp. 395-398.

[107] J. L. Nunez-Yanez, V. Chouliaras, and J. Gaisler, "Dynamic voltage scaling in a FPGA-based system-on-chip," in *Field Programmable Logic and Applications, 2007. FPL 2007. International Conference on*, 2007, pp. 459-462.

[108] L. Jeabin, N. Byeong-Gyu, and Y. Hoi-Jun, "Dynamic voltage and frequency scaling (DVFS) scheme for multi-domains power management," in *Solid-State Circuits Conference, 2007. ASSCC apos;07. IEEE Asian*, 2007, pp. 360-363.

[109] W. Phyu Myint, Z. Yuanjin, and Z. Bin, "A 0.18- mu m CMOS multirate filter bank asic for biomedical applications," in *Integrated Circuits, 2007. ISIC '07. International Symposium on*, 2007, pp. 153-156.

[110] K. Kiyoyama, M. Onoda, and Y. Tanaka, "A low current consumption CMOS latched comparator for body-implanted chip," in *Circuits and Systems, 2005. ISCAS 2005. IEEE International Symposium on*, 2005, pp. 1940-3 Vol. 3.

[111] Z.-G. Wang, X. Lu, W. Li, H. Wang, Z. Zhang, Y. Wang, and W. Cui, "Study of microelectronics for detecting and stimulating of central neural signals," Neural Interface and Control, 2005. Proceedings. 2005 First International Conference on, 2005, pp. 192-195.

[112] L. Bor-Shun, H. Jyun-Jhang, W. Wen-Jong, and S. Wen-Pin, "MEMS power receiver using piezoelectric cantilever beams and interdigitated electrodes," in *Systems, Man and Cybernetics, 2006. SMC '06. IEEE International Conference on*, 2006, pp. 3227-3232.

Appendix A: Implemented Encounter Script

Design Script

```
Puts "################################"
Puts "###"
Puts "### Load Design               "
Puts "###"
Puts "################################"

### uniquify the netlist (shell to execute before an encounter session)
### uniquifyNetlist -top

set HCMOS9GP_DIR /usr/local/hcmos9gp_902

setPreference MinFPModuleSize 1
loadConfig ../FILTER.conf

loadfootprint -infile ${HCMOS9GP_DIR}/SocEncounter_hcmos9gp_2.1/hcmos9gp_902.cfp

setInvFootPrint IVLL
setBufFootPrint BFLL
setDelayFootPrint DLY1LLP

setRCFactor -cap 1.1

set blockName design


Puts "################################"
Puts "###"
Puts "### CREATE IO                 "
Puts "###"
Puts "################################"

### add CORNERS and power PADs
loadECO ../FILTER.eco

### IO file
loadIoFile ../FILTER.io


Puts "#########################"
Puts "###"
Puts "### Create Floorplan     "
Puts "###"
```

```
Puts "#########################"

### define floorplan
floorPlan -r 1 0.80 70 70 70 70

### Add IO filler
source ../Script/IO_Filler.tcl


Puts "################################"
Puts "###"
Puts "### Create power stripes "
Puts "###"
Puts "################################"

source ../Script/create_global_net.tcl

### add power ring + stripes
source ../Script/pwr.tcl

### std-cell follow pin
source ../Script/followPin2.tcl

######## add power grid #######
#source ../Script/pwr_h_stripe.tcl
#source ../Script/pwr_v_stripe.tcl
#source ../Script/followPin.tcl

# save floor-plan
#saveFPlan ./fplan.fp

# check floor-plan
verifyGeometry

saveDesign ./FILTER.fp.enc
#source ./FILTER.fp.enc


Puts "####################"
Puts "###"
Puts "### Place Design ..."
Puts "###"
Puts "####################"

exec mkdir Timing

amoebaPlace -timingdriven -doCongOpt -highEffort -ignoreScan -ignoreSpare -QA -slack
init_virtual.slk

saveDesign ./FILTER.place.enc
#source ./FILTER.place.enc
```

```
checkPlace

buildTimingGraph
timeDesign -preCTS -outDir ./Timing/PLACE.timing


Puts "####################"
Puts "###"
Puts "### GPS        ..."
Puts "###"
Puts "####################"

setIPOMode  -highEffort -fixDRC -fixFanoutLoad -maxDensity 0.8 -reclaimArea
optDesign -preCTS

saveDesign ./FILTER.IPO.enc
# source ./FILTER.IPO.enc

timeDesign -preCTS -outDir ./Timing/IPO.timing


Puts "###############"
Puts "###"
Puts "### Run CTS..."
Puts "###"
Puts "###############"

specifyClockTree -clkfile ../FILTER.ctstch

ckSynthesis -forceReconvergent -report FILTER_cts.ctsrpt


saveDesign ./FILTER.POST_CTS.enc
#source ./FILTER.POST_CTS.enc

setAnalysisMode -clockTree

buildTimingGraph
timeDesign -postCTS -outDir ./Timing/POST_CTS.timing


Puts "########################"
Puts "###"
Puts "### GPS  post CTS    ..."
Puts "###"
Puts "########################"

setIPOMode  -highEffort -fixDRC -fixFanoutLoad -maxDensity 0.85 -reclaimArea
optDesign -postCTS

saveDesign ./FILTER.POST_CTS_IPO.enc
# source ./FILTER.POST_CTS_IPO.enc
```

```
timeDesign -postCTS -outDir ./Timing/POST_CTS_IPO.timing


Puts "################################"
Puts "###"
Puts "### Nanoroute            .... "
Puts "###"
Puts "################################"

# Filler Cell between std-cells
addFiller -cell FILLERCELL9 FILLERCELL8 FILLERCELL7 FILLERCELL64
FILLERCELL6 FILLERCELL5 FILLERCELL4 FILLERCELL32 FILLERCELL3
FILLERCELL2 FILLERCELL16 FILLERCELL15 FILLERCELL14 FILLERCELL13
FILLERCELL12 FILLERCELL11 FILLERCELL10 FILLERCELL1 -prefix FILLER

# connect all new std-cell instances to vdd/gnd
source ../Script/create_global_net.tcl


####################
## Route clocks first ##
####################
setAttribute -net @clock -weight 5 -avoid_detour true -bottom_preferred_routing_layer 4 -
preferred_extra_space 1
selectNet -allDefClock
setNanoRouteMode -quiet routeWithTimingDriven false
setNanoRouteMode -quiet envNumberProcessor 1
setNanoRouteMode -quiet route_selected_net_only true

globalDetailRoute


####################
## Route All Nets ##
####################
setNanoRouteMode -quiet routeFixPrewire true
setNanoRouteMode -quiet route_selected_net_only false
setNanoRouteMode -quiet routeWithTimingDriven false
setNanoRouteMode -quiet routeTdrEffort 1
setNanoRouteMode -quiet drouteFixAntenna true
setNanoRouteMode -quiet routeWithSiDriven true
setNanoRouteMode -quiet routeSiLengthLimit 200
setNanoRouteMode -quiet routeSiEffort normal

globalDetailRoute

saveDesign ./FILTER.POST_ROUTE.enc
#source ./FILTER.POST_ROUTE.enc

verifyGeometry
verifyConnectivity
```

```
verifyProcessAntenna

####################
## mode RC detail
####################

#setExtractRCMode -default
#setExtractRCMode -detail
#extractRC
#rcOut -spef FILTER.spef

#buildTimingGraph
timeDesign -postRoute -outDir ./Timing/POST_ROUTE.timing

####################
## last CTS analysis
####################

cleanupSpecifyClockTree
specifyClockTree -clkfile ../FILTER.ctstch
reportClockTree -report post_nr_route_ipo.ctsrpt -clk CLK -postRoute
reportClockTree -report post_nr_route_ipo.ctsrpt -clk RESET -postRoute


Puts "################################"
Puts "###"
Puts "### Post Route Optimization  ..."
Puts "###"
Puts "################################"

deleteFiller -prefix FILLER

setExtractRCMode -detail
extractRC

setIPOMode -highEffort -fixDRC -fixFanoutLoad  -maxDensity 0.85
optDesign -postRoute


##############################
# Filler Cell between std-cells
addFiller -cell FILLERCELL9 FILLERCELL8 FILLERCELL7 FILLERCELL64
FILLERCELL6 FILLERCELL5 FILLERCELL4 FILLERCELL32 FILLERCELL3
FILLERCELL2 FILLERCELL16 FILLERCELL15 FILLERCELL14 FILLERCELL13
FILLERCELL12 FILLERCELL11 FILLERCELL10 FILLERCELL1 -prefix FILLER

# connect all new std-cell instances to vdd/gnd
source ../Script/create_global_net.tcl

##########################"

verifygeometry -allowDiffCellViols
```

```
verifyConnectivity
verifyProcessAntenna

reportLeakagePower

fillnotch

saveDesign ./FILTER.POST_ROUTE_IPO.enc
#source ./FILTER.POST_ROUTE_IPO.enc

setExtractRCMode -detail
extractRC
#buildTimingGraph
timeDesign -postRoute -outDir ./Timing/POST_ROUTE_IPO.timing



Puts "################################"
Puts "###"
Puts "### Create abstract views : verilog / LEF / DEF / TLF / GDS   ..."
Puts "###"
Puts "################################"

exec mkdir RESULTS

########
### verilog
########
saveNetlist ./RESULTS/FILTER.v

########
### lef
########
lefOut ./RESULTS/FILTER.lef -stripePin -PGpinLayers 5 6

#######
### def
#######
defOut -floorplan -routing ./RESULTS/FILTER.def

#######
### gds
#######
streamOut ./RESULTS/FILTER_SoC.gds \
        -mapFile ${HCMOS9GP_DIR}/SocEncounter_hcmos9gp_2.1/gds2.map \
        -libName DesignLib \
        -structureName FILTER \
        -stripes 1 \
        -units 1000 \
        -mode ALL

#######
```

```
### tlf
#######
setExtractRCMode -detail
extractRC

genTlfModel

exec mv FILTER.tlf ./RESULTS/FILTER.tlf

#######
### sdf
#######

delayCal -sdf ./RESULTS/FILTER.sdf
```

Configuration Script

```
################################################
#                                              #
#  FirstEncounter Input configuration file     #
#                                              #
################################################
global HCMOS9GP_DIR
global rda_Input

#set cwd ./work

set rda_Input(import_mode) {-treatUndefinedCellAsBbox 0 -verticalRow 0 -
keepEmptyModule 1 }
set rda_Input(ui_netlist) "../FILTER.v"

set rda_Input(ui_netlisttype) {Verilog}
set rda_Input(ui_ilmlist) {}
set rda_Input(ui_settop) {1}
set rda_Input(ui_topcell) {FILTER}
set rda_Input(ui_celllib) {}
set rda_Input(ui_iolib) {}
set rda_Input(ui_areaiolib) {}
set rda_Input(ui_blklib) {}
set rda_Input(ui_kboxlib) {}
set rda_Input(ui_gds_file) {}
set rda_Input(ui_timelib,min)
"${HCMOS9GP_DIR}/CORE9GPHS_SNPS_AVT_4.1.a/SIGNOFF/bc_1.32V_m40C_wc_1.
08V_125C/PT_LIB/CORE9GPHS_Best.lib
${HCMOS9GP_DIR}/CORE9GPLL_SNPS_AVT_4.1/SIGNOFF/bc_1.32V_m40C_wc_1.08
V_125C/PT_LIB/CORE9GPLL_Best.lib
${HCMOS9GP_DIR}/CORX9GPHS_SNPS_AVT_7.1.a/SIGNOFF/bc_1.32V_m40C_wc_1.0
8V_125C/PT_LIB/CORX9GPHS_Best.lib
```

```
${HCMOS9GP_DIR}/CORX9GPLL_SNPS_AVT_7.1/SIGNOFF/bc_1.32V_m40C_wc_1.08
V_125C/PT_LIB/CORX9GPLL_Best.lib
${HCMOS9GP_DIR}/CLOCK9GPHS_SNPS_AVT_4.1/SIGNOFF/bc_1.32V_m40C_wc_1.0
8V_125C/PT_LIB/CLOCK9GPHS_Best.lib
${HCMOS9GP_DIR}/CLOCK9GPLL_SNPS_AVT_4.1/SIGNOFF/bc_1.32V_m40C_wc_1.0
8V_125C/PT_LIB/CLOCK9GPLL_Best.lib
${HCMOS9GP_DIR}/PR9M6_SNPS_AVT_2.1.a/SIGNOFF/bc_1.32V_m40C_wc_1.08V_12
5C/PT_LIB/PR9M6_Best.lib
${HCMOS9GP_DIR}/IOLIB_65_M6_LL_HCMOS9GP_SNPS_AVT_7.1/SIGNOFF/bc_1.32
V_m40C_wc_1.08V_125C/PT_LIB/IOLIB_65_M6_LL_Best.lib
${HCMOS9GP_DIR}/IOLIB_65_3V3_M6_LL_65A_HCMOS9GP_SNPS_AVT_7.0/SIGNO
FF/bc_1.32V_m40C_wc_1.08V_125C/PT_LIB/IOLIB_65_3V3_M6_LL_65A_Best.lib
${HCMOS9GP_DIR}/IOLIB_65_FT_M6_LL_65A_HCMOS9GP_SNPS_AVT_7.1/SIGNOF
F/bc_1.32V_m40C_wc_1.08V_125C/PT_LIB/IOLIB_65_FT_M6_LL_65A_Best.lib"

set rda_Input(ui_timelib,max)
"${HCMOS9GP_DIR}/CORE9GPHS_SNPS_AVT_4.1.a/SIGNOFF/bc_1.32V_m40C_wc_1.
08V_125C/PT_LIB/CORE9GPHS_Worst.lib
${HCMOS9GP_DIR}/CORE9GPLL_SNPS_AVT_4.1/SIGNOFF/bc_1.32V_m40C_wc_1.08
V_125C/PT_LIB/CORE9GPLL_Worst.lib
${HCMOS9GP_DIR}/CORX9GPHS_SNPS_AVT_7.1.a/SIGNOFF/bc_1.32V_m40C_wc_1.0
8V_125C/PT_LIB/CORX9GPHS_Worst.lib
${HCMOS9GP_DIR}/CORX9GPLL_SNPS_AVT_7.1/SIGNOFF/bc_1.32V_m40C_wc_1.08
V_125C/PT_LIB/CORX9GPLL_Worst.lib
${HCMOS9GP_DIR}/CLOCK9GPHS_SNPS_AVT_4.1/SIGNOFF/bc_1.32V_m40C_wc_1.0
8V_125C/PT_LIB/CLOCK9GPHS_Worst.lib
${HCMOS9GP_DIR}/CLOCK9GPLL_SNPS_AVT_4.1/SIGNOFF/bc_1.32V_m40C_wc_1.0
8V_125C/PT_LIB/CLOCK9GPLL_Worst.lib
${HCMOS9GP_DIR}/PR9M6_SNPS_AVT_2.1.a/SIGNOFF/bc_1.32V_m40C_wc_1.08V_12
5C/PT_LIB/PR9M6_Worst.lib
${HCMOS9GP_DIR}/IOLIB_65_M6_LL_HCMOS9GP_SNPS_AVT_7.1/SIGNOFF/bc_1.32
V_m40C_wc_1.08V_125C/PT_LIB/IOLIB_65_M6_LL_Worst.lib
${HCMOS9GP_DIR}/IOLIB_65_3V3_M6_LL_65A_HCMOS9GP_SNPS_AVT_7.0/SIGNO
FF/bc_1.32V_m40C_wc_1.08V_125C/PT_LIB/IOLIB_65_3V3_M6_LL_65A_Worst.lib
${HCMOS9GP_DIR}/IOLIB_65_FT_M6_LL_65A_HCMOS9GP_SNPS_AVT_7.1/SIGNOF
F/bc_1.32V_m40C_wc_1.08V_125C/PT_LIB/IOLIB_65_FT_M6_LL_65A_Worst.lib"

set rda_Input(ui_timelib) {}
set rda_Input(ui_smodDef) {}
set rda_Input(ui_smodData) {}
set rda_Input(ui_dpath) {}
set rda_Input(ui_tech_file) {}
set rda_Input(ui_io_file) {}
set rda_Input(ui_timingcon_file) {../FILTER.sdc }
set rda_Input(ui_latency_file) {}
set rda_Input(ui_scheduling_file) {}
set rda_Input(ui_buf_footprint) {}
set rda_Input(ui_delay_footprint) {}
set rda_Input(ui_inv_footprint) {}
set rda_Input(ui_leffile)
"${HCMOS9GP_DIR}/SocEncounter_hcmos9gp_2.1/hcmos9gp_soc_2.1.lef
${HCMOS9GP_DIR}/CORE9GPHS_SNPS_AVT_4.1.a/SIGNOFF/common/LEF/CORE9GP
```

```
HS_ANT.lef
${HCMOS9GP_DIR}/CORE9GPLL_SNPS_AVT_4.1/SIGNOFF/common/LEF/CORE9GPL
L_ANT.lef
${HCMOS9GP_DIR}/CORX9GPHS_SNPS_AVT_7.1.a/SIGNOFF/common/LEF/CORX9GP
HS_ANT.lef
${HCMOS9GP_DIR}/CORX9GPLL_SNPS_AVT_7.1/SIGNOFF/common/LEF/CORX9GPL
L_ANT.lef
${HCMOS9GP_DIR}/CLOCK9GPHS_SNPS_AVT_4.1/SIGNOFF/common/LEF/CLOCK9G
PHS_ANT.lef
${HCMOS9GP_DIR}/CLOCK9GPLL_SNPS_AVT_4.1/SIGNOFF/common/LEF/CLOCK9G
PLL_ANT.lef
${HCMOS9GP_DIR}/PR9M6_SNPS_AVT_2.1.a/SIGNOFF/common/LEF/PR9M6_ANT.lef
${HCMOS9GP_DIR}/IOLIB_65_M6_LL_HCMOS9GP_SNPS_AVT_7.1/SIGNOFF/commo
n/LEF/IOLIB_65_M6_LL.lef
${HCMOS9GP_DIR}/IOLIB_65_3V3_M6_LL_65A_HCMOS9GP_SNPS_AVT_7.0/SIGNO
FF/common/LEF/IOLIB_65_3V3_M6_LL_65A.lef
${HCMOS9GP_DIR}/IOLIB_65_FT_M6_LL_65A_HCMOS9GP_SNPS_AVT_7.1/SIGNOF
F/common/LEF/IOLIB_65_FT_M6_LL_65A.lef"

set rda_Input(ui_core_cntl) {aspect}
set rda_Input(ui_aspect_ratio) {1.0}
set rda_Input(ui_core_util) {0.7}
set rda_Input(ui_core_height) {}
set rda_Input(ui_core_width) {}
set rda_Input(ui_core_to_left) {}
set rda_Input(ui_core_to_right) {}
set rda_Input(ui_core_to_top) {}
set rda_Input(ui_core_to_bottom) {}
set rda_Input(ui_max_io_height) {0}
set rda_Input(ui_row_height) {4.92}
set rda_Input(ui_isHorTrackHalfPitch) {0}
set rda_Input(ui_isVerTrackHalfPitch) {1}
set rda_Input(ui_ioOri) {R0}
set rda_Input(ui_isOrigCenter) {0}
set rda_Input(ui_exc_net) {}
set rda_Input(ui_delay_limit) {1000}
set rda_Input(ui_net_delay) {1000.0ps}
set rda_Input(ui_net_load) {0.5pf}
set rda_Input(ui_in_tran_delay) {120.0ps}
set rda_Input(ui_captbl_file) {}
set rda_Input(ui_defcap_scale) {1.0}
set rda_Input(ui_detcap_scale) {1.0}
set rda_Input(ui_xcap_scale) {1.0}
set rda_Input(ui_res_scale) {1.0}
set rda_Input(ui_shr_scale) {1.0}
set rda_Input(ui_time_unit) {none}
set rda_Input(ui_cap_unit) {}
set rda_Input(ui_oa_reflib) {}
set rda_Input(ui_oa_abstractname) {}
set rda_Input(ui_sigstormlib) {}
set rda_Input(ui_cdb_file) {}
set rda_Input(ui_echo_file) {}
```

```
set rda_Input(ui_xilm_file) {}
set rda_Input(ui_qxtech_file) {}
set rda_Input(ui_qxlib_file) {}
set rda_Input(ui_qxconf_file) {}
set rda_Input(ui_pwrnet) {vdd vdde vdd5 }
set rda_Input(ui_gndnet) {gnd gnde \
REFA REFB REFC REFD KOFF \
A6SRC A5SRC A4SRC A3SRC A2SRC A1SRC A0SRC \
}
set rda_Input(flip_first) {1}
set rda_Input(double_back) {1}
set rda_Input(assign_buffer) {1}
set rda_Input(ui_gen_footprint) {0}
```

Appendix B: Buck Converter Plot MATLAB Code

```
Vd = 1.2
Vo = 1
Vr = 1
R = 5
fsw = input('Enter Switching Frequency in KHz ');
Ripple = input('Enter allowed % ripple ');
fsw = fsw*1E3
deltaV = (Ripple/100)*Vo
DC = Vo/Vd;
LC = 0.125*((1/fsw)^2)*(1-DC)*(Vo/deltaV)
C = input('Enter value of C in uF ');
C = C*1E-6;
L = LC/C
R1 = input ('Enter value of R1 (K) between 2 & 5 ');
R1 = R1*1E3;
rC = input ('Enter value of ESR ');
rL = input ('Enter value of DCR ');
DBW = 0.3*fsw
FESR = 1/(2*3.1415926535*rC*C)
FLC= 1/(2*3.1415926535*sqrt(L*C))
Rz2 = (DBW/FLC)*(Vr/Vd)*R1
Cz2 = 1/(3.14159*Rz2*FLC)
Cp1 = Cz2/((2*3.14159*Rz2*Cz2*FESR)-1)
Rz3 = R1/((fsw/(2*FLC))-1)
Cz3 = 1/(3.14159*Rz3*fsw)
s = tf('s');
% Transfer Function of Buck Converter
G = Vd/Vr; % 1/Vr is the effect of the PWM
N = 1+s*(rC*C);
D = 1+s*((L+((rC+rL)*R*C))/R)+(s^2)*(L*C);
Buck = (G*(N/D));
figure(1)
margin(Buck)
grid
G1 = (R1+Rz3)/(R1*Rz3*Cp1);
N1 = s + (1/(Rz2*Cz2));
N2 = s + (1/((R1+Rz3)*Cz3));
D0 = s;
D1 = s + ((Cp1+Cz2)/(Rz2*Cp1*Cz2));
D2 = s + (1/(Rz3*Cz3));
Type3 = G1*((N1*N2)/(D0*D1*D2));
figure(2)
bode(Type3)
grid
BuckType3 = Buck*Type3
figure(3)
```