A Reconfigurable High Speed Analog to Digital Converter Architecture for Ultra Wideband Devices

By,
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Submitted in Fulfilment of the Requirement for
The Degree of Doctor of Philosophy

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To my parents

Ananthakrishnan Mohan

&

Lakshmi Mohan

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Declaration of Originality

"I, **Anand Mohan**, declare that the PhD thesis entitled "**Reconfigurable Analog to Digital Converter Architecture for Ultra Wideband Devices**" is no more than 100,000 words in length, exclusive of tables, figures, appendices, references and footnotes. This thesis contains no material that has been submitted previously, in whole or in part, for the award of any other academic degree or diploma. Except where otherwise indicated, this thesis is my own work".

Signature: Date:

(Anand Mohan)

Acknowledgement

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List of Abbreviations

PDA	Personal Desktop Assistant
GPR	Ground Penetrating Radar
MHz	Megahertz
GHz	Gigahertz
UWB	Ultra Wide Band
RF	Radio Frequency
ADC	Analog to Digital Converter
CMOS	Complementary Metal Oxide Semiconductor
IEEE	Institute of Electrical and Electronic Engineers
DS-UWB	Direct Sequence—Ultra Wide Band
MB-OFDM	Multi-Band Orthogonal Frequency Division Multiplexing
HOSO	Home Office Small Office
RISC	Reduced Instruction Set Computer
EEG	Electroencephalogram
ECG	Electrocardiogram
WLAN	Wireless Local Area Network
GPS	Global Positioning System
PAM	Pulse Amplitude Modulation
PPM	Pulse Position Modulation
BPSK	Binary Phase Shift Keying

SNR	Signal to Noise Ratio
CDMA	Code Division Multiple Access
WPAN	Wireless Personal Area Network
BPF	Band Pass Filter
LNA	Low Noise Amplifier
AGC	Automatic Gain Control
MF	Matched Filter
OPSK	Orthogonal Phase Shift Keying
FFT	Fast Fourier Transform
NBI	Narrow Band Interference
FEC	Fixed Error Code
Σ-Δ	Sigma—Delta
SAR	Successive Approximation Register
LSB	Least Significant Bit
MSB	Most Significant Bit
CCD	Charge Coupled Device
DAC	Digital to Analog Converter
L-O	Local Oscillator
BER	Bit Error Rate
NF	Noise Figure
DRAM	Dynamic Random Access Memory
OP-AMP	Operational Amplifier
PSRR	Power Supply Rejection Ratio

NML	Non—Minimal Length
GBW	Gain Band Width
CMFB	Common Mode Feed Back
INL	Integral Non Linearity
DNL	Dynamic Non Linearity
SQNR	Signal to Quantisation Noise Ratio
SNDR	Signal to Noise Dynamic Range
SFDR	Spurious Free Dynamic Range
ENOB	Effective Number of Bits
THD	Total Harmonic Distortion
NMOS	N-Type Metal Oxide Semiconductor
PMOS	P-Type Metal Oxide Semiconductor
CML	Common Mode Logic
PMC	Probability of Missing Code
BT	Bluetooth
AMUX	Analog Multiplexer
PTC	Pass Transistor Configuration
HVT	High—V_T
SVT	Standard—V_T
ISI	Inter Symbol Interference
VAMS	Verilog Analog Mixed Signal

List of Publications

1. Mohan, A., Zayegh, A., Stojcevski, A., "New Design Scheme For High Speed Analog To Digital Converters", *Published in Journal of Association for Modelling and Simulation (AMSE),* France, 2009.

2. A. Mohan, A. Zayegh, A. Stojcevski, "A High Speed Analog to Digital Converter for Ultra Wide Band Applications", *Lecture Notes in Computer Science, Springer—Verlag Book Chapter EUC—2007*, pp. 169—180.

3. Mohan, A., Zayegh, A., Stojcevski, A., "Performance Comparison of Flash and Reconfigurable ADC for UWB Applications", *International Conference on Modelling and Simulation (AMSE 2010)*, Prague, 2010. In Press.

4. Mohan, A., Zayegh, A., Stojcevski, A., "A 90nm Low-Power High Speed Encoder Design for UWB Flash Analog to Digital Converter", *Proceedings of the International Conference on Modelling and Simulation (MS'08)*, Jordan, 2008.

5. Mohan, A., Zayegh, A., Stojcevski, A., "High Speed Ultra Wide Band Comparator in Deep Sub-Micron CMOS", *Proceedings of the IEEE International Symposium on Integrated Circuits (ISIC'07)*, Singapore, 2007, pp. 386—389.

6. Mohan, A., Zayegh, A., Stojcevski, A., "Comparator for High Speed Ultra Wideband A/D Converter", *Proceedings of the IEEE International Conference on Communication, Computer and Power (ICCCP'07),* Oman, 2007, pp. 1—5.

Abstract

In a world where wires still dominate high speed low power data communication, Ultra Wideband (UWB) medium has the potential to revolutionise wireless data transmission and reception. The UWB standards such as Direct Sequence UWB (DS-UWB) offer the unique possibility for very high speed low power communications with reduced device count and minimal interference from other communication mediums. The applications of this technology range from Wireless In-home device connectivity, short range man-to-man battlefield military communication to biomedical applications requiring continuous and immediate data transmission.

A core component of any communications device is its ability to convert real time analog signals to discrete values for fast and efficient processing. This gate that links the digital backend with the analogue front end is the Analogue to Digital Converter.

This thesis presents the design and implementation of two unique high speed analog to digital converters for Ultra Wideband radio. The first design is a custom fully differential Flash based analogue to digital converter with a finite output resolution of 4 bits and an effective sampling rate of 5 Gsps. The custom flash converter has an effective maximum power consumption of 286 mW, occupying an active total chip die area of 0.89 μm^2.

The second design implemented is a novel fully differential reconfigurable analog to digital converter. The performance of the novel reconfigurable converter is comparable to the Flash architecture but offers a dynamic output resolution from 1 to 4 bits. The reconfigurability has been implemented by a unique combination of high speed comparators and analog multiplexers. The design offers substantial savings in terms of power consumption and total area. Analysis of the converter function revealed a maximum effective power consumption of 197 mW with an active total chip die area of 0.282 μm^2. The reconfigurable converter achieves a 32% reduction in the power consumption compared to the custom flash design, with a saving of 58% in the area.

Chapter I: **Overview**

1.1 Introduction to this Research

Imagine a world of seamless connectivity without the hassle of wires criss-crossed in every which way making communication straightforward and uncomplicated. The advent of wireless technology has to a large extent brought closer the dream of a world without wires. Although wires still are the primary mode of secure and efficient communications, wireless technology is making inroads into systems and devices, such that efficiency and quality of service are still paramount.

There is an increasingly ferocious demand for systems and devices to function bereft of physical connections, be it in consumer electronics, bio-medical systems, construction and logistics or even for military applications. The market for consumer electronics has become the driving force in the use of wireless systems for high speed data transfer with good efficiency. Devices, such as Personal Desktop Assistant (PDA), Ground Penetrating Radar (GPR) and others, increasingly rely on wireless connectivity to send and receive data at very high speed, at short range and with high accuracy. One of the limitations in the implementation of such devices is the restricted availability in the use of commercially available communication frequency spectrum. The use of commercial radio frequency bands was restricted to bandwidths of the order of a few 100 Megahertz (MHz) to a Gigahertz (GHz) [1-3]. This enabled secure viable communication for needs restricted to narrowband applications, however in an ever changing world where there is an insatiable need of more for less, this brought about a problem of lack of bandwidth and overcrowding. In 2002, the Federal Communications Commission

(FCC) in the United States de-regulated the use of a block of frequency spectrum from 3.1 GHz to 10.6 GHz, previously used for military purposes and made it available for commercial uses [4]. Subsequently other countries including in Europe, Japan and Australia de-regulated the use of this block of frequencies for commercial applications, commonly known as the Ultra Wideband (UWB) spectrum [5]. This brought about huge revolution in the use of such a large frequency band and also with it new and ever improving system and device design methodologies.

1.2 Motivation

Ultra Wideband communication standard differs from conventional narrowband standards, such that each slice of information energy transmitted is distributed over an extremely wide frequency band unlike traditional narrowband standards. For example a simple sinusoid signal would appear as a spike or pulse in the transmission scheme as compared to a fully defined signal [6]. Some advantages that such a transmission scheme offers are the ability for;

a. Higher data transmission rates

b. Resistance to multipath fading and jamming

c. Reduced cost of off-the-shelf devices, amongst others;

Figure 1.1 shows the architecture of a simple Ultra Wideband Receiver.

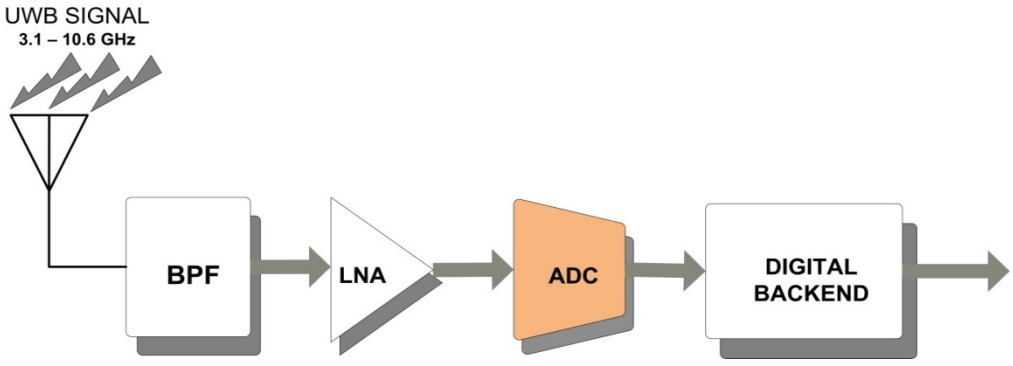


Figure 1.1: Block level diagram of UWB Receiver chain with ADC highlighted

The receiver consists of an antenna, radio frequency (RF) front end, analog-to-digital converter (ADC) and the digital backend. These blocks collectively receive, amplify, convert to bits and process any incoming signal impinged on the antenna. The highlighted part in Figure 1.1 is an analog-to-digital converter. The ADC is a core component of any receiver system. It is the gateway between the analog and the digital domains. Considering the fact that UWB signals are spread out over a large frequency range, the role of the analog-to-digital converter is crucial to sample and digitise each and every slice of information received. For such a task would require an ADC of very high sampling capability, good linearity margin, sufficient gain, moderate resolution and low power consumption [6, 7].

High speed design and low power consumption are the defining parameters in this research. This research involves circuit design techniques and topologies to obtain a reconfigurable ADC architecture that encompasses the primary goals concerning speed and power consumption. The main scope of this work targets applications for In-home wireless connectivity and Bio-Medical devices. Complementary Metal Oxide Semiconductor (CMOS) transistor technology is used for simulation and implementation purposes.

1.3 Research Aims and Objectives

The objective of this research is to design and implement reconfigurable analog-to-digital converter architecture for applications in In-home wireless systems and bio-medical devices. The specific aims of this research are;

- To investigate different Ultra Wideband receiver architectures and specify their requirements for In-home wireless and Bio-medical systems,
- Develop and implement a high speed CMOS Comparator,
- Review different architectures and implement a suitable high speed flash analog-to-digital converter architecture for In-home wireless and Bio-medical applications,

- Investigate reconfigurability property and implement a reconfigurable analog-to-digital converter architecture.
- Implement, analyse and compare the performance of the reconfigurable analog-to-digital converter specific to Ultra Wideband requirement for In-home wireless and Bio-Medical applications.

1.4 Techniques and Design Methodologies

The proposed techniques and design methodologies adopted in this research to accomplish the aforementioned aims are as follows;

- **Investigate different Ultra Wideband receiver architectures and specify their requirements;**

  An extensive study into different UWB receiver architectures will be carried out initially. As ultra high speed, low power consumption and re-configurability in design are the major aims of this research, a deep understanding of the specific requirements for the ADC will be obtained. A complete system level mathematical model of the UWB receiver architecture was performed. The different ADC parameters were then extracted and applied for use in the design.

- **Develop and Implement a high speed CMOS Comparator;**

  As the comparator is the heart of the analog-to-digital converter, different architectures of high speed comparators were studied and investigated. The most viable topology was then tested and optimised for performance and low power consumption with high switching speeds. Industry standard technology file and process have been used to verify its proper functionality.

- **Implementation of a suitable high speed custom Flash analog-to-digital converter architecture;**

  Different architectures for high speed ADC's were studied and modelled. The most suitable architecture then implemented and tested for its performance

corresponding to UWB specifications. Techniques for optimising speed and reduce power dissipation were also used for testing.

- **Review and Implement a Novel Reconfigurable analog-to-digital converter architecture;**

  Three of the most recent and viable reconfigurable architectures were reviewed analysed and detailed. A novel architecture of a reconfigurable analog-to-digital converter was then implemented and tested for its performance in terms of speed, power consumption, gain and resolution switching capability.

- **Implementation, Analysis and Comparison of designed converters;**
  A comprehensive analysis of both implementations, specifying benefits and trade-offs of each design then compared amongst each other to determine their suitability for UWB communications.

The entire system was then put together, including the novel reconfigurable architecture and the control system and tested for its optimum performance on an ST-Microelectronics® CMOS 90 nanometre 7-Metal Layer® transistor technology platform using Cadence Tools. Figure 1.2 shows the representation of the novel architecture implemented in this research.

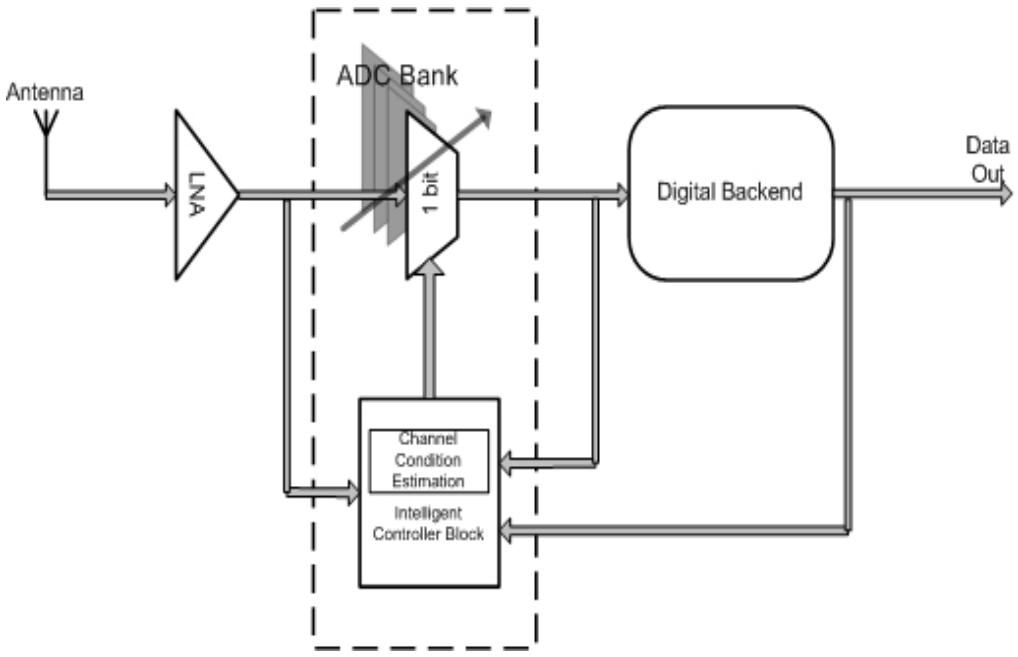


Figure 1.2: Representation of the Novel Reconfigurable Architecture

1.5 Originality of Thesis

This dissertation makes an effort to address the requirements for a high speed, low power, low cost, reliable mixed-signal analog to digital circuit design scheme, applicable to In-home wireless and Bio-medical devices.

This research therefore represents a contribution of knowledge in following key areas:

Power: The design and implementation of the reconfigurable ADC helps reduce the system complexity and power consumption, thereby increasing system efficiency and performance. The re-configurability property of the ADC plays a major role, as well as the design and implementation of a high speed comparator.

Performance: The performance of the device will be greatly improved with the implementation of the re-configurability property. The performance can now be varied to reflect the operating conditions of the circuit.

Speed: The device maintains the capability of high speed operation due to the implementation of a novel ADC architecture based on a high performance comparator and a fast analog multiplexer that can handle large bandwidths and therefore switch faster.

Weight: Portability being the operative word in communication systems, the implementation of this architecture has resulted in overall reduction in the number of components used in the receiver. This brings closer the single-chip idea of the entire receiver implemented on one substrate with no external components, thereby reducing the overall size and weight of the device.

Functionality: The device functionality has been increased with more options for easier implementation. The re-configurability property of the ADC provides the flexibility that is required for lower power consumption in UWB systems.

Cost: With reduced component numbers and implementation in CMOS technology, it has the potential to be a definite low cost solution. This is because CMOS technology currently offers the lowest and most cost effective viable chip implementation options available.

1.6 Thesis Organisation

This thesis is organised into 8 chapters. Subsequent to the Overview, Chapter 2 presents a literature survey of Ultra Wideband communication. A brief background of UWB and its origins have been described. Efforts to standardise UWB by the Institute of Electrical and Electronics Engineers (IEEE) and also the parameters set by different countries, including Australia have been presented. Direct-Sequence UWB (DS-UWB) and Multi-Band Orthogonal Frequency Division Multiplexing (MB-OFDM), the two main standards of UWB communication standards have been considered, with their advantages and disadvantages detailed carefully. Chapter 3 looks at the gateway between the analog and digital domain, the ADC. Different architectures have been presented and detailed. Some high speed architectures including Flash, Sub flash and Pipeline have been detailed more extensively with comparisons of their performance based on resolution, switching speed, gain, linearity, amongst others. Chapter 4 describes a high speed comparator architecture used in this work. Circuit techniques for building high speed topologies including, switch based logic, sample and hold and track-and-latch have been extensively reviewed. The chapter sets the requirements of the analog-to-digital converter and also details the proposed comparator architecture. It describes the construction, implementation and performance optimisation of the comparator architecture, further looking at gain, offset margin and metastability issues. Chapter 5 discusses the design techniques of each module of the Flash ADC architecture. It looks into topologies for voltage ladders, encoder and gate design styles and integration of the comparator and encoder sub-blocks. The chapter presents the implementation of the converter architecture and also describes layout considerations affecting chip performance and area. The architecture of a novel reconfigurable ADC is detailed in Chapter 6. The chapter also presents few reconfigurable topologies, describes the concept and implementation of supply switches, use of multiplexers and their role in the implementation of the reconfigurable architecture. The concept of a controller is also proposed and details its integration into the novel architecture. Chapter 7 presents the overall integration of the two ADC architectures detailed in this work. Performance comparisons of the two architectures have been made to determine the effectiveness of

each topology. Chapter 8 concludes this work and discusses at possibility of future work ensuing this dissertation.

1.7 Summary and Conclusions

This dissertation is a study into integrated circuit design, mixed signal architectures, communication standards, reconfigurable concepts, to name a few, targeting In-home wireless communications and Bio-medical devices. The study is an attempt to address the ever evolving challenges of portability, speed and power consumption that are the principal factors affecting In-home wireless and Bio-medical systems.

Chapter II: **Ultra Wideband**

2.1 Introduction to Ultra Wideband

Ultra Wideband (UWB) is a means of communication that's historically as old as Morse code but is new in its potential for far reaching applications. It is a communication scheme that primarily uses the frequency spectrum from 3.1 GHz to 10.6 GHz for short range, low power and high speed-high bandwidth communications. Communication is based on the use of sharp pulses with coded data represented by each of these pulses hovering about a centre axis frequency at very low emission levels minus the use of a high frequency carrier. Each pulse is miniscule in its time frame such that its energy is spread over the entire frequency range [6].

In the 1960s, UWB was primarily harnessed for its potential use in military applications [3, 6, 8]. In 2002, when the FCC in USA deregulated its use, it brought with it a host of issues and challenges. A UWB signal has a bandwidth of at least 500 MHz or a fractional bandwidth of 25 percent of its centre frequency [9, 10]. Ultra Wideband brings with it unique properties of non-interference with other systems, immunity to multi-path fading, frequency and bandwidth adaptive, simple system architecture, low cost digital solutions and being extremely difficult to detect. Figure 2.1 shows that a UWB signal spectrum occupies a wide frequency range and sits at a very low power level (-41.3dBm) as compared to other communication systems [3, 6, 11]. This is because the FCC has placed a limit on the amount of power that can be used by UWB device to minimise interference to other frequency devices. The limit means that only very low

power can be used for transmission and reception of UWB signals thereby effectively restricting the use of UWB to indoor, short-range communications for high data rates or very low data rates at substantial distances [12, 13].

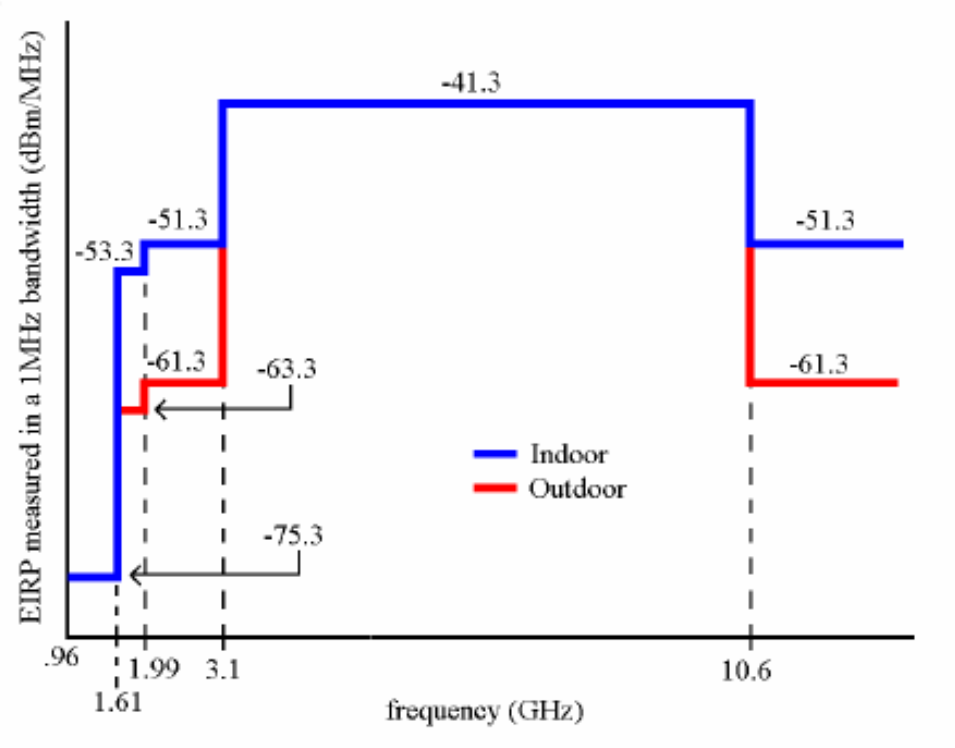


Figure 2.1: Spectral mask frequency occupancy of the UWB spectrum as defined by the FCC [4]

2.2 Applications of Ultra Wideband

Applications of Ultra Wideband range from usage in cellular networks, radar positioning to imaging, inter satellite tracking for military applications, seamless In-home wireless connectivity, Bio-medical health monitoring and physical/psychometric analysis, Transport and collision avoidance safety protocol systems, amongst others. In this thesis the main target of UWB is its potential for application for Bio-medical health care monitoring, In-home wireless connectivity and transport safety protocols.

2.2.1 In-home Wireless Connectivity

The potential use of Ultra Wideband for this application has in some measure brought about a revolution in the Home/Home Office/Small Office (HOSO) wireless connectivity segment. As Figure 2.2 illustrates, Ultra Wideband can be used as a connecting medium among many of these devices without the need to use dedicated cabling.

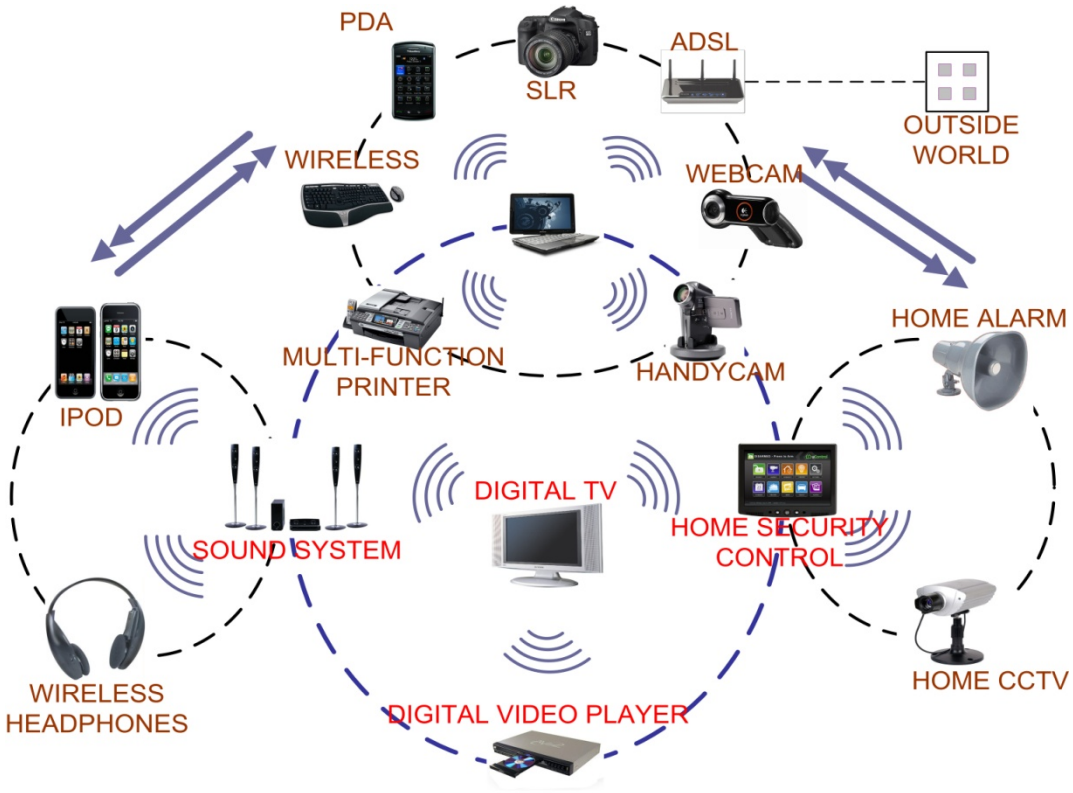


Figure 2.2: Seamless connectivity offered by UWB medium for HOSO environment

This reduces overall clutter and allows for a seamless integration of various systems and devices. The advantage of Ultra Wideband for such connectivity is its ability for high speed data transfer without the effects of interference from narrowband devices in its vicinity and also its previously mentioned capability to reject multi-path fading and jamming. This means that interconnectivity between multitudes of devices is possible without the loss of any data unlike narrowband systems. This allows a user sitting in a room at home to monitor and be aware of the situation of the security system present inside the house. The connectivity ensures that in-case of a breach the system is able to alert not only the owner but also emergency service for quick and effective response.

The system can be made to adapt to different condition prevalent in HOSO environments [14, 15].

2.2.2 Bio-Medical Applications

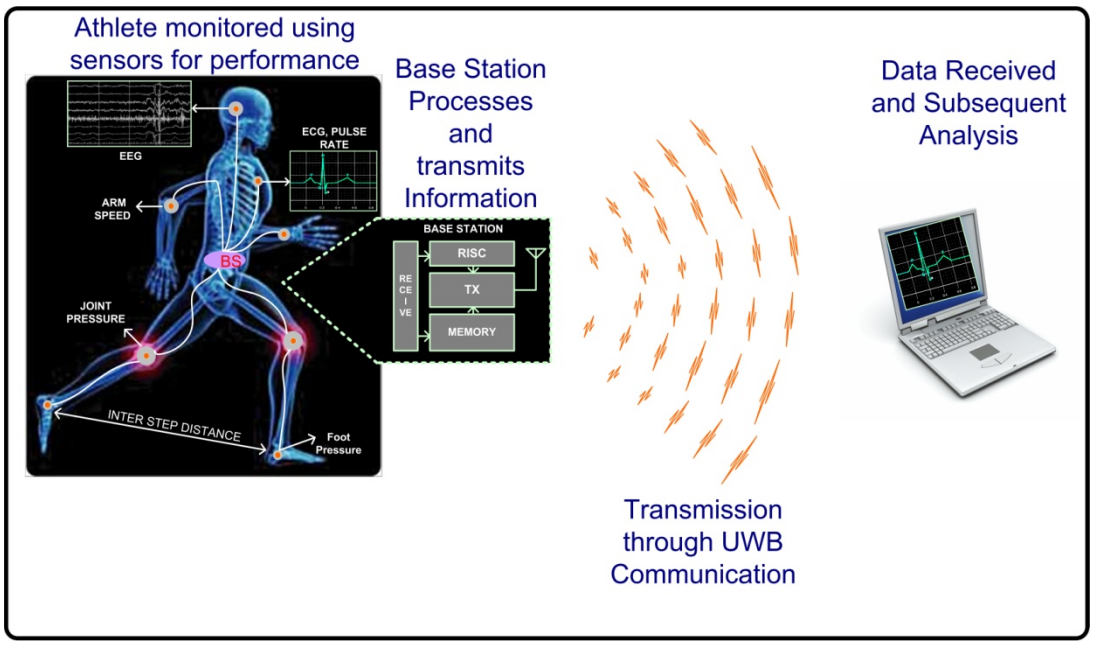


Figure 2.3: Application of Ultra Wideband transmission scheme put to use in the continuous monitoring of an athlete's training session

The potential for use of Ultra Wideband in Bio-Medical health care systems is enormous. The above Figure 2.3 is a typical example of its use for healthcare monitoring. The human in the figure is an athlete who has sensors place all over his body to monitor his vital signs including Electroencephalogram (EEG) for brain waves patterns, Electrocardiogram (ECG) for heart, arm speed, pressure on joints, inter-feet distance and pressure. The sensors transmit all the relevant information into a small base station comprising of a simple receiver, Reduced Instruction Set Computer (RISC) and memory module.

The information is then collated and transmitted by a simple transmitting module and antenna using the Ultra Wideband frequency range at a high data transfer rate to a computer for further analysis and processing. The information transmitted and received is a continuous process occurring in real-time to enable a medical physiotherapist to

ascertain if there are any potential for danger's to the athlete invoke the required preventative care measures.

This type of monitoring is finds usage in a host of other bio-medical situations concerning patient monitoring and preventative healthcare. The technique can be used inside hospitals to transmit patient's vital information to monitoring stations located throughout to enable quick and effective detection and cure. The scheme also finds use for patients who need continuous monitoring in aged-care centres and at bed-ridden at home, such that any deviation from set care patterns are immediately monitored and transmitted wirelessly to emergency centres. Monitoring include vitals such as temperature, blood pressure, respiration, pulse rate, detection of elderly patients falling or slipping, and patients with life-term medical conditions such as asthma, hypertension, obesity, post-operative recovery amongst others. The wireless monitoring also enables the patient to have a degree of freedom not be restricted to the length of the wires for their movement. The high speed communication scheme is also resistant to interference from mobile phones or Wireless Local Area Networks (WLAN) which are traditionally narrowband devices [16, 17].

2.2.3 Transport and Collision Avoidance Systems

Ultra Wideband is used as an effective means to manage transport safety systems and collision avoidance equipment. Vehicles fitted with Ultra Wideband sensors can be used to talk to each other in case of a dangerous situation and pre-programmed to apply immediate safety procedures so as to avoid the possibility of an incident. The application in this field is not only restricted to road vehicles but can also be adapted to suit vessels on water and certain types of aircraft that perform close formation manoeuvres.

This capability of UWB is unique in its ability to work in an environment full of other narrowband systems that are pre-existent and still perform with minimal interferences. Roadside collision avoidance systems use Ultra Wideband communication to effectively detect vehicular speed and also inform the driver of a potential accident spot to avoid crashing into barriers or other obstructions [18].

2.2.4 Precision Location and Tracking

Precision locating and tracking is another application of UWB that has wide ranging potential. The position locating and tracking plays an important part in disaster scenario's where emergency personnel need to know where each other are to effectively co-ordinate rescue and relief operations. The advantage that Ultra Wideband offers is that its high speed minimal interference communication solution can be used more effectively than satellite based Global Positioning Systems (GPS), which are susceptible to co-ordinate error and weather changes. A unique advantage lies in bushfire-fighting techniques where UWB clearly offers an advantage over traditional GPS location and tracking, which is affected by conditions of extreme smoke and fire [19, 20].

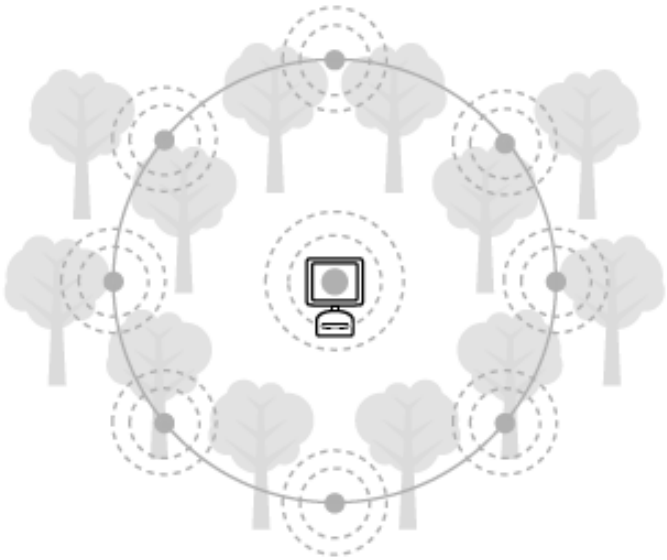


Figure 2.4: Sensor node to detect forest fires [20]

2.3 Characterising Ultra Wideband

The most important characteristic of Ultra Wideband based devices is their ability to transfer data at very high rate with very low power consumption at short distances. This is demonstrated by Shannon's Channel Capacity model given in equation 2.1.

$$C = f_B \times \log_2\left[1 + \frac{Signal}{Noise}\right] \tag{2.1}$$

where C is the Channel Capacity (bits per second) and f_B is the Channel Bandwidth (Hertz). Before dwelling in detail, let us first define UWB and put a perspective on its signalling scheme [6, 21].

2.3.1 Ultra Wideband signal and pulse shape

A UWB signal is defined as having a bandwidth in excess of 500 MHz or having a fractional bandwidth of 25 percent its centre frequency, whichever being greater and having a typical emission limit -41.3 dBm/MHz [6, 13]. A typical representation of this statement is shown in equation 2.1.

$$f_B = \frac{2(f_H - f_L)}{f_H + f_L} \geq 25\% \tag{2.2}$$

where f_B = fractional bandwidth of UWB signal, f_H and f_L are the upper and lower bounds of the frequency spread as shown in Figure 2.5.

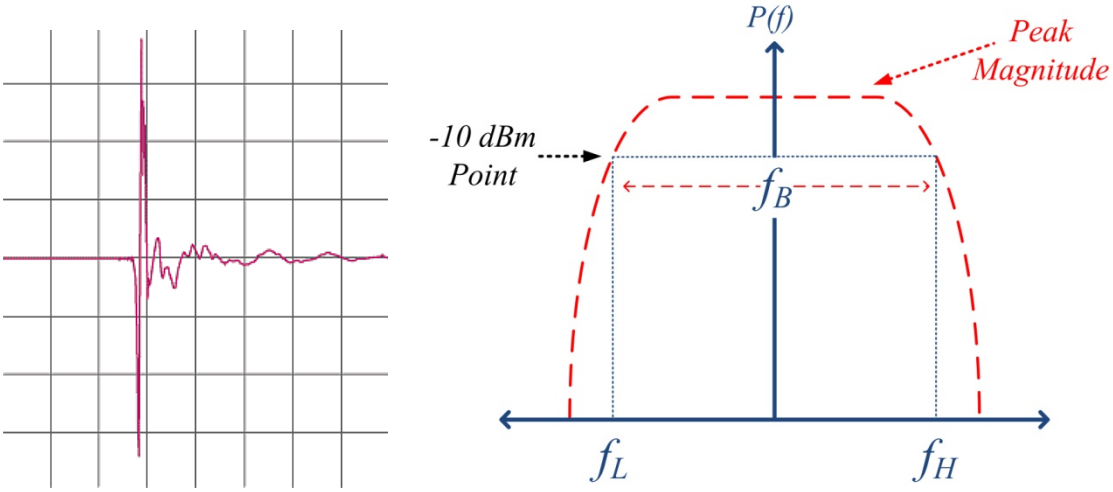


Figure 2.5: Illustration of a UWB pulse and frequency bandwidth for UWB signals with the fractional bandwidth, the upper and lower frequency limits and the -10dBm emission level [12]

For most purposes a typical UWB signal can be of any pulse shape, however arguably the most effective pulse shape is the Gaussian Pulse shape. The Gaussian cycle is used, as it can be adapted to carry information over the entire frequency envelope unlike a typical sinusoidal signal.

A typical Gaussian pulse can be represented using [22-24] mathematically, as shown in equation 2.3.

$$g(t) = \frac{A\sqrt{2}}{2\sqrt{\pi}\sigma} \cdot e^{\left[\frac{t^2}{2\sigma^2}\right]} \tag{2.3}$$

where t is the time interval, A is the amplitude and σ is the variance.

The following figures (2.6, 2.7a and 2.7b) show Gaussian pulse and its first derivative and frequency spectrum respectively adapted to suit UWB conditions under FCC. Figures 2.8a and 2.8b show the second derivative of the pulse and its subsequent frequency spectrum.

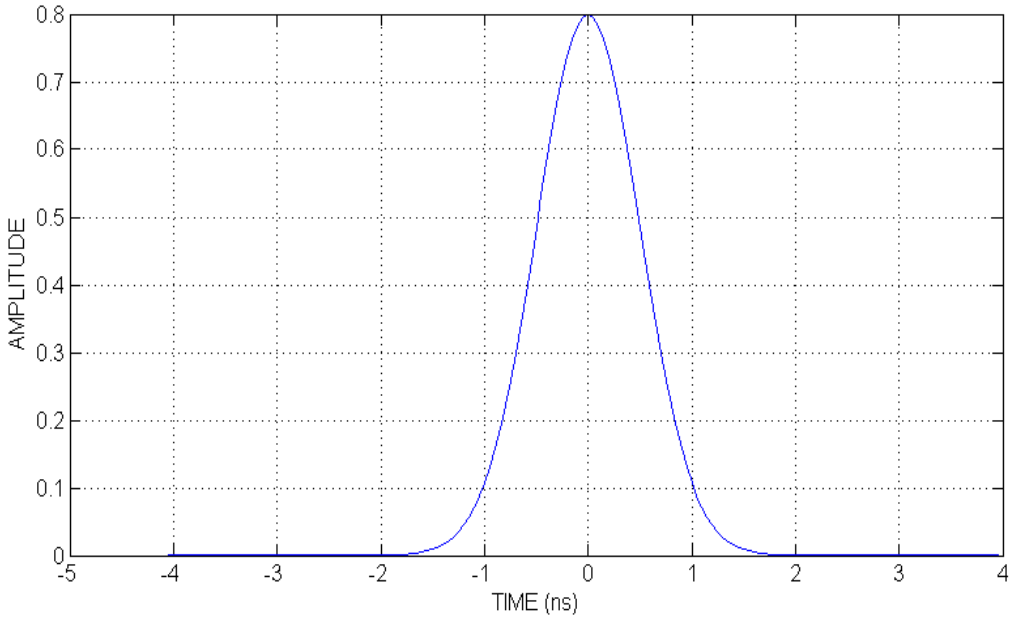
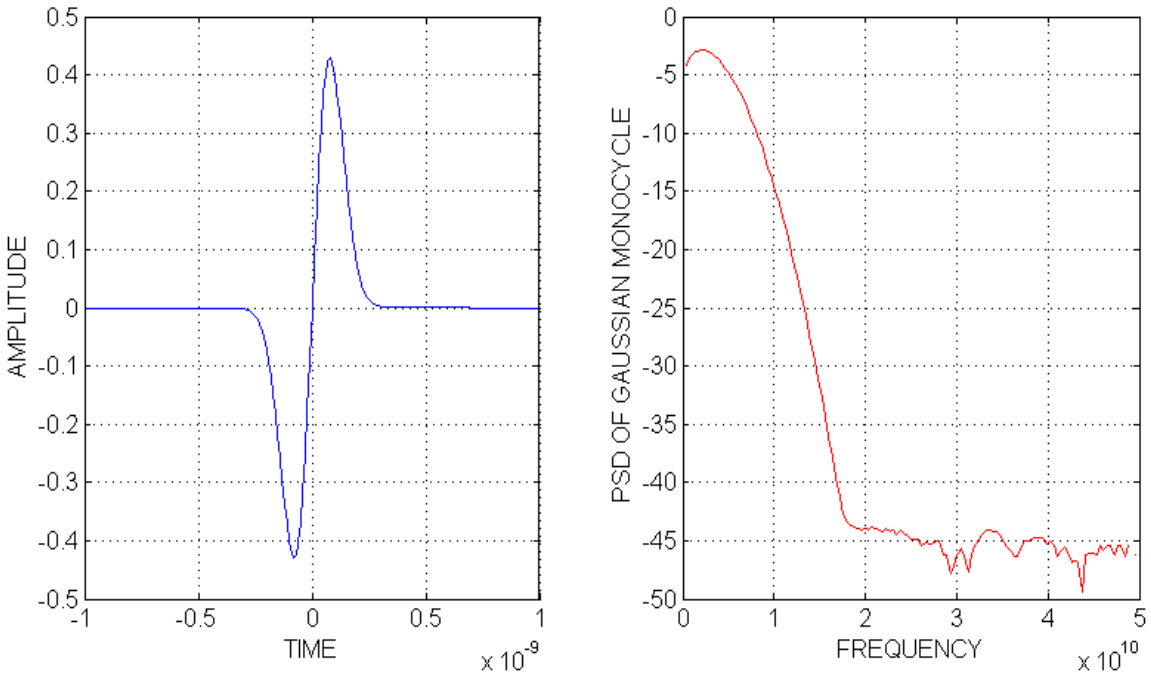
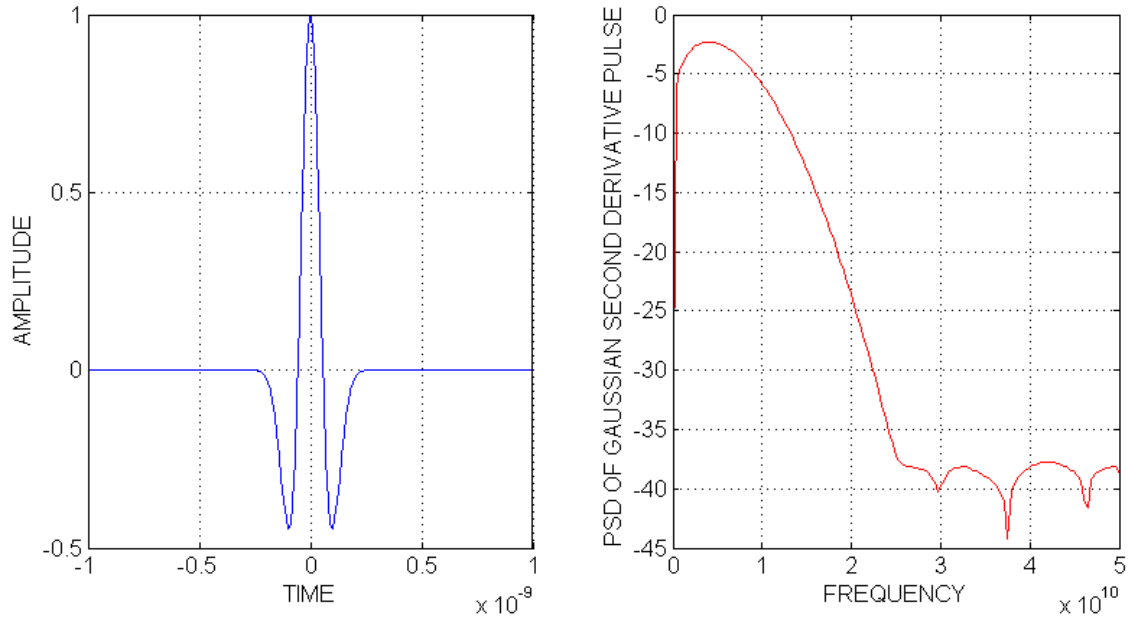


Figure 2.6: Pulse shape of a typical Gaussian signal used for UWB communication



(a) **(b)**

Figure 2.7: Gaussian first derivative frequency pulse and its corresponding frequency spectrum used for UWB communication



(a) **(b)**

Figure 2.8: Gaussian second derivative pulse and its corresponding frequency spectrum used for UWB communication

This pulsing scheme is then processed to carry information using traditional modulation approach such as Pulse Amplitude Modulation (PAM), Pulse Position

Modulation (PPM), and Binary Phase Shift Keying (BPSK) amongst others, without the need of a carrier. The processed information is then transmitted through an antenna where it undergoes Gaussian frequency shifting to emerge as a Gaussian monocycle. The time delay between the transmission and the reception of this signal leads to the Gaussian monocycle undergoing further frequency transformations to impact as a fifth or seventh derivative Gaussian pulse at the input of the receiver [23-25]. The following equations 2.4 and 2.5 shows the fifth $g^5(t)$ and seventh $g^7(t)$ derivative of the PAM based received signal.

$$g^5(t) = \frac{15A\sqrt{2}te^{\left[-\frac{t^2}{2\sigma^2}\right]}}{2\sqrt{\pi}\sigma^7} + \frac{5A\sqrt{2}t^3e^{\left[-\frac{t^2}{2\sigma^2}\right]}}{\sqrt{\pi}\sigma^9} - \frac{A\sqrt{2}t^5e^{\left[-\frac{t^2}{2\sigma^2}\right]}}{2\sqrt{\pi}\sigma^{11}} \quad (2.4)$$

$$g^7(t) = \frac{105A\sqrt{2}te^{\left[-\frac{t^2}{2\sigma^2}\right]}}{2\sqrt{\pi}\sigma^9} - \frac{105A\sqrt{2}t^3e^{\left[-\frac{t^2}{2\sigma^2}\right]}}{2\sqrt{\pi}\sigma^{11}} + \frac{21A\sqrt{2}t^5e^{\left[-\frac{t^2}{2\sigma^2}\right]}}{2\sqrt{\pi}\sigma^{13}} - \frac{A\sqrt{2}t^7e^{\left[-\frac{t^2}{2\sigma^2}\right]}}{2\sqrt{\pi}\sigma^{15}} \quad (2.5)$$

These equations will be put to use later on in this thesis to specify and define the link budget and set the design specifications for the ADC.

2.3.2 Comparison with other communication schemes

UWB Co-existence with other narrowband communication schemes have been previously detailed by [22, 26, 27] in quite some measure. From the equation 2.1, it can be seen that as the Bandwidth increases so does the channel capacity increase with a logarithmic change in the Signal to Noise Ratio (SNR). This means that higher the channel bandwidth leads higher data transfer rates [28-30]. This also means that a UWB system can achieve the same or far superior data throughput at a much lower SNR than pre-existent Narrowband systems eschewed by equation 2.1. The low SNR base for

UWB means that it is virtually free of any interference from adjacent high SNR narrowband systems and can thus co-exist without major issues [28-30].

Typical UWB systems make use of Code Division Multiple Access (CDMA) coding schemes to define each slice of transmitted and received information. The advantage of using such technique is that a large slice of bandwidth is used for extremely high data transfer and precision asset location capabilities. More of this will be explained while discussing UWB communication standards and receiver design. Figure 2.9 and succeeding table shows the UWB co-existence with other narrowband standards. It is seen that narrowband systems are typically restricted in their bandwidth to a maximum of 400MHz with a few like Wireless LAN 802.11a operating at a high frequency level of about 5 GHz. The difference in the power levels can also be discerned, confirming Shannon's capacity equation 2.1.

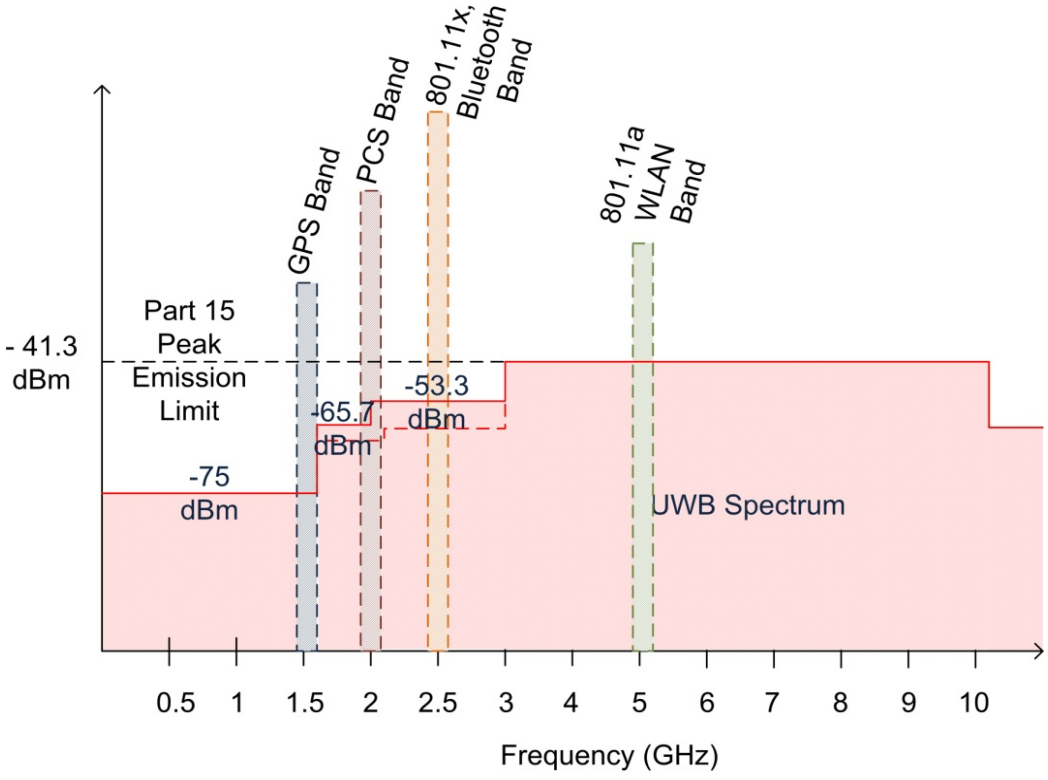


Figure 2.9: Co-existence of Ultra Wideband with other narrowband communication schemes such as GPS, Bluetooth and WLAN

The main challenge to UWB in terms of competing wireless technologies for HOSO and Bio-Medical applications are Wi-Fi LAN, Bluetooth and Zigbee. Taking a closer look at these specific communications standards;

- **Wi-Fi (802.11 x)** – Wireless LAN as a means of network connectivity technology has been around for a number of years. It has progressed effectively enough to replace cable based Ethernet in providing internet and data connectivity. However it has struggled to provide the same amount of data rate as compared to cable Ethernet until the emergence of the 802.11n standard. Cable based Ethernet provides 100 Mega bits per second (Mbps) connection while Gigabit Ethernet provides more, whereas Wi-Fi is restricted to 11 Mbps for 802.11b, 22 Mbps for 802.11a, 54 Mbps for 802.11g and 300 Mbps maximum for 802.11n. These rates are still relatively low compared to the potential of minimum 500 Mbps data rate acquirable through UWB communication [29, 30].

- **Zigbee and Bluetooth** – Zigbee and Bluetooth are recent communication standards with communication ranges of 20 feet for Zigbee and 30 feet for Bluetooth. They are serious contenders for short range wireless communications. The comparison in terms of cost leads Zigbee to march ahead of Bluetooth, however Bluetooth has a far superior and established data standrad. These two standards are typically applicable to non-bandwidth intensive uses as the comparable data rates do not match even close to Wi-Fi LAN. Zigbee has a maximum efficient data rate of around 500 Kilo bits per second (Kbps) and Bluetooth of about 1 Mbps [29, 30].

The following Table 2.1 details out different wireless technologies along with a comparison of each in terms of their range, data rate power consumption and spatial capacity.

Table 2.1: UWB comparison with different communication standards

Wireless Standard	Data Rate	Range	Frequency	Power	Spatial Capacity
UWB	> 500 Mbps – 5 Gbps	2 – 30 ft	3.1 – 10.6 GHz	Low	> 1500 Kbps/m^2
Bluetooth	0.2 – 1 Mbps	5 – 30 ft	2.4 GHz	Low	~ 25 Kbps/m^2
Zigbee	300 – 500 Kbps	15 – 20 ft	2.4 GHz	Low	~ 20 Kbps/m^2
802.11 a	22 Mbps	150 ft	5 GHz	High	~ 50 Kbps/m^2
802.11b	11 Mbps	500 ft	2.4 GHz	Medium	~ 30 Kbps/m^2
802.11g	54Mbps	100 ft	2.4 GHz	Medium	~ 80 Kbps/m^2
802.11n	150 – 300 Mbps	100 – 150 ft	2.4 / 5 GHz	Medium / High	~ 650 Kbps/m^2

2.4 Ultra Wideband Standards

The standardisation process for commercial usage of Ultra Wideband has been a challenge. Ever since UWB was de-regulated by the FCC and consequently by other countries in Europe and Australia, standardising UWB has not been an easy task. There have been differing views as to which signalling approach needs to be used. The Institute for Electrical and Electronics Engineers (IEEE) setup a task force called IEEE 802.15 which was a working group for looking into Wireless Personal Area Networks (WPAN). The two main groups are the Multi-Band Orthogonal Frequency Division Multiplexing (MB-OFDM) UWB group and the Direct Sequence UWB (DS-UWB) group [12, 13, 31]. The two differing groups have their own signalling scheme, which leads to different transceiver configurations and architectures, which in turn play a crucial role in determining the topology and requirements for the Analog to Digital Converter. As the primary scope of this work is the Analog to Digital Converter, the transmitter section of the UWB system will be out of purview and emphasis will be placed on the detailing of the receiver section of the system architecture.

The following sections detail out the two groups, with an overview of the different signalling approaches, and the different transmitter and receiver architectures. Section 2.4.1 details the approaches proposed by the MB-OFDM group and Section 2.4.2 details the efforts of the DS-UWB group.

2.4.1 Multi-Band OFDM UWB Standard

The MB-OFDM group was initially started by Intel and later on grew to include a number of other industry partners including Samsung, Panasonic, Texas Instruments and others. The industry groups were commonly referred to as the Multi-Band OFDM UWB Alliance (MBOA). The MBOA approach utilised the 7.5 GHz of frequency spectrum from 3.1 GHz to 10.6 GHz, by splitting them into 15 individual non-overlapping frequency bands, each occupying a little over 500 MHz of frequency spectrum. Figure 2.10 represents the division of the UWB spectrum as proposed by the MBOA group.

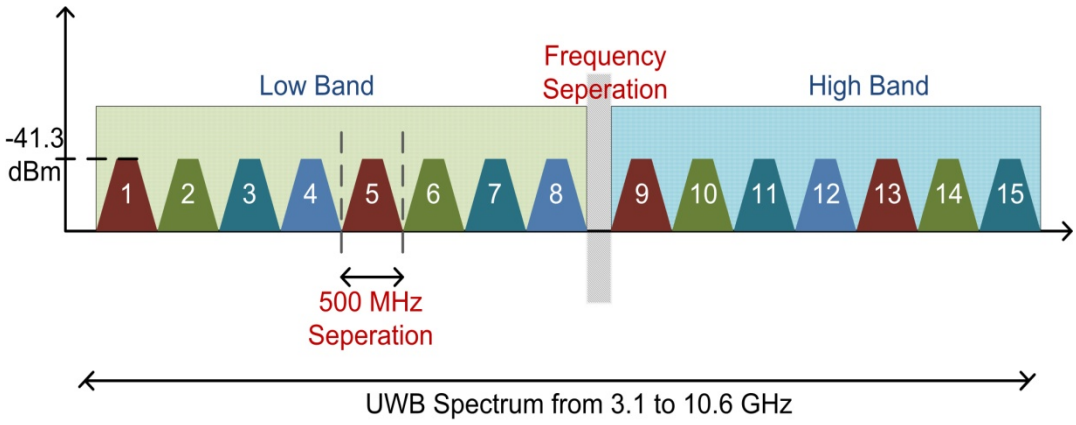


Figure 2.10: MBOA proposal for 3.1 to 10.6 GHz Ultra Wideband frequency spectrum with each band having a minimum frequency of 500 MHz

Due to the sub-divided nature of the standard proposal, the topology and communication scheme applied for MBOA also play an important part. Figure 2.11 shows a typical receiver architecture consisting of Band Pass Filter (BPF), Low Noise Amplifier (LNA), Automatic Gain Control (AGC), ADC, Matched Filter (MF), amongst others.

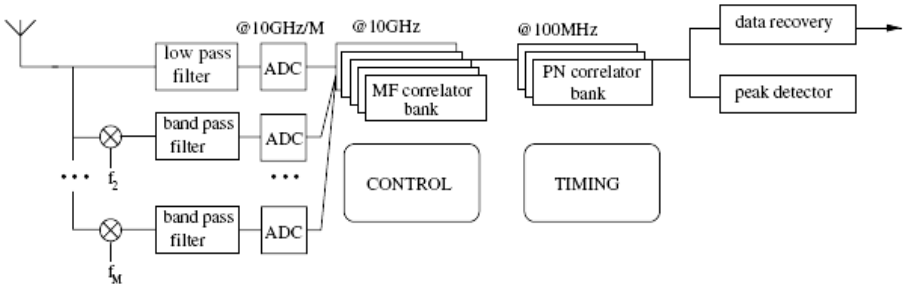


Figure 2.11: Channelized MB-OFDM UWB receiver topology consisting of parallel ADC and high performance Matched Filters [32]

The receiver is based on a frequency interleaved structure with each transmission pulse based on the number of divisions. The system is based on OFDM or Quadrature Phase Shift Keying (QPSK) signalling scheme. The receiver is based on a number of small time-divided correlators and subsequent time interleaved Analog to Digital Converters. Each converter then feeds an array of subsequent Matched Filters with then form part of the digital backend for de-spreading and decoding [33, 34]. The ADC requirements are of high resolution with low bandwidth and low sampling rates. However the number of ADCs required increase with increasing data rates. This means there is more complexity in the synchronisation for the digital section and possibly circuit design, especially for the digital backend having more power dissipation. The following Table 2.2 is a simple summary of the MBOA structure with the ADC requirements.

Table 2.2: Summary of MBOA Proposal

Bandwidth	500 – 528 MHz
Bands	13 – 15 Bands
Signalling Scheme	OFDM (N point FFT), QPSK
Access Methodology	Time / Frequency Interleaved
Pulse Interval	Greater than 100 ns
ADC	N-Time Interleaved Sigma – Delta High Resolution (6 – 8 bits) Low Sampling Rate (80 – 200 MHz)

2.4.2 Direct Sequence UWB Standard

The DS-UWB group was consisted of Xtreme Spectrum/Motorola and Freescale Semiconductor who were the leading proponents for this standard. The group grew to include other alliances such as Philips, Samsung to name a few. The DS-UWB approach utilised the 7.5 GHz of frequency spectrum from 3.1 GHz to 10.6 GHz, by splitting them into 2 non-overlapping frequency bands, the Lower band and the Upper band. The lower band covered the spectrum from 3.1 to 4.7 GHz and the upper band from 5.8 to 10.6 GHz. The intermediate frequency region from 4.8 to 5.7 GHz was left free for WLAN to remove any possibility of Narrow Band Interference (NBI) [15, 35, 36]. Figure 2.12 represents the division of the UWB spectrum as proposed by the DS-UWB group.

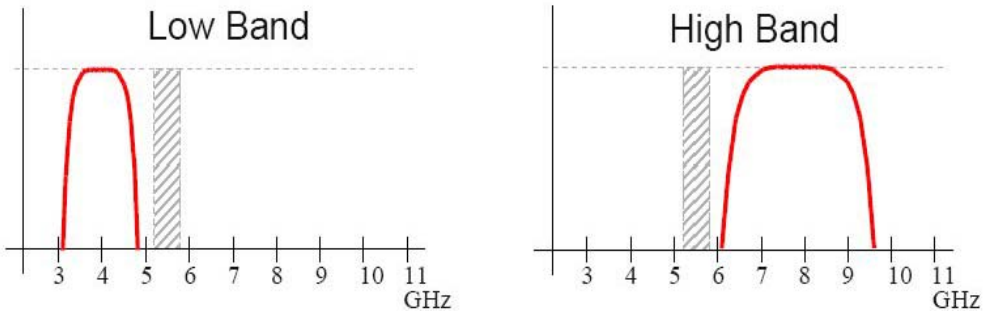


Figure 2.12: Two main Direct Sequence-Ultra Wideband spectrum bands

As with the MBOA the DS-UWB receiver structure too depends on the signalling scheme used. DS-UWB generally works on a PPM or PSK or BPSK modulation methodology. The receiver is based on a Code Division Multiple Access (CDMA) scheme where each slice of information is coded along with a preamble and individually or separately concatenated with Fixed Error Code (FEC) type Convolution (1/2 or L=7) or Reed-Solomon Codes (240, 224) [13, 37].

Figure 2.13 shows a DS-UWB receiver consisting of a BPF, LNA, Oscillator, I & Q Channel ADC and MF bank plus the digital backend.

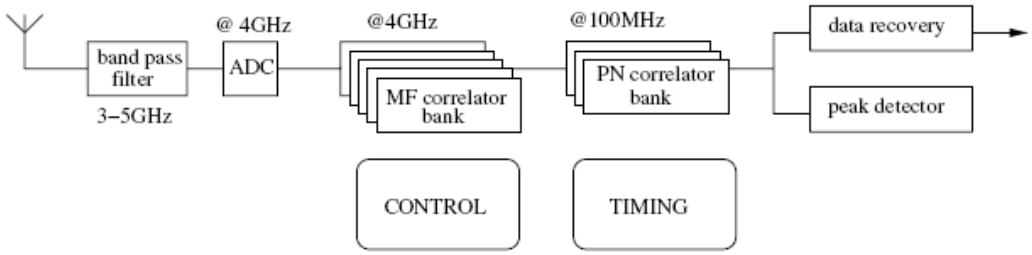


Figure 2.13: Direct Sequence-Ultra Wideband receiver with a single high speed Analog to Digital Converter and a high speed digital backend [37]

The requirements of the Analog to Digital Converter in this method are relaxed, however they still need to have a high sampling rate but with low to moderate resolution. This topology also makes use of lesser number of ADC's, thereby reducing the overall device count and saving on area and power consumption. The ADC's are also free of any synchronisation issues unlike that of the MBOA methodology. Table 2.3 summarises the DS-UWB standard and also details the requirements for the Analog to Digital Converter.

Table 2.3: Summary of DS-UWB Proposal

Bandwidth	2 GHz to 5 GHz
Bands	2 (Lower and Upper Band)
Signalling Scheme	PAM, PPM, PSK, BPSK
Access Methodology	Spread Spectrum CDMA
Pulse Interval	1 ns
ADC	High Speed FLASH/ Sub-FLASH Low Resolution (3 – 4 bits) High Sampling Rate (4 – 6 GHz)

The specific requirements of the type of data converter to be designed or used can be obtained from the link budget for the MBOA or DS-UWB scheme. Keeping in mind the requirements of reduced complexity, small area and power consumption, this thesis targets the DS-UWB methodology as the primary mode of communication for In-home wireless and Bio-Medical applications.

2.5 Summary and Conclusions

Ultra Wideband is a new and exciting technology standard that has the potential to revolutionise the wireless industry. It brings about the prospect of high speed data communication applicable to a plethora of disciplines. This chapter attempts to give the reader a not too comprehensive insight into what Ultra Wideband communication is all about. The review dwells on applications of UWB such as wireless connectivity in HOSO environment, Bio-Medical healthcare and monitoring, Precision Asset tracking and locating and collision avoidance systems. These applications play an important role in defining the future of the UWB wireless standard and the enormous potential it eschews. A comparison of UWB and other communication standards such as Zigbee, WLAN and Bluetooth have been made to enable the reader to understand as to where exactly UWB lies on the frequency plain. Different UWB standards like the MBOA and DS-UWB have been detailed to enable the reader to understand the two main receiver topologies that exist. The following chapter will define the Link Budget for the DS-UWB standard and look at different techniques for Analog to Digital Conversion, along with an attempt to justify the topology that is most suitable to such high speed data communication, all the while keeping area and power to their minimal.

Chapter III: **Analog to Digital Converter**

3.1 Introduction to Analog to Digital Converter

An Analog to Digital Converter (ADC) is the gateway that provides the link between the analog domain and the digital world. ADC is a mixed signal device that plays a crucial role in the performance of the receiver system and consequently impacts upon the data processing ability of the digital backend of the receiver.

It is a device that converts analog signals, be voltage or current to recognisable digital equivalents that can be further worked upon by the digital backend. Figure 3.1 shows a representation of the functioning of a typical ADC. An analog signal is applied at the input port of the converter, while a reference signal is applied to the reference port. The output ports of the converter show the digital form of the analog signal that has been processed. There are many different ADC architectures that are present depending on the requirements based on speed, accuracy, power consumption, resolution amongst others. Some of the established architectures are FLASH, PIPELINE, SIGMA-DELTA and Successive Approximation Register (SAR), to name a few [38, 39]. The following sections will describe each of these architectures and also detail the different performance metrics that characterise an analog to digital converter, so as to enable to determine the type of architecture and conversion technique suitable for Ultra WideBand communication.

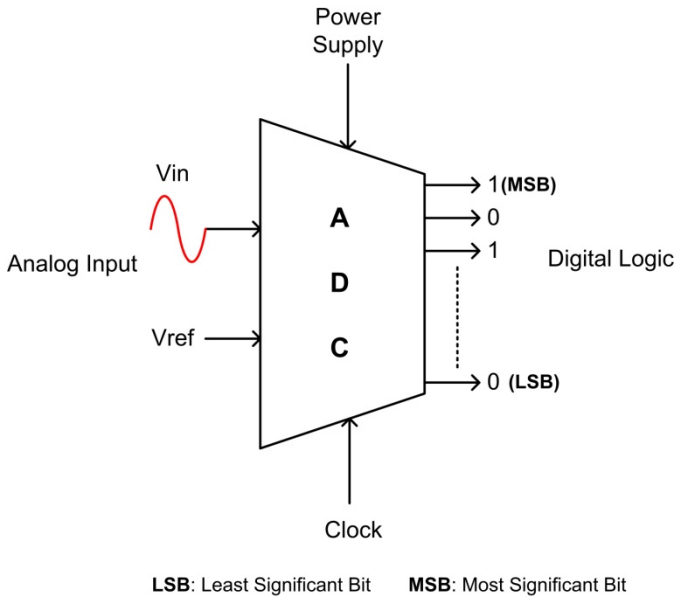


Figure 3.1: Functional representation of the analog to digital conversion process

3.2 Converter Architectures

3.2.1 FLASH Converter

The parallel ADC or more commonly, the FLASH converter is the simplest and fastest converter in the ADC family. The parallel nature of the FLASH converter makes it suitable for high speed high bandwidth applications. A drawback of this architecture is that it is power hungry, consumes significant die area and offers only low to moderate output resolution. As a standalone design FLASH architectures are used for very high frequency conversion or more commonly adopted into larger architectures like Sigma-Delta ($\sum$-Δ) to perform high speed sub-conversion tasks [39-45].

Figure 3.2 shows a representation of FLASH converter architecture. The parallel nature of the architecture is ascertained from the arrangement of the comparator array. An N-bit converter requires approximately 2^N-1 comparators to perform the digitising operation. A resistor ladder comprising of 2^N number of resistors provides each comparator with a set reference voltages that are compared against the analog equivalent to help the comparator go to logic high or logic low. Each comparator has a reference voltage of one bit difference from the comparator above it. As an analog input propagates to each of the comparator, it is compared with the reference voltage to

generate logic **High** at the output of the comparator when the input signal is greater than the reference level. As the analog input varies and falls below a certain reference level, that particular comparator registers a logic **Low** at the output [42, 44, 45].

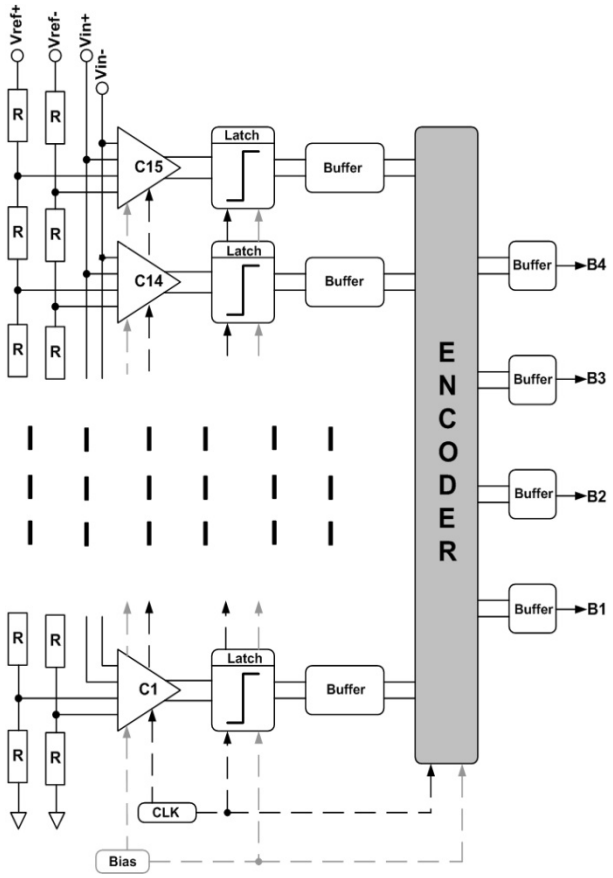


Figure 3.2: Typical FLASH Analog to Digital Converter architecture with the reference ladder network, comparator bank and encoder

The outputs of the comparators are unique as they represent a thermometer code of the analog signal. This representation is synonymous with that of a mercury thermometer, and hence the name. This thermometer representation is then fed into a binary encoder circuit that deciphers each level to a standard digital value of **One** or **Zero**. Although FLASH architectures have 2 main parts in the comparator and the decoder, the comparator can be thought of as the heart of the device. Typically comparators are composed of low gain cascaded stages with very high clocking speeds to enable wide band operation for high frequency conversion. They are designed to have input offsets

comparable to 1 LSB and have high tolerance to metastability errors to overcome the possibility of false codes being produced at the output [39, 44, 45].

3.2.2 PIPELINE ADC

Pipeline analog-to-digital converters are very popular architectures with conversion speeds from few tens of megahertz to few hundred megahertz. They have resolution capability from 6 bit to 16 bits. Owing to their high resolution capability and moderate to high sampling rate, they are more widely used in Charge Couple Device (CCD) imaging, digital receiver, communication base station, cable modem, and Ethernet devices. However for high speed applications beyond the GHz range, FLASH topology is still the architecture of choice. A typical pipelined ADC architecture is shown in Figure 3.3 [38, 45-48].

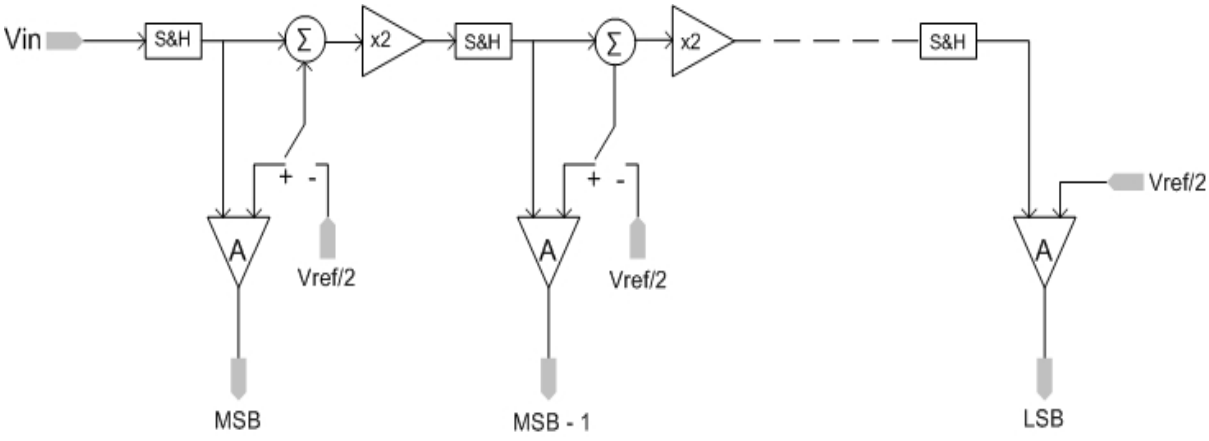


Figure 3.3: Structure of the pipeline analog to digital converter

As seen from Figure 3.3, each ADC stage consists of a Sample and Hold (S&H) circuit, which samples the analog signal, at certain discrete intervals and holds the value of the input until the occurrence of the succeeding clock cycle. The output is then fed through an amplifier and also passed onto the next stage after subtracting the reference of the preceding stage. This function is performed in each of the stages to obtain the requisite bits until the final stage. Typically the pipelined converter has N stages to obtain an N bit output. Pipelining is a way to increase throughput, however they have drawback of significant latency and area consumption [38, 45-48].

3.2.3 Successive Approximation Register (SAR) ADC

Successive Approximation architectures are very popular for high resolution and low to medium speed applications. Current architectures have capabilities of sampling at several megahertz with resolution ranging from 9 to 18 bits. SAR is a fairly complex architecture due to the number of components it incorporates to perform the mixed signal conversion. Outputs are typically extracted through a data card with serial interface or parallel bit count with increased number of pins in the layout. A typical architecture of the Successive Approximation ADC is shown in Figure 3.4 [38, 45, 49, 50].

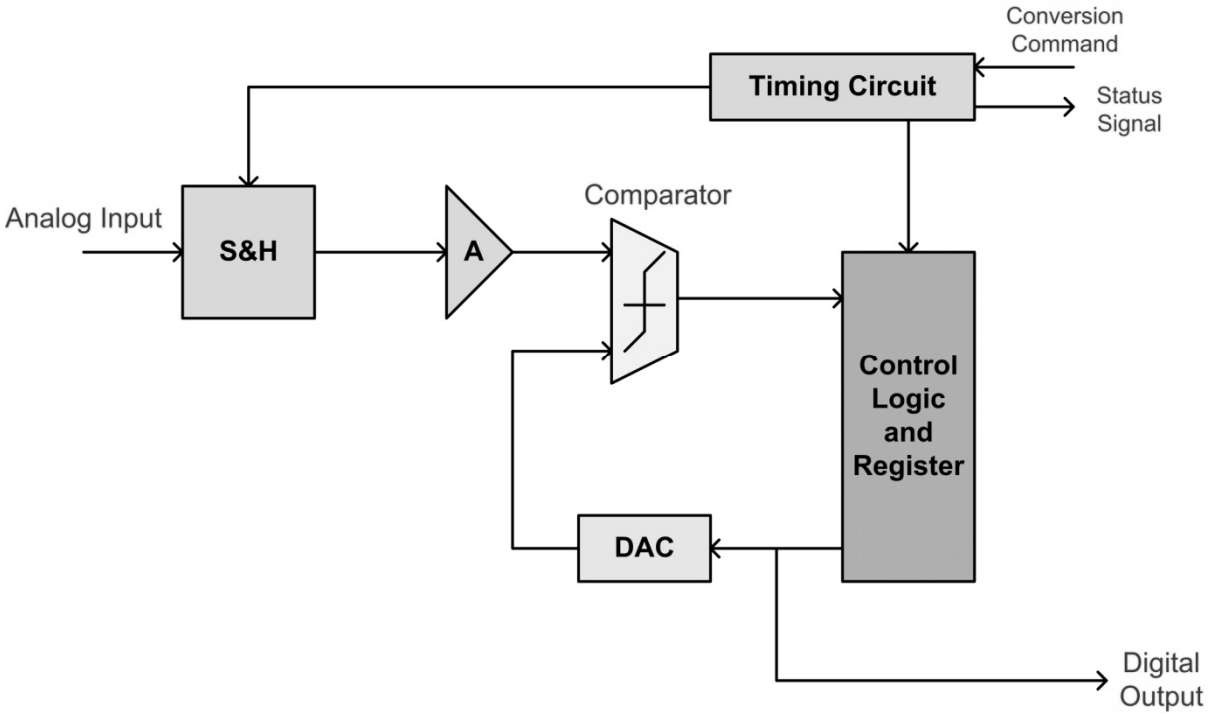


Figure 3.4: Successive Approximation Register (SAR) mixed signal device

The ADC makes use of an input Sample and Hold (S&H) circuit with amplifier to sample and basically hold the signal constant at the beginning of each conversion cycle. Initially at the start of the process the Digital to Analog Converter (DAC) is set to its middle value reference output. The comparator then discerns if the Sample and Hold output is greater or lesser than the DAC output. The result of the comparison is then stored into the successive approximation register. For the second bit, the DAC is set to one-fourths or three-fourths the reference and the entire process repeated [38, 45, 49, 50].

3.2.4 Sigma-Delta (∑-Δ) ADC

Sigma-Delta analog to digital converters are used in high precision and high accuracy applications. The converter consists of a 1-bit digital-to-analog converter that functions as a switch. It also comprises (Figure 3.5) of a comparator, Integrating circuit and Digital Filter. Typically functionality of a sigma-delta converter makes use of a tolerable over sampling ratio to perform highly accurate conversions [38, 45, 51].

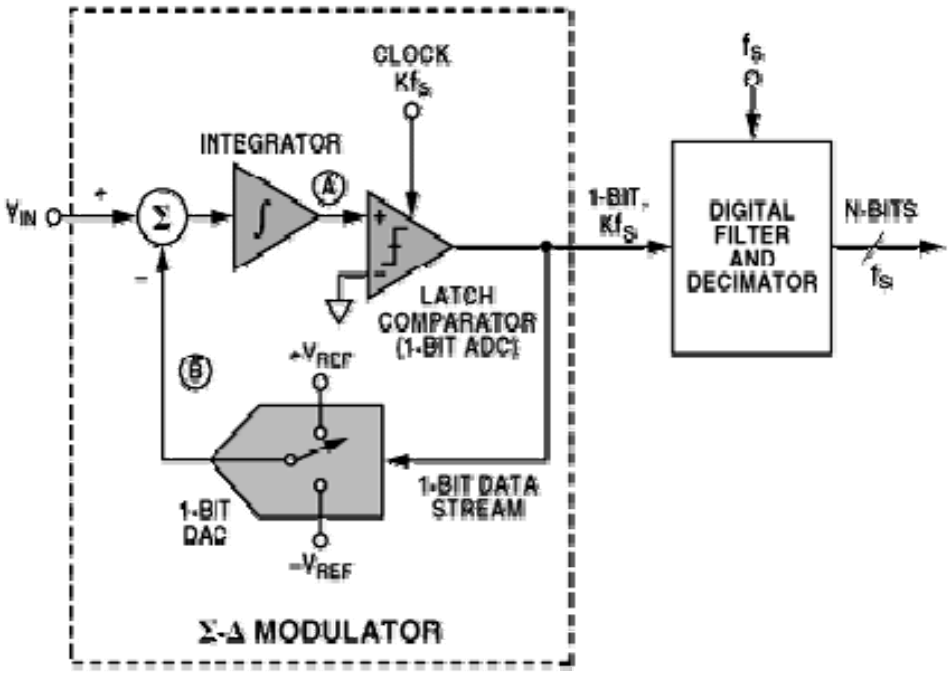


Figure 3.5: Architecture of a Sigma-Delta Analog to Digital converter consisting of an integrator, comparator, switch DAC and decimation filter [45]

The working of the converter can be explained by applying a low frequency signal at the input. The single bit digital-to-analog converter then samples and quantises the input at a high sampling rate. The output is then compared through a comparator and passed onto the decimation filter where noise components and the sampling rate are reduced, thereby increasing the overall resolution and its accuracy. The accuracy of the converter is heightened by using the over-sampled clocking mechanism and the reference circuitry. Unlike Flash topology, where the reference resistors are susceptible to noise, this is not the case in sigma-delta. On the other hand these converters are suitable for very low speed applications, and are the slowest of all the converter topologies. Due to the oversampling mechanism, the actual conversion of the input signal takes quite a few

clock cycles to perform. The design of the decimation filter is also a challenge due to its inherent complexity while converting the analog value into a digital equivalent [45].

3.2.5 Integrating/Dual-Slope ADC

Integrating analog to digital converters are popular architectures and are also more commonly known as Dual-Slope analog to digital converters. The Integrating architecture is more commonly referred to as the single slope converter.

This consists mainly if an operational amplifier to obtain a ramping signal that will be used to compare with the input signal using a comparator. The digital counter calculates the time difference for the ramping signal to cross the input. The dual slope mechanism then integrates the input voltage over a fixed time interval, which corresponds to the highest count. As the counting interval concludes, the counter is then reset and the opposite signal is applied to the integrator input. This signal results in the integrator "de-integrating" its value, until the output becomes zero. The counter is then stopped and the integrator reset. During this process the charge that has been built in the integrating capacitor during the integrating cycle must equal that during the de-integrating cycle, to enable the output ratio to be proportional in binary terms. Figure 3.6 shows the timing diagram of a Dual-Slope ADC [38, 45].

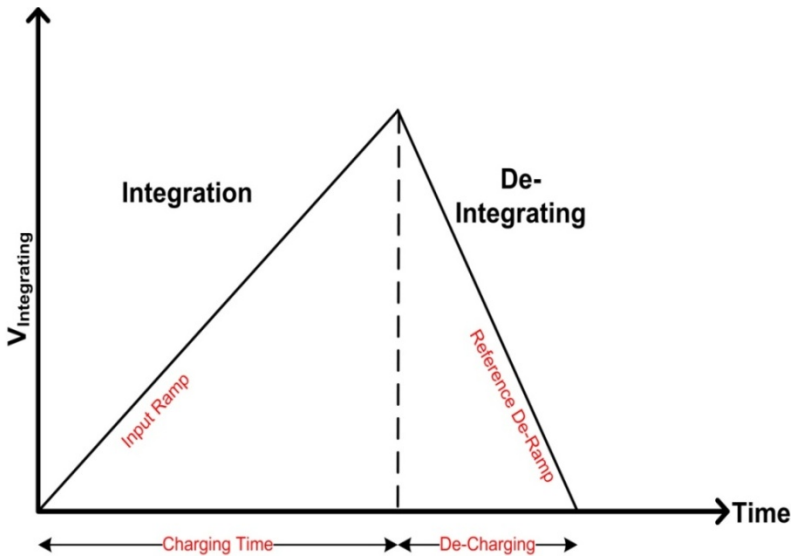


Figure 3.6: Timing diagram for a dual slope integrating analog-to-digital converter

Integrating converters are slow speed devices and are typically applicable to low bandwidth requirements. They have good immunity to high frequency noise and useful in very noisy environments [38, 45].

3.3 Comparison of Converter Topologies

The previous sections have discussed the most popular converter architectures and have described the detailed the working of each of these architectures. The following Table 3.1 gives a gist of these architectures in terms of their resolution, conversion methodology, sampling rate, area amongst other, corresponding to each converters advantage or disadvantage.

Table 3.1: Comparison of different converter architectures

ADC Type	Resolution	Sampling Rate	CHARACTERISTIC
FLASH	4 to 8 bits	100 MHz – 5 GHz	▪ High speed ▪ High Bandwidth ▪ High Power Consumption ▪ Large area / die size ▪ Matching difficulties ▪ Thermometer to Binary Encoder
PIPELINE	12 to 16 bits	10 MHz – 100 MHz	▪ High throughput ▪ Moderate Bandwidth ▪ Low Power Consumption ▪ Moderate area / die size ▪ Self-calibration techniques
SAR	10 to 16 bits	50 KHz – 500 KHz	▪ Very High resolution and accuracy ▪ Low Bandwidth ▪ Low Power Consumption ▪ Low Sampling Rate
SIGMA-DELTA	14 to 20 bits	100 KHz – 500 MHz	▪ High output resolution ▪ Moderate to High speed ▪ High Bandwidth ▪ Moderate Power Consumption ▪ On Chip digital filtering
INTEGRATING	16 bits typical	40 KHz – 100 KHz	▪ High resolution ▪ Low Bandwidth ▪ Low Power Consumption ▪ Low sampling rate ▪ Good noise immunity

3.4 Link Budget

An analysis of the receiver link margin is crucial in setting the requirements for the ADC. Consider a typical receiver architecture shown in Figure 3.7. It consists of a Front-End Band Pass Filter (BPF), Low Noise Amplifier (LNA), down conversion using a mixer and a Local Oscillator (L-O), Automatic Gain Control (AGC), high speed ADC and the post processing digital backend.

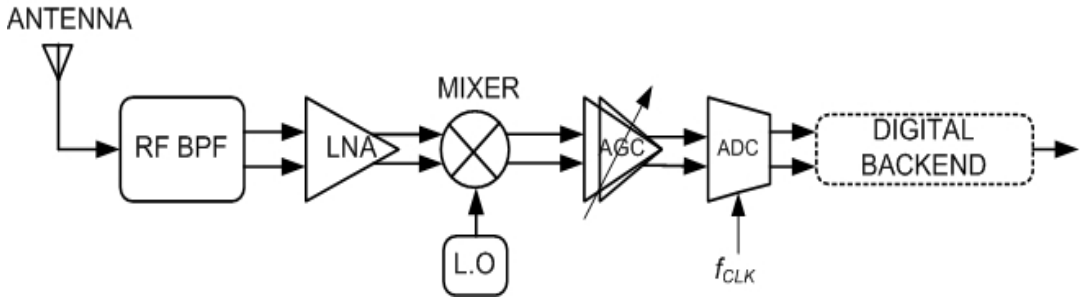


Figure 3.7: Typical Ultra Wideband receiver architecture used for high speed communications

To specify the receiver requirements consider the following [52];

- Operating Band ***B***: 3.1 GHz to 4.9 GHz / 6.25 GHz to 7.36 GHz
- Receiver Data Rate R_d: 220 / 480 megabits per second (Mbps)
- Link Distance **d**: 1 meter to 6 meters
- Sensitivity S_{inp}: -82 dBm
- Sensitivity Reference Maximum S_M : -60 dBm
- Bit Error Rate (BER) : 10^{-4}

Let us consider a Gaussian signalling scheme with the input at the receiver equivalent to the fifth and the seventh derivative of the Gaussian pulse as shown in equations 3.1 to 3.3.

$$g(t) = \frac{A\sqrt{2}}{2\sqrt{\pi}\sigma} e^{\left[-\frac{t^2}{2\sigma^2}\right]} \tag{3.1}$$

$$g^{5}(t) = \frac{15A\sqrt{2}te^{\left[-\frac{t^2}{2\sigma^2}\right]}}{2\sqrt{\pi}\sigma^{7}} + \frac{5A\sqrt{2}t^{3}e^{\left[-\frac{t^2}{2\sigma^2}\right]}}{\sqrt{\pi}\sigma^{9}} - \frac{A\sqrt{2}t^{5}e^{\left[-\frac{t^2}{2\sigma^2}\right]}}{2\sqrt{\pi}\sigma^{11}} \quad (3.2)$$

Taking into consideration a Direct Sequence UWB (DS-UWB) communication scheme, the total $SNR_{rec,ip}$ input is [52, 53] given by Equation (3.3)

$$\begin{aligned} SNR_{rec,ip} &= S_{inp} - N_{thermal} \\ &= S_{inp} - 10\log(k.T.B) \\ &= \text{-38.4 dBm} \end{aligned} \quad (3.3)$$

where k = Boltzmann's Constant = 1.3806*10^{-23} m^{2}kg/s^{2}K, T is the absolute temperature = 273 K, $N_{thermal}$ is receiver thermal noise and B is the receiver bandwidth.

The SNR for the input to the AGC/ADC can be evaluated in-terms of the receiver bit error rate and the Processing Gain (P.G) [52, 53] as shown in equation (3.4)

$$\begin{aligned} SNR_{adc,ip} &= BER - 10\log(PG) \\ &= BER - 10\log(B/R_d) \\ &= \text{-3.8 dB} \end{aligned} \quad (3.4)$$

where PG is the receiver processing gain = ratio of the used bandwidth $\boldsymbol{B}$ and the data rate $\boldsymbol{R_d}$.

Using Equations (3.3) and (3.4), the Noise Factor at the analog input of the ADC N_F can be estimated to be equal to

$$\begin{aligned} N_F &= SNR_{rec,ip} - SNR_{adc,ip} \\ &= 10 \text{ dB} \end{aligned} \quad (3.5)$$

The input receiver dynamic range is a factor of the maximum reference sensitivity and the receiver sensitivity. The characterisation of the dynamic range is important to specify the requirements for the input gain. Assuming a receiver dynamic range of 53 dB and an ADC full scale signal ($\boldsymbol{S_F}$) limit of 20 dBm the AGC gain can be calculated to be equal to 26 dBm. The total gain $\boldsymbol{G_R}$ can be calculated to be equal to about -75 dBm. Using this and the equation set by Friis [52, 54] the total Noise Figure $\boldsymbol{NF_R}$ for the receiver can be constructed based on equation 3.6;

$$NF_R = 1 + (NF_1 - 1) + \frac{(NF_2 - 1)}{G_R} + \ldots\ldots\ldots \quad (3.6)$$

Using typical construct values for the receiver based on the DS-UWB [55] scheme in the upper band we can specify the following values for the Baseband RF filter, the LNA and the input mixer as;

- Noise Figure for the RF Baseband Filter : $\boldsymbol{NF_{RF\text{-}filter}}$ = ***1.5 dBm***
- Noise Figure for the front end LNA : $\boldsymbol{NF_{LNA}}$ = ***2.5 dBm***
- Noise Figure for the Mixer : $\boldsymbol{NF_{MIXER}}$ = ***7.5 dBm***

As can be seen from the values above the total Noise figure to the mixer is about 4 dBm, which leaves 7.5 dBm for specifying the Noise Figure for the remaining analog section of the receiver. Using a maximally flat attenuation filter for the baseband with an inherent attenuating factor of around 40 dB, a fourth order or fifth order Bandpass filter will be needed to transmit a 1 GHz frequency spectrum in the upper band at a minimum Nyquist sampling rate of 2 GHz [52, 54].

From the above specification it can be discerned that the ADC bandwidth is between 600 MHz and 2 GHz. This leads to a sampling rate between1.5 Gsps to 4 Gsps. The next stage is to obtain the ADC resolution to begin the design of the converter. To obtain the resolution parameters, [52, 55] give a good overview of the UWB scheme of these parameters which can be applied to this design. The ADC noise can be considered as the sum of the ADC thermal noise and the total noise figure. The noise margin ($\boldsymbol{NM_{ADC}}$) is the ratio of the inherent ADC noise $\boldsymbol{N_{ADC}}$ and the output noise $\boldsymbol{N_{O.}}$ The $\boldsymbol{N_{ADC}}$ is a factor of the linearity noise ($\boldsymbol{L_N}$) and the quantified noise level ($\boldsymbol{L_Q}$). It is needed to specify a ADC linearity margin of $\boldsymbol{X_M}$ such that;

$$L_N = N_O - X_M + 7 \; ; L_M < L_{ADC} \quad (3.7)$$

Now the total quantified noise level can be adapted from [55] and calculated as shown in equation 3.8;

$$L_Q = N_O + 10\log_{10}[10^{-0.1X_{ADC}} - 10^{0.1(6-X_M)}] \quad (3.8)$$

Taking into account that the ADC linearity margin $\boldsymbol{X_M}$ and the ADC noise $\boldsymbol{L_N}$ to be about 15 dBm and 25 dBm respectively we can obtain the total Signal to Noise Ratio (SNR) at the output of the ADC as;

$$SNR_{adc,op} = DR - 10\log_{10}[10^{-0.1X_{ADC}} - 10^{0.1(6-X_M)}] \quad (3.9)$$

Using the typical SNR equation at the output of the ADC we deduce using equation 3.9 and the typical SNR to bit range factor of 6.02N + 1.76, that the minimum required resolution is **4** bits. From the aforementioned discussion we infer that the fastest converters that can handle such requirements are the FLASH based architectures [52, 53, 55]. Table 3.2 gives a summary of the target specifications that will be used to quantify the requirements to design the ADC.

Table 3.2: Summary of Target ADC Requirements

Communication	DS-UWB Standard
Input Frequency Range	600 MHz to 2.2 GHz
ADC Sampling Rate	1.5 Gsps to 4 Gsps
Minimum Resolution	4 bits
Target SNR	~ 26 dB
Target SFDR	~ 26.5 dBm
ADC Architecture	Full FLASH
Implementation	CMOS Technology 180 nm / 90 nm

3.5 Summary and Conclusions

This chapter is an attempt to quantify the analog to digital converter as a true mixed signal device and highlight its importance in the design of high speed receiver

structures for most communication scheme. The chapter defines and discusses the most commonly used analog to digital converter architectures such as FLASH, PIPELINE, SIGMA-DELTA, SAR and DUAL-SLOPE INTEGRATING. Each section describes the use and application of these architectures. A summary highlighting the strengths and weakness of each of these converters are also presented so as to give a broad overview of the analog to digital converter as a purely mixed signal device which plays a very crucial part and is intrinsic in its ability to convert real world signals to discrete values. It is also important to note that due to the very small amount of literature present on reconfigurable analog to digital converter architectures for UWB, a brief study of these architectures will be presented later on in this thesis.

The chapter also describes in detail the link budget for the analog to digital converter which is the cornerstone to specify the target requirements for the design and implementation of the high speed analog to digital converter for a UWB communications scheme. The link budget concluded that the FLASH converter is the most viable and suitable ADC architecture that can be used for the requirements that were laid out. The following chapter(s) will detail out the design of the FLASH architecture, starting from the design and implementation of high speed comparator architecture to the design of a high performance encoder, culminating in the integration of these sub modules to obtain an integrated design.

Chapter IV: **Comparator Design**

4.1 Introduction

The comparator is generally described as the "heart" of the analog-to-digital converter device. They are true mixed signal devices, and play a very important part in the design of high speed data converters. The design and implementation of the comparator and its subsequent performance is crucial to the overall successful implementation of the data converter system. Comparators can be classified into two types depending on architecture. Static comparators are those which perform threshold detection based on the input and reference without a clocking mechanism. These are simple devices with fairly easy circuit implementation, but however find no real use in the world of high speed data converters. Dynamic comparators on the other hand, make use of the phase/time based clocking mechanism to perform the switching action. The speed of the clocking mechanism typically defines the speed of the comparator and typifies the overall speed of the analog-to-digital converter. The typical dynamic comparator is an analog to digital conversion device with two analog inputs and a single digital output. The ideal comparator transfer function is as shown below in equation 4.1.

$$V_{out} = \begin{cases} \text{High} & ; V_{in} > V_{ref} \\ \text{Low} & ; V_{in} < V_{ref} \end{cases} \tag{4.1}$$

Other uses of clocked comparators include sense amplifiers for Dynamic Random Access Memory (DRAM) arrays, and Input/Output (I/O) sensors to highlight a few. Circuit techniques to improve speed, linearity and reduce the inherent input and output offset voltage and minimise power consumption have been central to the design specifications, fuelled by the never-ending search for faster, more accurate digitisation. The dynamic comparator in essence is a clocked difference detection circuit with slight pre-amplification and output latching [56-58].

The design of high speed clocked comparators presents an entirely new set of constraints and advantages. The foremost among the limiting factors are;

- Presence of digital clock feed-through which acts as a noise source, thereby hampering the decision speed, and also impinging upon the input offset voltage.
- Un-correlated sampling timing leads to timing jitter creating problems during the output settling and therefore impacts on the overall propagation speed of the circuit.

Inherent advantages of the clocked comparator include a relaxed stability requirement, which creates the potential for faster performance. Typical dynamic comparators also do not require the abject linearity of analog signal amplifiers and can use adaptive nonlinear positive feedback latching mechanism at the back end to significantly improve swing, reduce settling time and decision time and minimise slewing. A dynamic comparator having 4 bits of accuracy with a very low input common-mode range requires very small short channel signal amplification factor. Due to the relaxed gain requirement of the preamplifier and the overall circuit, a multi-stage design is more suitable for high speed conversion, with focus on preamplifier linearity and latch speed [57, 59, 60].

4.2 Performance Characteristics of Clocked Comparators

Before dwelling into the design of the comparator it is important to understand some of the issues related to performance of the comparator. Figure 4.1 shows the most basic

representation of a clocked comparator, consisting of an input amplifier also known as a preamplifier and a clocked latch.

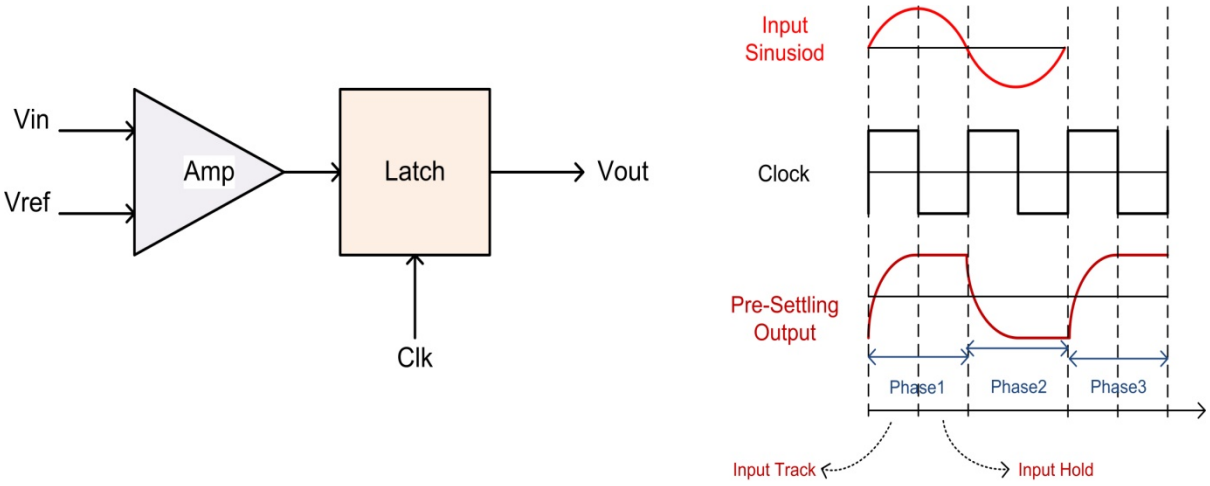


Figure 4.1: Typical representation of a clock Track and Hold Comparator and its corresponding signalling scheme with pre-settling output

The operation of the comparator can be divided into a two step mechanism. During Phase1 the circuit tracks the input depending on whether the input is above or below the reference level. This typically happens during the first half of the clock cycle. During the second half of the Phase 1 clock cycle the circuit then holds the output until the arrival of the increasing edge of the succeeding Phase 2 clock cycle. During Phase 2 the circuit then performs the same action as in Phase 1, with however the input reversed in its phase. This mechanism of tracking the input and holding it during each clock interval enables the comparator to function as a stable device, without the need for a front end sampling switch. As the comparator is meant to be a discrete time device without the need for a continuous clocked operation, the gain of the initial preamplifier dictates the overall response of the circuit. Referring to Figure 4.1, we shall now briefly discuss the various tradeoffs that affect the inherent performance of the comparator.

4.2.1 Comparator Offset

Comparator offset (V_{OS}) is typically the voltage that needs to be applied at the input to obtain a crossing point between the upper and lower logic levels. Taking an operational amplifier (OP-AMP) view, it can be said that for a zero differential input, the corresponding output is also zero. However, this is theoretically correct but practically

impossible to achieve. The problem is further compounded by the needs for faster switching in high speed comparators. Typically to obtain that zero output, a nominal voltage needs to be applied, that which is known as the offset voltage. For an OP-AMP, a simple unity gain configuration can be used to measure the offset, however in the case of differential comparators with differential output, it is imperative to measure the output crossover switching point from the zero origin as the output voltage offset. This is shown in Figure 4.2 [58].

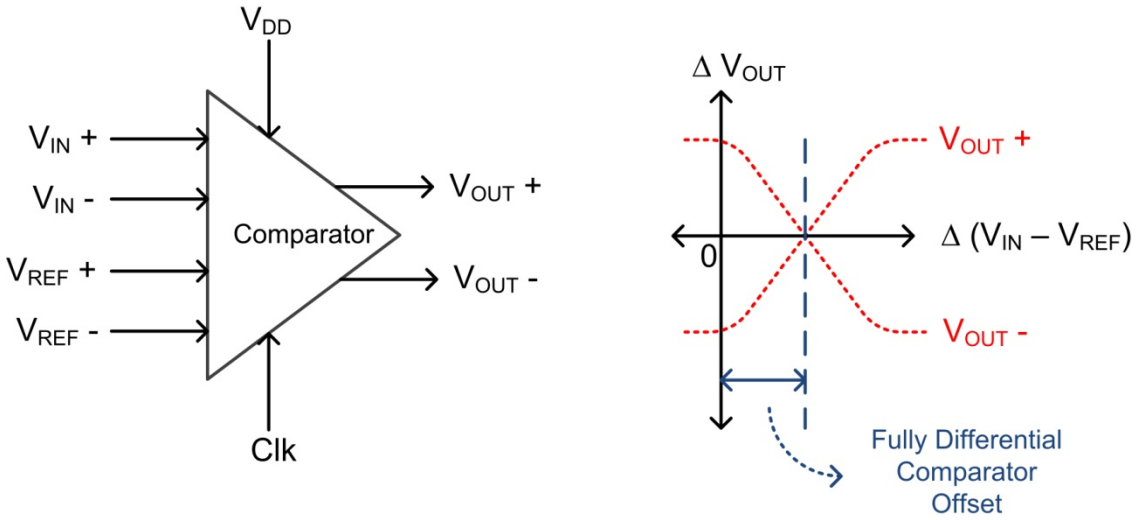


Figure 4.2: Response of the fully differential comparator output with the deviation from origin corresponding to the offset

The aforementioned comparator offset is heavily influenced by factors such as architecture, supply voltage, input sensitivity and channel length modulation, amongst others. Further on in this chapter, during the design consideration for the high speed comparator, a discussion of the needs and advantages/disadvantages of different offset cancellation techniques will be presented [58].

4.2.2 Comparator Sensitivity

Sensitivity can be defined as the least or the minimum voltage at the input which results in a rail to rail output voltage at a particular time constant. Sensitivity requirements for high speed comparators are pretty relaxed due to the presence of a front end Automatic Gain Control (AGC) circuit in most receiver architectures. Taking into consideration a 4 bit FLASH Analog to Digital Converter, would require an effective sensitivity of 0.5

(Least Significant Bit) LSB (i.e. 4 bits=2^4 = 16 logic levels = 1/32 LSB), which for a 1V reference supply translates to 31.25 mV. This means that the comparator should be capable of amplifying a very low 31.25 mV input signal to a 1V rail to rail output. However, this requirement is heavily dependent on the availability of the front end AGC, total number of comparator stages and of course the final switching time speed of the comparator [61].

4.2.3 Comparator Overdrive Recovery

Overdrive recovery is an important consideration in the design of high speed comparators. This time can be explained by considering a large input signal impacting on the gain of the comparator causing the output of the gain stage to settle at either supply voltage (V_{DD}) or ground voltage (V_{GND}). During the gain operation, as the input changes phase, the transistor requires a certain pre-charging time at the gates to enable the comparator to produce the requisite output logic. To enable this operation the comparator takes a slightly longer time than its inherent response time. This extra time is generally referred to as the Overdrive Recovery Time (t_{OV}) of the comparator [58, 61].

4.2.4 Supply Noise Rejection

Supply noise rejection is a term analogous to Power Supply Rejection Ratio (PSRR) in OP-AMP circuits. Consider applying a small signal in series with the positive or the negative power supply, results in a corresponding signal at the output with a given differential amplification. The ratio between this gain from the power supply and the differential gain of the comparator is the Supply Noise Rejection Ratio or PSRR. This ratio is important as it shows the ability of the comparator to reject input spur signals coming from the power supply. For mixed-signal circuits this ratio is an important consideration. It is to be noted that the supply voltage applied to the comparator is not the voltage generally applied to the input pins in the package. From Figure 4.3 it can be seen that the voltage applied to the package pin feeds through the bonding into the

circuit pads. Generally the pads have a resistive and capacitive barrier, with the bonding providing an inductive barrier as well [58, 62].

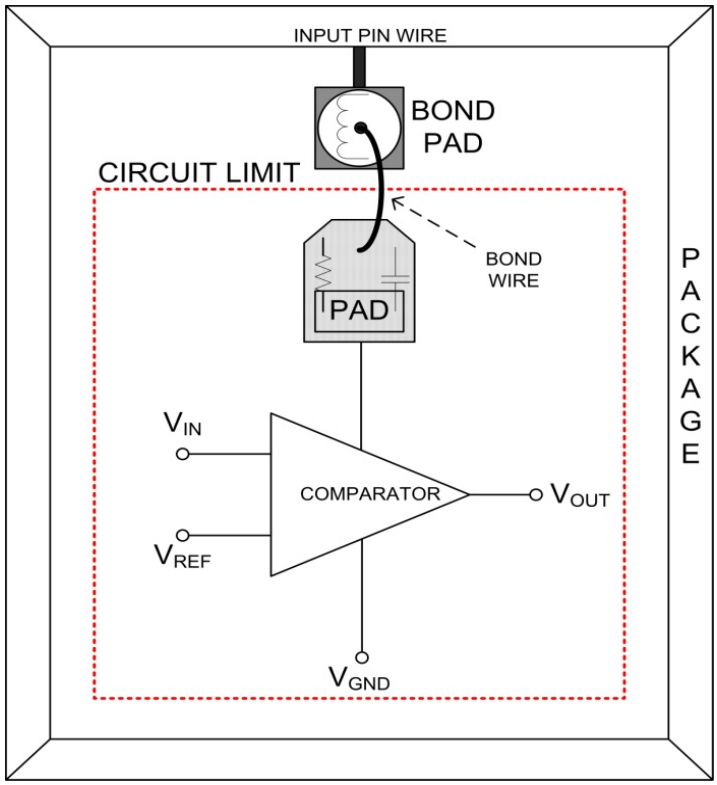


Fig 4.3: Various components affecting the flow of supply voltage into the comparator circuit from package to circuit level

The bonding wire and pin together have an estimated inductance of about 0.5-1.5 μH/mm, depending on length of bond wire and bondpad area [63]. The pad metal layers have a specific resistance that depends on the length of the connection. This mesh of inductances, capacitances and resistances leads to a drop in the voltage between the external pin and the actual supply voltage. Therefore the input supply current that needs to be accounted for is not only the one in analogue preamplifier but the spur caused by the inductive current change $L\Delta I/\Delta t$ noise contribution [58, 62].

The supply noise rejection factor plays an important part, depending on the speed of operation of the comparator circuit. This ratio degrades as frequency of operation increases and at high frequencies in the giga-hertz range a ratio of 15-20 dB is the maximum possible. However supply considerations during circuit design and of course careful implementation of the floor planning during layout can help to minimise these errors [58, 62].

4.2.5 Output Voltage Swing

The difference in the voltage levels along the output node of the comparator, such that the output is still a viable quantity is quantified as the output voltage swing. The output swing is generally a fraction of the difference in the V_{DD} and GND voltages. In a high speed comparator the preamplifier generally has an output swing anywhere from 15% to 30% of the V_{DD}-GND voltage. The succeeding latching stages provide a further 10%-20% swing, with the final latching and buffering stage pulling the comparator output node to rail to rail levels [61].

4.3 Comparator Process Size Considerations

Before dwelling into the design aspect of the comparator, it is important to understand the role played by CMOS device technology in the design of stable high speed circuits. Over the past few decades there has been a steady decline in the size of process used for designs, resulting in reduced interconnections and geometries. This factor is clearly demonstrated by Moore's Law [64]. The advantages of this downscaling in feature size are reduced supply voltage V_{DD}, lower power supply, reduced chip area, faster device operation and lower cost of production. A brief overview of the impact of this downscaling on the Digital and Analog design is presented in the following sections.

4.3.1 Digital Design

Speed and power are the two of the most important considerations in the design of any logic circuit. In the design of digital circuits, the speed of the switching logic is solely determined by the loading capacitor the output logic gate encounters. The load capacitance (C_L) is composed of the input capacitance of the next stage and the parasitic capacitance of the interconnection. Typical consideration of a digital designer is that these capacitances are proportional to the geometry size of the devices and the interconnections. The reduction of the feature size is the primary way to reduce

unwanted parasitic capacitances. This in effect increases the transition speed and reduces the power consumption of the circuit. The main sources of power dissipation are static and dynamic power dissipation as shown in equation 4.2 [65].

$$P_{dynamic} = \frac{1}{2} \cdot V_{DD}^{2} \cdot f \cdot C_L \tag{4.2}$$

$$P_{static} = V_{DD} \cdot I_{leak} \tag{4.3}$$

Where

$P_{dynamic}$ = Dynamic Power Dissipation P_{static} = Static Power Dissipation

V_{DD} = Supply Voltage f = Switching Frequency

C_L = Circuit Load Capacitance I_{leak} = Leakage Current

The scaling-down of the feature size helps reducing the load capacitance of the logic gate. Furthermore as seen from equations 4.2 and 4.3 the supply voltage is directly proportional to the power dissipation, hence reduction of the supply voltage is beneficial both in reducing the static and dynamic power consumption of the CMOS digital circuits [65]. Currently 90nm designs are the basis for mass production of digital designs, with the trend continuing to 65nm and 45nm in the coming years.

4.3.2 Analog Design

The primary advantages for analog design using nanometre feature size are similar to digital trends of faster, more effective and area efficient devices. The benefit of using the smaller feature size can be explained further using equation 4.4, which shows the relationship of transconductance g_m to the current and transistor sizing [66-67]:

$$g_m = \left(2\mu C_{ox} \cdot \frac{W}{L} \cdot I_D \right)^{\frac{1}{2}} \tag{4.4}$$

Where

g_m = Transconductance of the transistor μ = Device mobility parameter

W/L = Ratio or Width to Length I_D = Drain Current

To enable high speed operation, sizing the transistor in weak inversion region, with certain drain current, higher transconductance can be obtained from the transistor that has higher gate oxide capacitance or has shorter channel length. Clearly from equation 4.4 it can be discerned that moving to the nanometre range is beneficial to analog design. However, moving to nanometre design, leads to a number of challenges (advantages / disadvantages) which are detailed to certain extent below [66, 67].

- **Supply voltage** is typically limited to 1V range as concerns over the maximum field strength inside the transistor and hot carrier reliability dominate the operating range.

- **Threshold voltage (V_T)** of the transistor does not scale the same way as the supply voltage, due to constrains during switching on – off the transistor. As a consequence, there is a decrease in the available opening for voltage swing above the transistor overdrive voltage, calculated as $V_{GS} - V_T$. This is further illustrated in Figure 4.4 below:

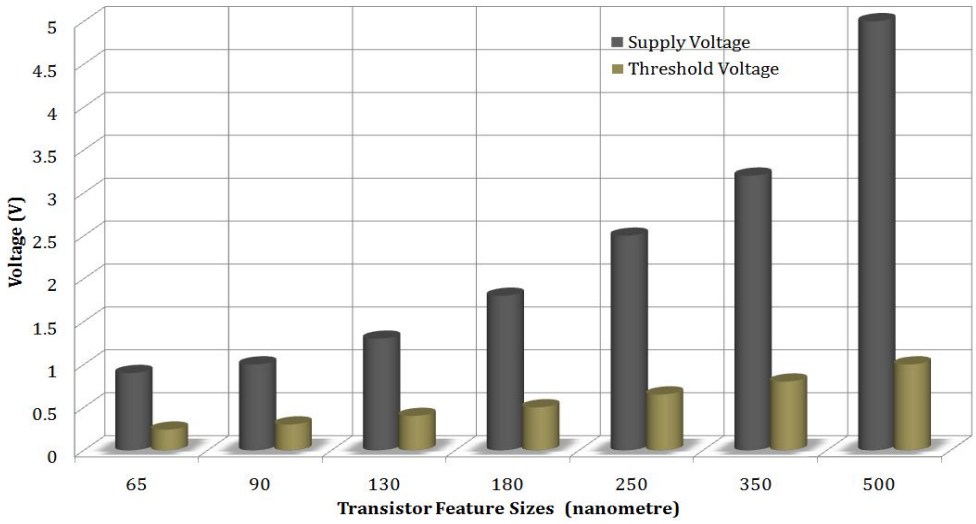


Figure 4.4: Comparison of typical transistor supply and threshold voltages against the different technology nodes for features sizes ranging from 65nm to 500nm

- **Channel length modulation** plays an important role in affecting the intrinsic device gain. To get a deeper understanding of this impact, consider equation 4.5, which shows the relationship between the gain and the device parameters [66-68].

$$A_{transistor} = \frac{g_m}{g_{ds}} \tag{4.5}$$

Where

$A_{transistor}$ = Transistor Intrinsic Gain

g_m = Device Transconductance

g_{ds} = Device output conductance

Considering that the intrinsic gain is the maximum gain that a transistor can achieve without deteriorating into breakdown, due to channel length modulation. It can be noted that the output impedance reduces greatly with reduced channel lengths. Figure 4.5 shows the change in transition frequency and intrinsic gain for the different technology nodes of a single transistor with overdrive at 0.4 V [66-68].

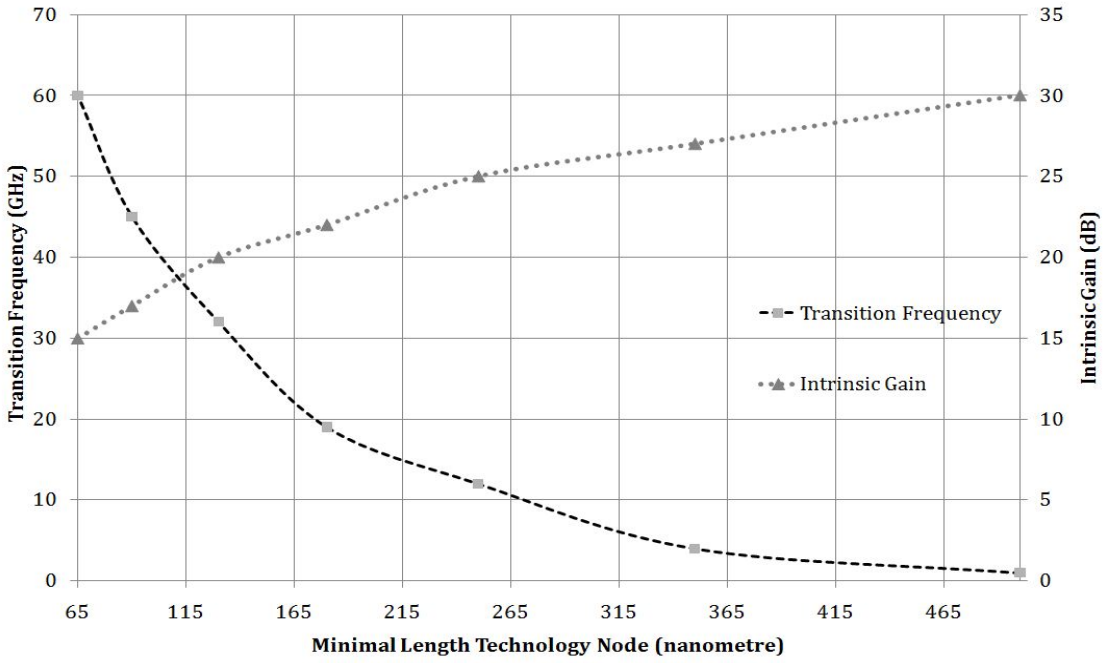


Figure 4.5: Variation in the Transition Frequency and Intrinsic Gain for a single transistor with overdrive of 0.4 V for different technology nodes at minimal length [66-68]

It can be seen that as the transistor channel length increases, the transition frequency (f_T) decreases quite rapidly. This results in a trade-off for the intrinsic gain versus the speed of operation, and is one of the primary bottlenecks in the design of analog circuits. To compensate for this trade-off typically high speed analog circuits use carefully biased transistors with multiple stages providing requisite gain. This however leads to the demise of cascode configurations, typically in preamplifiers as they make use of Non-Minimal Length (NML) transistors to provide decent overdrive recovery for the succeeding stages. However the use of minimal length devices results in reduced substrate body effect which makes stability biasing of analog circuits in the nanometre range easier [67].

- **Device Matching** is another important consideration especially in the design mixed signal circuits. Consider a typical FLASH ADC whose performance is determined by the offset of the comparators. It is well known that the offset of the comparator defines the overall matching error of a FLASH converter. Equation 4.6 shows the matching coefficient *M(N)* of a specific transistor such that;

$$\sigma(N) \propto \frac{M(N)}{\sqrt{W \bullet L}} + N_o \tag{4.6}$$

Where

$\sigma(N)$ = Standard Deviation N_o = Parameter Constant

Transistor manufacturing and process variations such as dopant fluctuations, surface roughness also contribute to changes in *M(N)*. Threshold voltage matching is especially important for synchronisation of parallel comparators in high speed FLASH ADC's. The descent into the nanometre range results in decreased thickness of the gate-oxide and allows for more control over the channel length. This has a domino effect on the matching for low to moderate dynamic range ADC's [67, 69].

Taking into consideration the aforementioned advantages / disadvantages of using nanometre transistor technology node, the following section details out the design of a high speed CMOS comparator for UWB ADC. Two implementations of the comparator were carried out using two technology different technology nodes i.e. 90nm from ST-

MICRO / CMP® and 180nm from TSMC®. The following section describes the two implementations and the final choice of the technology node for the ADC.

4.4 Comparator Design

This section presents a detailed view of the design of a high speed comparator used to implement a fast converter for UWB applications. The design follows the requirements set in section 3.4 of this work detailing the ADC link budget. The comparator implemented in this work is a 4 stage design consisting of an input Preamplifier, Track and Latch Stage, Output Regenerative Latch and a buffer, the first 3 of which are as as shown in Figure 4.6.

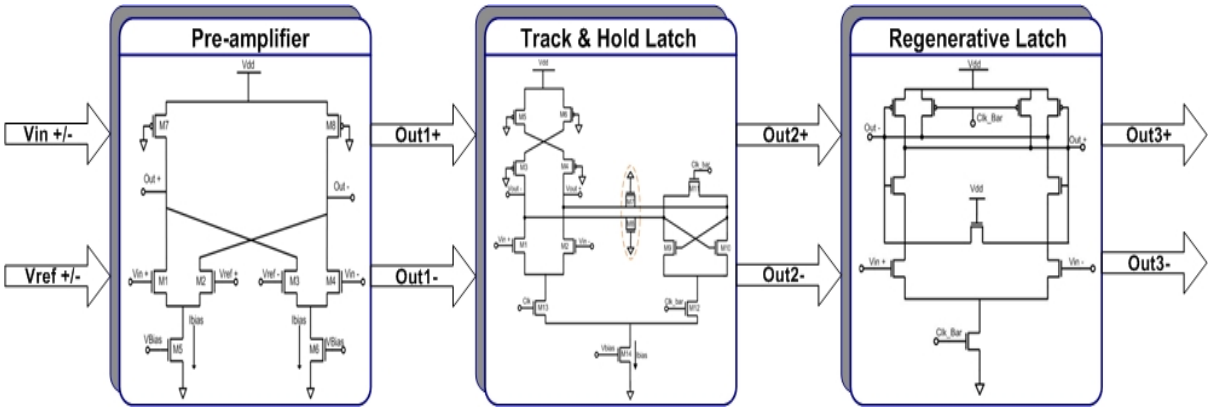


Figure 4.6: Block level schematic of the dynamic comparator implemented in this work

4.4.1 Preamplifier Design

The preamplifier stage was used to amplify the input signal so as to give the comparator better sensitivity to the input signal change. It was also used to isolate the input of the comparator from kickback noise that could seriously degrade the performance of the subsequent latching stages. Typical comparator sensitivity is of the order of 10's of milli-Volts for high dynamic range comparators. This sensitivity figure is an important factor in the choice of the preamplifier topology. CMOS OP-AMPS using closed loop configurations struggle to meet this demand and have sensitivity capabilities ranging

from 30 to 50% greater than the required amounts. This results in the preamplifier having a large offset that affects the following latching stages causing major problems in the overall matching for FLASH architectures. A number of OP-AMP configurations [67, 70, 71] were tested for their use as a preamplifier. However it was found that the closed loop configuration inhibits the comparator performance by providing low gain and mismatch or moderate gain with slower transition. This resulted in the use of open loop configuration for the preamplifier. It was found that with the open loop configuration, the same amount of gain or a slight increase in the gain was possible using cascaded stages without compromising on the speed. This was done by considering g_m and C_L based on the small signal behaviour of the preamplifier [72].

The output response of the preamplifier was considered using a single pole response with an exponential time constant r_0C_L as shown in equation 4.7;

$$V_{out}(t) = V_{in} \bullet g_m \bullet r_0 \bullet (1 - e^{-t/r_0 C_L}) \tag{4.7}$$

Where

$V_{out}(t)$ = Preamplifier output response at time t

V_{in} = Preamplifier Input Voltage

Taking into account high speed operation, the feasibility of waiting for the entire response time is void as only the initial time period is used to determine the output time response. Using this argument it is possible to re-write equation 4.7, thereby removing the exponential decay for time periods lying within r_0C_L as shown in equation 4.8.

$$V_{out}(t) \simeq V_{in} \cdot \frac{g_m}{C_L} \cdot t \quad ; \quad t \ll r_0 C_L \tag{4.8}$$

The resultant change demonstrates that the output voltage changes as a variation of the change in the slope g_m/C_L . This extrapolation leads to an important consideration that the static gain of the preamplifier is not a key factor in high speed applications [73].

Using this argument the preamplifier designed in this work concentrated on the differential switching response rather than providing high gain. The designed preamplifier is as shown in Figure 4.7.

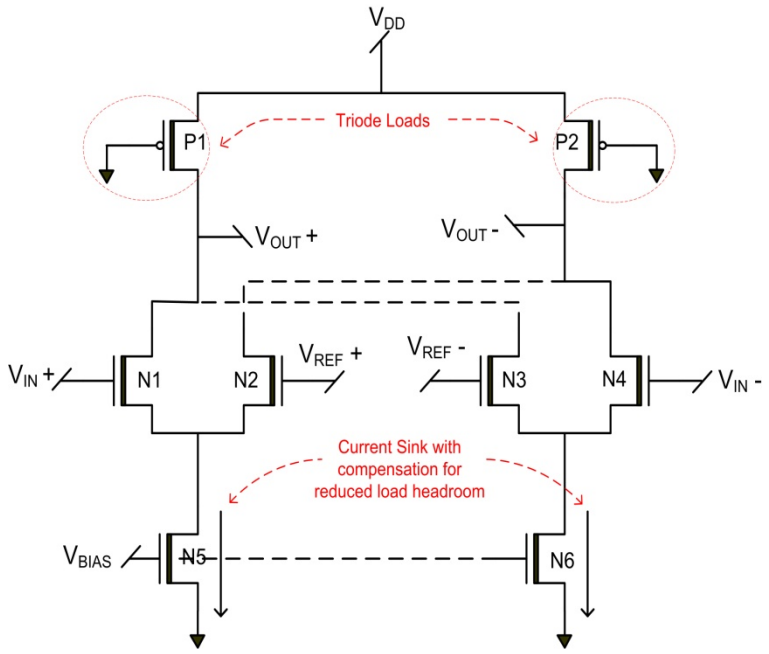


Figure 4.7: Architecture of the high speed fully differential preamplifier consisting of NMOS differential pairs at the input and PMOS loads biased in triode

The preamplifier presented in 4.7 is a fully differential design consisting of 4 inputs and 2 outputs. The four inputs are a differential balance for the input into the comparator and a differential balance for the reference voltages. The advantage of such a topology is its high tolerance to supply noise variations and rejection of kickback noise affecting the output. The output of the preamplifier is proportional to the difference between (Vin+ — Vin-) and (Vref + — Vref-) [60, 72].

The preamplifier was designed using near minimum-length devices so as to obtain the maximum possible speed. The width of the input differential pair transistors (N1 to N4) were sized based on g_m and load capacitance C_L. As the output feeds into the latching stage, the load capacitance is comprised of mainly the parasitic capacitance of the interconnect wire. As the W/L ratio is increased, the input pairs become bigger resulting in a larger g_m and correspondingly higher Gain-Bandwidth Product (GBW). It was important to note that further increase in the width yielded in increased power consumed by the input pair. The increased W/L ratio however has a positive effect on the input offset of the comparator. As the input pairs were balanced, the bias transistors

sink equal amounts of current through the 4 devices yielding to a stable g_m and thereby reducing any mismatch that the input loading may have caused. The input offset of the preamplifier was calculated based on equation 4.9 [60, 72, 74].

$$V_{os} = \left[\frac{\Delta L_{N-i}}{L_{N-i}} + \ldots + \frac{\Delta L_i}{L_i} + \frac{\Delta W_{N-i}}{LW_i} + \ldots + \frac{\Delta W_i}{W_i} \right] + V_T \tag{4.9}$$

Choice of the load transistors was another important factor in the successful implementation of the preamplifier. The preamplifier was designed using PMOS loads sized to operate in the triode region. This was done so as to meet the requirements for high speed and low signal swing. The output signal swing of the comparator was not the overriding consideration as compared to ability of the preamplifier to have a low switching time constant. This type of separately biased triode load is typically a more stable current provider in terms of its current to capacitance ratio than a self-biased diode-connected load. This is due to the fact that the voltage headroom is not curtailed by the gate voltage and can be grounded to obtain the maximum possible overdrive by reducing the size of the load devices and the additional capacitive loading they contribute. Unlike the case of typical diode based loading, where gate-source capacitance (C_{GS}) is the primary contributor to the load capacitance, in this case bulk-drain capacitance (C_{DB}) and gate-drain capacitance (C_{GD}) are the main contributors. The PMOS loads also help in keeping V_{GS} separate from V_{DS}, which is crucial to maximising signal swing and increasing the output common mode. The disadvantage that this loading brings however is its susceptibility to output Common-Mode Feedback (CMFB) errors as a result of process and supply changes. This results in the requirement of an output CMFB circuit, which degrades output time constant and contributes to a larger power overhead. Due to the fully differential open loop nature of the preamplifier, the loads are not overly affected by the CMFB variations. The loads were sized to provide a stable r_{ON}, using up a small amount of biasing current, keeping the output nodes at low impedance, corresponding to small dc gain. Rigorous simulations were performed to test functionality and performance. The sizing of these loads as mentioned was carried out based on the need for small gain and good overdrive recovery. This meant that it was important for the circuit to sense a small input signal equivalent after a large output signal. This meant that the gain of the preamplifier needed to be kept at an optimal value so as to not load the output with high impedance thereby affecting the time

constant at the output node. Due to large W/L of the input transistors, the g_m is kept fairly stable leading to a small output resistance corresponding to low gain. The small size of the load transistors, results in it affecting the input referred offset of the preamplifier in an adverse manner. This meant that the loads could not be kept at minimal length; however their size ratio could be maintained [60, 72, 74].

The preamplifier test circuit and its corresponding output response of the preamplifier is as shown in Figures 4.8, 4.9 and 4.10.

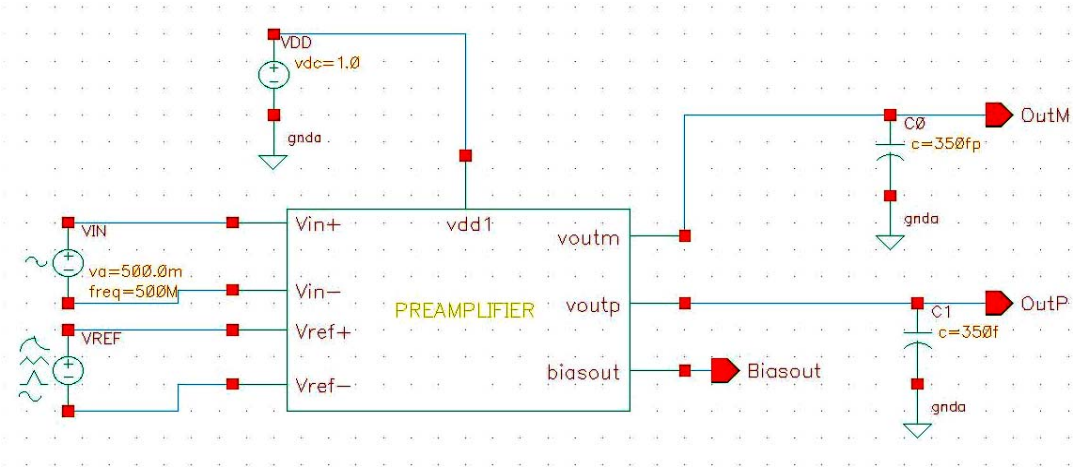


Figure 4.8: Test setup for the fully differential preamplifier with an input frequency of 500 MHz

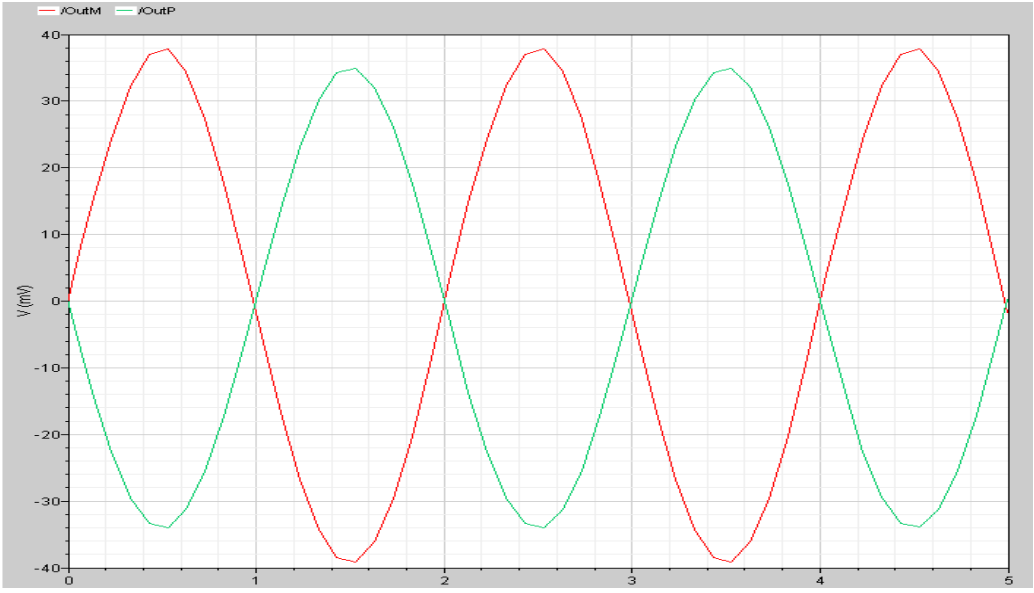


Figure 4.9: Transient output response of the preamplifier for a 30 mV input

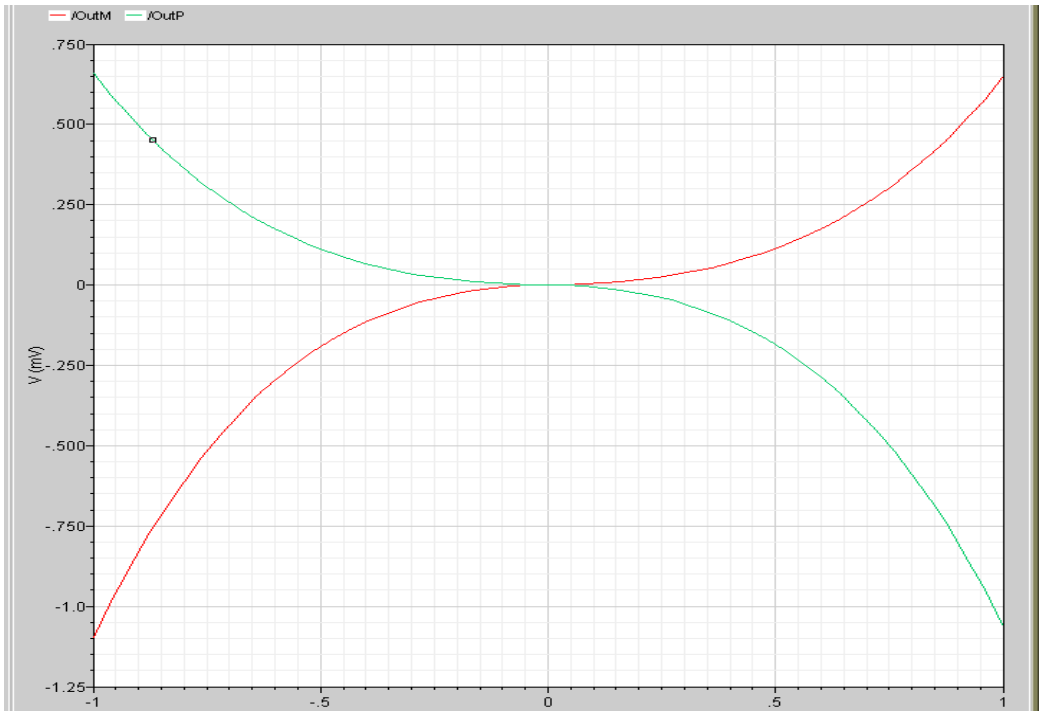


Figure 4.10: Preamplifier dc response of the preamplifier with minimal offset deviation from zero.

The performance of the preamplifier is shown in Table 4.1 with comparison of implementation in 90nm and 180 nm technology nodes.

Table 4.1: Performance of the preamplifier for different input conditions

Characteristic	**ST-Micro 90nm**	**TSMC 180nm**
Maximum Gain		
@ 2GHz input	1.1	2.6
@ 650 MHz input	2.5	4.2
3-dB Output BW		
@ 2GHz input	2.5 GHz	2 GHz
@ 650 MHz input	2.5 GHz	2.6 GHz
Maximum Offset		
@ 2GHz input	22 mV	65 mV
@ 650 MHz input	18 mV	45 mV
Standalone Power		
@ 2GHz input	450 µW	800 µW
@ 650 MHz input	280 µW	320 µW
Supply Voltage	1 V	1.8 V

From Table 4.1 it can be seen that the preamplifier meets the requirements for a high speed comparator design. The 90nm technology node is the most optimal in the comparison of the two technologies, in-terms of output offset, speed of operation and the power consumed. The 90nm node can handle bandwidths almost double that of the 180nm node, which is crucial to its performance in Gigahertz frequency environments.

The preamplifier as discussed above provides only a small amount of gain and swing at the input stage. Further gain and swing is achieved using a Track and Latch stage, discussed in the following section.

4.4.2 Track and Latch

Figure 4.11 shows the track and latch amplifier used in the comparator. The latch was used for its capability to offer high speed and low swing operation [60, 72, 74]. The latch also has good tolerance to meta-stability errors. It has input differential pairs (N1 and N2) that turn on when the clock is high and track the input from the previous stage. When the clock is low, the latching stage takes over, providing positive feedback and slight amplification. The latch has the ability to operate at high speeds due to the reduced output swing. The clocking transistors N6 and N7 are carefully balanced to work analogous of each other to provide a 180 degree phase difference at the gates of the two transistors. The bias transistor N8 was sized to provide low swing and along with the triode loads provide lower charging and discharging times for the latch.

The latch common mode level was set to $V_{DD}/2$ through careful sizing of the input NMOS and the PMOS load pairs. As was the case with the preamplifier design the PMOS load transistors P1 and P2 are biased such that they operate in the triode region. This enables the latch to achieve faster settling without the need to pre-charge the comparator output nodes to V_{DD}.

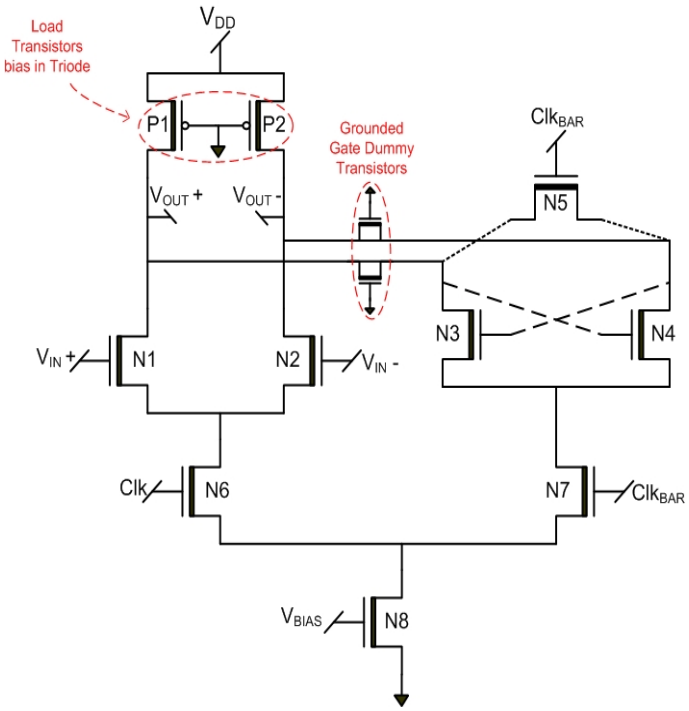


Figure 4.11: Track and Latch circuit with the clock used as mode select and dummy transistors for glitch suppression

A crucial advantage of this latch can be observed when the clock low during the latching phase. The latch has the ability to hold the tracked sampled value in the drain node capacitance, such that during positive feedback the input pair acting as cross coupled inverters do not have to discharge every time to provide small gain and overdrive recovery. This has a domino effect on the ability of the latch to switch faster between clock phases, thereby speeding up the entire comparator block [74, 75].

The input transistors N1 and N2, for this latch were sized large enough to overcome any metastability error problems and provide low gain. The offset of the latch is not a major issue as the input pairs have moderate g_m as compared to that of the preamplifier, which dominates the total comparator offset. The output stage of the latch was stamped with a reset switch N5 to keep the gain at constant, during the tracking phase. This allows for good overdrive recovery from a large signal impacting on the input nodes during the previous clocking cycle. The output lines also have 2 grounded gate dummy transistors that act as very small capacitors to reduce the glitch impacting on the succeeding stage to less than 0.08 V. The output of the track and latch stage is as shown in Figure 4.12.

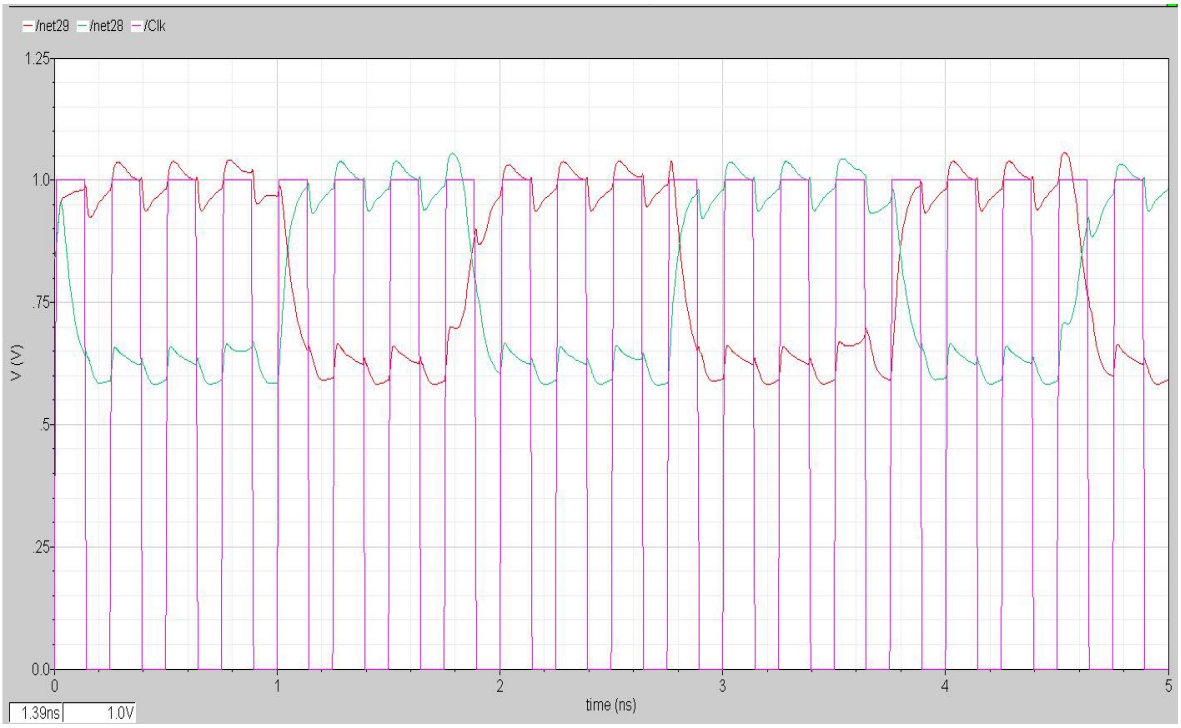


Figure 4.12: Differential output response of the intermediate track and latch stage. The outputs have been interlaced over the clocking signal to provide an idea of the gain and the low swing operation of the latch

From Figure 4.12 it can be noted that the Track and Latch provides a small amount of gain to the comparator but however over coming any metastability issues that may affect the succeeding stage. The response is switched due to the low output node impedance with a comparatively small output swing of 0.4V. The succeeding latch overcomes this problem by slewing slower but providing a larger swing from rail to rail.

4.4.3 Regenerative Latch

Figure 4.13 shows the output latch used in this comparator. The latch uses positive regenerative action to provide a rail to rail output. The rail to rail output can be obtained by setting the output nodes to the same rail i.e. V_{DD}/GND or 0.5 V_{DD}. As the clock is out of phase with the input, the feedback mechanism provides positive regeneration even for a small input differential voltage, thereby pulling the output nodes from rail to rail [60, 65, 72].

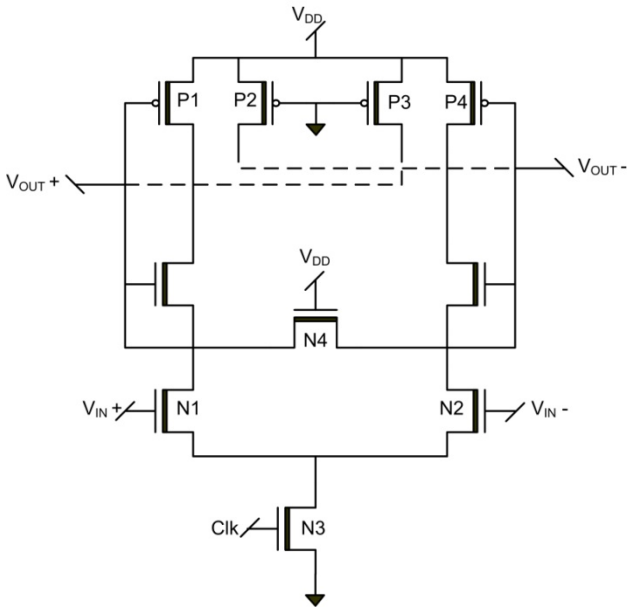


Figure 4.13: Regenerative latch used in this work to obtain steady state rail to rail output swing

The latch exhibits moderate speed unlike the fast transition of the pervious stage, and has been sized to offer a reduced higher output swing. The latch works by switching on the input transistor pairs N1 and N2 when the clock is high and pre-charging the outputs to V_{DD} when the clock is low. The output capacitances for the latch have different charging and discharging times, allowing the feedback stage along with the loads to give the required logic levels. The latch is self biased and thereby has lower power consumption unlike the previous stages [60, 72] . The latch also makes use of a VDD control to provide accurate transition from tracking to the settling stage via the use of switching transistor N4. The latch however is susceptible to metastability errors. This is because the output swings from V_{DD} to GND which requires the output node capacitance to undergo increased charging and discharging. This leads to an increase in the RC time constant along the output node that draws extra current through the PMOS loads. The extra current drawn impacts on the output slew of the PMOS transistors, thereby slowing the latch down. Metastability is the condition where the latch cannot discern a small difference between the input signals residing below 0.5 LSB, thereby causing the latch to skip that transition and outputs a wrong value. To overcome this metastability issue a fast Track and Latch stage was placed in the 2^{nd} stage of comparator implementation. The two latching stages combine to provide an increased regeneration time constant and also enhanced gain at the output of the comparator. The output of the regenerative stage is as shown in Figure 4.14.

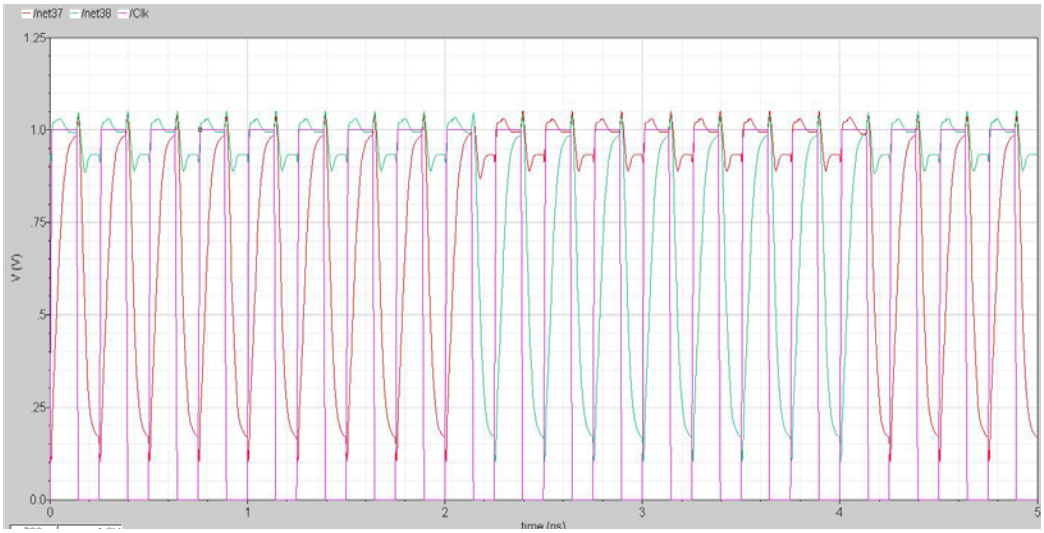


Figure 4.14: Output of the regenerative latch offering a higher swing almost from rail to rail with a 3.5 GHz clock

From Figure 4.14 it is noted that the latch offers higher swing than that of the previous stage but however struggles to settle the output within the clock half cycle. This disadvantage of the latch is overcome by using a buffer stage at the output as shown later on in section 4.5.

4.5 Comparator Performance

The final comparator circuit is illustrated in Figure 4.15. The two latching circuits work during opposite clocking phases. It is seen that the comparator outputs are pulled to the V_{DD} rail during the reset phase during every clocking cycle. This means that the opposite output nodes switch within half a cycle creating problem for the succeeding digital encoding stage. To prevent this final unity gain inverter buffer circuit was added to the output of the final latch so as to settle the outputs to enable the digital logic to understand the voltage levels.

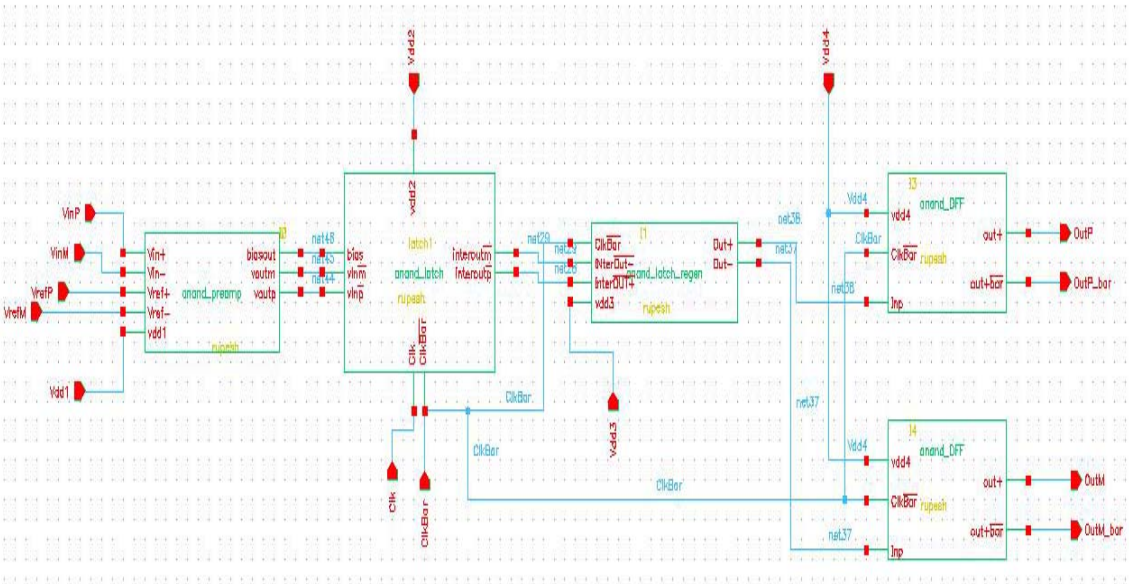


Figure 4.15: Final implementation of the 4 stage comparator consisting of an open loop preamplifier, two latching stages with positive feedback and a output buffer

The comparator was tested for its application to different reference levels corresponding to a 4 bit FLASH Analog to Digital Converter. The comparator trip points that were used for the different reference levels are as shown in Figure 4.16.

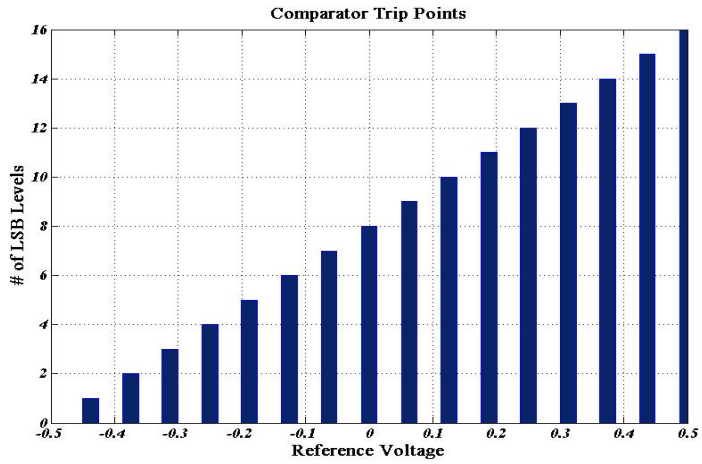


Figure 4.16: Different comparator trip points used to test functionality for a 4 bit FLASH Analog to Digital Converter reference levels

The final output of the comparator is shown in Figure 4.17. The comparator was tested for different inputs ranging from 500MHz to 2.5 GHz. The figure shows the final settling of the outputs after the use of a high speed buffer.

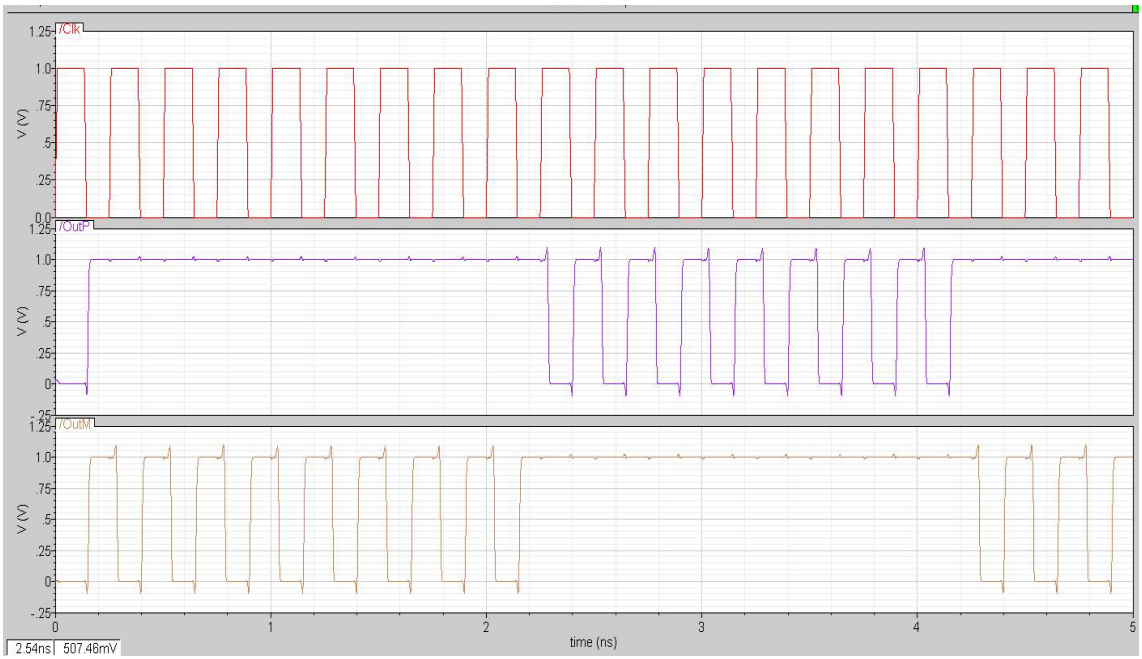


Figure 4.17: Final comparator output at the end of the buffer stage which was used to settle the output slewing that was prevalent in the previous stage

The above mentioned configuration was tested for different input and clocking frequencies and sensitivity levels to verify its complete functionality for use in a FLASH ADC for UWB applications [60, 72]. Table 4.2 shows the performance characteristics of the comparator based on its implementation and testing using 90nm and 180nm CMOS transistor technologies.

Table 4.2: Performance summary of the designed comparator

Characteristic	ST-Micro 90nm	TSMC 180nm
Maximum Gain @ 2GHz input (CLK= 4 Gsps)	3.5	4.1
@ 650 MHz input (CLK= 4Gsps)	4.7	5.2
3-dB Output BW @ 2GHz input	6 GHz	2 GHz
@ 650 MHz input	6 GHz	2.6 GHz
Maximum Offset @ 2GHz input	30 mV	85 mV
@ 650 MHz input	27 mV	53 mV
Standalone Power @ 2GHz input	3.7 mW	8.1 mW
@ 650 MHz input	3.1 mW	6.4 mW
Settling Time Percentage @ 2 GHz	48% h-c*	>85% h-c*
@ 650 MHz	32% h-c*	67% h-c*
Supply Voltage	1 V	1.8 V

*h-c denotes the clock half-cycle

From the table it can be discerned that the 90nm technology node holds the most promise for the design of high speed analog to digital converters. The comparator using 90nm technology node has a 28% reduction in the offset at an input of 2GHz, clocking at 4 Gsps as compared to the 180nm node. Considering that the comparator was designed to operate at 0.5 LSB level i.e. 32.125 mV, it can be seen that the offset at 2GHz lies below that threshold. This implies that the comparator can handle a large input bandwidth and simultaneously work at a high clocking frequency. Figure 4.18 shows the offset performance of the comparator in 90nm and 180nm.

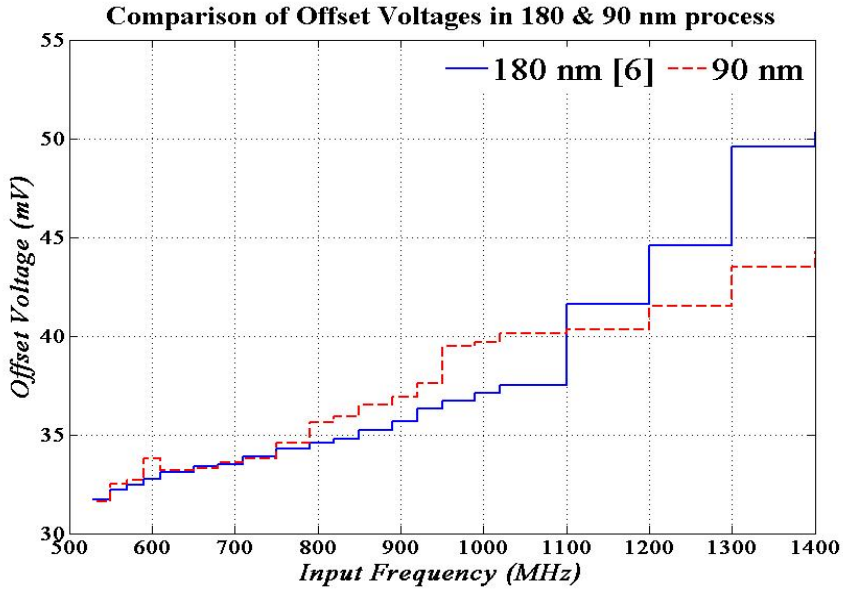


Figure 4.18: Offset performance of the comparator against the input frequency for both 90nm and 180nm nodes

The 90nm node also offers a significant advantage in the settling time constant as compared to the 180nm node. At a 2GHz input, the output takes .48τ to settle within half the clock cycle as compared to the 180nm node which takes almost double the time. This is important as the settling time determines the ability of the comparator to perform successfully in a large overdrive environment. The reduced settling time also helps to minimise the total current drawn by the PMOS loads from the supply by the self-biased regenerative stage, thereby providing additional power saving to the comparator. The total power consumed by the comparator designed in the 90nm node is 3.7mW at 2GHz/4Gsps, which is a saving of more than 50% as compared to the same design, implemented using the 180 nm node.

4.6 Conclusion

This chapter describes the design and implementation of a high speed comparator for a DS-UWB based Analog to Digital Convertor. An introduction to the concept of the comparator was presented at the beginning. An in-depth overview of the different comparator performance constraints such as Offset Error, Sensitivity, Supple Noise Rejection, Overdrive Recovery and Voltage Swing have been presented to enable the reader to get an understanding of the various factors that affect the performance. A detailed look into how technology affects the design of Integrated Circuits in the Digital and the Analog Domain was also depicted. Due to the comparator being a true mixed signal device, the analog section of the technology node was explained in more detail than the digital section. This was done because the implications of technology downscaling on digital domains have been researched extensively; however the impacts in the analog world are seeing light of day only in recent time frames.

The chapter then goes on to present the detailed design of the high speed comparator, consisting of 4 stages, 3 of which are distinct in their own ways. The author has made an attempt to demonstrate the significance that the technology nodes can play an important role by designing and testing the same comparator on both 90nm and 180nm CMOS platforms. The result of this activity has been explained in the Performance section and to a large extent justifies the need to use the 90nm CMOS technology platform for this work.

This comparator was now used as the basis to implement the high speed FLASH converter and the Reconfigurable converter, which have been detailed out in the succeeding chapters of this thesis.

Chapter V: **Implementation of Custom Flash Converter**

5.1 Introduction

The previous chapter describes in detail the design and implementation of the high speed open loop comparator used in this work. The following chapter describes the design and implementation of a high speed Flash Analog to Digital Converter, making use of the high speed comparator described in Chapter 4. From the Chapter 3 review of different Analog to Digital Converter architectures, it was established that the Flash topology is the most suitable choice for implementation into Direct Sequence Ultra Wideband Receiver Systems. The parallel nature and unique architecture of the Flash converter presents a number of key design challenges and opportunities in its implementation. The various sections of this chapter will highlight these challenges and describe the methods undertaken to address them. As well known the Flash topology can be divided into three distinct sections comprising of the Resistor Ladder, Comparator Array and the High Speed Encoder. Each of these sections, on their own and together subsequently matched to complete the final architecture, present a number of challenges that need to be tackled effectively so as to make this design a viable solution. The chapter will also detail out the process and the methodology of the layout of the ADC chip for fabrication and also present key findings as well as the various performance characteristics that define an effective converter.

Before dwelling into the different sections that make up this design, it is important to visit in detail some of the performance parameters that define and govern the ADC to get a better understanding of the working of this design. Section 5.2 details out these parameters and characteristics, with the following sections describing the different topological parts.

5.2 Flash ADC Performance Characteristics

Typical testing of ADC performance are based on characteristics which can be divided into two main groups;

- Firstly **Static Characteristics** that describe the linearity parameters like Quantisation Error (**Q_e**), Integral Non-Linearity (**INL**) and Differential Non-Linearity (**DNL**)
- Secondly **Dynamic Characteristics** such as the Signal to Noise Quantisation Ratio (**SQNR**), Signal to Noise Ratio (**SNR**), Signal to Noise Distortion Ratio (**SNDR**), Spurious Free Dynamic Range (**SFDR**), Effective Number of Bits (**ENOB**) and Total Harmonic Distortion (**THD**).
- Apart from the above two some of the other performance characteristics that need to be considered include Jitter Errors, Metastability for Logic Encoder, Matching of comparator array, Transistor Mismatch affecting design, Missing and Sparkle Codes at the output, amongst others.

5.2.1 Static Performance Characteristics

5.2.1.1 Quantisation Error (Q_e)

Quantisation is typically a process where a continuously varying analog signal is split into a number of levels, each representing a portion of that analog signal in terms of its time stamp and voltage level. For example, an N-bit converter would have 2^N number of

quantisation levels. The process wherein a continuously varying signal is transformed into digital equivalent, results in an error which is commonly referred to as the Quantisation Error (**Q_e**). Q_e can be defined as the difference of the actual analog value of the input to the ADC to the ideal staircase value. It can be further explained using Figure 5.1, showing the relation between the ADC transfer curve and its corresponding quantisation error value [76].

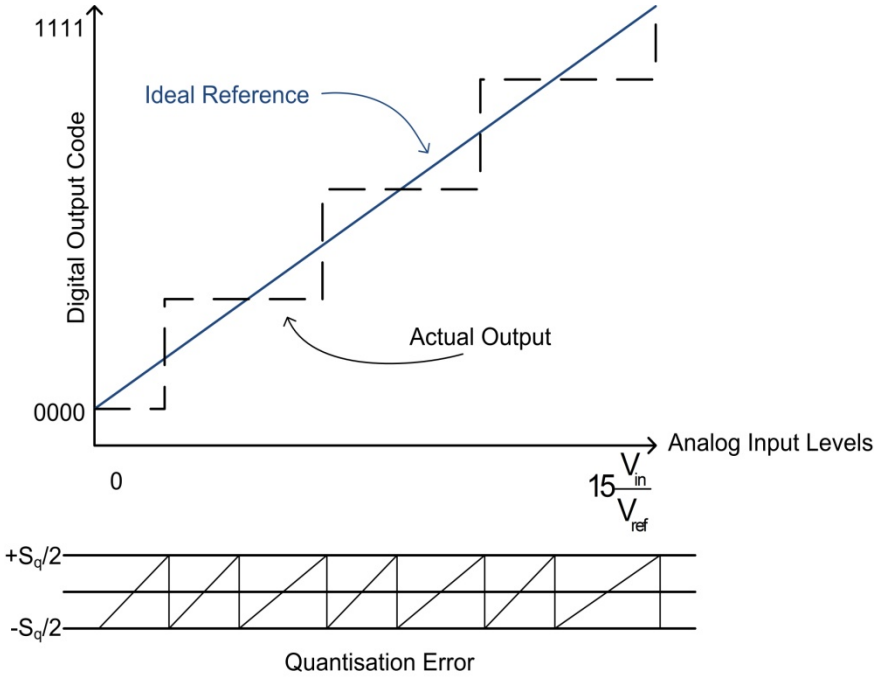


Figure 5.1: Relation between the ADC input, output and the subsequent quantisation error for a ramp based analog input

The conversion process shown in Figure 5.1 is based on a ramp based analog input signal **V_{in}**. As the signal is quantised, its results in 2 parameters, the quantised voltage **V_q** and the quantisation step size of **S_q**, with **D_{code}** being the digital output code value and N being the resolution of the Analog to Digital Converter. Equations 5.1 and 5.2 demonstrate the mathematical relation between these quantities [77].

$$\frac{V_q}{S_q} = D_{code} + Q_e \tag{5.1}$$

$$S_q = \frac{V_{infs}}{2^N} \tag{5.2a}$$

where, **V_{infs}** is the full scale input voltage that is applied to the analog to digital converter. The quantisation error can also therefore be defined as the ratio of V_{in}/S_q.

Typically the maximum quantisation error lies between $-S_q/2$ and $+S_q/2$ i.e. within 1 LSB of the output for optimal operation as shown in equation 5.2b [77].

$$-\frac{S_q}{2} < Q_e < +\frac{S_q}{2} \tag{5.2b}$$

5.2.1.2 Differential Non Linearity (DNL)

Differential Non Linearity as seen in Figure 5.2., is calculated based on the step transition size between the ideal step size and the actual step size. The ideal step width is defined as the single LSB of the converter [76, 77].

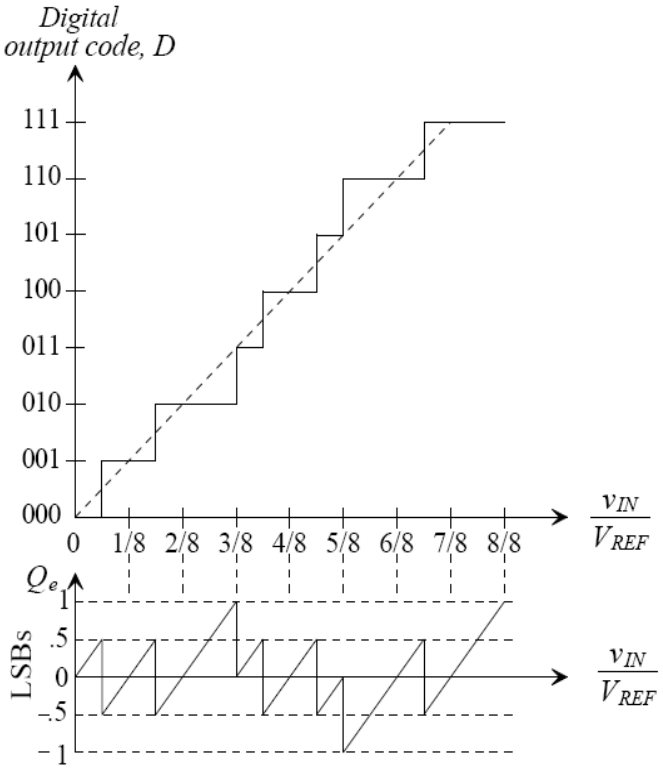


Figure 5.2: Differential non linearity of the analog to digital converter along with the deviation in quantisation levels [76]

For a number of data codes ranging from 0 to M the DNL can be expressed as shown in equation 5.3.

DNL = Actual Code Size – Ideal Code Size

$$DNL(i) = \frac{Code(i+1) - Code(i)}{1\,LSB} - 1 \tag{5.3}$$

5.2.1.3 Integral Non Linearity (INL)

Integral Non Linearity can be defined as the deviation from the centre of the ideal code line for each code point measured as shown in Figure 5.3.

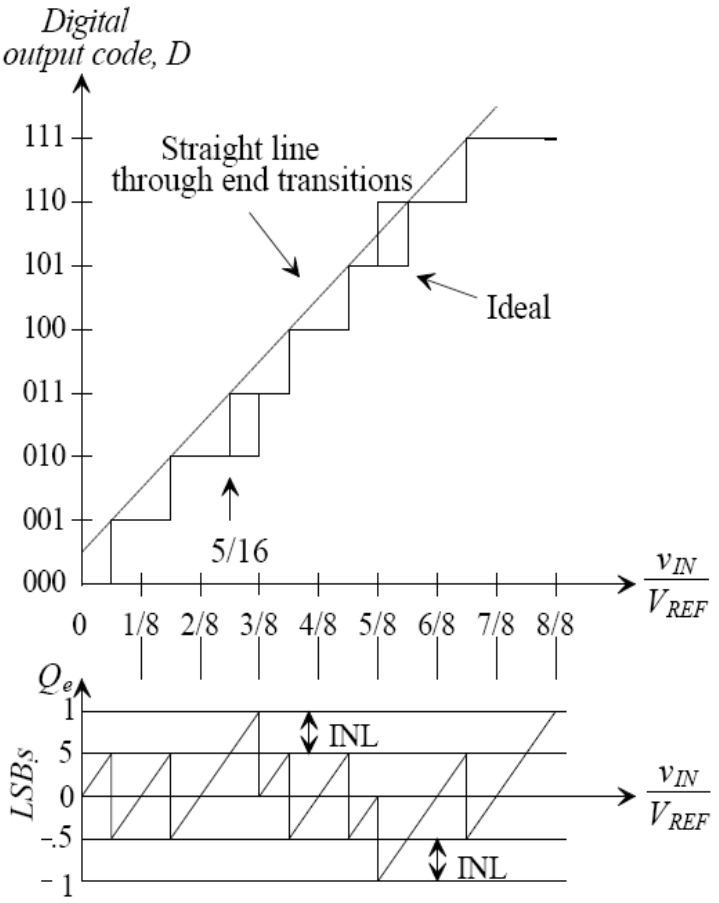


Figure 5.3: Integral non linearity of the analog to digital converter along with the deviation in quantisation levels [76]

The INL of an analog to digital converter can be extrapolated mathematically using equation 5.4 [76].

$$INL(i) = \frac{Code(i) - (1\,LSB * i + Code(i))}{1\,LSB} \tag{5.4}$$

5.2.2 Dynamic Performance Characteristics

The dynamic performance characteristics of the analog to digital converter system are based on conversion of the input and output values from the time domain into the frequency domain. The subsequent analog input and digital output are processed in the frequency domain using Fast Fourier Transform (FFT) techniques, and the resultant frequency components define the different dynamic characteristics.

5.2.2.1 Signal to Noise Quantisation Ratio (SQNR)

Taking into consideration, from equation 5.2b that the quantisation error Q_e has an even distribution over the interval ranging from $-S_q/2$ to $+S_q/2$, the integral of Q_e over this interval gives the mean squared value (equation 5.5), which can be used to define the Signal to Quantisation Noise Ratio (SQNR) [76, 78].

$$|Q_e^{\,2}| = \frac{1}{S_q}\int_{-\frac{S_q}{2}}^{+\frac{S_q}{2}} Q_e^{\,2}\, d(Q_e) = \frac{S_q^{\,2}}{12} \tag{5.5}$$

Considering a sinusoidal signal input with an root mean squared (RMS) amplitude of $V_{infs}/2\sqrt{2}$, such that $V_{infs} = 2^N S_q$. The ratio of the RMS value of the input to the RMS value of the quantisation noise shown in equation 5.5 defines the Signal to Quantisation Noise Ratio (SQNR) of the analog to digital converter [76, 77] as shown in equation 5.6a and 5.6b;

$$SQNR(V) = \frac{\frac{V_{\inf s}}{2\sqrt{2}}}{\frac{S_q^{\,2}}{12}} = \frac{\frac{V_{\inf s}}{2\sqrt{2}}}{\frac{S_q}{\sqrt{12}}}$$

$$= \frac{S_q * 2^N}{2\sqrt{2}} * \frac{\sqrt{12}}{S_q} \tag{5.6a}$$

$$SQNR(V) = 1.2247 * 2^N$$

when converted to the logarithmic domain gives us the following equation;

$$SQNR(dB) = 20\log_{10} SQNR(V)$$

$$= 20\log_{10}(1.2247 * 2^{N}) \quad (5.6b)$$

$$SQNR(dB) = 1.76 + 6.02N$$

5.2.2.2 Signal to Noise Ratio (SNR)

Typically the ratio of powers of the fundamental signal to the noise present in the system defines the Signal to Noise Ratio (SNR) of the analog to digital converter system. Integration of the noise power over the frequency interval ranging from fundamental DC to $f_s/2$, gives the total noise present in the system. Subsequent noise frequency harmonics are omitted in the evaluation for convenience. Considering this, the typical SNR of the ADC is expressed as shown in equation 5.7.

$$SNR(dB) = 10\log_{10}\left(\frac{Signal\ Power\ (P_{Sig})}{Noise\ Power\ (P_N)}\right) \quad (5.7)$$

During testing, in case of an ideal noiseless system the SNR shown in equation 5.7 is equal to the SQNR mentioned in equations 5.6a and 5.6b. Therefore for an N bit converter the free of quantisation effects , the maximum SNR calculable is the SQNR [76, 77].

5.2.2.3 Signal to Noise Distortion Ratio (SNDR)

Signal to Noise Distortion Ratio (SNDR) can be defined as a ratio of the total signal power P_{sig} to the cumulative sum of the total noise P_N and distortion powers P_{Dis} present in the system. The SNDR can also be thought of as a summation of the system SNR plus higher frequency harmonics. The measurement of the SNDR is a similar process to that of the SNR, along the same frequency interval. Equation 5.8 shows the equivalent formula for SNDR calculation [76, 77].

$$SNDR(dB) = 10\log_{10}\left(\frac{P_{Sig}}{P_N + P_{Dis}}\right) \tag{5.8}$$

5.2.2.4 Spurious Free Dynamic Range (SFDR)

In order to define and understand the Spurious Free Dynamic Range (SFDR) of the analog to digital Converter, Figure 5.4 can be taken into consideration as a reference point. As can be seen from the figure, the SFDR of the ADC is the ratio or more correctly the difference in the amplitude of the output signal to the amplitude of the largest spur present in at the input. The logarithmic measurement yields a ratio of the two quantities i.e. P_{Sig} and P_{Spur} as described in equation 5.9.

$$SFDR(dB) = 10\log_{10}\left(\frac{P_{Sig}}{P_{Spur}}\right) \tag{5.9}$$

The figure shows the SFDR measurement range for an ADC over the entire frequency range, with the highest tone recorded at the input frequency and the spur recorded close to the sampling rate of the system [76, 77].

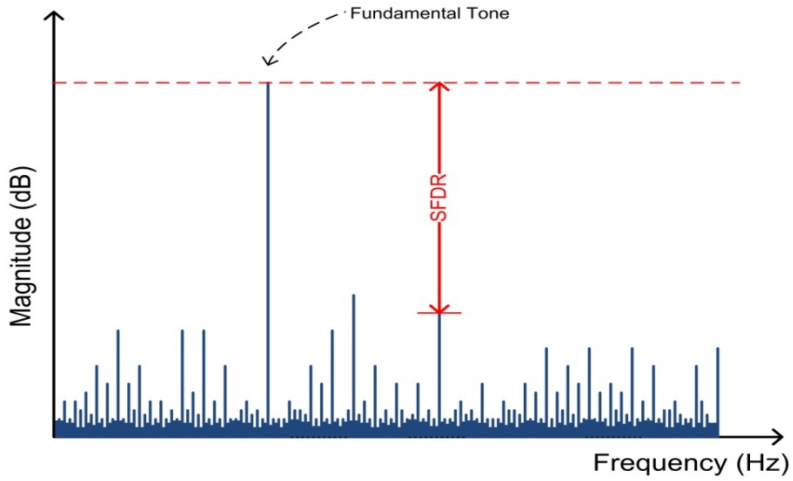


Figure 5.4: SFDR measurement range for a analog to digital converter

5.2.2.5 Effective Number of Bits (ENOB)

The concept of Effective Number of Bits (ENOB) can be thought of as analogous to that of the calculation for SNR, however in this situation making use of the previously mentioned SNDR for calculation. The ENOB is typically a measure of the lowest limit of

the permissible ADC resolution for a certain SNDR. Typically the ENOB and its relation to the SNDR are as shown in Equation 5.10.

$$ENOB = \frac{SNDR(dB) - 1.76}{6.02} \tag{5.10}$$

The ENOB is a very effective measure of the maximum achievable sampling frequency for the analog to digital converter. The frequency at which there results in a 0.5 bit reduction in the resolution of the ADC, comparable to a 3 dB drop in the SNDR of the ADC, defines the maximum conversion rate of the system. This is further illustrated in Figure 5.5 [76, 77].

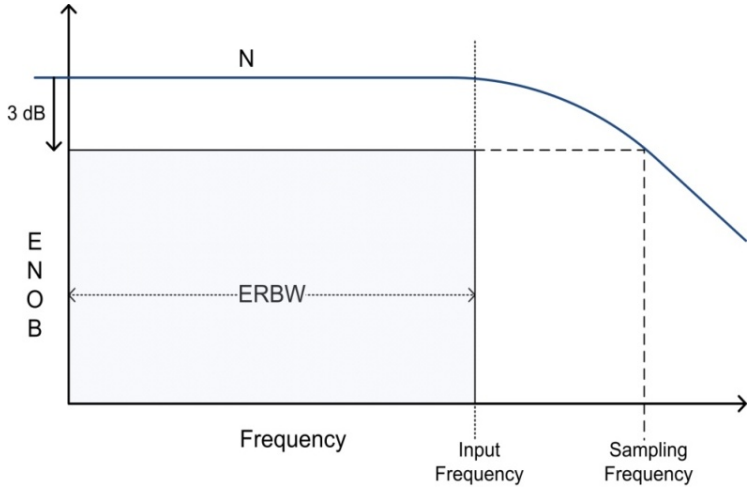


Figure 5.5: Relation between the ENOB, ERBW and the sampling and input frequencies

In addition the ENOB is also useful in determining the Effective Resolution Bandwidth (ERBW) of the ADC system as depicted in Figure 5.5 above [79].

5.3 Flash Analog to Digital Converter Architecture

As mentioned previously the Flash design typically consists of three main sections, i.e. Comparator Bank, Reference Generator and the Encoder, which put together make up the entire converter system.

The previous chapter (Chapter 4) describes in detail the design and functioning of the fully differential high speed comparator used in this work. The following sections will

detail out the design and functioning of the fully differential Reference Ladder and the different high speed encoder structures investigated for integration into the ADC design.

5.3.1 Design of Differential Reference Ladder

An accurate design of a fully differential reference ladder is crucial to the correct functioning of the entire Flash ADC system. The integration of Reference Ladders into the ADC system can be successful only if due consideration is given to the various errors that can act upon the design thereby generating improper voltage values, affecting the output of the converter. The reference generator used in flash ADCs usually consists of one or two chains of resistors [80, 81].

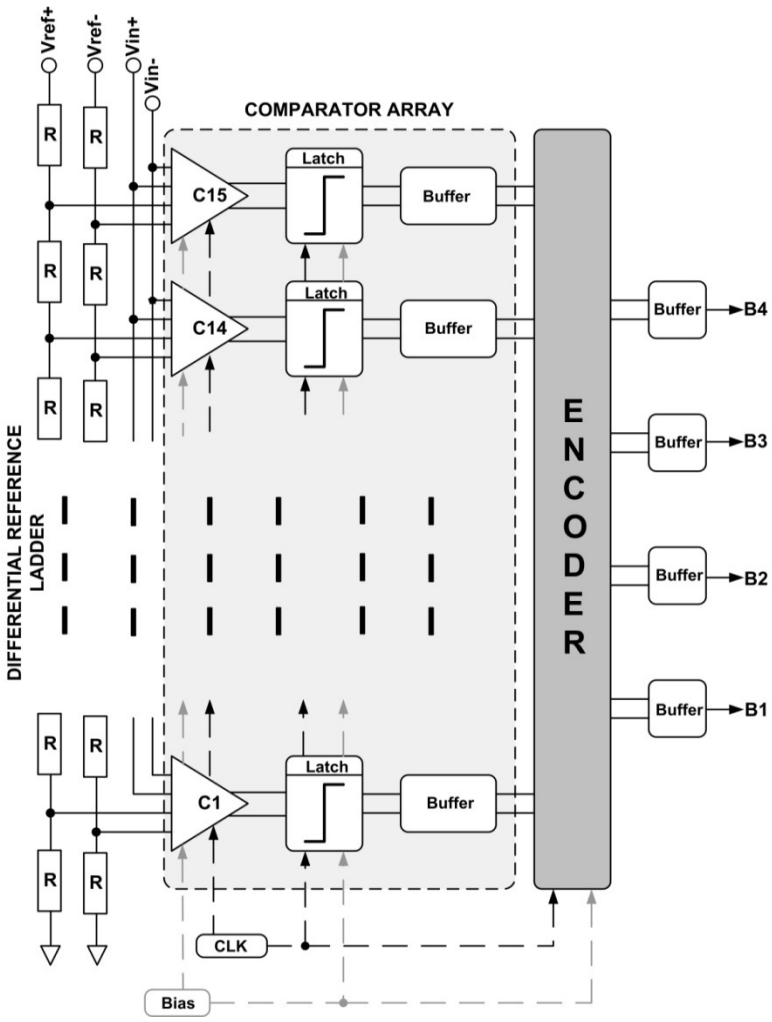


Figure 5.6: Illustrates a complete 4-bit Flash ADC system including differential reference ladder, comparator array and encoder

Two chains are required when differential comparators are used. In this design the input and output signals are fully differential, hence only both chains are used, as illustrated by Figure 5.6 [80].

The reference ladder is primarily designed using resistors to enable a stable voltage division across all comparators. However, due to mismatch between the various nets and components, the effective resistance of the resistors in the reference ladder tend to deviate from their typical values by ± δR. Assuming this deviation from nominal to have a Gaussian profile with the mean distribution centred about absolute zero mean and ± δR , the standard deviation, this variance is shown in equation 5.11 [82];

$$\delta R \cong N(0, R) \tag{5.11}$$

where N = number of Bits of the ADC

R = Resistance Value of each resistor in the ladder

As a result of the resistance mismatch the effective voltage output from the ladder also varies from their typical values. This variation of the reference voltages causes a nonlinear transfer function in the ADC system, resulting in multiple harmonics at its output. These effects are included in the behavioural models of the ADCs designed in this work. Another potential error is the signal feed through of the input signal to the reference ladder outputs. This feed through occurs due to the presence of parasitic capacitances present between the inputs of the comparators. This feed through can be reduced by designing the reference ladder to have a bias current sufficient enough to overcome the harmonics at the output resulting in a stable voltage level along the net. This results in the total resistance of the reference ladder being low enough to output a stable voltage, but not too low so as to draw extra power from the supply net [82].

A clearer understanding of these issues is presented in the following sections.

5.3.1.1 Input Feed Through

As illustrated in Figure 5.7, there is parasitic capacitance that exists between the gate and source of the input transistors. This gate-source capacitance (C_{GS}) impacts a large amount onto the total capacitance (C_{Ref}) present between the input signal net and the reference signal net at the input of the comparator as it is the main coupling capacitor at the comparator input.

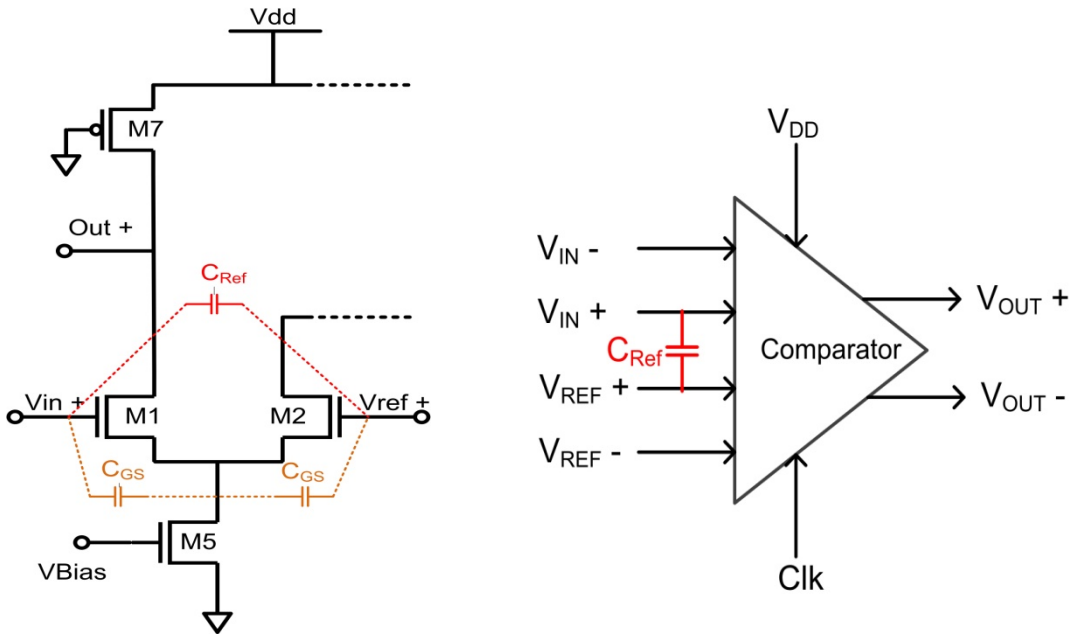


Figure 5.7: Input feed through capacitances for the comparator (b) using Pre-amplifier half-circuit configuration (a)

The input signal feed through causes a variation in the voltages generated by the reference ladder. This voltage variation can be large if the resistance of the different resistors is not sufficiently low enough. However, if the resistance is chosen too low the reference net consumes extra power [82]. Figure 5.8 shows a small scale model of the reference ladder, which is used as the platform for determining the optimum resistance value.

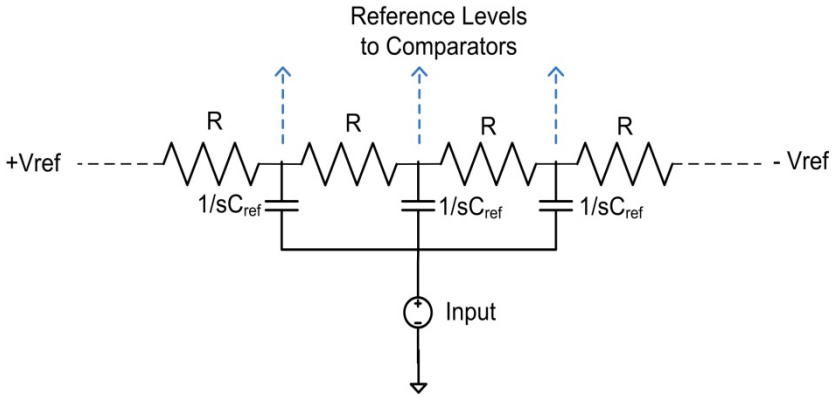


Figure 5.8: Small signal circuit for input feed through analysis of the reference ladder used in Flash ADC

Considering that the total resistance of all the resistors in the reference ladder i.e. R_1.....R_N, is given as R_T and the sum of all the C_{Ref} as C_T, we can infer that for an N bit Flash ADC;

$$R_T = R*(2^N - 1) \tag{5.12}$$

$$C_T = C_{\mathrm{Re}\,f} * 2^N \tag{5.13}$$

The worst case input feed though typically occurs at the middle of the reference ladder due to the effect of corresponding capacitances of comparators above and below this mid-level range [82]. A 4 bit converter with 15 reference levels and input frequency f_{in}, the expression for the total feed through resistance can be inferred as;

$$R_T \le 7.3\frac{V_X}{\pi f_{in} V_{input} C_T} \approx \frac{7.3\eta_{LSB}}{\pi f_{in} C_T 2^N} \tag{5.14}$$

such that $$\frac{V_X}{V_{input}} = \frac{\eta_{LSB}}{2^N},$$

where V_X = Voltage at mid-level of reference ladder

V_{input} = Input Voltage

η_{LSB} = LSB numbers

Using equation 5.14, it is derived that for an input frequency of 2 GHz, with total capacitance of 106 fF, with feed through of less than 1 LSB, the total resistance of the reference ladder is 29.4 Ω. This results in an individual reference resistor value, obtained from equation 5.12 of approximately 1.95 Ω. Therefore for a 1 V full scale reference voltage, the total power consumed by the reference ladder is approximately 34 mW. The above resistances are relatively small, that the resultant power consumption is quite large, driving up the entire power consumption of the Flash ADC by an estimated total of 15%. In order to reduce the reference ladder power consumption, it is required to increase the reference resistance in-turn leading to a higher input-reference feed through.

To overcome the above mentioned power problem, a series of dynamic (transistor) capacitors were used in this work to decouple the reference ladder output. The transistor's functioning as dynamic capacitors, were used to split the reference net into 4 de-coupled sections. This de-coupling effect meant that the small signal circuit analysis shows that the worst case input feed through impacts at the mid-level of each separated section as compared to the middle of the original ladder. The ratio of the W/L of the transistor was determined such that the resulting feed through is reduced as a fraction of the original feed through, thereby enabling the use of a larger resistor in the reference ladder. Figure 5.9 shows the small signal equivalent circuit of the de-coupled circuit.

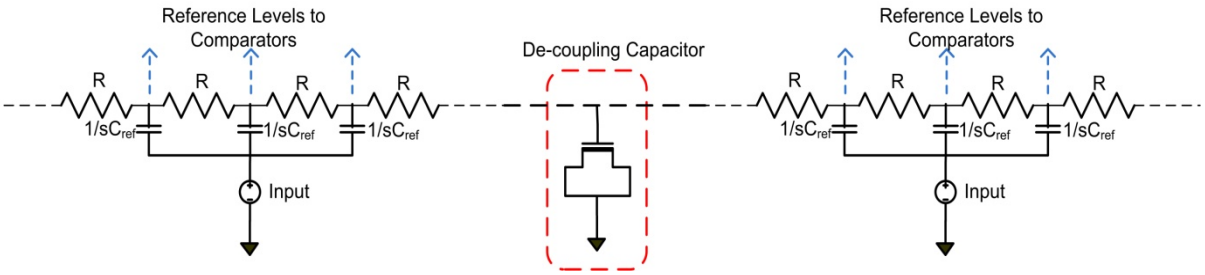


Figure 5.9: Reference net de-coupled into sections using an active NMOS as the dynamic de-coupling capacitor

The result of this de-coupling means that equation 5.14 can be modified to include the de-coupling number η_D such that;

$$R_T \leq \frac{7.3\eta_{LSB}}{\pi f_{in} C_T \eta_D} \tag{5.15}$$

where $\eta_D \leq 2^N$.

Considering η_D as four, the maximum reference net resistance can be increased to 500 Ω, with each resistor having a value of 33.3 Ω, an increase of nearly 20%. This increase has a cumulative effect of reducing the total power consumed by the reference ladder to 2 mW, a substantial drop of 62.5 %. This reduction in the power consumption of the reference ladder, impacts on the total power consumed by the converter, by a significant amount. The downside of this reduction is however an increase in the total real-estate used by the converter [77, 82].

5.3.1.2 Resistor Mismatch Issues

Resistor mismatch in the reference ladder causes significant concern, as it results in the actual resistance value deviating from the desired value. This results in the deviation of the different levels, leading to irregular output from the comparator bank. Taking the reference net resistor variation as δR, and subsequent deviation as $\sigma_{R(dev)}$, an analytical model was simulated and its variations plotted to estimate the maximum deviation from nominal values. The analytical model was created using a Gaussian distribution of the variation as shown in equations 5.15 and 5.16 [77, 82, 83].

$$\sigma_{R(dev)} \propto \frac{\delta R(N)}{N\,\delta R(0)} \tag{5.15}$$

$$\sigma_{Vref} \propto \frac{\delta V(N)}{N\,\delta V(0)} \tag{5.16}$$

As the ENOB output target is the overriding concern, the mismatch was measured for resistance variation and supply variation σ_{Vref}. Figures 5.10 (a) – (b) show the results of these measurements from simulations performed on the reference net analytical model.

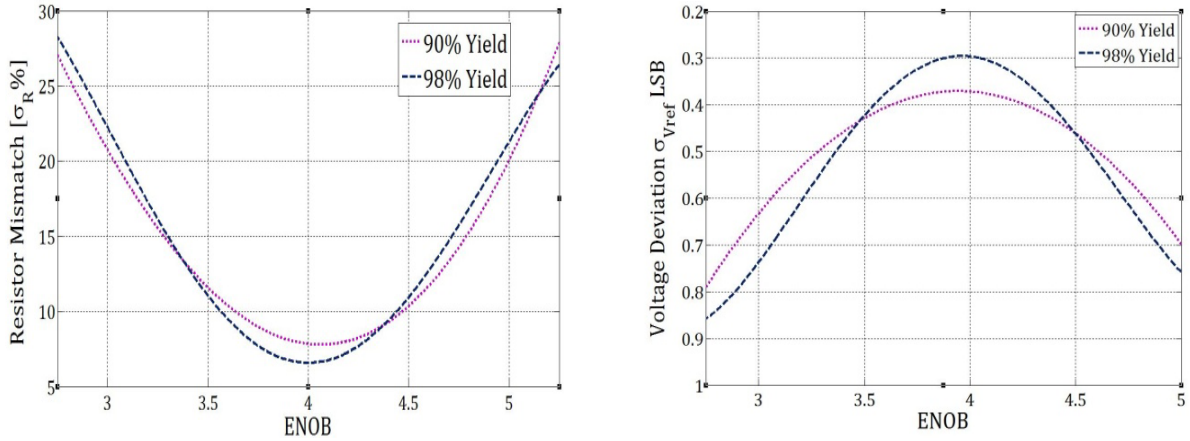


Figure 5.10: Mismatch and voltage deviation for the resistor ladder

From the figures it can be discerned that for an ENOB target close to 4 bit, the resistance mismatch accounts to a maximum of 6% for 98% yield and 9% for 90% yield estimates. The supply variations also are also measured to be steady at 0.3 LSB for 98% yield and 0.54 LSB for 90% yield estimates. The calculation of these values shows that the target reference resistance and supply voltage hold steady for the Flash ADC designed in this work.

5.3.2 Design of High Speed Encoder

As mentioned before the 3 main stages of the Flash Architecture are the reference ladder, comparator and the encoder. The design and functionality of the high speed encoder plays an important role in defining the optimum performance including speed, power, metastability and area of the entire ADC design. Typically the speed of the encoder is one of the limiting factors affecting the overall performance of the converter.

The following sections describe the different encoder architectures explored in this thesis along with their gate sub-circuit design and performance related to the specifications set out earlier.

5.3.2.1 ROM Encoder

A typical encoding methodology for Flash architecture is shown in Figure 5.11. It is composed of diodes and a pull down resistor network. This type of topology, although being the simplest and easiest to design has its limitation in terms of speed and functionality.

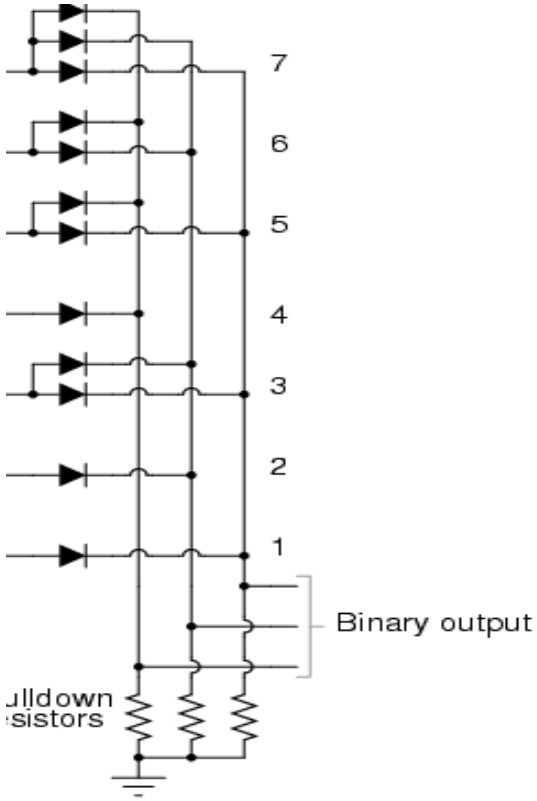


Figure 5.11: Typical ROM Encoder for FLASH ADC

The overall performance of the converter in terms of linearity, Signal to Noise Ratio (SNR), Signal to Noise-Distortion Ratio (SNDR) is co-dependent on the performance of the encoder [42]. The ROM Encoder although simplistic in design is not an effective architecture for high speed design.

5.3.2.2 Thermometer to Binary Encoding

In the flash architecture, the outputs of the comparators are linearly increasing or decreasing. This linear variation leads to what is called as a Thermometer encoding methodology. Most modern encoder designs are based on the thermometer to binary conversion scheme [84, 85].

$$\begin{aligned} K_1 &= \overline{C_1\overline{C_3}} \bullet \overline{C_5\overline{C_7}} \bullet \overline{C_9\overline{C_{11}}} \bullet \overline{C_{13}\overline{C_{15}}} \\ K_2 &= \overline{C_2\overline{C_6}} \bullet \overline{C_{10}\overline{C_{14}}} \\ K_3 &= C_4\overline{C_{12}} \\ K_4 &= C_8 \end{aligned} \tag{5.17}$$

$$\begin{aligned} B1 &= K1 \oplus B2 \\ B2 &= K2 \oplus B3 \\ B3 &= K3 \oplus B4 \\ B4 &= K4 \end{aligned} \tag{5.18}$$

Equations 5.17 and 5.18 demonstrate the process of transforming the 16 comparator levels into a 4 bit binary representation, utilising an intermediate gray coding technique to avoid code skipping or metastability issues [84, 86-88]. Figure 5.12 shows the gate-level representation of the thermometer to binary encoding scheme.

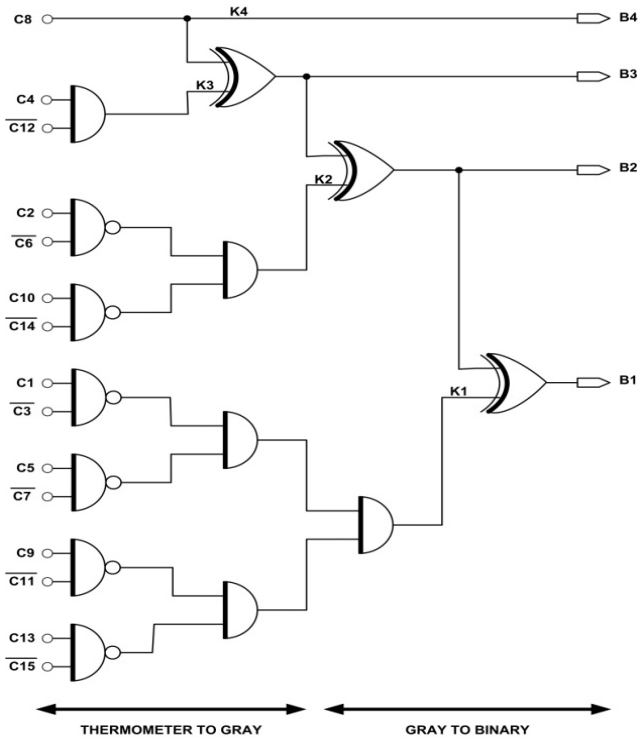


Figure 5.12: Gate level implementation of the thermometer to binary encoder

To explore other alternatives apart from the universal gate level implementation, the thermometer to binary encoder was also designed using a Wallace Tree Structure as shown below in Figure 5.13 [89, 90].

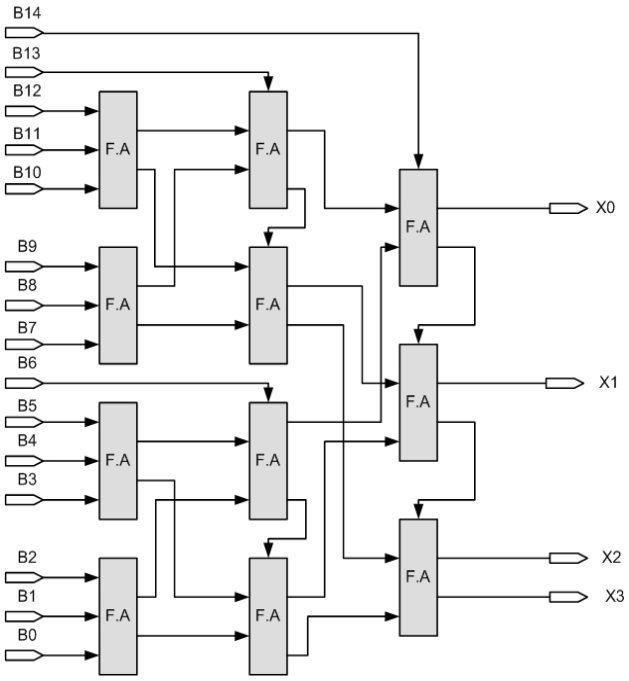


Figure 5.13: Thermometer to binary encoder using the Wallace Tree methodology

The Wallace Tree is typically composed of a number of full adders that are linked to obtain an N bit output. Traditionally Wallace Tree encoder structures are built using multiplexers [90-92]. The Wallace Tree shown in figure 4 was designed for a 4 bit flash ADC and is made up of 11 full adders which encode the 15 bit input to a 4 bit binary logic.

5.3.2.3 Encoder Sub-Circuit Design

The design of each of these individual components for the aforementioned 2 encoder configurations was performed using two methodologies. A static implementation was carried out by using only 2:1 Multiplexers on both the topologies. A dynamic implementation using Common Mode Logic (CML) gate design was also performed on both structures shown in figures 5.14 and 5.15 and their respective outputs compared for performance.

- **CML Implementation**

Figure 5.14 shows the design of a NAND/AND gate using a fully differential CML technique. The input pair transistors are fully differential to provide good immunity against supply noise and mismatch. The gate makes use of a differential clocking mechanism too which offers good immunity against linearity errors [42, 92].

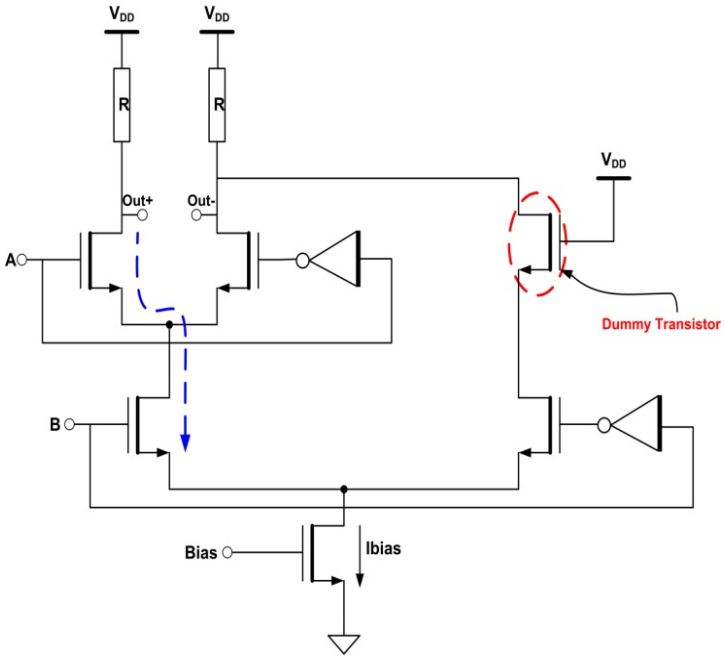


Figure 5.14: CML gate implementation for NAND/AND functionality

- **MUX Implementation**

Figure 5.15 shows a multiplexer gate used in the implementation of the full adder circuit for the Wallace Tree Encoder. The multiplexer was designed using simple transmission gate logic with the outputs inverted to obtain a NAND/AND functionality [65, 92, 93].

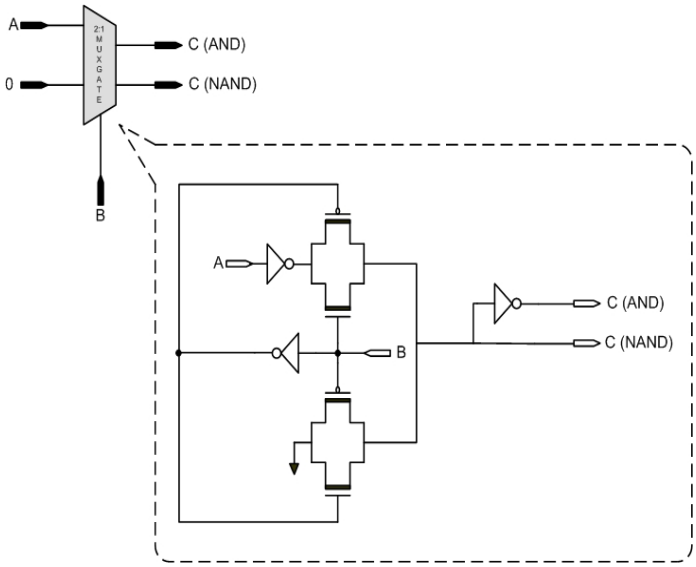


Figure 5.15: Multiplexer based gate used in the encoder design

From figure 5.15, the traditional architecture for the multiplexer can be modified to work as a typical gate. The select lines of the multiplexer was used as the secondary input and one of the regular inputs were grounded so as to feed a constant zero to the input logic. The output tapped can then be inverted so as to obtain a AND as well as a NAND gate [92].

5.3.2.4 Pipelining

Pipelining of the encoder stages is an important performance enhancer in terms of the overall delay reduction in the circuit. However pipelining a circuit means that there is an additional power and area consumption. There are few ways to pipeline a circuit including adding buffers, inverters for sharper roll-off but the most effective methodology is by the use of latches and flip-flops. To pipeline a circuit it is necessary to split the circuit into sections and induce the latches wherein the gate fan-in is the maximum. In this thesis pipelining was performed on both the encoder architectures and the results compared. Two different types of latches were used to implement the pipelining. One of the latches is a CML based fully differential latch. The advantage of this latch is its very low swing operation, high resistance to input jitter and use of a fully

differential clocking mechanism. The clocks regulate the speed of operation of the latches and in turn also have an effect in the total gate delay of the encoder [85, 87, 92].

Figure 5.16 shows the circuit of the CML latch identical to the latch used for the comparator implementation explained in Chapter 4.

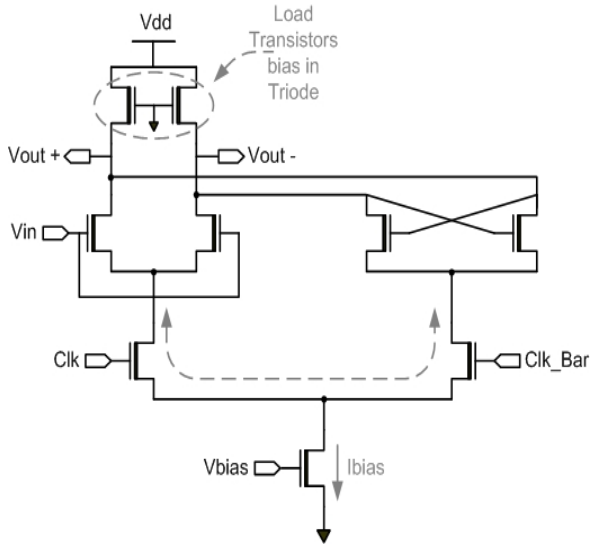


Figure 5.16: Circuit diagram of a CML latch used for pipelining the encoder

As mentioned before the structure of the CML latch is based on a track and hold mechanism. The load, typically composed of resistors was replaced by NMOS transistors biased carefully in the triode region. This was done so as to maximise the speed of the latch to enable low swing and faster slewing. The only drawback was the increased possibility of supply noise injection but there was enough voltage headroom available to minimise this effect [92, 94].

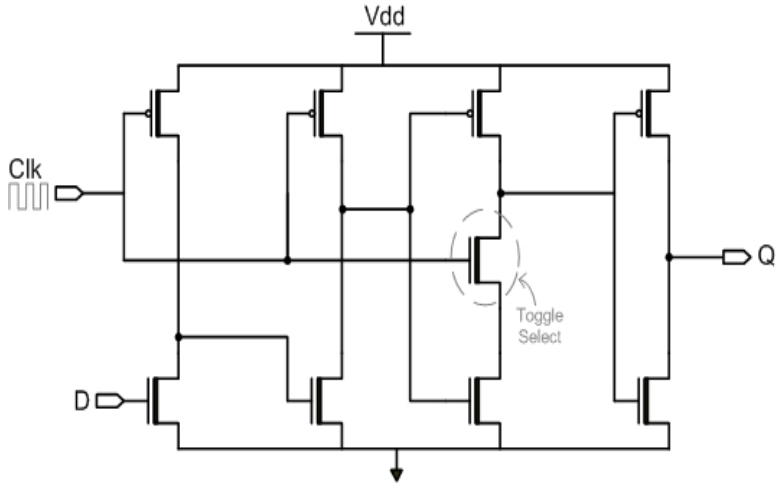


Figure 5.17: Inverter chain D-type Flip Flop latch used for encoder pipelining [94]

The other type of latch (Figure 5.17) used was an inverter chain based flip-flop. The latch is made up of two sections based on a master-slave inverter chain configuration. The toggle transistor at the middle is carefully sized so as to allow precise switching of the clock to reduce any delay at the output. The speed of the inverter chain along with the single phase clock effectively determined the total gate delay present in the circuit [94]. The following section discusses the implementation results of the two architectures (Priority Thermometer to Binary and Wallace Tree Thermometer to Binary) before pipelining and after one and two stage pipelining using the aforementioned latch and flip-flops.

5.3.3 Encoder Implementation and Performance

The propagation delay typically sets the maximum switching frequency of the encoder. It is seen that however the power consumed by the encoder is proportional to the switching frequency. The following graphs give an overview of the total power consumed for different switching frequencies for both the priority and the Wallace tree configuration. Figures 5.18 and 5.19, show the performance of the encoders without pipelining, in terms of their total power consumption and their Probability of Missing Code (PMC).

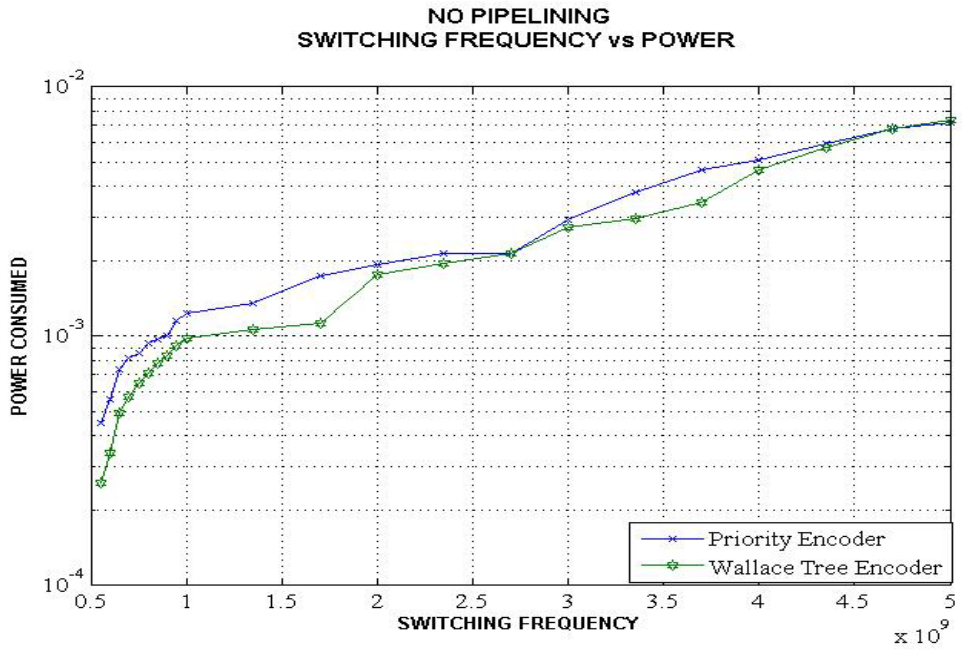


Figure 5.18: Power performance versus switching frequency without pipelining

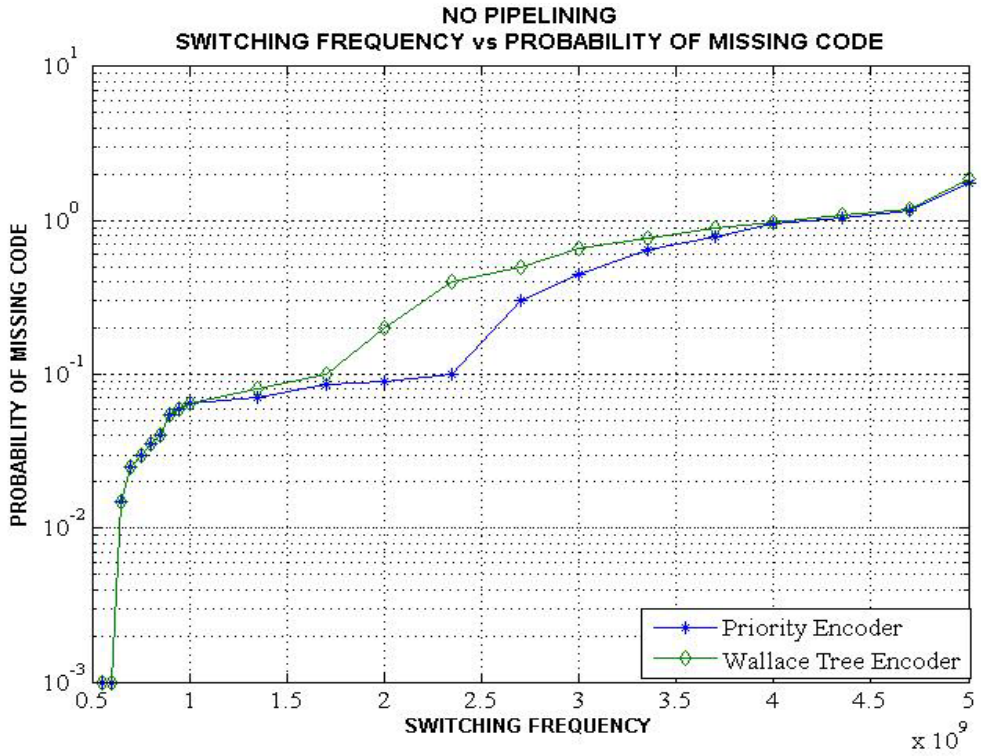


Figure 5.19: Probability of Error versus Switching Frequency without pipelining

It can be observed from Figures 5.18 and 5.19 that the power consumed by the encoder increases significantly at higher frequencies. It is also observed that there is a greater chance of missing codes without the use of pipelining due to the increase in the overall propagation delay of the gates.

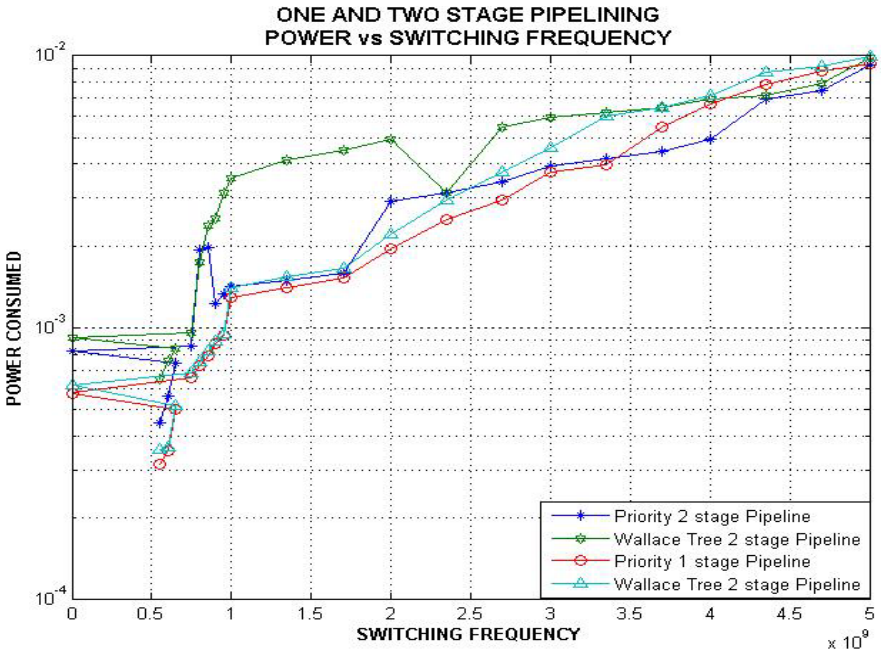


Figure 5.20: Power performance versus switching speed for one and two stage pipelining

To mitigate these effects one stage and two stage pipelining was performed on the encoder. The results of the pipelining are shown in Figures 5.20 and 5.21 respectively for power performance and erroneous code.

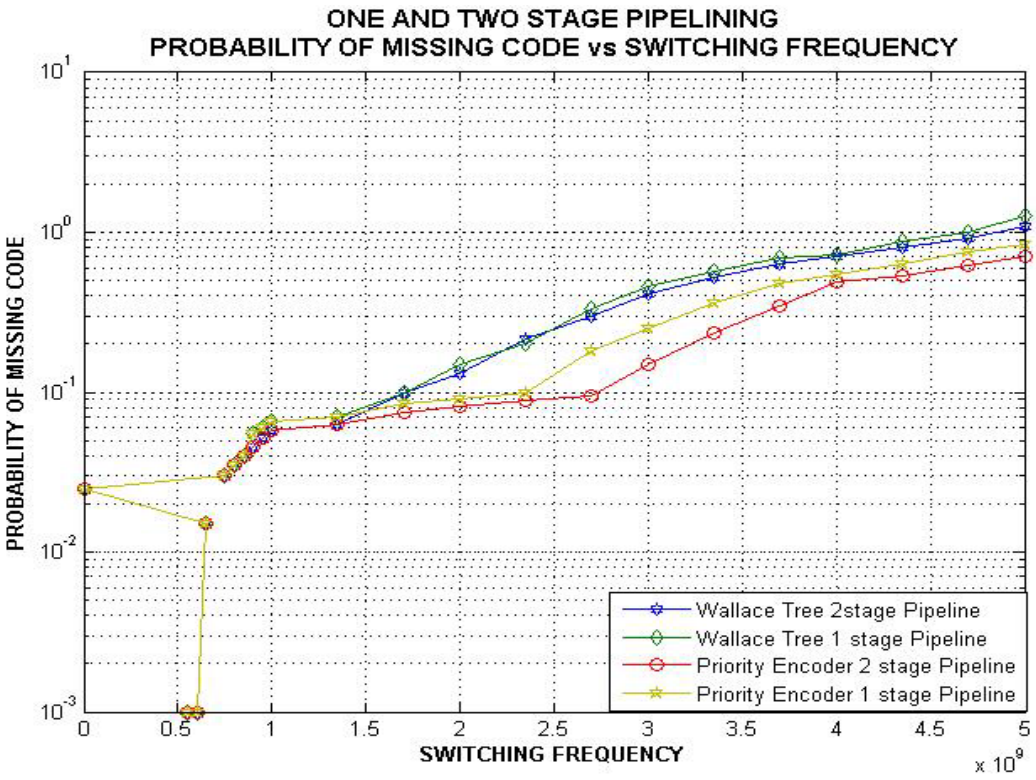


Figure 5.21: Probability of Error versus the Switching frequency for one and two stage pipelining

From the two graphs it is observable that pipelining decreases the probability of missing codes significantly. Moreover multistage pipelining does provide a less probability of missing codes, however at an additional cost of increased power consumption.

From the results it can be observed that pipelining increases the overall performance of the encoder with however an increase in the amount of power consumed. Some critical observations from the graphs conclude that CML designed encoder performed the best overall with the least probability of missing codes. At lower frequencies the Wallace tree encoder had reasonably good performance in terms of the total power consumed but is susceptible to erroneous code problems.

The schematic of the implemented encoder using Cadence Virtuoso Design Suite is as shown in Figure 5.22. The encoder was tested for its performance on a high speed flash ADC to meet the requirements set for this design.

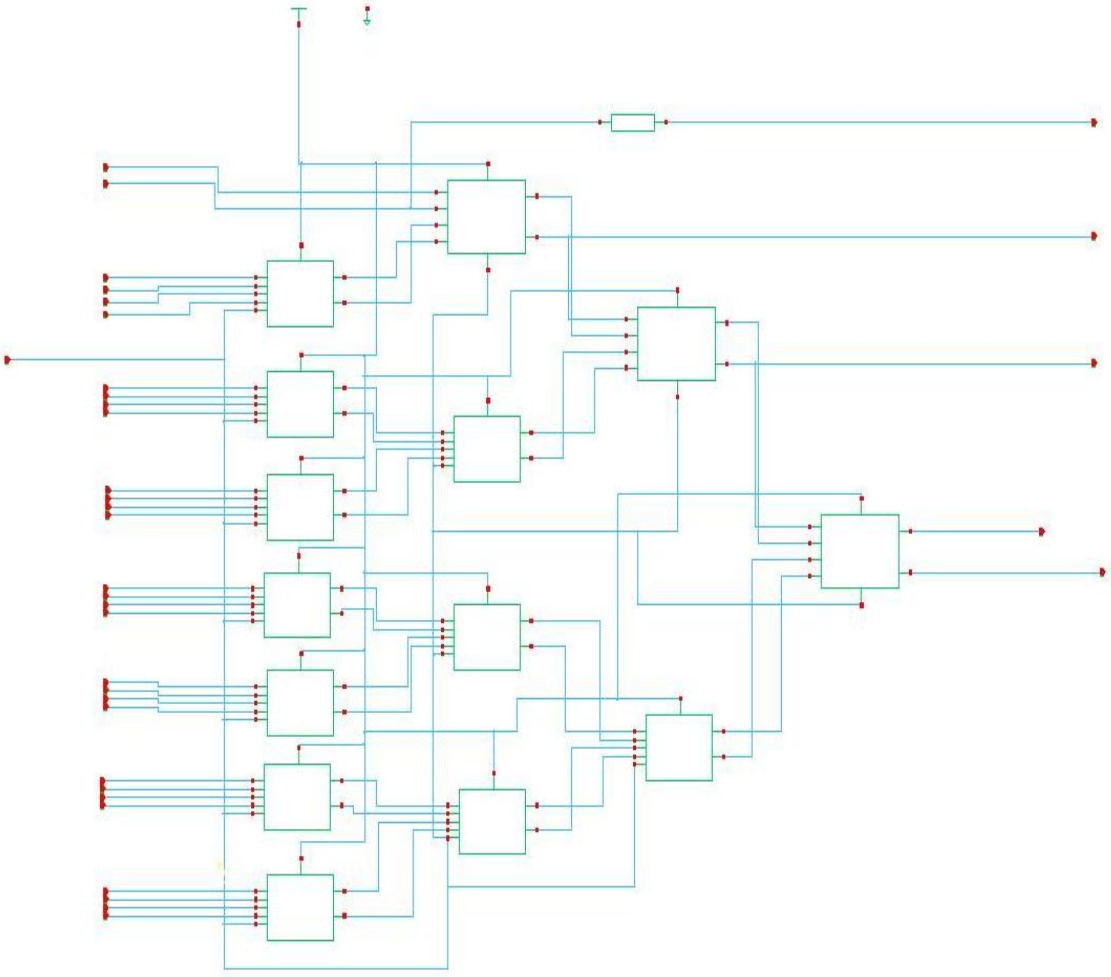


Figure 5.22: Gate level circuit of the implemented encoder for the high speed FLASH ADC

5.4 Flash ADC Top Level Implementation

Having designed the three sections of the converter, it was required to collate and integrate them together to obtain a fully functional design. The high speed Flash Analog to Digital Converter was designed and simulated in Cadence Design Environment using standard V_T ST-Micro 90nm CMOS technology. The design was simulated based on a 1 V supply with a 1 V full-scale reference.

The complete design of the Flash converter is shown below in Figure 5.23. The figure shows the three sections of the ADC, with the high speed Encoder at the centre surrounded by 15 fully differential comparators, each fed by a resistor reference ladder. The schematic drawing of the implemented ADC represents the actual arrangement in the floor plan of the layout of the Flash ADC.

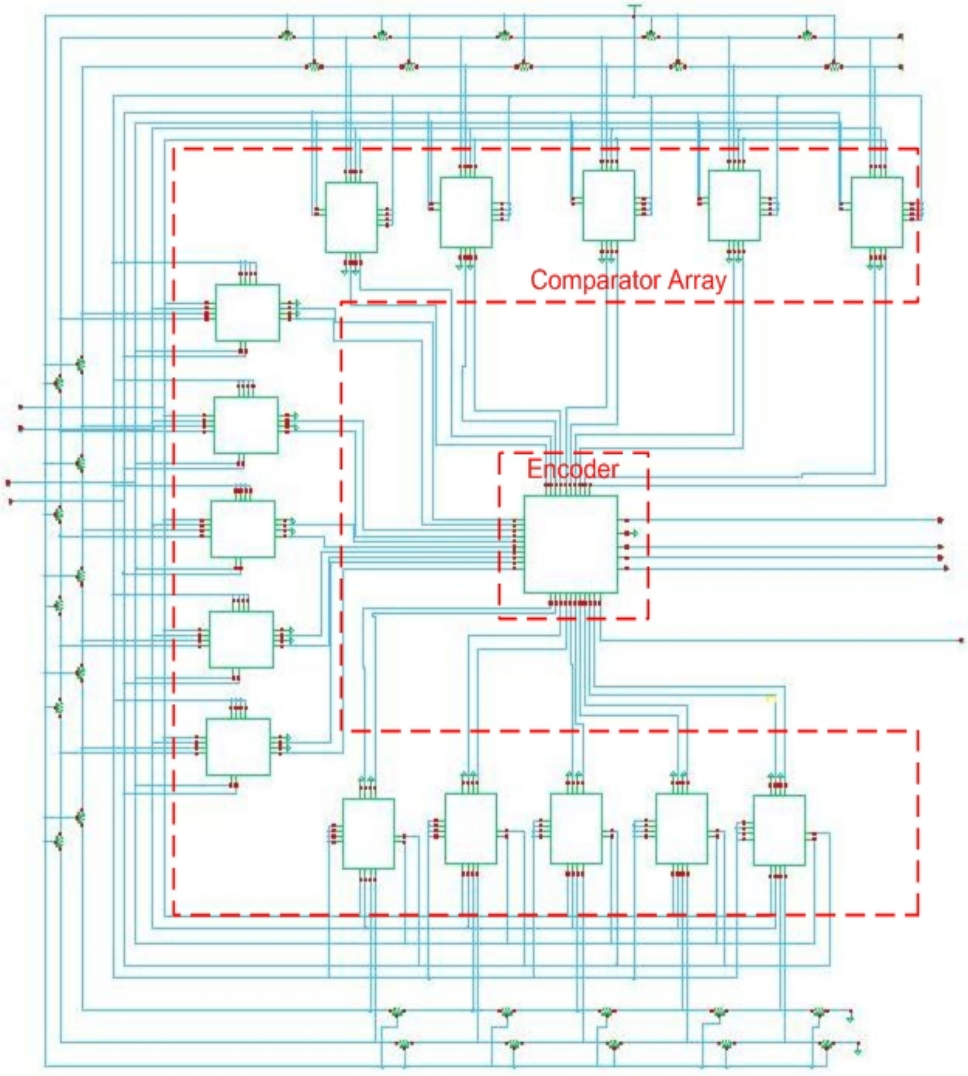


Figure 5.23: Circuit schematic of the complete Flash Analog to Digital Converter

The floor planning of the layout of the Analog to Digital Converter is important in order to minimise the effects of parasitic that play havoc on the output of the converter introducing offset due to mismatch, comparator slewing, clock and output signal delay, amongst others [95, 96]. For the implementation of the Flash ADC in this thesis a

disjointed E-Shaped Floor plan with the encoder occupying the centre was conceived. The reason for implementing the E shape was to take full advantage of the differential output comparator and the reduced distance from the comparator output to the encoder input. The E design also minimises the total amount of input feed through affecting the comparator and reduces the overall mismatch between different comparators.

Traditional Parallel I (P-I) shaped Flash ADC floor planning suffers from a few issues in relation to its performance as follows;

- Distance between the reference node high value and the reference node low value causes signal integrity issues at the input to the comparator. Increasing the width of the signal path leads to increased parasitic capacitance affecting the input.

  In this floor plan the maximum distance between the reference node pins is only 5 comparators at each side of the E, thereby minimising the total parasitic impacting at the input of the respective comparator.

- In the P-I floor plan there in a possibility of large mismatch between the comparator at the top of the design and bottom of the design. This leads to a large offset at the comparator output due to switching node variations affecting the signal baseline at the comparator output.

  The E plan overcomes this issue by a factor of 1/3 as along each side, there exists a mismatch between a maximum of 5 comparators instead of 15 in the P-I plan.

- The P-I floor plan typically needs a bottom and top drain comparator which act as dummies to mitigate the negative effects of mismatch and large output capacitances due to uneven distribution of current feedback affecting the encoder input.

  The E floor plan reduces the negative effect induced by the current feedback as the current is split equally into the 3 arms.

The above advantages of the E floor plan come at an additional cost of need for extra pins in the layout, which result in duplicate pads for the entire ADC chip. The extra pads, depending on foundry and manufacturing may lead to increased cost during packaging.

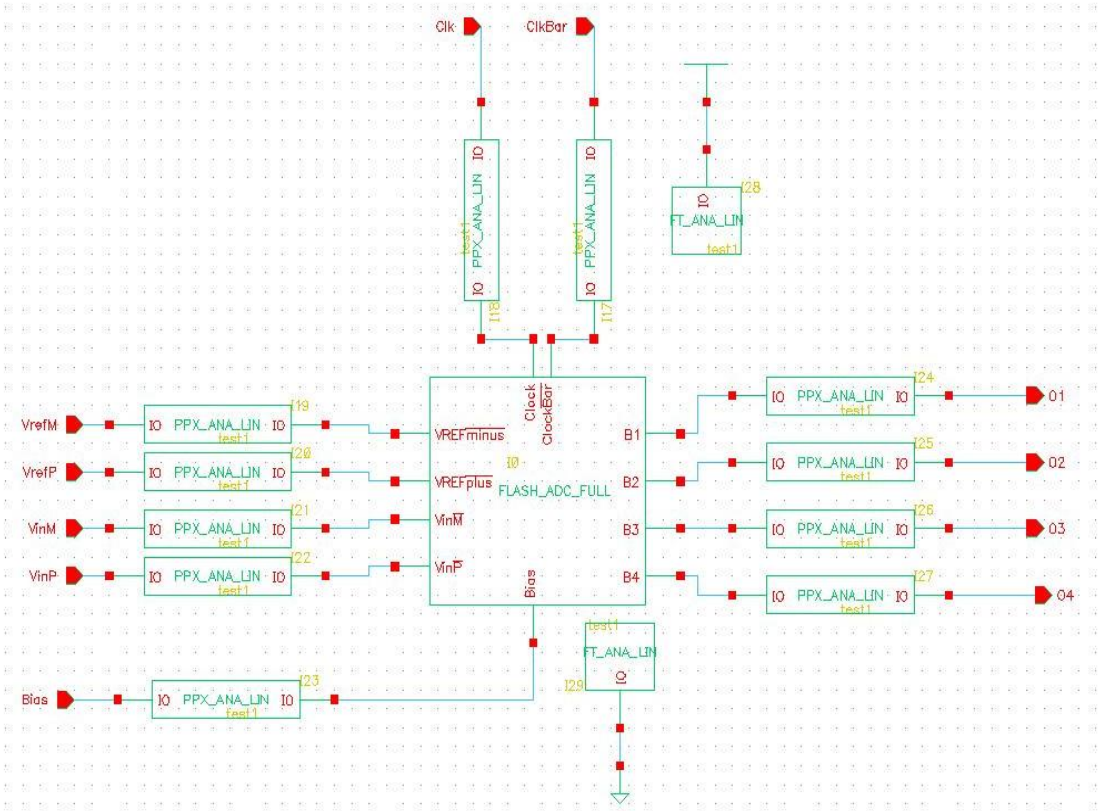


Figure 5.24: Schematic of the Flash ADC with pad configuration at the various I/O's

Figures 5.24 and 5.25 show the circuit schematic and the complete chip level layout implementation of the high speed Flash analog to digital converter.

A total of 7 metal layers were used to perform the routing. The complete routing of the analog to digital converter was performed manually without the use of any auto-routing means.

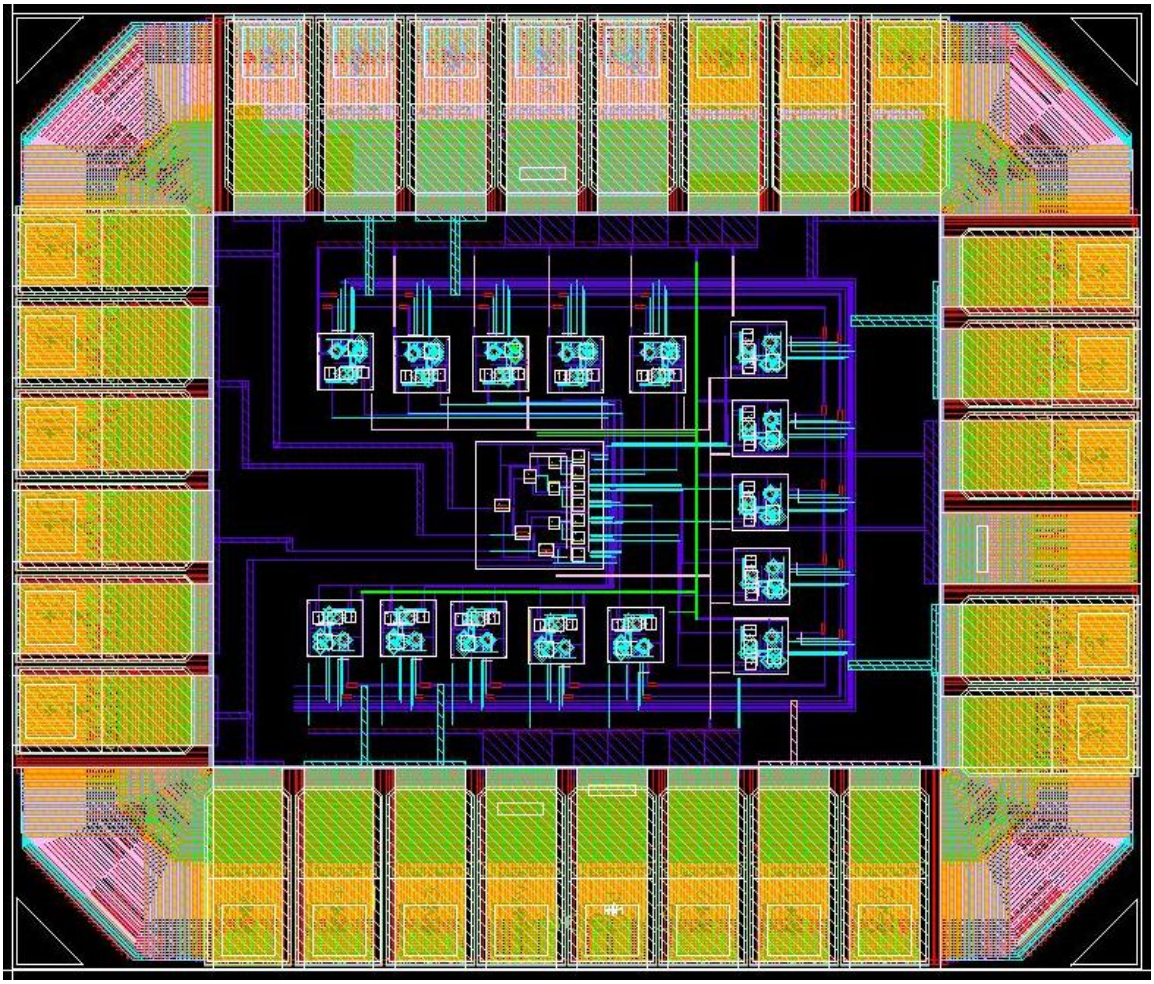


Figure 5.25: Complete chip level layout implementation of the high speed Flash analog to digital converter

An in-depth analysis of the post layout working of the ADC was performed in adherence to the requirements for UWB signalling, as set previously in the thesis. The functionality of the various performance parameters of power consumption, linearity (INL and DNL), dynamic range, signal to noise ratio, amongst others will be presented in Chapter 7. This was done so as to set a reference and perform a full and comprehensive comparison to the reconfigurable architecture, which will be discussed in the following chapter.

5.5 Conclusion

This chapter describes the design and implementation of a high speed fully differential Flash analog to digital converter for a DS-UWB communications scheme. An introduction was given into the different performance characteristics that are used to verify the functionality of the converter design. An in-depth look into the different Static

characteristics like Quantisation Error, INL and DNL and Dynamic performance characteristics like the SNR, SNDR, ENOB, amongst others were presented. This was done to obtain an insight into the parameters that govern the functioning of the design presented in this chapter and also define the result of the working of the reconfigurable design which will be detailed in the following chapter.

The chapter then goes onto present the detailed design of the reference ladder and discusses methods to deal with issues such as input feed through and mismatch. The chapter then goes on to detail the design of a high speed encoder. An overview of the different types of encoder designs was presented as well as a functional comparison between the Priority thermometer to binary encoder topology and the Wallace Tree thermometer to binary encoder topology to determine best suited for this converter design. Issues relating to encoder power consumption and missing codes, with and without pipelining were discussed to enable an informed choice.

The chapter finally concludes with an in-depth discussion of the top level implementation of the Flash converter, along with the successful integration of the three main sections i.e. Reference Ladder, Comparator Array and Encoder. Issues related to layout floor planning and routing were detailed along with a minor comparison of the typical chip floor plan and the disjointed E shaped plan.

This chapter now sets a performance base for a comprehensive discussion and comparison with the design of the reconfigurable analog to digital converter which will be presented in the following chapter of this thesis.

Chapter VI: **Novel Reconfigurable Analog to Digital Converter**

6.1 Introduction

The term "reconfigurable" refers to an action or a state of action, wherein the end result is a dynamically quantity that is interdependent on the surroundings that govern the functioning of the said quantity or system. To put a perspective in terms of its relevance to an analog to digital converter, it means that the output resolution or number of bits of the ADC is a value or quantity that is not static but can be made to change depending on the conditions input into the converter system.

In this thesis an attempt is made to implement this dynamicity in terms of the final output resolution of the ADC, depending on factors at the input. This chapter will demonstrate the attempt to implement a bit varying converter, specifically designed to handle the large bandwidth requirement for functioning in a DS-UWB communication scheme. The chapter will also highlight the main challenges involved in the implementation of such a converter, along with the advantages and disadvantages of the design. To demonstrate proof of concept a detailed comparison of the functioning of the reconfigurable design will be presented in Chapter 7, comparing it to the design implemented in Chapter 5.

This chapter will demonstrate the ability of the converter to switch its output resolution between 2 to 4 bits, attempting to function however within the set requirements of

input bandwidth, sampling rate and other performance metrics that govern the ADC functionality.

6.2 Background into Reconfigurable Converters

Before embarking onto the modalities of the design it is important to take a brief look to the few other types of reconfigurable converters in existence. The brief review will help obtain a comparison of their functioning attributes and as to how they compare with work detailed in this chapter.

There are very few reconfigurable analog to digital converters which are designed specifically to target the needs for high speed DS-UWB communication. Nicole et.al. [97] demonstrates a pipeline analog to digital convertor that is suitable for WCDMA/GSM to enable operations in 3G mobile systems. The ADC using pipeline topology has a 1.5 bit/stage resolution to enable reduced power operation. The ADC has a maximum sampling frequency of 15 MHz. The maximum resolution is 10 bits along with a tuneable DC voltage from 1.0—1.5 V range. The convertor uses two non-overlapping clocks of different phases.

Another design by Hsu et.al. [98], is also based on a pipeline time interleaved design with the resolution tuneable from 5 to 7 bits however, with a maximum sampling rate of 1.1 Gsps. The ADC has been implemented for a MB-OFDM UWB communication scheme and using 90nm CMOS process. The reconfigurability is achieved in 2 stages, with the pipeline mode for lower resolution and the Σ-Δ mode for higher resolutions. The ADC however has a maximal input frequency of 550 MHz keeping with MB-OFDM requirements.

Martin et.al. [99] also detail a reconfigurable analog to digital converter for UWB and also Bluetooth (BT) applications. The reconfigurable design consists of two ADC's, one for UWB signalling based on capacitive interpolation flash design and the second a quantiser of Σ-Δ for BT applications. The receiver is a dual mode architecture employing two separate channels, one for each communication scheme. Both ADC's have a maximum resolution of four bits, with the ADC for UWB having a maximum sampling rate of 528 MSPS and the one for BT sampling at 1 MSPS. The UWB ADC in

this design is targeted to work in the MB-OFDM scheme. The UWB ADC was designed to have a maximum bandwidth of 264 MHz, having a dynamic range of 30 dB while working in the MB-OFDM scheme.

The three ADC's listed above target low speed sampling and communication objectives. The second ADC comes closest to dealing with UWB communication but however is restricted in its ability to sample at 1.1 Gsps with a 550 MHz input. The attempt in this work is to design a converter capable of sampling an input of 1.5 GHz or more employing a multi-GHz sampling rate. This design is in keeping with the requirements for a DS-UWB communication scheme, that which has been detailed out previously in this thesis.

The following sections will discuss in detail the different sections that make up the reconfigurable design and present the final implemented converter.

6.3 Reconfigurable ADC Concept

Classical flash based architectures although achieving high speeds have a serious drawback in the amount of power consumed by the ADC. As previously seen the parallel architecture has 2^N-1 comparators relating to 2^N-1 logic levels. This results in a 2^N fold power consumption. For communication mediums employing high bandwidth signalling, requiring a large sampling rate, poses a problem of high power consumption.

The following subsections present a new power saving design for high-speed ADC's, based on the marriage between pipeline and flash architectures. A simple representation of the typical pipeline ADC is as shown below in Figure 6.1.

A pipeline ADC uses an input sample and hold circuit to perform initial sampling, the output of which is then fed into an OP-AMP. The OP-AMP which behaves as a comparator, then compares the input with Vref/2. Depending on whether the signal level is higher or lower the output is then passed through a summing circuit and a multiplier circuit before feeding into the second stage sample and hold. Also a final error correction and timing synchronisation circuit is required to obtain a proper output [100].

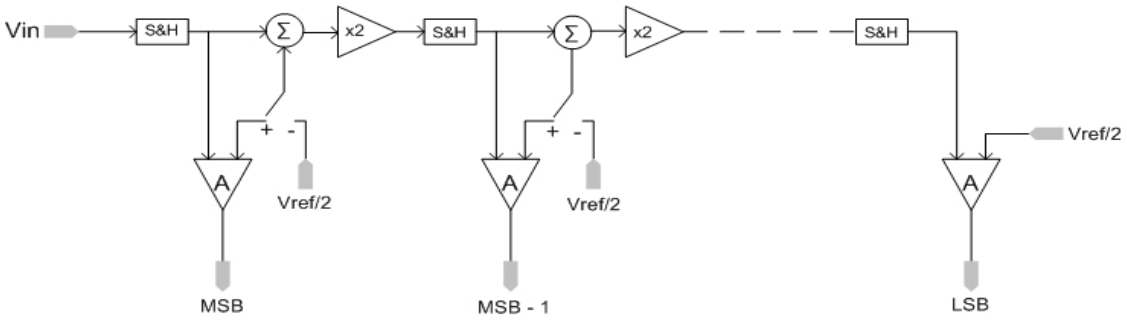


Figure 6.1: Typical architecture of a pipeline ADC

The Pipeline ADC has the disadvantage of using several stages to obtain a single bit output. This introduces unnecessary delay in the circuit, hampering its speed, due to many summers and multipliers used to perform a single operation. Maximum sampling rate for pipeline ADC are about 300 Msps, which doesn't put it into UWB range. Depending on the input present at each stage, the amplification factor of each input OP-AMP may need to be different, putting additional strain on the working of the multiplier and summation circuit, which also may need to compensate for the extra gain.
The Flash ADC on the other hand is invariably followed by the thermometer to binary encoder which has its own issues with mismatch and power consumption. In addition if Controllability is desired in terms of resolution, the encoder has to be modified and hence needs to be made programmable involving higher power consumption and additional hardware costs.

The idea for a reconfigurable architecture was to design and implement a converter that achieves speeds relative to that of full flash architecture's, however with appreciable power and hardware reduction based on the reconfigurability.

It is known that a comparator needs a specific reference that is compared with the input to determine whether the output is high or low. Consider a situation where in the output of the comparator determines and sets the threshold for the succeeding stage comparator. This scenario allows cascading of multiple stages, where in each stage provides an output, the combination of the outputs of all the different stages, setting the resolution of the analog to digital converter. The concept can be implemented by using high speed comparators along with accurate and fast analog multiplexers. To obtain a clearer understanding, consider the top level representation shown in Figure 6.2.

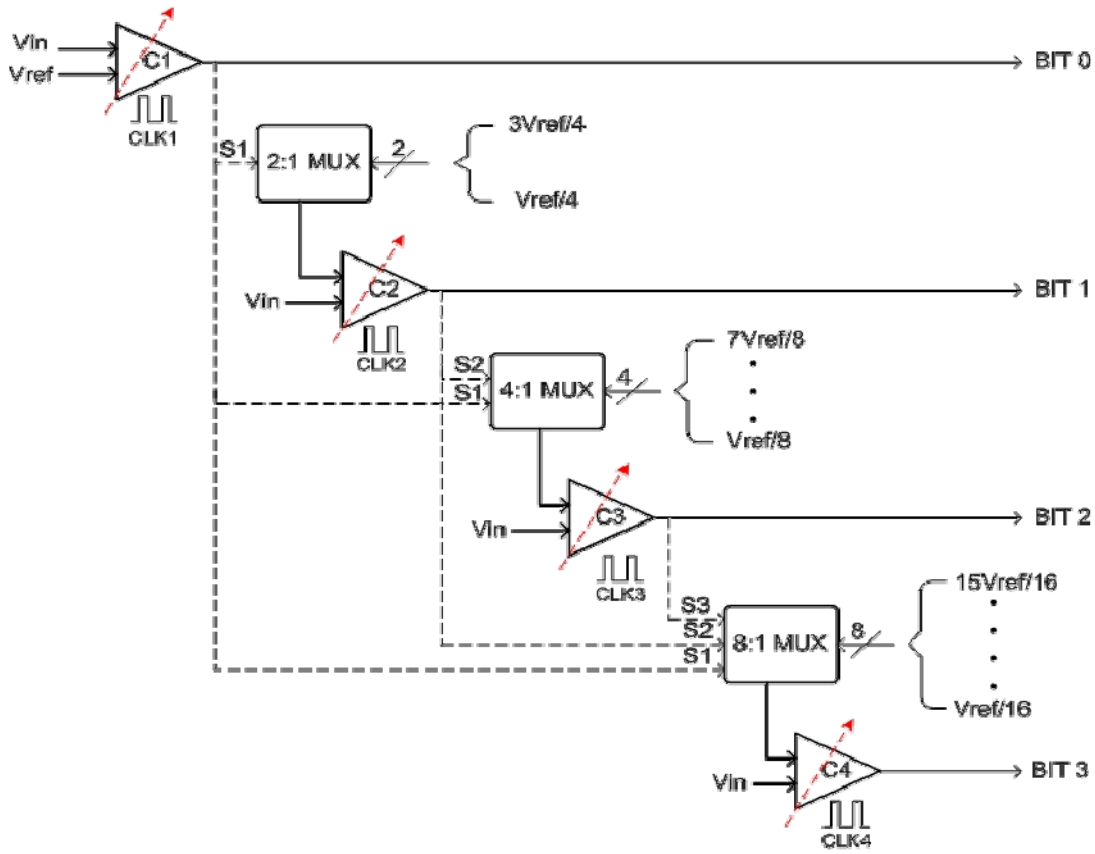


Figure 6.2: Basic representation of the reconfigurable architecture [100]

Each comparator stage is preceded by a multiplexer that selects the reference threshold depending upon the output from previous stage. Between two stages there is an effective 0.5 2:1 multiplexer delay (τ_{mux}). The higher order multiplexers were designed by combining different 2:1 multiplexer stages with the first stage, which in turn sets the threshold values just after the first output has arrived. For the 4 bit design the final output effectively arrives after a delay of $2*\tau_{mux}$. The difference in the reduced evaluation and pre-charging time for the comparators allows for the use of a skewed clocking methodology, reducing the need for pipelining and clock matching in for subsequent stages. The clocks have effectively small duty cycles which help in each of the comparators not experiencing any clock matching issues which may require additional latching circuitry at the output. The design also reduces the need for an encoder circuitry or any form of co-ordination circuitry as the output bits are a direct binary representation of the different analog levels. The design has a major advantage in that it uses only N comparators instead of 2^N, thereby making the power consumption a linear factor of the resolution and not exponential like a flash ADC [100].

In order to explain the working of the reconfigurable concept, consider the flow diagram presented in Figure 6.3.

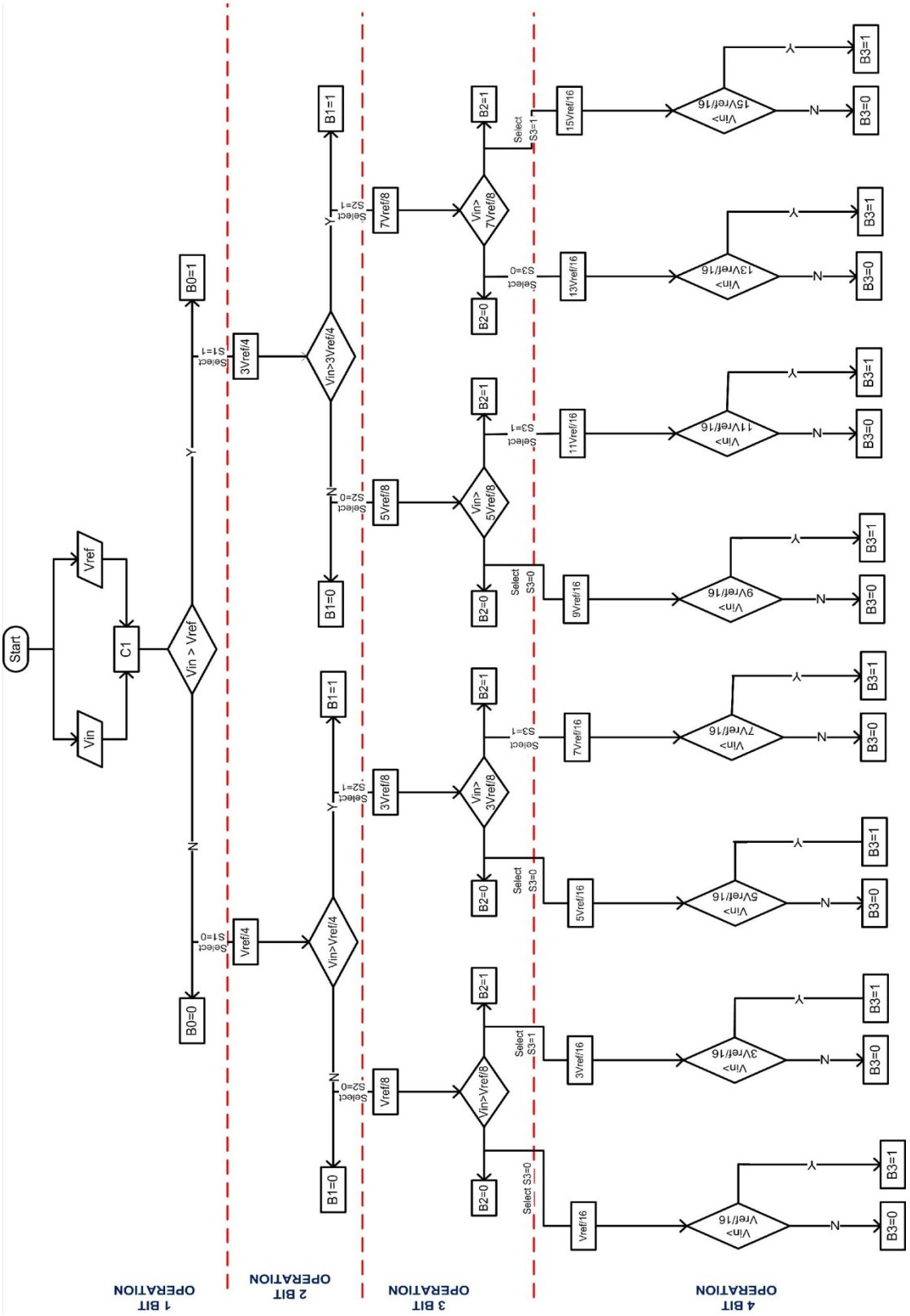


Figure 6.3: Flow diagram of the reconfigurable concept

The flow diagram of the reconfigurable concept shows that the converter can be operated in any mode ranging from 1 to 4 bits depending on requirement. Consider a four bit operation whereby the entire circuit is active.

For a reference connected to 1 V, the half maximum value is 0.5 V which is considered to be Vref i.e. Vref/2 (0.5 V) is Vref. In this design a 1 V reference was considered, however the reference node can be set to any voltage depending on requirement. It was however found that setting the primary reference below 0.35 V, would result in improper operation and missed bit value at the outputs of the succeeding stages.

The first comparator C1 compares the input to the reference and produces an output high (B0=1) or an output low (B0=0) depending on the value of the input signal. The comparator compares the input based on a small duty cycle clock, level triggered on active high rather than edge triggered. This was done so as to enable the comparator to settle during active low of the clock.

The output of the comparator C1 then is fed into the select input (S1) of the first 2:1 multiplexer (MUX1). For the condition where B0=0, S1 is also set as 0 and when B0=1, S1 =1. MUX1 has 2 input lines which carry the reference voltages Vref/4 (0.25 V) and 3Vref/4 (0.75 V), representing the upper and lower threshold values. When S1=0, the output of MUX1 is Verf/4, which is set as the reference voltage for comparator C2 and when S1=1, the output of MUX1 is 3Vref/4 which is set as the reference voltage for comparator C2. Depending on the input and the reference selected during the 2nd clocking cycle, C2 produces an output high B1=1 or output low B1=0. The combination of the two outputs B0 and B1 result in 4 distinct binary levels i.e. 00, 01, 10 and 11, which is a 2 bit representation an analog signal.

Table 6.1 shows the operation of the reconfigurable concept in 1 bit mode and 2 bit mode. The 1 bit mode has only comparator C1 in active state, whereas the 2 bit operation requires both comparators C1 and C2 to be active. The “X” in table 6.1 is meant as a don’t-care condition as during 1 bit operation, the output of comparator C2 is null.

Table 6.1: Function for 1 and 2 bit operation of the reconfigurable concept

Condition	Bit B0	Bit B1	Bit B2	Bit B3	Next Stage Select
For 1 Bit Operation C1=Active					
Vin < Vref/2	0	X	X	X	S1=0 (Vref/4)
Vin > Vref/2	1	X	X	X	S1=1 (3Vref/4)
For 2 Bit Operation C1=Active C2=Active					
S1=0; Vin < Vref/4	0	0	X	X	S2=0 (Vref/8)
S1=0; Vin > Vref/4	0	1	X	X	S2=1 (3Vref/8)
S1=1; Vin < 3Vref/4	1	0	X	X	S2=0 (5Vref/8)
S1=1; Vin > 3Vref/4	1	1	X	X	S2=1 (7 Vref/8)

During phase 3 i.e. 3 bit operation, the outputs of the two comparators C1 and C2 function as select line inputs to the 4:1 multiplexer (MUX2). MUX2 is a combination of 2 MUX1 designs, comprising of 2 select lines and 4 input lines that carry the reference voltages Vref/8, 3Vref/8, 5Vref/8 and 7Vref/8. The combination of the outputs of C1 and C2, sets S1 and S2. Depending on the S1S2 combination, one of the input lines is selected and set as the reference voltage for comparator C3. C3 then performs the comparison with the reference and outputs a high (B2=1) or low (B2=0). The high or low values set the select reference for the succeeding stage i.e. S3=0 or S3=1 depending on the combination of S1 and S2. Table 6.2 shows the different combinations for a 3 bit operation.

Table 6.2: Combination for 3 bit operation

Condition	Bit B0	Bit B1	Bit B2	Bit B3	Next Stage Select
For 3 Bit Operation C1=Active C2=Active C3 = Active					
S1S2=00;Vin < Vref/8	0	0	0	X	S3=0 (Vref/16)
S1S2=00;Vin > Vref/8	0	0	1	X	S3=0 (3Vref/16)
S1S2=01;Vin < 3Vref/8	0	1	0	X	S3=0 (5Vref/16)
S1S2=01;Vin > 3Vref/8	0	1	1	X	S3=0 (7Vref/16)
S1S2=10;Vin < 5Vref/8	1	0	0	X	S3=0 (9Vref/16)
S1S2=10;Vin > 5Vref/8	1	0	1	X	S3=0 (11Vref/16)
S1S2=11;Vin < 7Vref/8	1	1	0	X	S3=0 (13Vref/16)
S1S2=11;Vin > 7Vref/8	1	1	1	X	S3=0 (15Vref/16)

For the final phase involving 4 bit operation, the outputs of the three preceding comparators C1 – C3 play an important role in setting the value of the select lines. The three outputs feed into an 8:1 multiplexer (MUX3) comprising of 8 input lines, which are selected by a combination of S1S2S3 from 000 to 111. MUX3 was designed as a combination of 2 MUX2 circuits. The output of the comparator C4 depends on the value of the reference input set by a combinational selection of the outputs of comparators C1 to C3. Depending upon this reference, C4 produces either an output high (B3=1) or an output low (B3=0). The functional truth table for complete 4 stage operation is shown in Table 6.3.

Table 6.3: Functional truth table for complete 4 bit operation

Select	Condition	Bit B0	Bit B1	Bit B2	Bit B3
S1S2S3=000	Vin < Vref/16	0	0	0	0
S1S2S3=000	Vin > Vref/16	0	0	0	1
S1S2S3=001	Vin < 3Vref/16	0	0	1	0
S1S2S3=001	Vin > 3Vref/16	0	0	1	1
S1S2S3=010	Vin < 5Vref/16	0	1	0	0
S1S2S3=010	Vin > 5Vref/16	0	1	0	1
S1S2S3=011	Vin < 7Vref/16	0	1	1	0
S1S2S3=011	Vin > 7Vref/16	0	1	1	1
S1S2S3=100	Vin < 9Vref/16	1	0	0	0
S1S2S3=100	Vin > 9Vref/16	1	0	0	1
S1S2S3=101	Vin < 11Vref/16	1	0	1	0
S1S2S3=101	Vin > 11Vref/16	1	0	1	1
S1S2S3=110	Vin < 13Vref/16	1	1	0	0
S1S2S3=110	Vin > 13Vref/16	1	1	0	1
S1S2S3=111	Vin < 15Vref/16	1	1	1	0
S1S2S3=111	Vin > 15Vref/16	1	1	1	1

From Table 6.3 it can be seen that the output resembles a priority encoder disposition similar to that of the thermometer to binary output of a full flash analog to digital converter. A unique advantage of the above design is, even if comparator C2 is off, comparators C1, C3 and C4 produce an output which is congruous with a 3 bit working representation, albeit the reference levels having a less than 1LSB voltage difference,

not significant enough to cause error at the output. The output from the ADC needs no binary calibration as the result is a straightforward sequence and furthermore does not suffer from the metastability and missing code problem encountered by flash ADC's. The comparators also do not suffer from any input feed through problems as they are triggered with different duty cycles.

The following sections will detail out the implementation of the design using control switches and multiplexers and the challenges encountered during the design cycle. Primary emphasis has been placed on the discussion of the design of the multiplexers and control/enable switch, as the comparator design has already been discussed in Chapter 4 of the thesis.

6.4 Design of Novel Reconfigurable Converter

6.4.1 Design of a Novel Dynamic Self-Biased Analog Multiplexer

The novel analog multiplexer (AMUX) was design based on CMOS switching operation and optimised for high speed fully differential operation. The design of the switch was important considering that the switching speeds in this work were of the order of hundreds of picoseconds to a few nanoseconds. Before settling on the design, two types of design mechanisms were studied and tested for their suitability. The two designs were based on active body biasing and use of clock boosting mechanism.

The use of complementary switching is the primary mechanism that governs the working of analog multiplexer. A single transistor, either NMOS or PMOS are switches in their own right. Depending on the gate voltage applied, the transistor turns ON or OFF, thereby either conducting or restricting the flow of current through either the source or drain terminals.

From equations 6.1 and 6.2 [76], the switching voltage or more commonly known as threshold voltage is given by $V_{TH,N}$ for an NMOS transistor or $V_{TH,P}$ for a PMOS transistor.

$$V_{TH,N} = V_{TH,0} + \gamma_N \left[\sqrt{|2\varphi_F + V_{BS}|} - \sqrt{|2\varphi_F|} \right] \quad (6.1)$$

$$V_{TH,P} = |V_{TH,0}| + \gamma_P \left[\sqrt{|2\varphi_F - V_{BD}|} - \sqrt{|2\varphi_F|} \right] \quad (6.2)$$

where $V_{TH,0}$ = Zero Bias Threshold Voltage

γ_N and γ_P = Body Effect Parameters for NMOS and PMOS devices

V_{BS} = Bulk—Source Potential for NMOS

V_{BD} = Drain—Bulk Potential for PMOS

φ_F = Fermi Potential i.e. 2 $\varphi_F \sim 0.75V$

In typically functioning of NMOS and PMOS devices the Bulk potentials for PMOS and NMOS are kept constant with the BULK terminals tied to V_{DD} or GND/V_{SS} respectively. As the potential between the bulk and the source increases beyond 0 V for an NMOS i.e. $V_{BS} > 0$, $V_{TH,N}$ also rises from being $V_{TH,0}$. Consider CMOS (PMOS and NMOS transistors) architecture in Pass Transistor Configuration (PTC), controlled by a Switching Signal, applied at the Gate as shown in Figure 6.4.

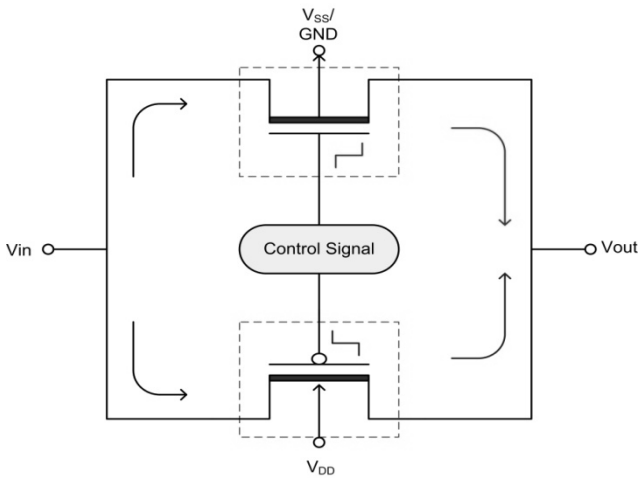


Figure 6.4: Simple CMOS switch in PTC setting

From the figure it can be seen that depending upon the control signal applied, either the NMOS or the PMOS transistors are switched ON and the input passes through the respective transistor, appearing as the output. It is important to note that the efficiency of passage and the amount of signal transmitted depends on the transconductance $g_{DS,N}$

and $g_{DS,P}$ for NMOS and PMOS transistors. Considering Vin as the input voltage that needs to be fed through, equations 6.1 and 6.2 can be modified to represent a more realistic appreciation of the transmission gate functionality, as shown in equations 6.3 and 6.4.

$$g_{DS,N} = \frac{KP_N}{2} * \frac{W}{L} * \left[V_{DD} - Vin - V_{TH,N} - \gamma_N \left(\left[\sqrt{|2\varphi_F + Vin|} - \sqrt{|2\varphi_F|} \right] \right) \right] \quad (6.3)$$

$$g_{DS,P} = \frac{KP_P}{2} * \frac{W}{L} * \left[Vin - |V_{TH,P}| - \gamma_P \left(\left[\sqrt{|2\varphi_F + V_{DD} - Vin|} - \sqrt{|2\varphi_F|} \right] \right) \right] \quad (6.4)$$

To exemplify the above two equations, consider the active transconductance working of the transistors as a function of voltage from GND to V_{DD}. The conductivity of the switching pair in Figure 6.4, depends on the voltage relative to the source and drain terminals and not solely dependent on the gate voltage. This functioning is illustrated in Figure 6.5.

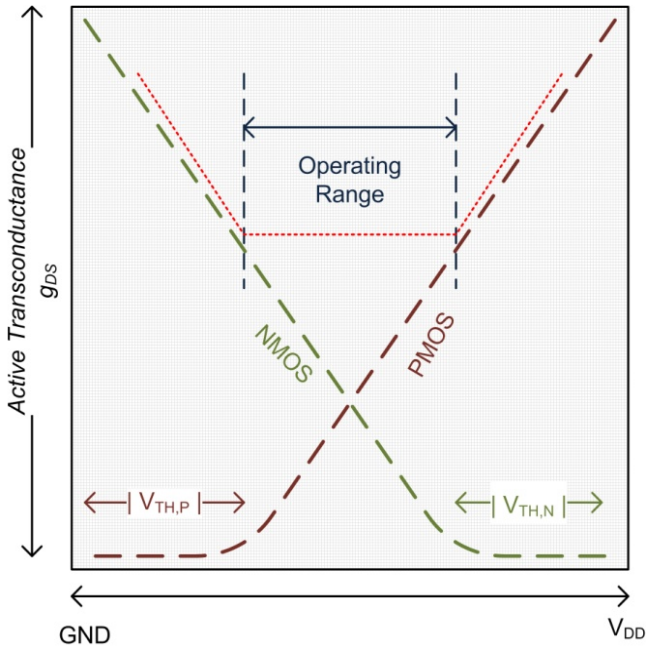


Figure 6.5: Active operating range for the CMOS switch

The active transconductance impacts to a large extent on the quality of the signal passing through the transistors. In order to make certain full scale operation, signals

that exceed V_{DD} are required the gate control or the body potential of the transistors needs to be reduced.

Increasing the control voltage at the gate, leads to a technique known as bootstrapping. The process involves a voltage doubler circuit inserted between the control voltage and the gate terminal as shown in Figure 6.6.

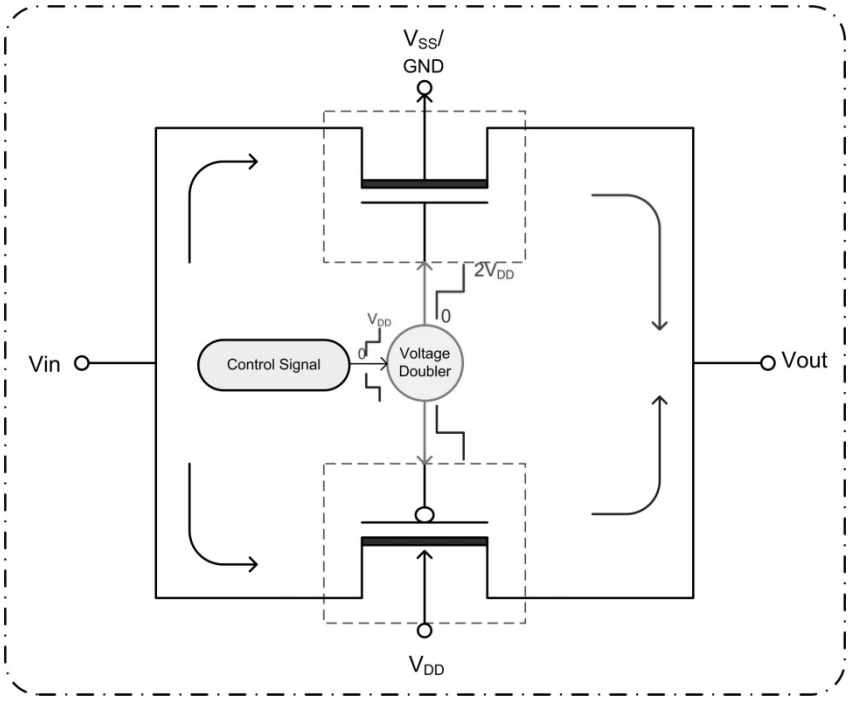


Figure 6.6: Implementation of bootstrap process using a voltage doubler

The voltage doubler is typically a clock doubler circuit that pushes the swing of the control signal to twice the V_{DD} limit. The problem with introducing a dynamic clock into a static circuit is that charge injection and clock feed through becomes a serious problem. The charge injection is useful for operation in high speed circuits, however introduces performance problems for deep submicron transistors. The reduction of the transistor feature size, introduces leakage effects, which reduces the amount of charge between the drain—source terminals, causing the voltage doubler circuit to fail and causing the transconductance of the drain—source node to fluctuate. This effect also impacts on the power consumption of the switch causing it to more than double, due to increased compensation inside the doubler circuit [101].

Another technique to is to perform active biasing of the bulk terminal of the primary switch transistors, to lower the threshold voltage. This technique enables a faster ON time for the two transistors, however introduces second order effects in terms of large sub-threshold leakage. An illustration of this technique is shown in Figure 6.7.

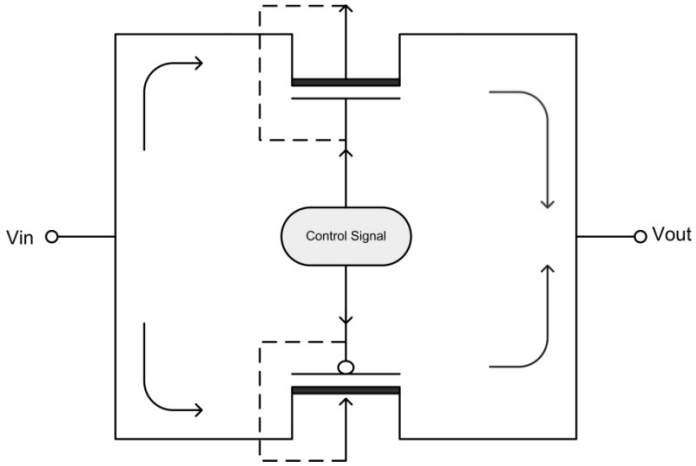


Figure 6.7: Active biased switch circuit

The active biasing technique involves switching the bulk voltage in conjunction with the gate voltage. The switch has the bulk terminal connected directly to the corresponding gate terminal. This process has 2 modes, a typical forward bias transistor and an active reverse bias mode. Considering opposite polarity functioning, as the gate voltage of the NMOS is high, and that of PMOS low, the bulk of the NMOS is pulled high and that of the PMOS is pulled low. This renders the substrate junctions of both transistors of the switch into forward bias mode. As the polarity at the gate voltage reverses, the bulk of the NMOS is pulled low and that of the PMOS is pulled high. This results in the substrate junctions being active reverse bias. Typical leakage current for a 1 V peak to peak sinusoidal input at 1.3 GHz was estimated at 1.67 μA.

Due to the problems associated with transconductance, charge injection effects and large leakage current, a modified design for high speed switch was imperative. The new switch implemented in this work, incorporates features of the aforementioned switch architectures. Figure 6.8 shows the circuit diagram of the modified CMOS switch used to design the 2:1 multiplexer.

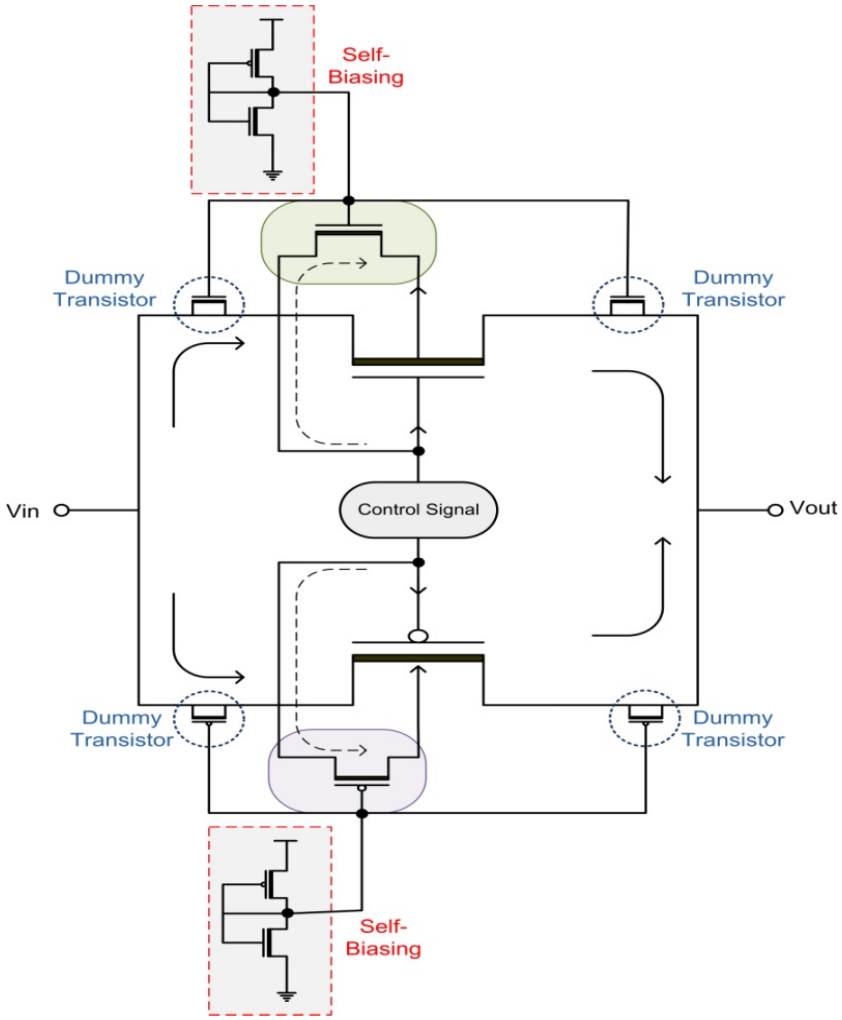


Figure 6.8: Modified dynamic self-biased switch design used to implement 2:1 multiplexer

The switch was designed to work with voltages not exceeding 1 V and was optimised to operate at switching speeds close to 4GHz range, in conjunction with the comparator clocking speeds. The switch makes use of active body biasing technique, however was modified to remain at a specific voltage range between 0.25 V to 0.3 V. Instead of switching based on the transition of the control signal, a stabilizer transistor was incorporated to make sure that the potential at the bulk does not degrade at high frequencies. Two dummy transistors were placed along the input and output lines to control overshoot, sized to provide a very small capacitance of 102 fF. The value of 102 fF was chosen so as to ensure that the overshoot is within a manageable range of ±0.025 V with the increase in the output slew not more than 75 ps. The gate potential for stabilizer transistors were fed from a self-biased voltage generator, thereby reducing the need for external bias input. As the bulk potential is more gradually variable, the

leakage effects due to sudden switching are minimised by many orders of magnitude. The switch was designed for a 0 to 0.75 V gate input transition to the two primary transistors, with additional headroom provided to ensure that a 1 V signal does not drive the two transistors into early saturation. The switch has a maximum ON resistance variation of 0.3 KΩ from 1.56 KΩ to 1.89 KΩ, with a maximum extracted leakage current not exceeding 210 nA for a 2 GHz input signal.

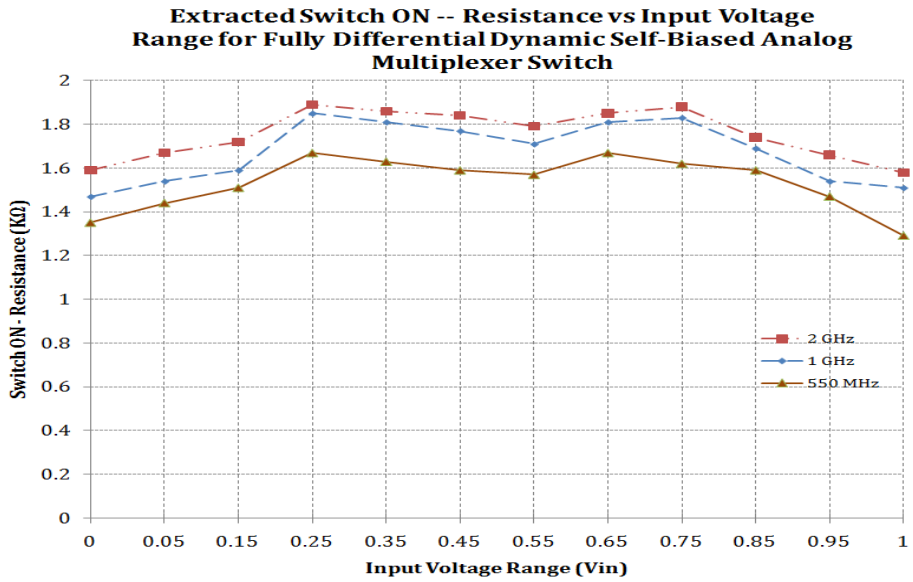


Figure 6.9: Extracted ON resistance for different input frequencies of the novel modified fully differential dynamic self-biased switch

From Figure 6.9, the maximum variation of the switch on resistance for different input frequencies does not exceed more than 0.3 KΩ for any of the 3 cases shown above. This result reinforces the reliability of the switch for high large frequency operation. A comparison of the performance of novel design to the other designs is shown in Table 6.4.

Table 6.4 shows the performance comparison of three different analog switches

Type	Novel Switch	Bootstrap	Active biased
Input Range Sinusoidal Signal	0 – 0.75 V / 1 V	1 V	1 V
Input Frequency	≥ 500 MHz – 2 GHz	≤ 1.3 GHz	≤ 725 MHz
Output Slew	≤ 75 ps	> 2 ns	> 12.5 ns
Output Delay	≈ 165 ps	≈ 1.4 ns	≈ 15 ns
Maximum Leakage Current	210 nA @ 2 GHz	1.67 µA @1.3 GHz	27 µA @ 725 MHz
Supply Voltage	1 V	1 V	1 V
Output noise	9.7 µV/√Hz	1.1 µV/√Hz	54 µV/√Hz
Technology	ST-MICRO® 90nm 7 Metal Layer CMOS		

The design of the switch being finalised, modifying it to operate as a 2:1 multiplexer was relatively simple. As the outputs of the comparators are fully differential, the designed multiplexers were also fully differential, with each 2:1 multiplexer consisting of a differential input and output mechanism as shown in Figure 6.10.

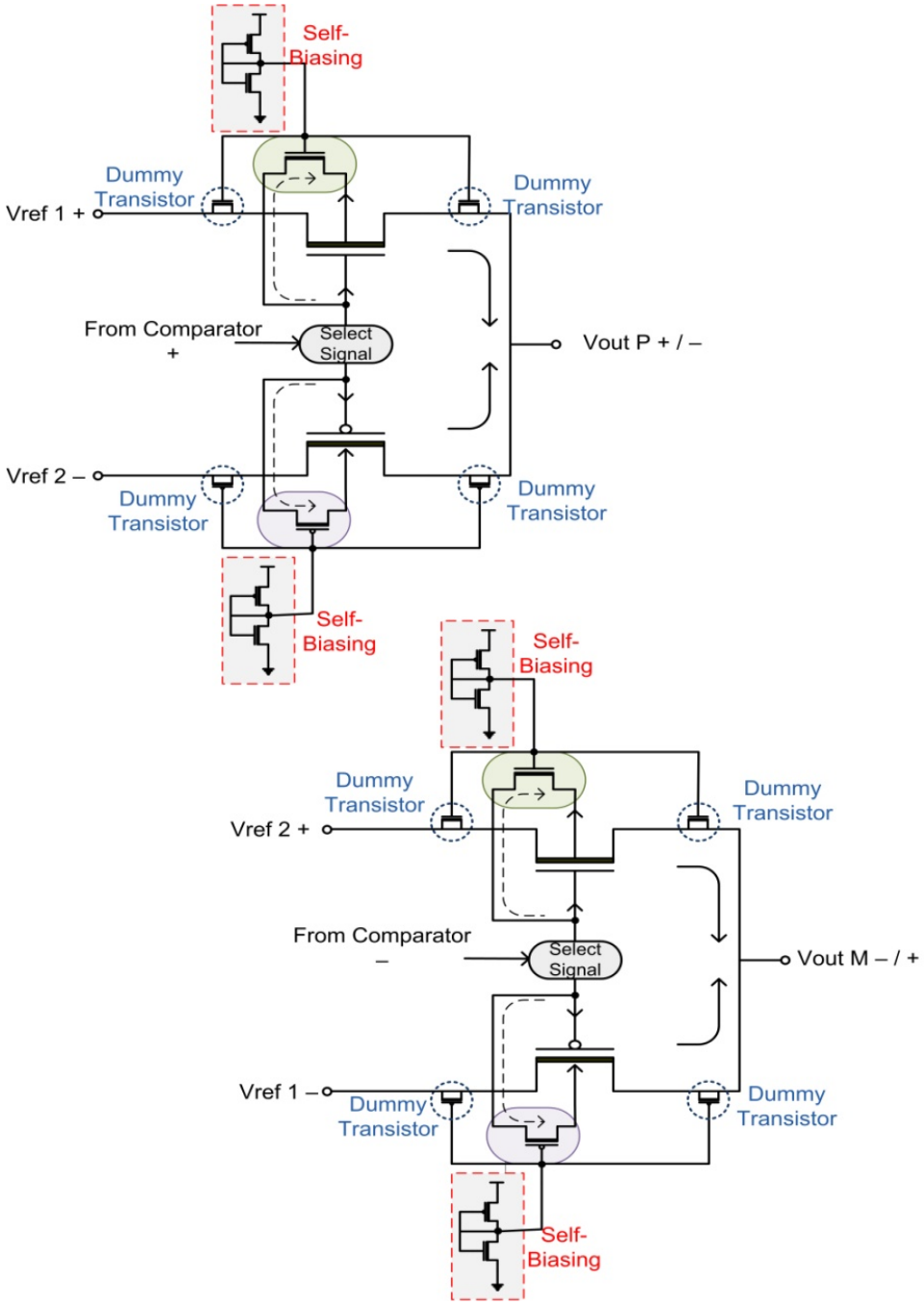


Figure 6.10: Fully differential dynamic self-biased 2:1 analog multiplexer implemented for the reconfigurable converter

6.4.2 Comparator Enable Circuitry

In order to perform the reconfiguration, an enable circuit was required along with each of the comparators and multiplexers to implement an ON – OFF functionality depending upon an input from a control signal. The enable circuit was designed based on the switch implemented in Figure 6.7. The design in Figure 6.7 was modified to function as a supply switch for the comparators. The design of the enable circuit is shown in Figure 6.11 (a) and the comparator implementation in Figure 6.11 (b).

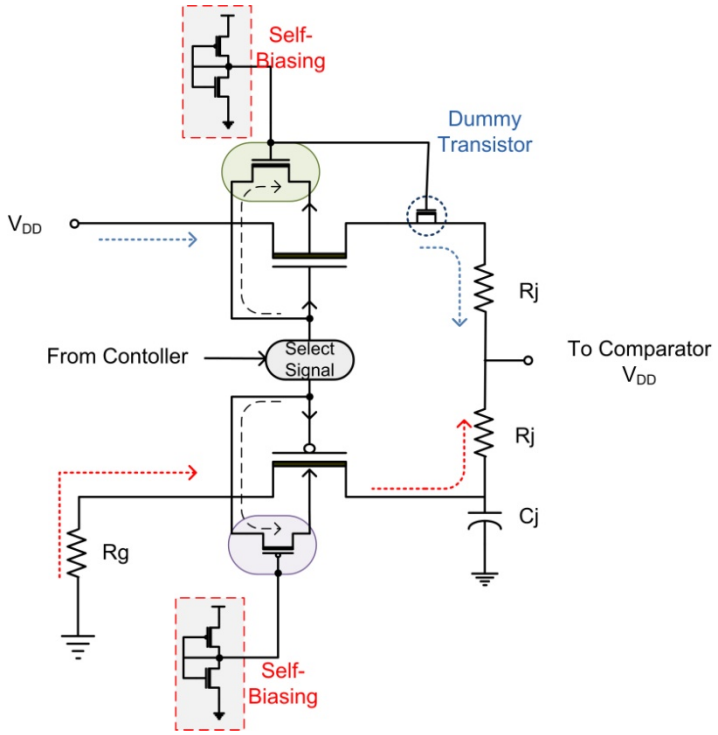


Figure 6.11 (a): Enable circuit for reconfigurability

The circuit was designed using High-V_T (HVT) transistors instead of Standard V_T transistors to ensure the lowest possible leakage. The dynamic biasing of the bulk was performed to raise the bulk voltage close to 0.6 V. The input to the top NMOS is the DC supply voltage, while the bottom PMOS is connected to a ground node. The Rj resistors were used to ensure no feed through or feedback into the supply nodes. The Rg resistor ensuring no ground bounce affects the input line.

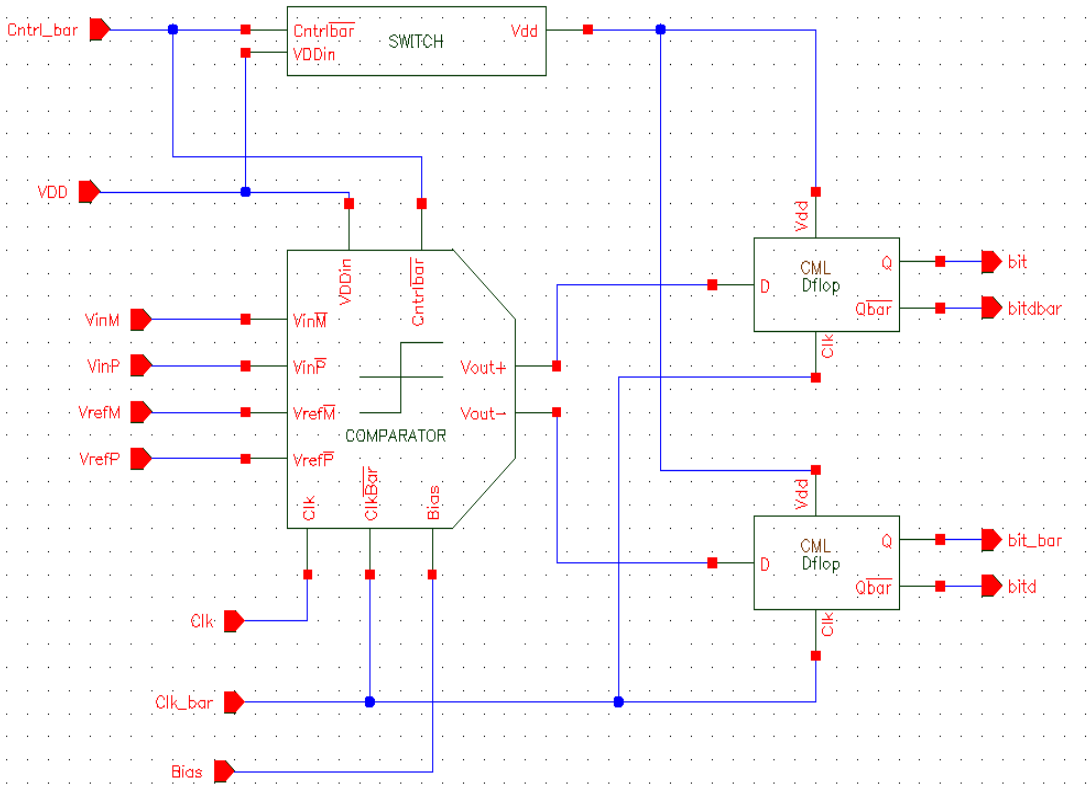


Figure 6.11 (b): Comparator circuit with the enable circuit

The dummy capacitor along the V_{DD} path and the Cj along the ground path were used to help minimise and absorb any fluctuations in the DC signal that might affect the comparator V_{DD} node.

Figure 6.12 shows the comparison of the settling times for SVT and HVT transistors. It is seen that the SVT transistors have a much faster settling time as compared to HVT transistors with the trade-off however being the increased glitch along the output switching node. The reduced glitching of the HVT is advantageous as it has a much lower impact on the V_{DD} for the comparator. The Cj capacitor was used to absorb into the ground node, the reduced glitch from the HVT transistor in low impedance mode. The extra settling time is also useful to ensure that the supply node of the comparator has enough time (during OFF or ON function) to settle and propagate a constant DC signal devoid of any jitter and glitches.

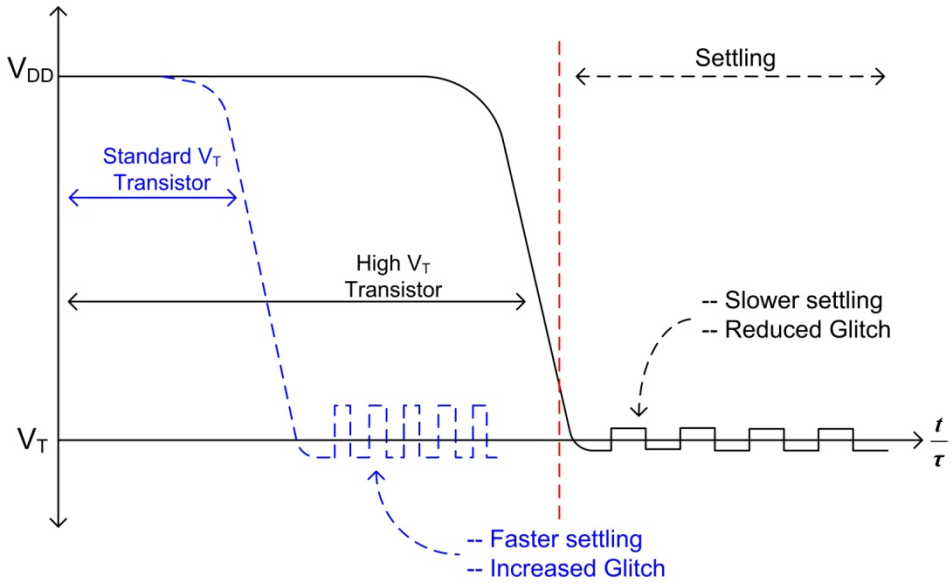


Figure 6.12: Settling time comparison between SVT and HVT transistors

6.4.3 Converter Clocking Scheme

Figure 6.13 shows the reduced duty cycle clocking mechanism used in this design. The converter was designed based on a time shifted skewed clocking mechanism, using a very small duty cycle to trigger each of the comparators.

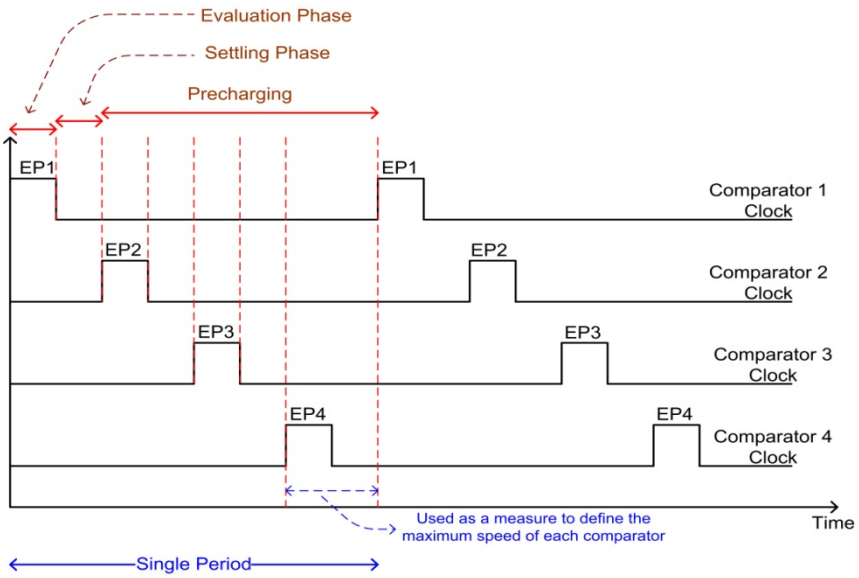


Figure 6.13: Clocking mechanism used in the reconfigurable design

Each comparator was triggered by a clock having 3 phases in a single clock period. The first phase was the Evaluation Phase (EP). The EP is during which the respective comparator triggers and performs the comparison based on track and hold mechanism. The next phase is the settling phase. The settling phase is used to ensure that the comparator output settles within $1/4^{th}$ of the total clock period. The final phase is the pre-charge time, wherein the clock completes the settling and waits for the next cycle, during which subsequent comparators trigger and perform their respective operations. The long pre-charge time is useful as typically PMOS drivers require an added evaluation time. The speed of the comparator and that of the ADC is determined by the combination of the evaluation phase and the settling phase. By use of a cumulative clocking scheme for each of the bits, the total speed of the complete design is measurable to that of the high speed flash converter discussed in Chapter 5. This sort of clocking scheme has the added advantage of completing the evaluation of all the comparators within a single time period thereby removing the need for any timing synchronisation circuit at the output.

6.5 Implementation of Novel Reconfigurable Converter

The novel reconfigurable converter was implemented using SVT and HVT ST-Micro 90nm CMOS transistor technology. The design was implemented for a 1 V supply, fed through a unique switching mechanism. The multiplexers designed were each fed from a differential 1V resistor reference ladder. A combination of the fully differential 2:1 MUX was used to implement the 4:1 MUX and the 8:1 MUX.

The complete design of the novel reconfigurable converter is as shown below in Figure 6.14. The figure shows the different parts of the converter comprising of 4 fully differential comparators, each triggered by a unique reduced duty cycle clock with an enable circuit to either turn OFF or turn ON the comparator.

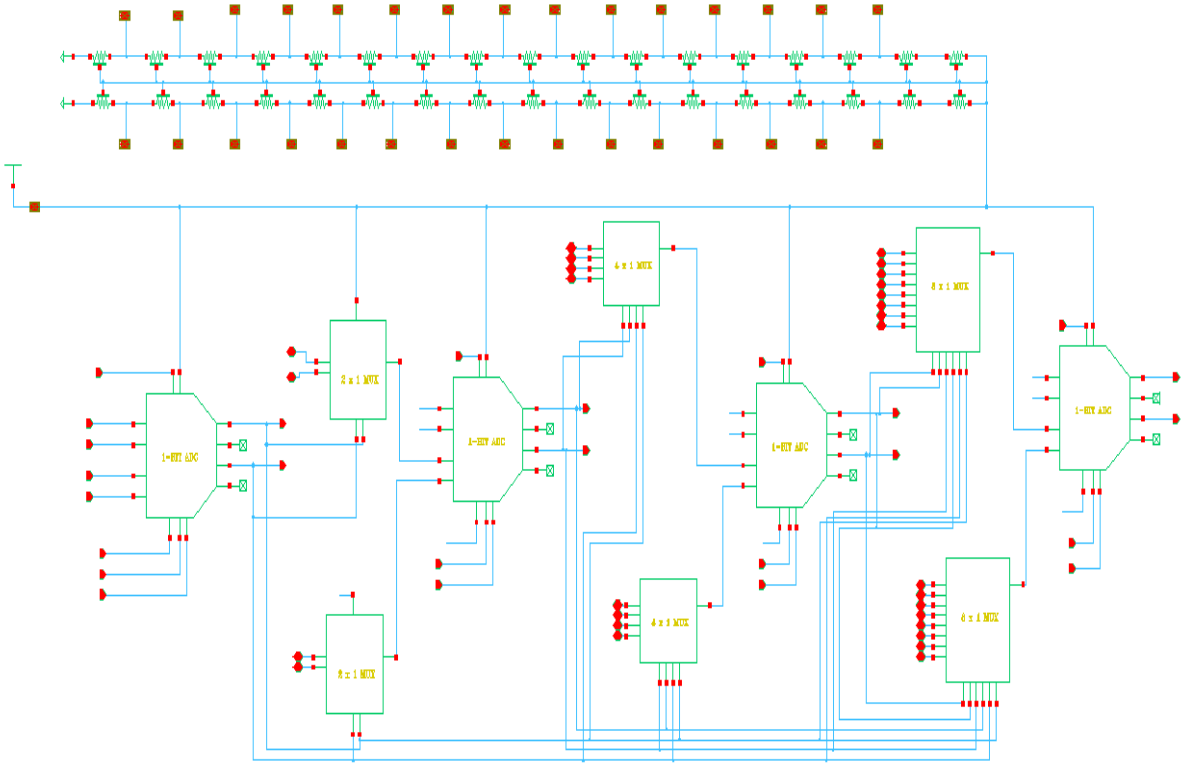


Figure 6.14: Schematic implementation of the novel high speed reconfigurable analog to digital converter for UWB

The floor planning of the converter layout was undertaken similar to that of the flash converter, making sure that parasitic effects do not play havoc on the output of the converter. Careful device matching between the different transistors ensured that the output does not degrade with RC effects and is not impacted by the capacitances inside the pads [95].

Some of the techniques employed in the routing to make the design less susceptible to noise and other mismatch effects are as follows;

- The fully differential comparators and multiplexers were placed symmetrically and have a common centriod arrangement.
- Due to high input frequencies, all the input lines to the comparators, using poly layer routing were placed over an N+ layer to minimise substrate noise effects.

- The resistor reference ladder has 2 dummy resistors on either side to make sure that boundary conditions are matched. Resistors were also interleaved in order to minimise mismatch between them.
- In order to minimise contact delays, each connection between two layers has 4 vias arranged in a grid pattern to minimise second order inductance and capacitances and also minimise first order resistance.
- To minimise eddy current for high speed operation, individual ground planes for the comparators and the multiplexers were laid out in a slotted mesh pattern.
- To ensure reduced start-up rush current, a small 100fF capacitor was placed inside each of the enable circuits between V_{DD} and ground.
- Multiple ground contacts were used to ensure reliability and proper grounding. All poly layer routing was kept to less than 1.5 µm to reduce wire resistance.
- Ground lines were placed on either side of close differential clock lines to minimise antenna effects.

Figures 6.15 and 6.16 show the pad level schematic and complete layout of the high speed novel reconfigurable analog to digital converter, routed using 7 metal layers.

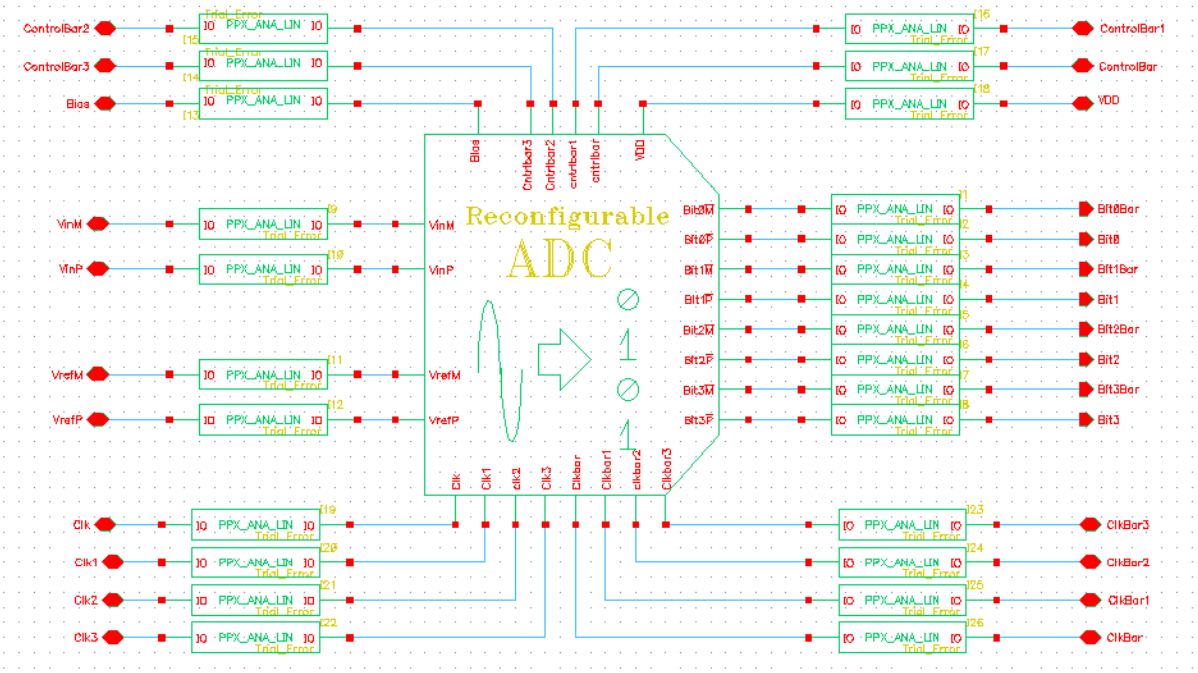


Figure 6.15: Pad level schematic of the fully differential novel reconfigurable ADC

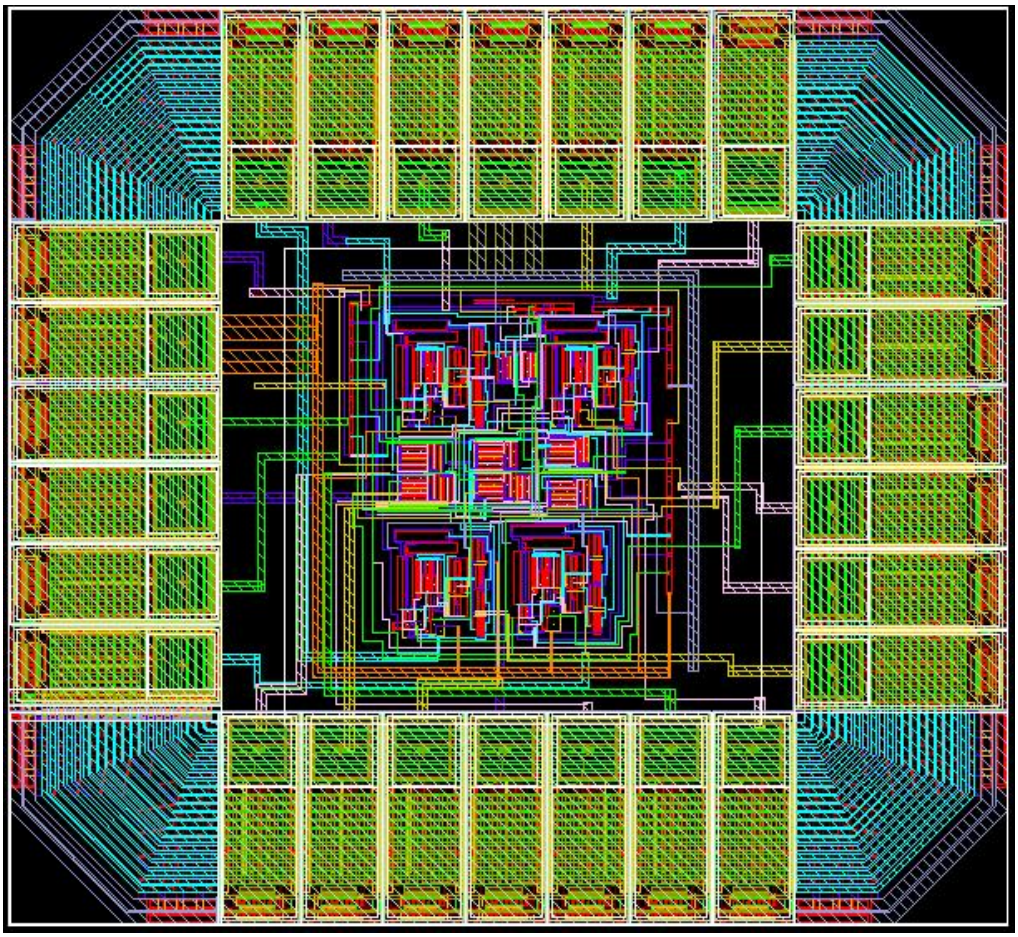


Figure 6.16: Complete chip level layout implementation of the novel reconfigurable analog to digital converter

An in-depth analysis of the post layout working of the novel reconfigurable analog to digital converter was performed in adherence to the requirements for UWB signalling, as set previously in the thesis. A comprehensive discussion of the various performance parameters of power consumption, linearity (INL and DNL), dynamic range, signal to noise ratio, amongst others will be presented in Chapter 8, along with a comparison of the characteristics of the converters presented in Chapter 6 and this chapter.

6.6 Proposed Concept of Controller Based Reconfigurability

The above designed reconfigurable converter is based on a static implementation of the reconfigurable concept. A manual operation of switching ON and OFF the comparators to obtain an output representation from 1 to 4 bits was implemented. One of the

primary reasons governing the need for such a converter was its use in an environment where the signal maybe affected by interference and noise issues. For instance, if there are large effects of Inter Channel Interference (ISI) of transmitters and repeaters from Bluetooth or Wireless LAN communication methods, operating close to the receiver chip, first order and second order effects may impact on the quality of the signal that the converter is able to digitise. In a noisy environment an output with a larger resolution is less susceptible to digital extraction errors as compared to one with lower resolution. However during a more stable environment, the ability of the converter to save power by switching OFF the comparators is unique and advantageous when operating in the GHz frequency range.

An idea of a controller that can reconfigure the converter in real time based upon a certain characteristics of signals and noise present within the primary signal to be digitised is plausible. The controller would essentially trip the comparators ON or OFF depending upon factors like the quality of signal at input of the receiver and ADC, output of the ADC and possibly output of the receiver chain. The intelligence of the controller would be its ability to analyse the different data collected and make a judgement based upon certain pre-defined conditions set forth within its memory banks. Figure 6.17 shows a representation of the controller concept for application within the receiver chain.

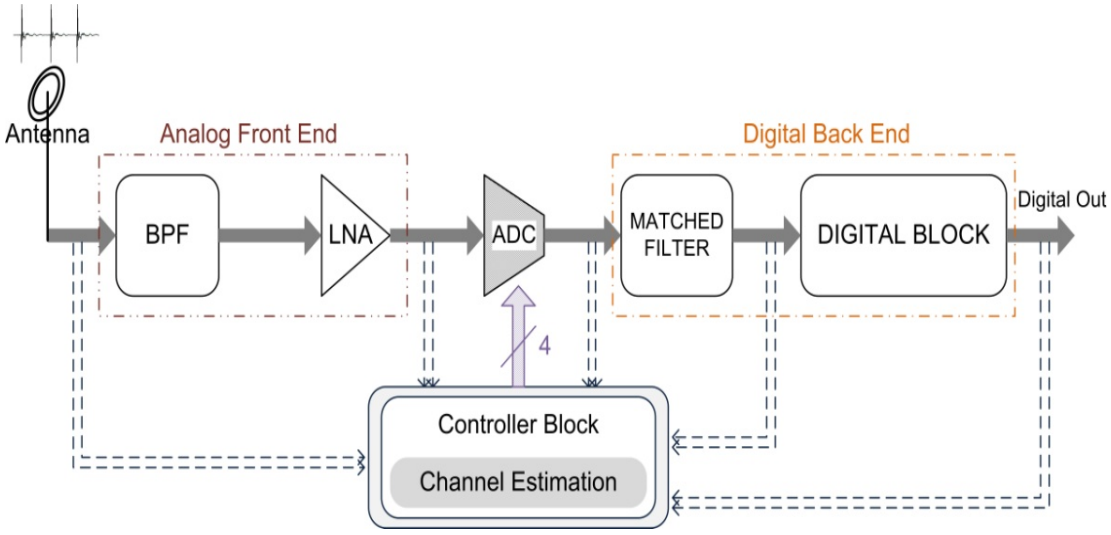


Figure 6.17: Representation of the controller concept within the receiver chain for reconfigurability

To understand the working of the controller block, a brief flow diagram representing the different modes to reconfigure the analog to digital converter is shown in figure 6.18.

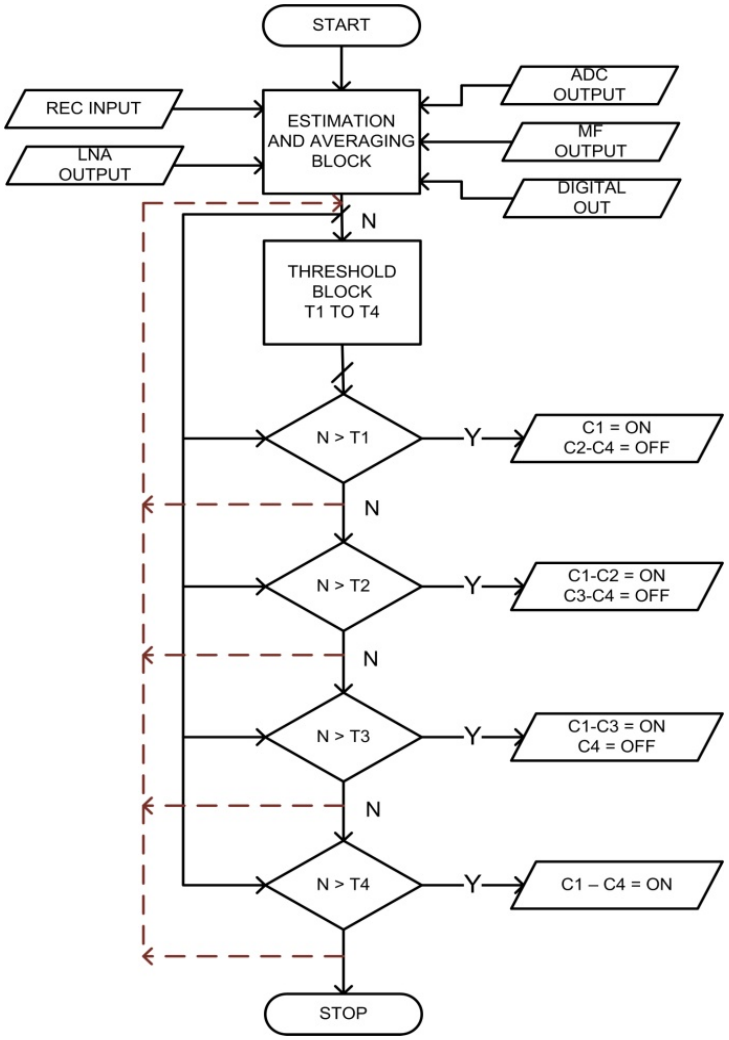


Figure 6.18: Flow diagram of the different operating modes of the controller

The flow diagram from Figure 6.18 shows the conceptual operation of the dynamic controller. The controller comprises of an intelligent signal Estimation and Averaging Block, which sets four different levels of operation within the Threshold Block from T1 to T4. The Estimation and Averaging block analyses each signal based upon a quality factor stored inside a memory array within the block. Depending upon the quality of the signal and an averaging throughout the receiver chain, a comparison to the threshold levels from T1 to T4 is performed. Considering N as the output of the Estimation and

Averaging Block, N is then compared with T1 to T4. Depending upon each comparison, a control signal is sent to each of the comparators to either switch them ON or OFF.

Due to the simultaneous functioning based on analog and digital inputs, the controller concept was implemented using a Verilog-AMS (VAMS) modelling language to test functionality. An implementation using Cadence Virtuoso Suite was performed and the controller tested along with the reconfigurable converter. The VAMS modelling was based on 4 threshold values ranging from 0.25 to 1 for the comparison process. The performance of the controller and an estimated impact on the power dissipation of the complete reconfigurable design has been presented in Chapter 7. The controller presented in this work is meant as a proof of concept design to verify a dynamic reconfiguration model.

6.7 Conclusion

This chapter describes the design and implementation of a novel high speed fully differential reconfigurable analog to digital converter for a DS-UWB communications scheme. An introduction into the concept of reconfigurability was presented along with a brief discussion of the three main reconfigurable converters present.

The chapter gives a detailed overview of high speed analog switch architectures and presents a novel design, implemented for this work and as the basis of a high speed fully differential dynamic 2:1 multiplexer. The novel switch was also modified along with SVT and HVT transistors to function as an enable circuitry for switching ON and OFF respective comparators, in order to implement the reconfiguration function. The chapter also discusses the unique pulse shifted clocking scheme employed to perform the reconfiguration. The clocking methodology was based on four differential clocks, each having three phases of Evaluation, Settling and Pre-charge.

A complete implementation of the design was then presented along with a chip level layout. Some unique layout floor planning techniques for high speed design , to minimise supply noise, mismatch and improve reliability and yield have also been discussed

The chapter finally concludes with a brief discussion of the proposed concept of controller based dynamic reconfigurability. An overview of the working of the

controller has been presented along with a flow diagram detailing some of the steps which would be used to perform the dynamic reconfiguration. To test a proof of concept the controller was implemented using VAMS modelling language to accommodate the simultaneous input of analog and digital signals. A complete implementation of the controller system is beyond the scope of this work, but however will be addressed when taking this research further.

The performance of the reconfigurable design along with the impact of the controller on the power consumed by the design will be discussed in Chapter 7. A comparison of the design performance with that of the flash design presented in Chapter 6, will also be provided in Chapter 7, along with the inherent advantages and disadvantages of the two designs in relation to their suitability for UWB communication.

Chapter VII: **Implementation Results and Analysis**

7.1 Introduction

The design of the custom flash and the novel reconfigurable converters being completed, a comprehensive testing of both ADC's was undertaken to characterise their performance for DS-UWB communication. A complete analysis of the performance of both converters will be presented in this chapter along with a comparison of their performances [102]. The testing for each of the full chip designs was based on a testbench as represented in sections 7.2 and 7.3 using Cadence Virtuoso IC5141USR4 Design Platform. The results of the ADC were then exported into a data file which was read using a MATLAB® code for further analysis.

This chapter is divided into three parts. Section 7.2 will discuss the implementation results of the custom Flash converter designed in Chapter 5. The following Section 7.3 will then discuss the performance of the Reconfigurable converter implemented in Chapter 6 and detail the SFDR, linearity, ENOB and power consumption for different modes. Section 7.4 will then provide a comparison of the two topologies along with the benefits and drawback of each of the designs. The Spurious Free Dynamic Range, Effective Number of Bits (see figures 5.4 and 5.5) and power consumption were the three primary factors used for analysis and comparison in this work.

7.2 Implementation Results of Custom Flash Converter

Figure 7.1 shows the testbench for the custom Flash Converter used to perform the analysis. The output of the converter was exported into a data file and then read into MATLAB. The results highlighted in this section are an analysis of the design based on extrapolated MATLAB data transferred from Cadence Virtuoso platform.

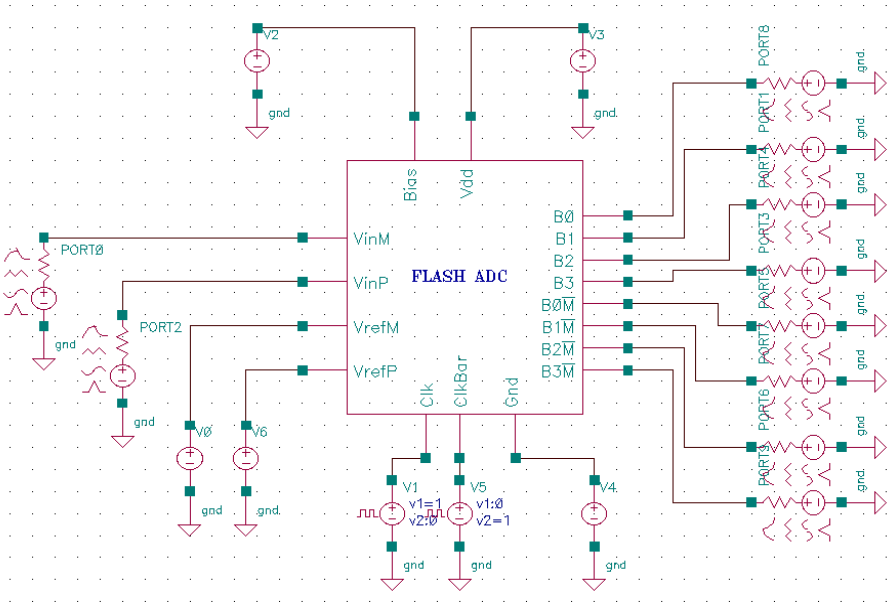


Figure 7.1: Testbench for the Flash ADC

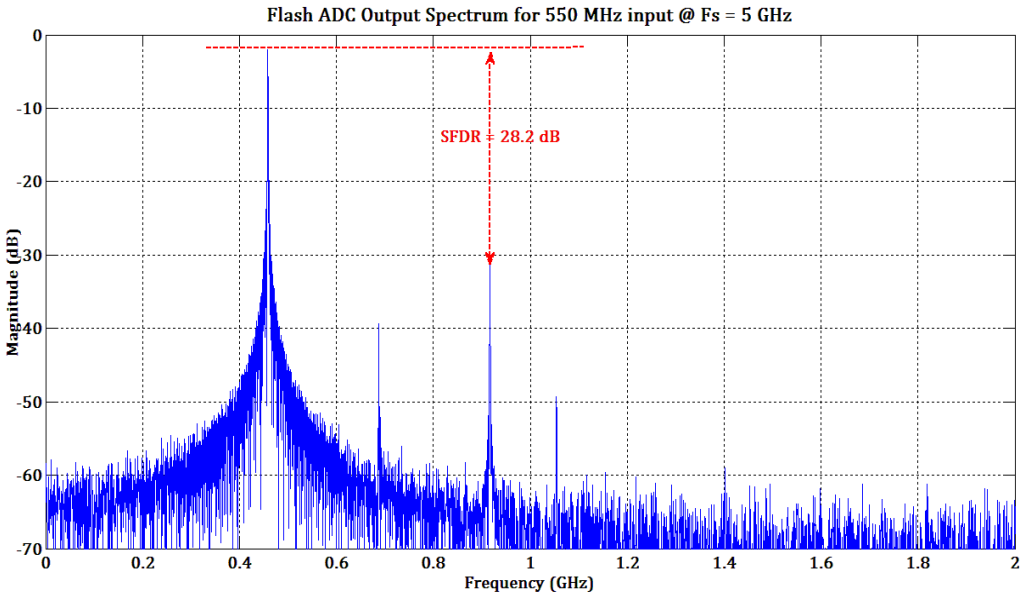


Figure 7.2: Flash ADC Output FFT Spectrum for 550 MHz input sampled at 5 GHz

Figures 7.2 and 7.3 show the output FFT spectrum for the Flash ADC designed in Chapter 5. Figure 7.2 represents the spectrum for a 550 MHz, 0.9 V p-p sinusoidal input signal, sampled at 5 GHz. From the figure it can be discerned that the maximum SFDR of the system is 28.2 dB. The SFDR was based upon the largest spur present at the output.

Figure 7.3 also shows the FFT output spectrum for a 0.9 V p-p sinusoidal input signal, however with a fundamental input at 2.1 GHz, sampled at 5 GHz. The SFDR for this iteration is 27 dB based upon the highest spur.

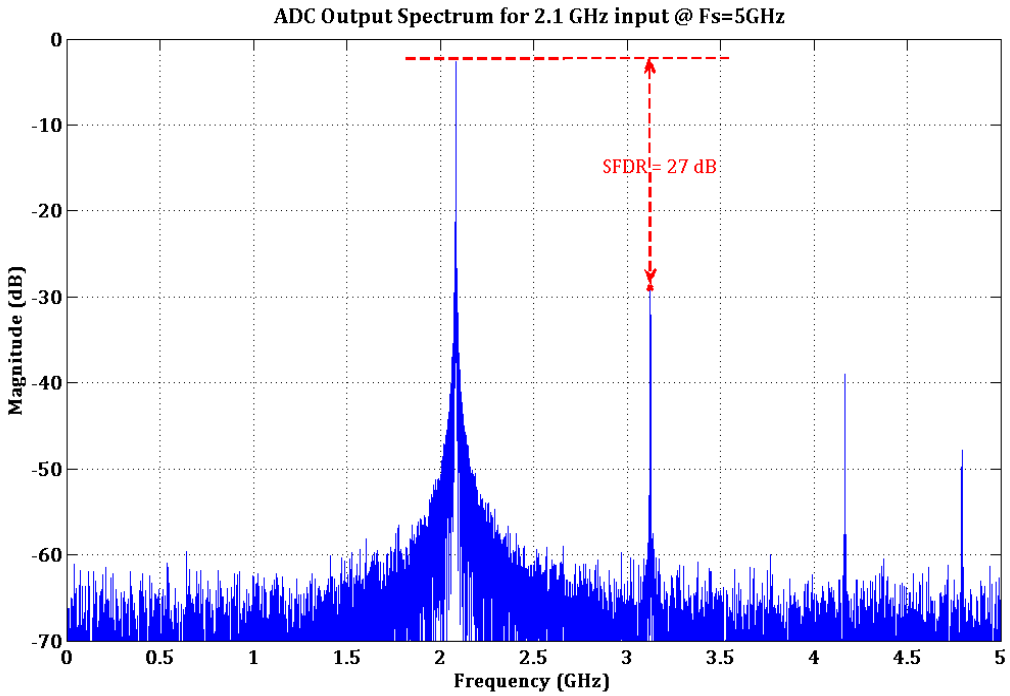


Figure 7.3: Flash ADC Output FFT Spectrum for 2.1 GHz input sampled at 5 GHz

Figures 7.2 and 7.3 were based on 5000 samples averaged from 25 runs. A comparison of the different dynamic ranges for input frequencies varying from 550 MHz to 3 GHz is shown in figure 7.4. The comparison is based upon a data set from sampling at 5 GHz, 4 GHz and 2.5 GHz. Figure 7.4 shows that there is degradation in the SFDR as the input frequency increases and approaches the sampling frequency. At 5 GHz sampling, the converter is approaching its operational limit and this is represented as fluctuations upon the dynamic range as can be seen from Figure 7.4.

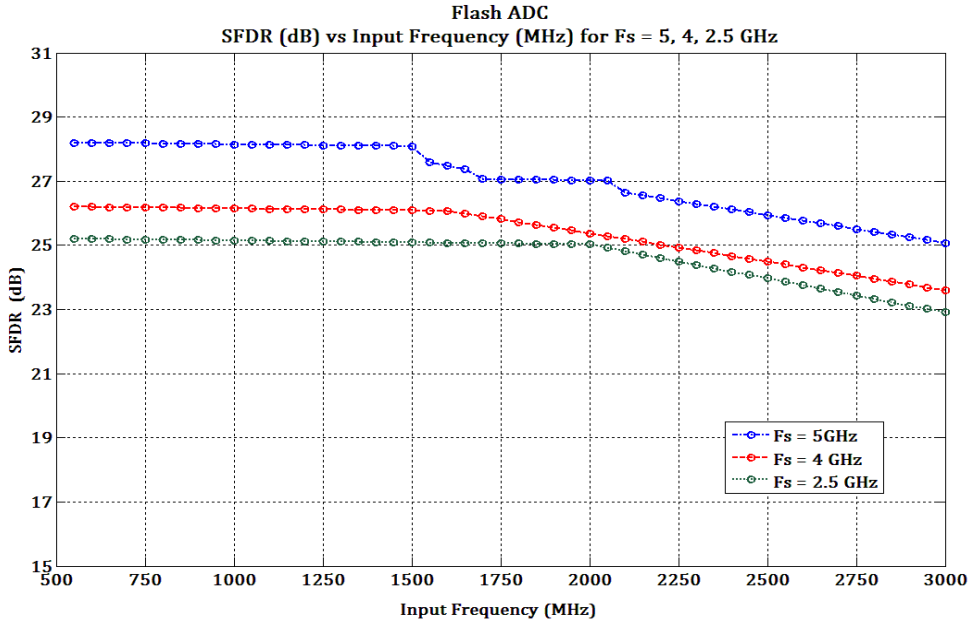


Figure 7.4: Comparison of the SFDR vs the Input Frequency range fro 3 different sampling rates

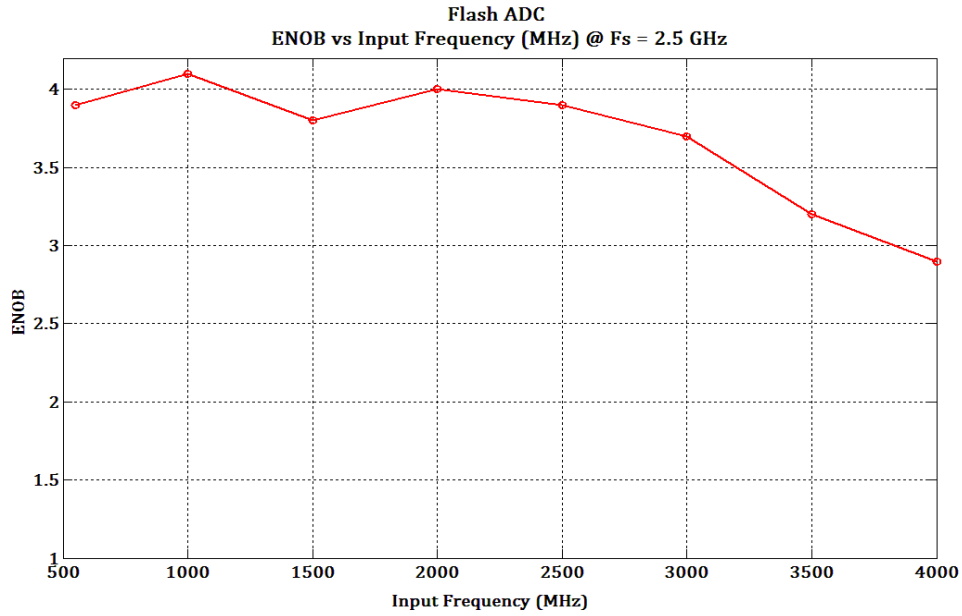


Figure 7.5: Change in the output ENOB for different input frequencies sampled at 2.5 GHz

Figures 7.5 and 7.6 show the variation in the output ENOB for different input and sampling frequencies. From figure 7.5, the ENOB stays steady for inputs up to 2.5 GHz, degrading gradually by 0.5 bit for inputs up to 3 GHz. It can be seen that for inputs beyond 3 GHz the ADC starts to breakdown in resolution with the degradation in the ENOB rising more that 1 significant bit as the input frequency approached 4 GHz and beyond. A similar analysis of the ENOB performance for different sampling frequencies

shows that the ADC experiences severe degradation in terms of ENOB at sampling rates beyond 5 GHz.

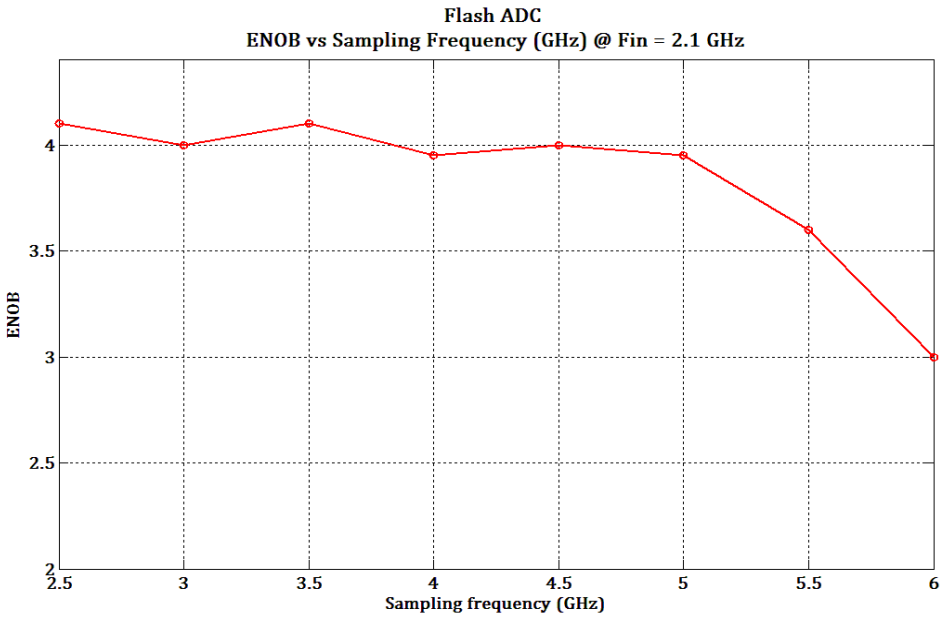


Figure 7.6: Change in output ENOB for different sampling frequencies for a 2.1 GHz sinusoidal input signal

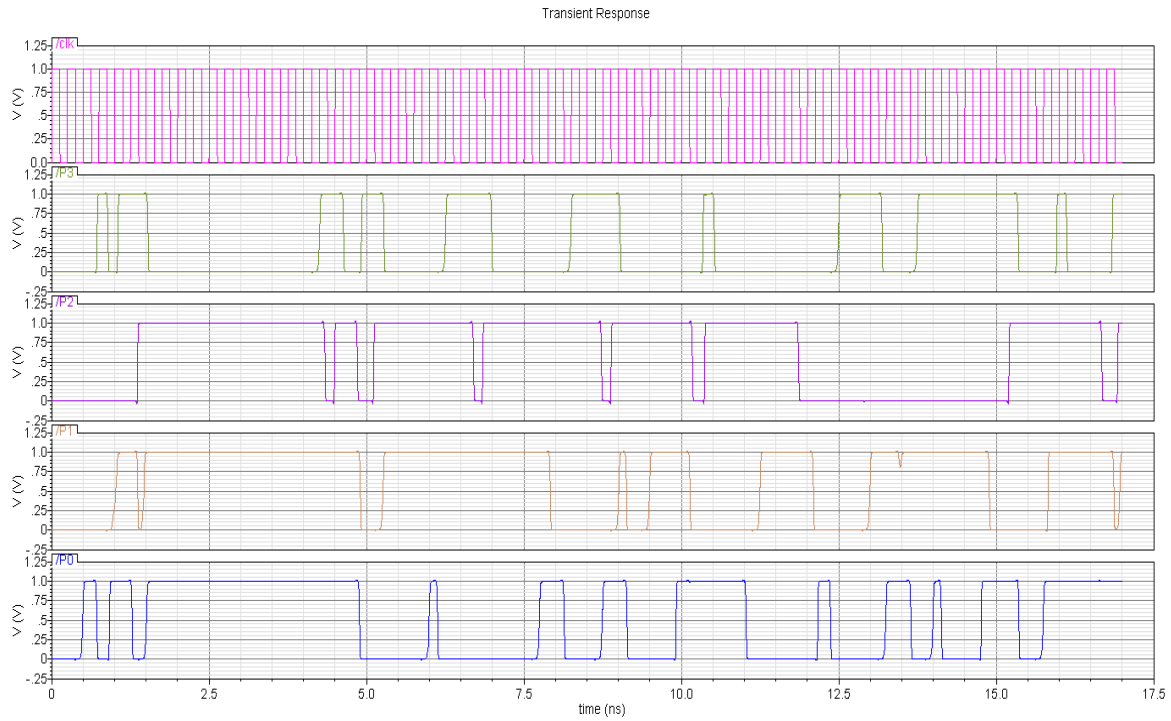


Figure 7.7 (a): Positive node output of the 4 bit flash converter designed in this work

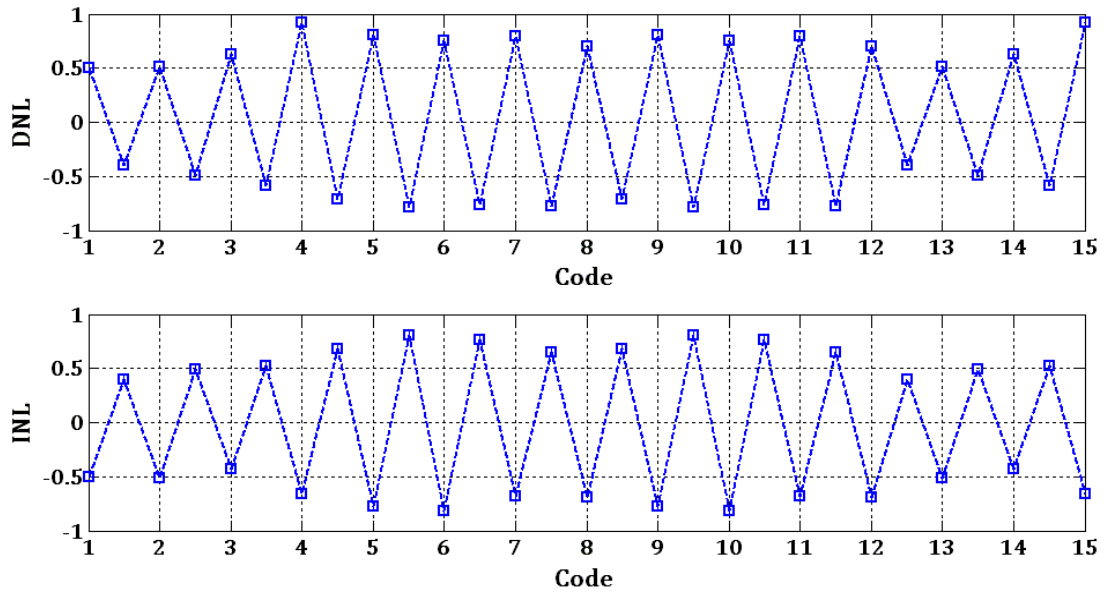


Figure 7.7 (b): Linearity Performance for Custom Flash Converter

Figure 7.7 (a) shows the output of the implemented Flash ADC, while figure 7.7 (b) shows the linearity performance. Figure 7.8 represents the total power consumed by the Flash converter for different input and sampling frequencies. A summary of the complete performance of the Flash design is presented in Table 7.1.

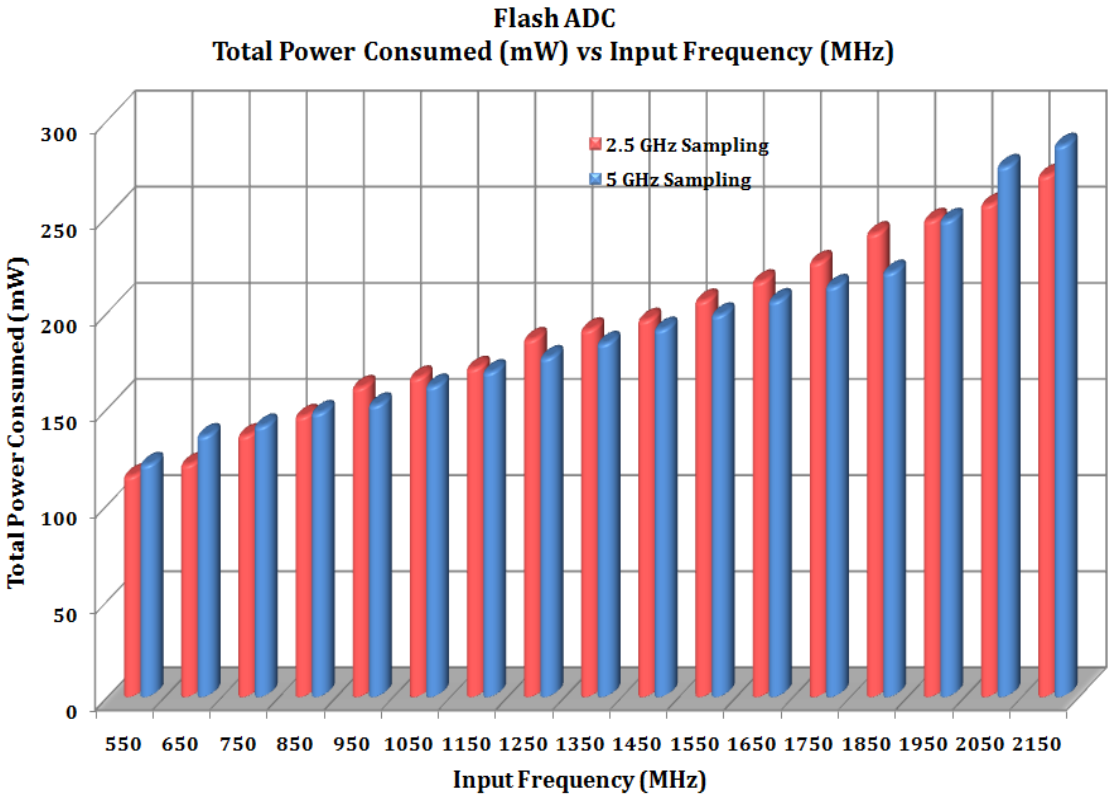


Figure 7.8: Power consumption of the Flash converter

Table 7.1: Performance characteristics of the Flash converter

Parameter	**Flash Converter**	
Input Signal Range	1 V p-p	1 V p-p
Input Frequency	550 MHz	2.1 GHz
Resolution	4 bits	4 bits
Supply Voltage	1 V	1 V
Sampling Rate	2.5 Gsps	5 Gsps
Maximum Sampling Rate	6 Gsps	6 Gsps
Maximum INL	-0.82 / +0.84	-0.62 / +0.54
Maximum DNL	-0.92 / +0.76	-0.52 / +0.65
SNR	27.94 dB	27.76 dB
SFDR	28.2 dB	27.46 dB
ENOB	3.95	3.87
Maximum Power Consumption	114 mW	286 mW
Die Area	0.945 µm * 0. 995 µm	
Structure	Fully Differential Parallel	
Technology Node	ST-Micro® CMOS 90nm 7-Metal Layer Transistor Technology	

To summarise from Table 7.1 the maximum effective sampling rate of the Flash converter stands at 5 Gsps for failure free performance. The converter has an effective power consumption of 114 mW for a 550 MHz input sampled at 2.5 GHz, which rises to 286 mW for a 2.1 GHz input sampled at 5 GHz. The SNR of the converter varies from 27.94 dB at 550 MHz to 27.76 dB at 2.1 GHz. The designed converter is a fully differential complementary parallel architecture implemented using ST-Microelectronics® 7-Metal Layer CMOS 90nm technology, with an active die area of 0.89 μm^2.

7.3 Implementation Results of Reconfigurable Converter

Figure 7.9 shows the testbench for the novel fully differential reconfigurable converter along with the dynamic concept controller. The output of the converter was exported into a data file as mentioned previously for analysis within MATLAB.

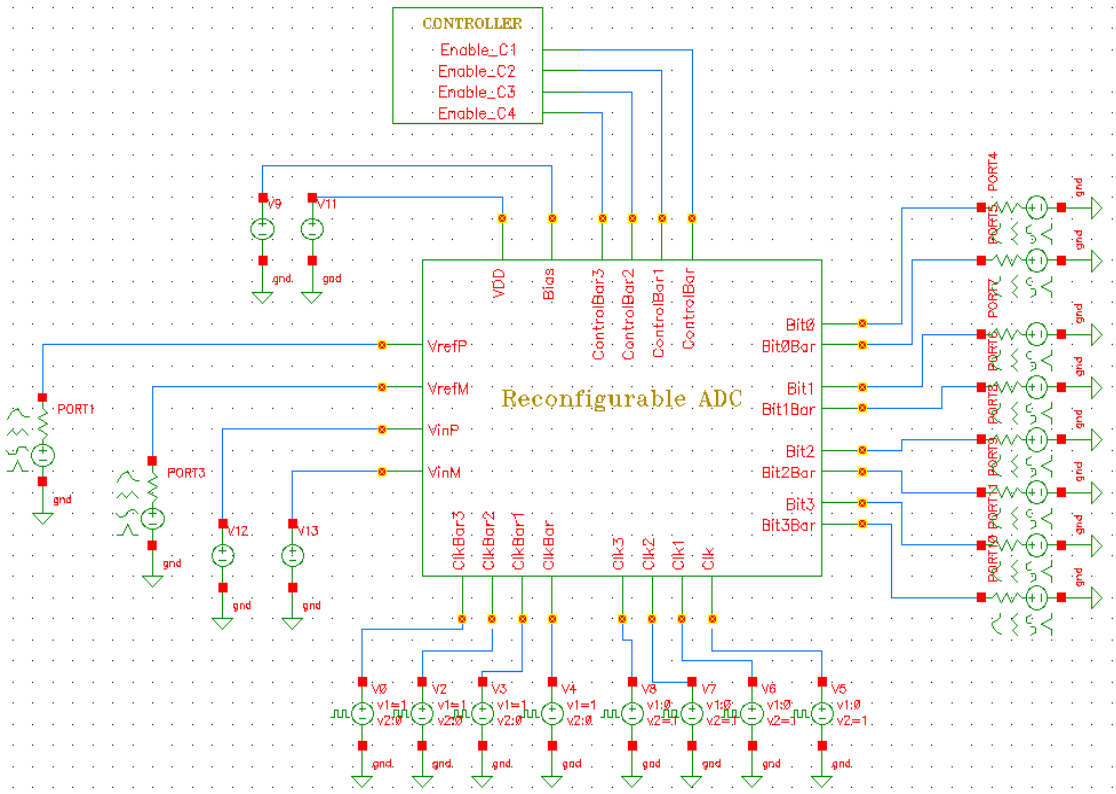


Figure 7.9: Test bench of the implemented differential reconfigurable converter

Figures 7.10 (a) and (b) show the output FFT spectrum for the reconfigurable converter in 4 bit and 3 bit operating modes for a 0.5 V p-p sinusoidal, 2.1 GHz input signal sampled at 5 GHz.

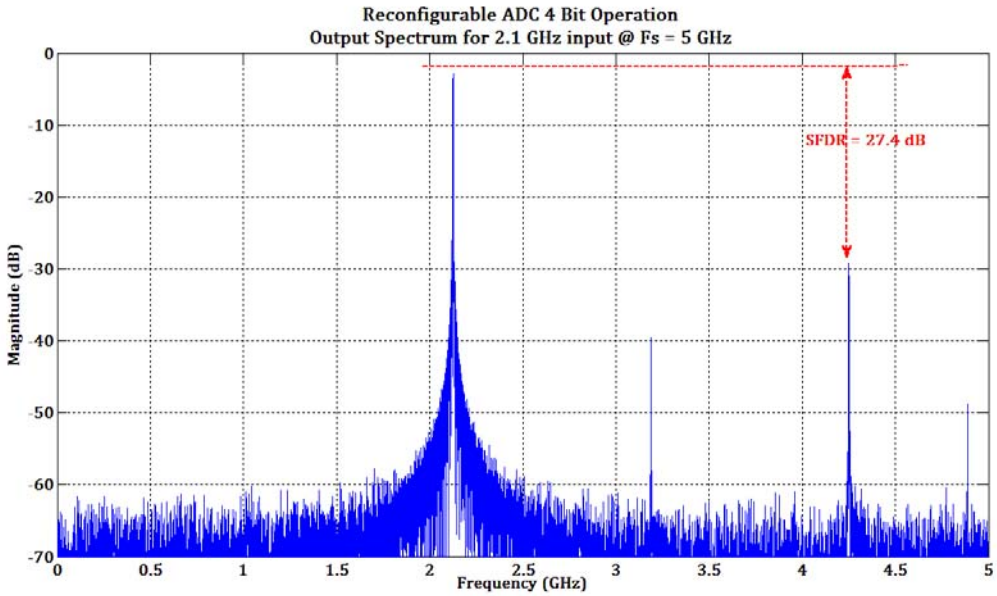


Figure 7.10 (a): FFT output for reconfigurable converter in 4 bit mode

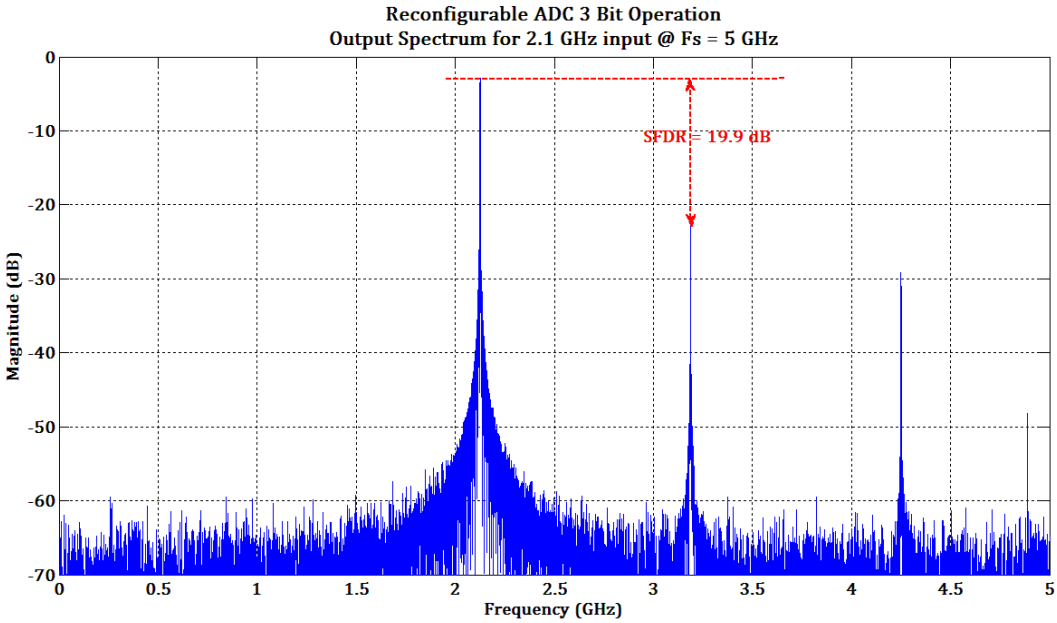


Figure 7.10 (b): Output for the reconfigurable converter for 3 bit operation

The SFDR during 4 bit operation was observed as 27.4 dB based upon the highest spur at the second harmonic, while in 3 bit mode was observed to be 19.9 dB based upon the highest spur at the first harmonic. Figure 7.11 shows the plot of the SFDR variation versus the input frequency sampled at 2.5, 4 and 5 GHz. Figures 7.12 (a) and (b) show the SFDR variation across a range of input frequencies for 2 to 4 bit operation sampled at 2.5 GHz and 5 GHz.

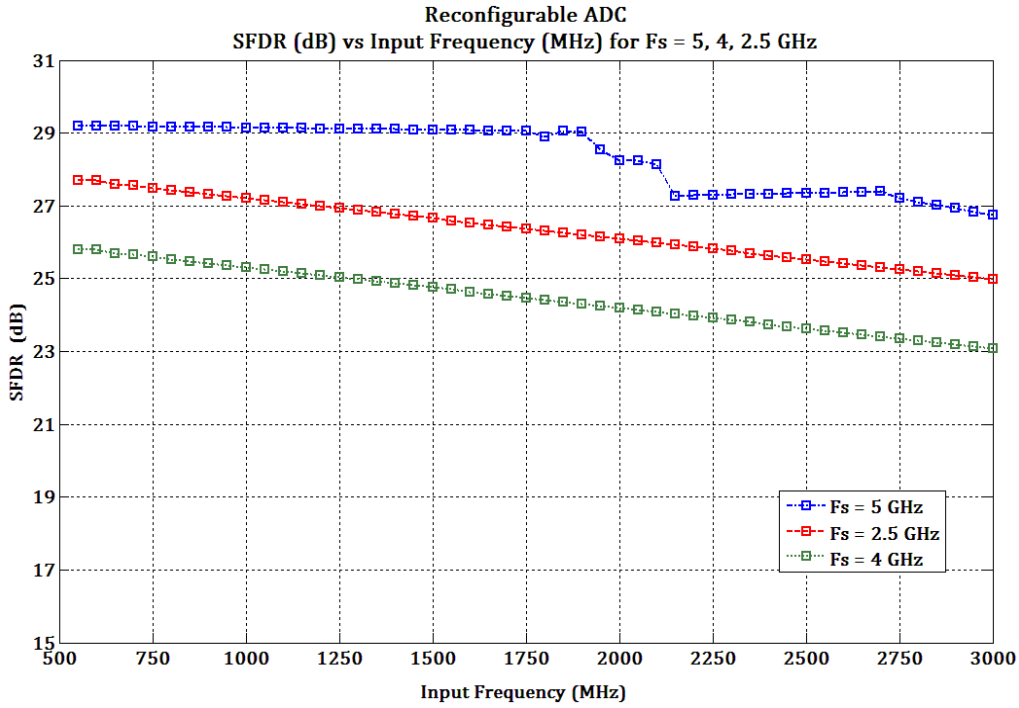
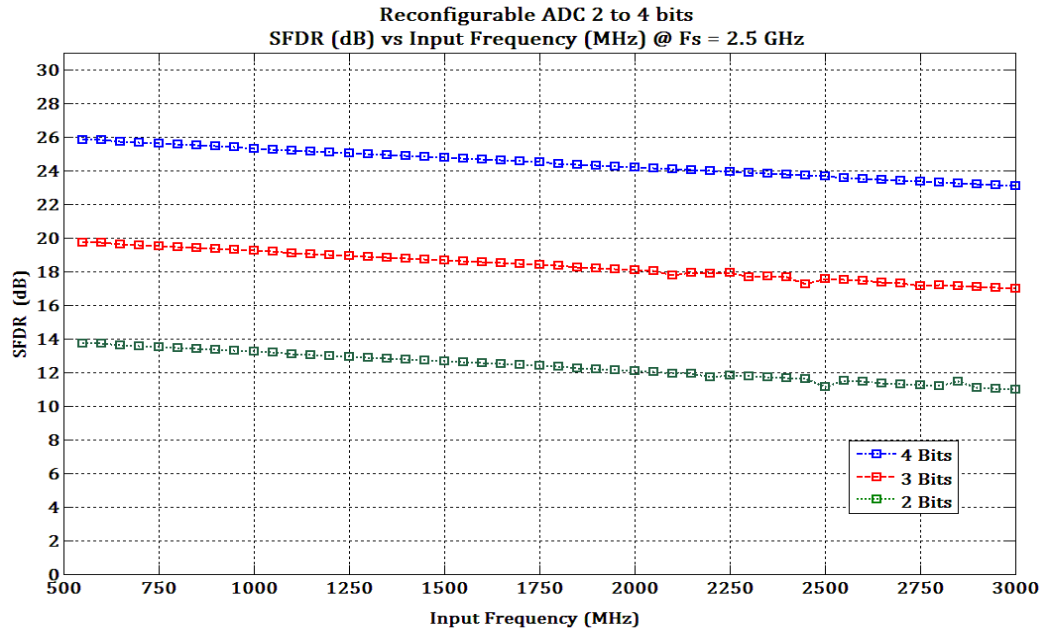
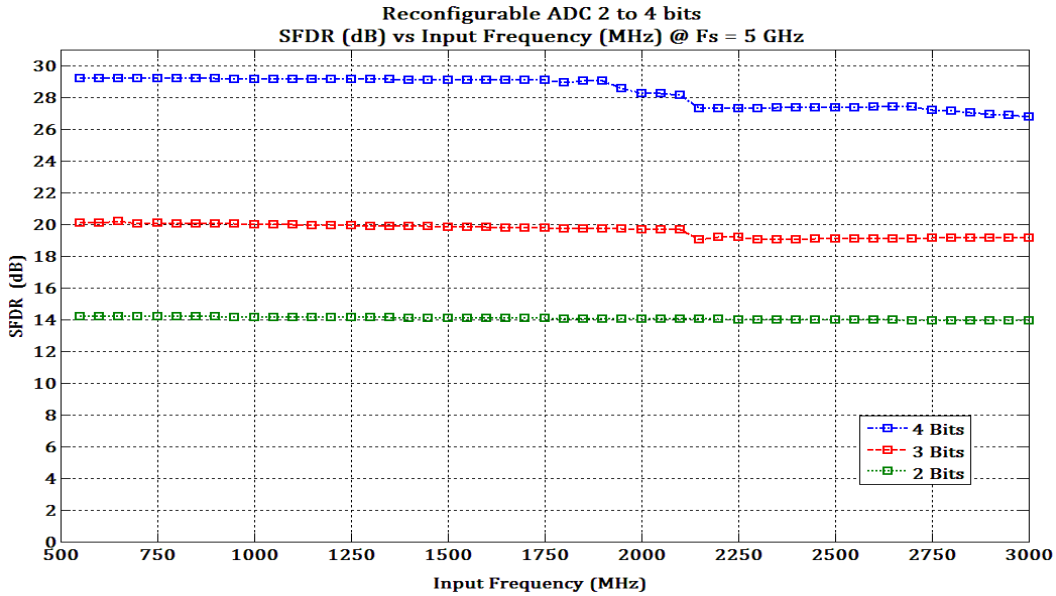


Figure 7.11: SFDR variation versus input frequency sampled at 5, 4 and 2.5 GHz



(a)



Figures 7.12 (a) and (b): Variation in the SFDR for different input frequencies of the reconfigurable converter operating from 2 to 4 bits, sampled at 2.5 and 5 GHz respectively

From Figures 7.11 and 7.12 it can be observed that the degradation in the SFDR is more pronounced at higher input frequencies and specifically when the converter is operating in 4 bit mode. The degradation impinges less on the output dynamic range, becoming more linear and stable for 2 and 3 bit operation. Figure 7.13 shows the variation in the ENOB versus the sampling frequency for a 2.1 GHz input, with the converter operating from 2 to 4 bits.

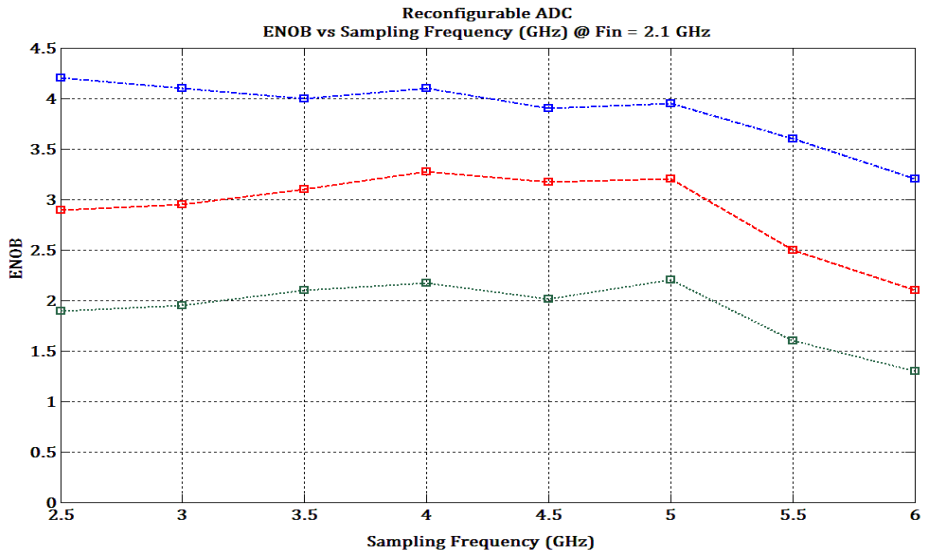


Figure 7.13: Variation in ENOB versus the sampling frequency during 2 to 4 bit operation for 2.1 GHz input signal

Figure 7.13 shows that as the sampling frequency increases beyond 5 GHz, the variation in the ENOB are more pronounced and effectively degrades by greater than 0.5 bit at frequencies close to 5.5 GHz and above. This shows that the maximum failure free sampling limit for the converter stands at 5 GHz during very high frequency operation. Figure 7.14 shows the INL and DNL for the reconfigurable converter for 4 bit operation.

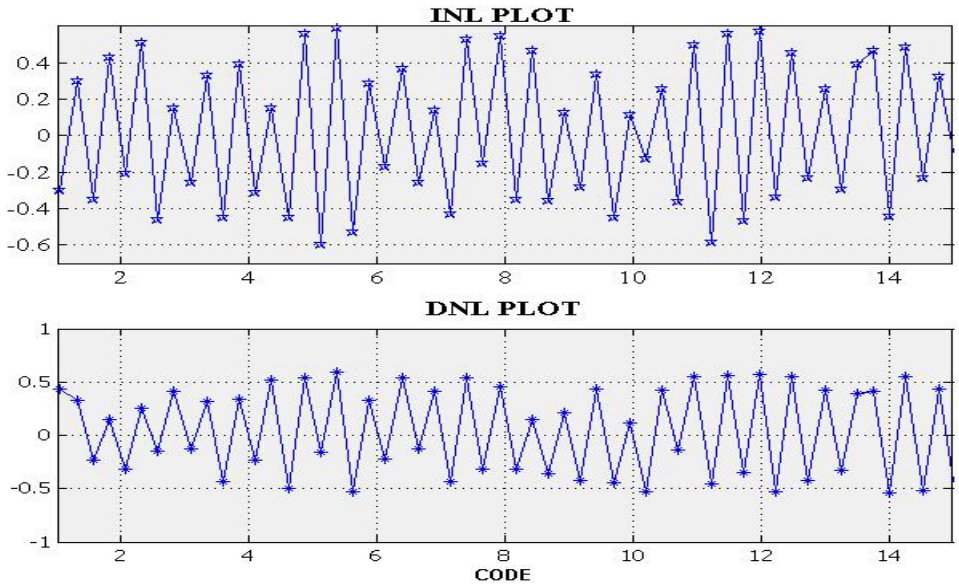


Figure 7.14: Maximum INL and DNL for the reconfigurable converter during 4 bit operation

Figure 7.15 shows the power consumption of the reconfigurable architecture along with the impact of the controller for 2 to 4 bit operation.

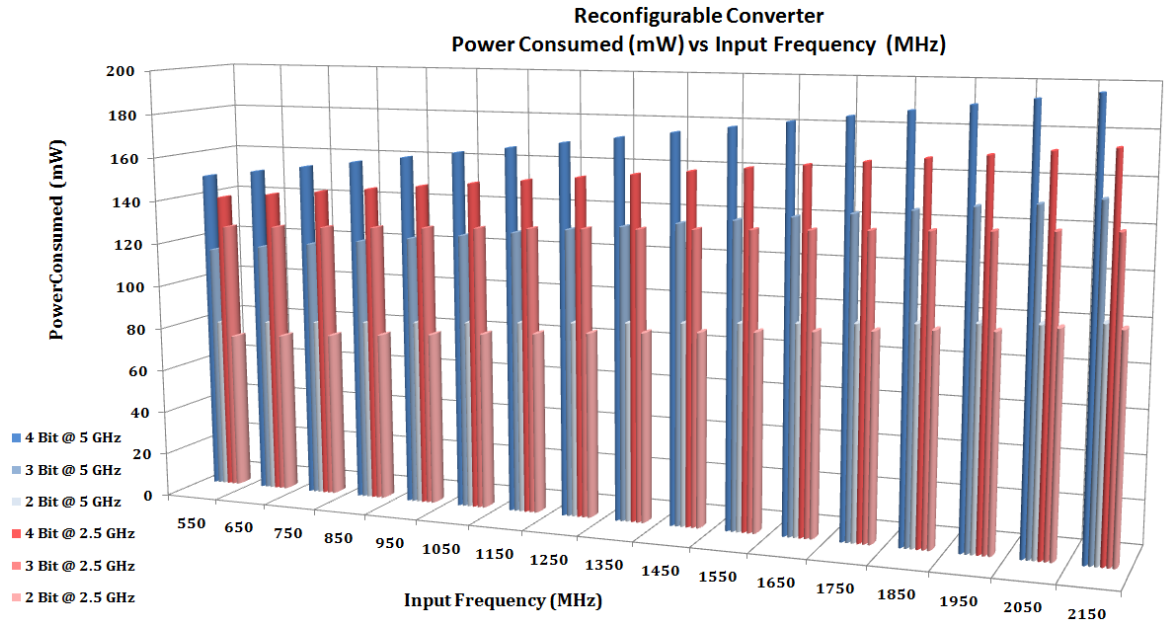


Figure 7.15: Power consumption of the reconfigurable converter along with estimated impact of controller consumption

Table 7.2: Summary of the reconfigurable converter performance for 2, 3 and 4 bit operation

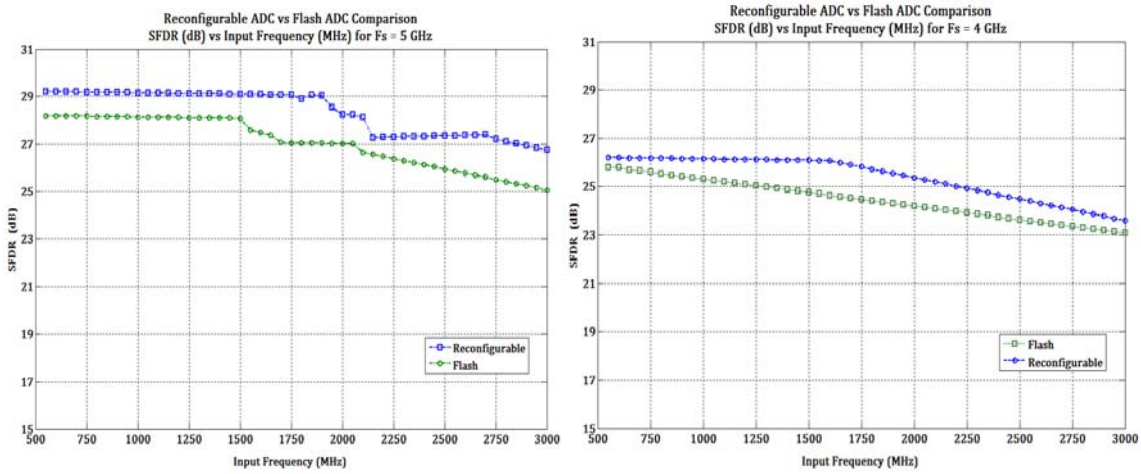
Parameter	Reconfigurable Converter		
	4 bit	**3 bit**	**2 bit**
Input Signal Range	1 V p-p	1 V p-p	1 V p-p
Input Frequency	2.1 GHz	2.1 GHz	2.1 GHz
Resolution	4 bits	3 bits	2 bits
Supply Voltage	1 V	1 V	1 V
Sampling Rate	5 Gsps	5 Gsps	5 Gsps
Maximum Sampling Rate	5 Gsps	5 Gsps	5 Gsps
Maximum INL	-0.61 / +062	-0.47 / +0.34	-0.23 / +0.34
Maximum DNL	-0.52 / +066	-0.42 / +0.45	-0.42 / +0.25
SNR	27.94 dB	19.43 dB	14.05 dB
SFDR	27.4 dB	19.9 dB	14.19 dB
ENOB	3.9	3.17	2.25
Maximum Power Consumption	197 mW	154 mW	103 mW
Die Area	0.577 µm * 0.489 µm		
Structure	Fully Differential Reconfigurable		
Technology Node	ST-Micro® CMOS 90nm 7-Metal Layer Transistor Technology		

Table 7.2 summarises the performance of the reconfigurable converter operating in 2, 3 and 4 bit modes. The dynamic range of the converter varies from 27.4 dB during 4 bit operation to 14.19 dB for 2 bit mode. The maximum SNR varies from 14.05 dB to 27.94 dB, while the ENOB differs from 2.25 to 3.9 bits. Maximum power consumption ranges

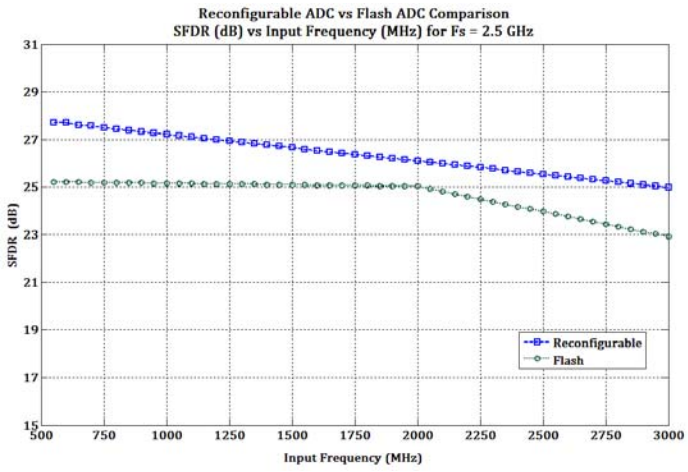
from a high of 197 mW in 4 bit mode to 103 mW in 2 bit mode at 5 GHz sampling rate. The total active die area of the converter chip is 0.282 μm^2. The converter performance was based on a 1 V p-p sinusoidal input based upon a 1 V dynamic supply voltage.

7.4 Performance Comparison of Custom Flash and Novel Reconfigurable Converters

The following section details out the performance comparison of the flash and reconfigurable converts based on three primary factors of SFDR, ENOB and power consumption. The comparison done is to enable the reader to obtain an understanding the benefit and the trade-off of either design.



(a) **(b)**



(c)

Figure 7.15 (a) to (c): Comparison of SFDR versus input frequency for Flash and Reconfigurable Converters at 2.5, 4 and 5 GHz sampling frequencies

Figures 7.15 (a) – (c) paint a picture showing that at 5 GHz sampling both the Flash and the Reconfigurable converters have undergo instability in their dynamic ranges with the reconfigurable converter experiencing 5% added variation with respect to the flash converter. However at 2.5 and 4 GHz sampling the reconfigurable converter exhibits more stable dynamic range degradation as compared to the Flash converter. The flash converter however has a better monotonicity in terms of spurious free dynamic range at 5GHz however the reconfigurable exhibits stable monotonic operation at 2.5 and 4 GHz sampling. Table 7.3 also shows a comparison of the different ENOB for both converters.

Table 7.3: Comparison of ENOB for Flash and Reconfigurable designs

ENOB	Flash Converter 4 bit	Reconfigurable Converter		
		4 bit	3 bit	2 bit
2.1 GHz input @ 5 GHz Sampling	3.87	3.9	3.17	2.25
2.1 GHz input @ 4 GHz Sampling	4.15	3.9	3.35	2.2
2.1 GHz input @ 2.5 GHz Sampling	4.1	4.25	2.9	1.95

The comparison of the ENOB shows that both the flash converters and the reconfigurable designs demonstrate an equitable variation with no variation exceeding 0.25 bits, exhibited by both converters. This result along with the comparison of the SFDR performance above reinforces that the case of the reconfigurable converter operating on par with that of the Flash converter for DS-UWB communications. The result meets the requirements set forth in the earlier chapters of this work. The dynamic range and effective bits comparison pave the way for the comparison of the total power consumed by both designs. The founding requirement set forth at the beginning of this thesis was to implement a reconfigurable design that would reduce the total power consumption of a flash analog to digital converter, but however achieving a similar performance in terms of speed, dynamic range, and output resolution.

The following graph in Figure 7.16 represents this reduction in power and provides a comparison of the power consumed by both the flash and the reconfigurable designs. Table 7.4 shows the total power saving achieved by the implementation of the

reconfigurable converter as compared to a flash converter operating within the same input signal range and sampling frequency.

Table 7.4: Provides a comparison of the total power consumed

Fin = 2.1 GHz, Fs= 5 GHz	Dynamic %	Static %	Total (mW)	Saving %
Flash 4 bit	97 %	~ 3 %	286 mW	**~ 32 %**
Reconfigurable 4bit	94.5 %	~ 5.5 %	197 mW	
Reconfigurable 4 bit with controller	94.5 %	~ 5.5 %	210 mW	**~ 27 %**

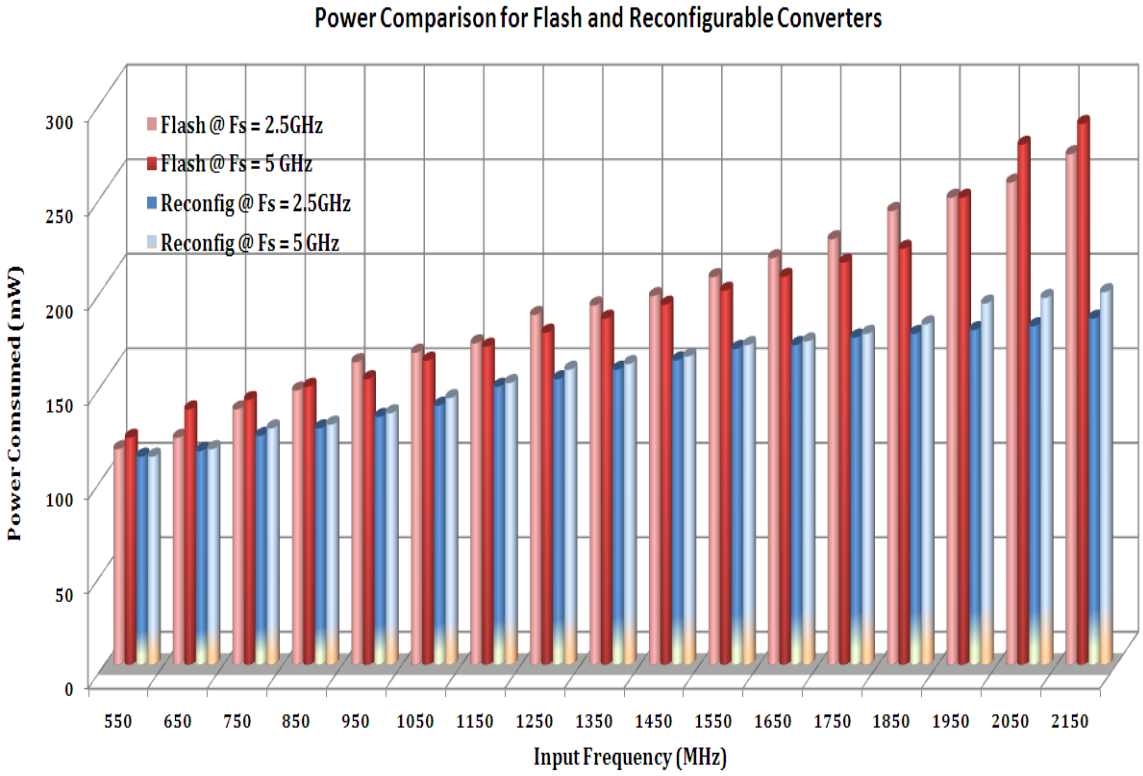


Figure 7.16: Comparison of the power consumed by the flash and reconfigurable converters

From Figure 7.16 and Table 7.3 it can be discerned that the reconfigurable converter operating at the similar maximum specification of 2.1 GHz input and sampling at 5 GHz, achieves a total power saving of 32 %. The incorporation of the concept controller pushes up the power consumption of the reconfigurable design, however still managing to achieve a power saving of 27 %. One drawback of the reconfigurable design is that there is an increase in the total static power consumption of the design, due to the active body biasing of the analog multiplexers. This increase in static power consumption

however is not sufficient enough to play major role within the operating conditions of the reconfigurable converter.

Another saving obtained by the implementation of the reconfigurable converter was the reduction in the overall die area between the two converters. The flash converter occupies a total active die area of 0.89 μm^2 while the reconfigurable converter has a maximum active die area of 0.282 μm^2, an overall reduction of 58 %.

Table 7.5 shows a comparison of different converters associated with this work

Parameter	**Flash**	**Reconfigurable Converter**			**[97]**	**[98]**	**[99]**
	4 bit	**2 - 4 bit**			**10 bit**	**5-7 bit**	**6 bit**
Input Signal Range	1 V p-p	1 V p-p	1 V p-p	1 V p-p	1 V p-p	1 V p-p	1 V p-p
Input Frequency	2.1 GHz	2.1 GHz	2.1 GHz	2.1 GHz	100 KHz	400 MHz	400 MHz
Resolution	4 bits	4 bits	3 bits	2 bits	10 bits	7 bits	6 bits
Supply Voltage	1 V	1 V	1 V	1 V	2.5	1.3 V	1.8 V
Sampling Rate	5 Gsps	5 Gsps	5 Gsps	5 Gsps	15 Msps	550 Msps	528 Msps
Maximum Sampling Rate	6 Gsps	5 Gsps	5 Gsps	5 Gsps	15 Msps	1.1 Gsps	528 Msps
Maximum INL	-0.62 / +0.54	-0.61 / +062	-0.47 / +0.34	-0.23 / +0.34	+/- 1 LSB	+/- 1.5	+/- 1.24
Maximum DNL	-0.52 / +0.65	-0.52 / +066	-0.42 / +0.45	-0.42 / +0.25	+/- 0.4 LSB	+/- 0.36	+/- 0.74
SNR	27.76 dB	27.94 dB	19.43 dB	14.05 dB	40 dB	41.6 dB	30 dB
SFDR	27.46 dB	27.4 dB	19.9 dB	14.19 dB	55.7 dB	41 dB	67 dB
ENOB	3.87	3.9	3.17	2.25	8.9	6.8	5.4
Power	286 mW	197 mW	154 mW	103 mW	13.5 mW/bit	46 mW/bit	63 mW
Die Area	0.945 µm * 0. 995 µm	0.577 µm * 0.489 µm			0.2 mm^2	0.19 mm^2 /bit	N/A
Structure	Fully Differential				Pipeline	Pipeline	Flash
Technology Node	ST-Micro® CMOS 90nm 7-Metal Layer Transistor Technology				0.25 µm BiCMOS7	90 nm CMOS	180 nm CMOS

7.5 Conclusion

This chapter presents implementation, testing and comparison of the results performance of the custom Flash and the reconfigurable designs implemented in this thesis. Section 7.2 of the chapter presents the performance of the Flash converter designed in Chapter 5. Some of the key outcomes observed from the implementation and testing of the design were the operational limit for the Flash Converter at 6 GHz, with a maximum effective SFDR of 27.46 dB. The ENOB for the converter stands at 3.87 bits with a maximum power consumption of 286 mW.

Section 7.3 presented the overall implementation and testing results for the novel reconfigurable converter designed in Chapter 6. The key outcomes from testing of the converter were the successful reconfigurability from 2 to 4 bits for input and sampling considerations on par with that of the Flash converter. The converter exhibited a variation in the SFDR from 27.4 dB for 4 bit operation to 14.9 dB for 2 bit operation. The ENOB for the converter remained stable at the critical input frequency of 2.1 GHz and sampling frequency of 5 GHz. The total power consumed by the converter was 197 mW for complete 4 bit operation and arose to 210 mW with the integration of the controller concept into power calculations.

Section 7.4 presented a comparison of both converters based on three criteria of SFDR, ENOB and power consumption. The comparison concluded that in terms of SFDR and ENOB both converters achieved similar results and met the initial requirements set forth for DS-UWB communication specified at the beginning of this thesis. The crucial observation from the comparison of the two converters was the saving of 32 % in the total power consumed by the reconfigurable converter in full operation mode with respect to the Flash Design. An estimated saving of 27 % was also achieved with the integration of the concept controller. The only trade-off observed from the reconfigurable design was an increase in the static power consumption due to body biasing of the analog multiplexer detailed in Chapter 6. It was observed that the static consumption was only 5.5 % of the total power consumption and not large enough to affect the functioning or yield of the converter. Another outcome of the reconfigurable design was a saving of 58 % in total active die area between the two converters.

Chapter VIII: **Conclusion and Future Scope**

This thesis presented the design and implementation of a novel reconfigurable analog to digital converter for DS-UWB communications. The design was a fully differential architecture comprising of four comparators and 3 multiplexers. The converter presented provides an alternative to the use of flash analog to digital converters for high speed communications. The capability of the novel reconfigurable design to switch OFF and ON comparators was crucial in its ability to reconfigure effectively.

Previous work involving reconfigurable converters for high speed applications were restricted to low operating frequencies, functioning within the MB-OFDM UWB communication scheme. The design presented in this work was an attempt to implement a converter for the lesser targeted DS-UWB scheme, due to its high bandwidth and sampling requirements. The target of this work was to implement a variable bit converter to satisfy the ever increasing technological and operating requirements of DS-UWB communication for application into Bio-Medical, Wireless In-Home connectivity, transport and collision avoidance systems, amongst others. The design presented in this thesis achieved the requirements set forth by these systems in relation to the output resolution, input bandwidth, sampling rate, dynamic range requirements.

The work presented targets the critical needs for addressing power, area, speed, cost, size and linearity for applications using DS-UWB communication medium. The work demonstrates the effectiveness of the novel converter in addressing and meeting these

critical needs. The designed converter is a realistic approach targeted at low power high speed Ultra Wideband communications specifically directed towards Direct Sequence UWB communication.

Section 8.1 presents some of the key research outcomes from this work, while section 8.2 concludes this thesis by looking into the future direction and scope of work presented for the research conducted in this thesis.

8.1 Key Research Contributions

This thesis presented the design and implementation of a novel reconfigurable analog to digital converter for DS-UWB communications. The reconfigurability of the design was based upon the dynamicity of comparators and the ability to switch them OFF and ON as required. The novel converter was implemented based on unique active bulk biased analog multiplexers which were used to determine the reference voltage level for the succeeding stage comparator. The research also explored the possibility of implementing a real time dynamic controller to control the reconfiguration process. The controller was a concept whose functionality is based upon the quality and type of signals obtained from the input to the receiver chain, output of LNA, output of ADC and from the digital backend. The intelligence in the controller was based upon its ability to estimate and average the impinged signals and compare them to specific thresholds. The concept was designed using Verilog-AMS modelling language and tested for its functionality along with the designed reconfigurable converter.

A high speed fully differential flash converter was also implemented to satisfy the requirements for DS-UWB communication. The flash converter was based upon unique fully differential comparators and a modified encoder. The flash converter was based upon a modified E shaped architecture enabling closer integration of the encoder along with the comparator array. The flash converter designed was a verification of the designed comparator and a proof of functionality for high bandwidth high sampling DS-UWB communication. The designed flash converter was also used to set a benchmark reference to implement the novel reconfigurable converter. The benchmarking was to enable a comprehensive performance comparison of the two converters presented in

this work in terms of performance metrics such as power, speed size, linearity, dynamic range, effective resolution, amongst others.

Some of the key contributions from this research work are as listed below;

- Investigation into the various applications of high speed communication, focussing upon the differences between Ultra Wideband and other communication schemes. An in-depth look into MB-OFDM and DS-UWB communications.

- Review of the various analog to digital converters present, with an analysis of the suitability of each of them for UWB communications. Mathematical approach to set the design requirements for the target converter for DS-UWB applications.

- Design and implementation of a fully differential open loop high speed comparator, based upon the requirements set forth previously. Comparator designed was a unique 4 stage architecture comprising of a preamplifier, track and hold latch, regenerative latch and high speed buffer. The designed comparator was used to implement the flash and reconfigurable converters.

- Design and implementation of a high speed fully differential flash analog to digital converter based upon an E-shaped parallel architecture. Comprehensive look into the different topologies for high speed encoder, with the implementation of a modified fully differential high speed Common Mode Logic based design.

- Design and implementation of a novel reconfigurable analog to digital converter, employing a switch OFF and ON mechanism for power saving. Investigation of switch types and implementation of a novel analog multiplexer and enable circuitry. Investigation of a real time dynamic controller to perform reconfiguration.

- Comprehensive test and analysis of both flash and reconfigurable converters in along with an in-depth comparison of the performance of the two designs. The results obtained show that the reconfigurable

converter achieves a maximum power saving of 32 % for complete 4 bit operation, dropping to 27 % with the inclusion of the concept controller. A 58 % saving in the total active area occupied by the reconfigurable design as compared to custom flash converter.

- Matching characteristics of linearity, dynamic range, effective resolution, verifies the performance of the reconfigurable converter on par with that of the high speed flash, however achieving a reduced power and area profile.

To the best of the authors knowledge the contribution to research presented in this work targeted specifically at DS-UWB communication have been not been addressed or have so in a very minimalistic capacity. The work presented in this thesis is an attempt to address and overcome this shortcoming.

8.2 Future Scope of Work

The work presented in this thesis can be used as a stepping stone to undertake future research targeting high speed analog to digital converters for high data rate communications. One of the possible motivations in the future is to apply the reconfigurable design into the still under developed field of 60 GHz communications targeting wireless data rates of the order of 50 to 100 Gbps. The stepping stone for that work would enable a possible shift of the converter implementation into 65 and 45 nm CMOS technology. The use of non-uniform sampling to reduce the ADC complexity along with non-finite resolutions may also be considered in taking this research further.

The dynamic controller presented in this work is a proof of concept, which has not been explored to full potential due to scope of work. It is hoped that the research into this concept can be taken further to implement into a system level functionality targeting not only UWB but also other communication mediums. The low power and intensely complex nature of future high speed communications may drive the need for real time power saving options.

Impact of static leakage will become a large factor for high speed communications and occupy an increased portion of the total power consumption for technology nodes lesser than 90nm. The multiplexers in this work led the reconfigurable converter to have a total static power dissipation of 5.5 %. However it is foreseeable that this limit will rise for 65 and 45 nm transistor nodes. Minimising this impact of leakage power upon the total power consumption could be another driving force for the future adaptation of this research.

The research presented in this work is a realistic attempt to deal with the shortcomings present in DS-UWB communications. The author hopes that this research contribution is measurable and apt.

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Appendix

Appendix A

Matlab Code for Cadence Data Analysis

Ocean Script for Output Dump

```
;Dump for Custom Flash Testbench

library = "ADC"
cell = "Flash_Testbench"
view = "config"
process= "CMOS090"
capacitor = "CMOS090"
resistor = "CMOS090"

queue =  nil
jobname = "Flash_run"
dumpfile = strcat("~/ToMatlab/Flash_run.txt")

;Dump for Reconfigurable Testbench

library = "ADC"
cell = "Reconf_Testbed"
view = "config"
process= "CMOS090"
capcitor = "CMOS090"
resistor = "CMOS090"

queue =  nil
jobname = "Reconf_run"
dumpfile = strcat("~/ToMatlab/Reconf_run.txt")
```

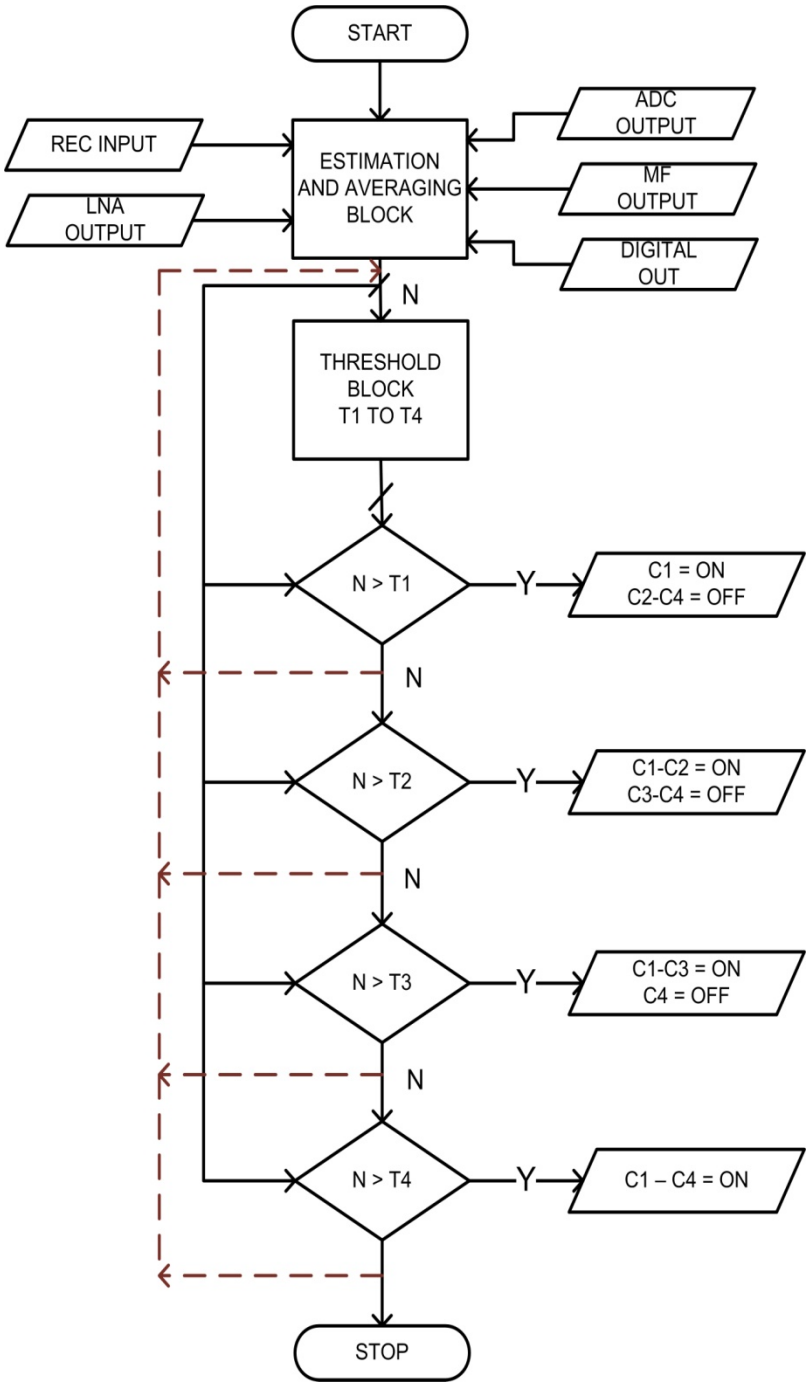
Script Read Into MATLAB and Processing

```
function [Voltage, Time] = read(Flash_run.txt)

  [Val, Voltage, Time] = textread(Flash_run.txt, '%f %f %f');

  Voltage = Val;

function [mag, fre] = getmag(Val, Time, Voltage)

  if(bin > 5000)

    if(time < bin(time))

      mag = time(1:bin).* 0.5(bin);
```

```
   else
     mag = 0.5.*time (bin));
   end
  end
  mag = abs(mag(Voltage, bin));
  fre = (0:rbin)*fre/bin;
for (bin=1:N)
          if(N=4)
          mag=fft(ceil(Voltage), fre));
          else
          if(N=3)
          mag=(fft(0.75.*ceil(Voltage), fre));
          else if(N=2)
          mag=fft(0.5.*ceil(Voltage), fre));
          else
          mag=fft(0.25.*ceil(Voltage, fre));
          end
          end
end
plot(db20(ceil(mag), fre, ‘grid --’);
xlabel('Frequency (GHz)');
ylabel('Magnitude (dB));
```

Appendix B

Concept Controller Flow Diagram and Verilog-AMS Code



```
//Verilog-AMS HDL for "Reconf Controller" "verilogams"


`include "constants.vams"
`include "disciplines.vams"
module Est_Avg(Input_Avg, ADC_inp, LNA_oup, Rec_oup, MF_oup, Ant_inp);
output Input_Avg;
electrical Input_Avg;
input ADC_inp, LNA_oup, Rec_oup, MF_oup, Ant_inp;
electrical ADC_inp, LNA_oup, Rec_oup, MF_oup, Ant_inp;
analog begin
        for (V(ADC_inp, LNA_oup, Rec_oup, MF_oup, Ant_inp))
        module estimate(@ top (V(Input_Avg), 0.1)
        V(Input_Avg) = @(average(ADC_inp, LNA_oup, Rec_oup, MF_oup, Ant_inp);
        end module
        end;
end module


module controller (Input_Avg,cntrl1, cntrl2, cntrl3, cntrl4,clk);
input Input_Avg,clk;
electrical Input_Avg,clk;
output cntrl1, cntrl2, cntrl3, cntrl4;
electrical cntrl1, cntrl2, cntrl3, cntrl4;
parameter real T1=.25;
```

```
parameter real T2=0.5;
parameter real T3=0.75;
parameter real T1=1.0;
analog begin
        @(cross(V(clk)-0.5,+1)) begin
                if(V(Input_Avg) > T1)
                begin
                        V(cntrl1)=1.0;
                        V(cntrl2)=0.0;
                        V(cntrl3)=0.0;
                        V(cntrl4)=0.0;
                end
                else if ((V(Input_Avg) > T2) & (V(Input_Avg) < T1))
                begin
                        V(cntrl1)=1.0;
                        V(cntrl2)=1.0;
                        V(cntrl3)=0.0;
                        V(cntrl4)=0.0;
                end
                else if ((V(Input_Avg) > T3) & (V(Input_Avg) < T2))
                begin
                        V(cntrl1)=1.0;
                        V(cntrl2)=1.0;
```

```
                V(cntrl3)=1.0;
                V(cntrl4)=0.0;
            end
            else if ((V(Input_Avg) > T4) & (V(Input_Avg) < T3))
            begin
                V(cntrl1)=1.0;
                V(cntrl2)=1.0;
                V(cntrl3)=1.0;
                V(cntrl4)=1.0;
            end
        end
endmodule
```