A Digital Up-Conversion Architecture for Future High Efficiency Wireless Base Stations

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"I, Vandana Bassoo, declare that the PhD thesis entitled 'A digital up-conversion architecture for future high efficiency wireless base stations' is no more than 100,000 words in length including quotes and exclusive of tables, figures, appendices, bibliography, references and footnotes. This thesis contains no material that has been submitted previously, in whole or in part, for the award of any other academic degree or diploma. Except where otherwise indicated, this thesis is my own work."

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Abstract

Over the past few years, there has been a growing need for wireless communications with higher data rates and ubiquitous coverage, and these must be achieved at reduced cost and with a lower carbon footprint. This evolution in wireless demand places a big burden on transmitter architectures. The need for higher efficiency has stimulated research into the potential replacement of current linear power amplifiers (PAs) by switch mode power amplifiers (SMPAs) at cellular frequencies. The radio frequency (RF) PA currently accounts for a significant part of the cost, and most of the power requirements of a typical wireless base station.

This research is focused on the modulation and up-conversion circuits for generating the SMPA drive signals. The switched ('on'/'off') nature of the amplifier drive signal creates an opportunity for an all-digital solution removing traditional analog components such as the digital to analog converters, reconstruction filters, quadrature modulator and local oscillators. Digital signal processing techniques used for signal modulation are extended to digital upconversion to generate suitable drive signals for the SMPA. In this thesis, a sigma-delta ($\Sigma\Delta$) based technique is used to embed a complex modulation scheme such as OFDM into a single 'on'-'off' bit stream.

The first contribution of this thesis is the proposal of an all-digital modulation and up-conversion architecture that combines polar quantisation with Cartesian $\Sigma\Delta$ filtering. The drive waveform has a maximum of one pulse per half period thus limiting the number of switchings and hence increasing efficiency. It is shown that the proposed architecture provides an adjacent channel power (ACP) of lower than -50 dB for a bandwidth of over 100 MHz. An oversampling ratio of eight is required to meet the ACP specifications of wireless local area network (WLAN) and an oversampling of 32 is required to meet the third generation partnership project (3GPP) mobile phone standards. The all-digital approach described in this thesis is currently unfeasible for these frequency bands due to the limitations of today's digital circuit technology. However, this approach can be used for lower carrier frequencies such as those found in the very high frequency (VHF) region.

The non-uniform polar quantiser is mathematically analysed to derive the quantisation noise power generated from a Gaussian symmetric input signal. Simulations show the performance diverges from that predicted when signal levels are low. Further analysis, based on limit cycle operation, confirms the low level behaviour of the quantiser in a $\Sigma\Delta$ loop. At low powers the signal noise ratio (SNR) increases at a rate of 0.5dB/dB in the desired signal. This improves to 1dB/dB at medium powers and drops to 0 dB/dB in the overload region.

Finally, problems associated with converting polar values into pulse widths and pulse positions are investigated. Spurious tones observed in the spectrum are attributed to the pulse position modulation (PPM) process and their generation is

explained by the digital nature of the waveforms. A mathematical analysis is proposed to predict the size and position of the unwanted spectral components. Simulations and practical measurements are also carried out using both single-carrier and multi-carrier signals. It was also shown that a three-level waveform, for push-pull operation, attenuates and in many cases completely removes the spurs. Even so the amount of carrier frequency offset adjustment is strictly limited, if WLAN or 3GPP spectrum mask requirements are to be met.

Acknowledgements

First, I would like to thank my supervisor, Prof. Mike Faulkner, who introduced me to research and has provided me with invaluable advice, guidance and support over the years. Having a wealth of knowledge in my research area, he has been a great mentor and spent countless hours patiently explaining even the most trivial concepts. I would like to thank him for his encouragement and his belief in my abilities.

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To my family.

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List of Abbreviations

ΣΔ - Sigma Delta

3GPP - Third Generation Partnership Project

4G - Fourth Generation

ACP - Adjacent Channel Power

ADC - Analog to Digital Converter

AM - Amplitude Modulation

BW - Modulation Bandwidth

CAPEX - Capital Expenditure

DAC - Digital to Analog Converter

DSP - Digital Signal Processing

EDGE - Enhanced Data Rates for GSM Evolution

EER - Envelope Elimination and Restoration

EVM - Error Vector Magnitude

FFT - Fast Fourier Transform

GaN - Gallium Nitride

GHz - Gigahertz

GMSK - Gaussian Minimum Shift Keying

HF - High Frequency

LDMOS - Laterally Diffused Metal Oxide Semiconductor

LINC - Linear Amplification of Non-Linear Components

LTE - Long Term Evolution

MSE - Mean Square Error

NTF - Noise Transfer Function

OFDM - Orthogonal Frequency Division Multiplexing

OPEX - Operating Expenditure

OSR - Oversampling Ratio

PA - Power Amplifier

PAPR - Peak to Average Power Ratio

PCB - Printed Circuit Board

PDF - Probability Density Function

PM - Phase Modulation

PPM - Pulse Position Modulation

PWM - Pulse Width Modulation

QPSK - Quadrature Phase Shift Keying

RMS - Root Mean Square

RF - Radio Frequency

SMPA - Switch Mode Power Amplifier

SNR - Signal to Noise Ratio

SQNR - Signal to Quantisation Noise Ratio

SSB - Single Side Band

STF - Signal Transfer Function

UHF - Ultra High Frequency

VHF - Very High Frequency

WCDMA - Wideband Code Division Multiple Access

WLAN - Wireless Local Area Network

ZVS - Zero Voltage Switching

List of Mathematical Notations

u_I - Cartesian in-phase component of input signal

u_Q - Cartesian quadrature component of input signal

R - Amplitude component of the polar $\Sigma\Delta$ filtered signal

θ - Phase component of the polar $\Sigma\Delta$ filtered signal

Q_R - Amplitude quantisation block

Q_θ - Phase quantisation block

$\hat{R}$ - Quantised amplitude

$\hat{\theta}$ - Quantised phase

$\hat{I}$ - Cartesian in-phase feedback to $\Sigma\Delta$ filters

$\hat{Q}$ - Cartesian quadrature feedback to $\Sigma\Delta$ filters

N_P - Number of phase increments

n_p - Pulse position delay in clock periods

f_{clock} - System digital clock frequency

f_c - Carrier frequency

N_A - Number of amplitude quantisation levels

v - Pulsewidth in number of clock periods

T_{clk} - Time period of system digital clock

$u(...)$ - A step function of amplitude 1

L_R - Threshold for quantised amplitude

L_θ - Threshold for quantised phase

f_s - Sample rate of $\Sigma\Delta$ filters

f_{sbp} - Sample rate of bandpass $\Sigma\Delta$ filters

V_{dd} - Voltage drain drain

$OSR_{\Sigma\Delta}$ - Oversampling rate of $\Sigma\Delta$ filters

H - Number of half periods between each update of $\Sigma\Delta$ circuit

G_T - Gain term of the $\Sigma\Delta$ architecture

B_{OFDM} - OFDM bandwidth

$N_0(f)$ - Quantisation noise power spectral density introduced by quantiser

δ - Small constant increment of input signal

N_T - Number of pulses after which a large pulse occurs in the quantiser

f_{ssb} - Frequency of single side band tone

T_{ssb} - Time period of the single side band tone

T_g - On period of the pulse train

T_c - Time period of carrier

$\tilde{S}_k(f)$ - Spectrum of oscillator signal

$\tilde{G}_k(f)$ - Spectrum of gate signal

$\tilde{Y}_k(f)$ - Convolution of spectrum of oscillator signal and gate signal

Chapter 1

Introduction

The existing third generation network deployed around the world is not sufficient to meet the needs of new upcoming bandwidth intensive applications. A recent study estimated that by 2013, 80% of the three billion broadband users will be connected through a wireless device [1]. This has to be achieved within the constraints of today's fragmented spectrum, multiple operating standards and the need for a low carbon footprint. A fourth generation (4G) wireless system will be required to transmit higher bit rates in a more flexible manner. Fig. 1.1 shows a roadmap of the evolution of wireless technologies. Both cellular and wireless local area network (WLAN) technologies are converging towards a single universal standard, 4G. 4G networks are expected to deliver data rates between 100 Mbps to 1 Gbps. The 4G standard can therefore be described as mobile, broadband, seamless and ubiquitous [2]-[9].

Consequently, the next generation wireless transmitter architectures need to use innovative technologies to be bandwidth efficient, power efficient, broadband and flexible. The radio frequency (RF) power amplifier (PA) is a crucial element of any

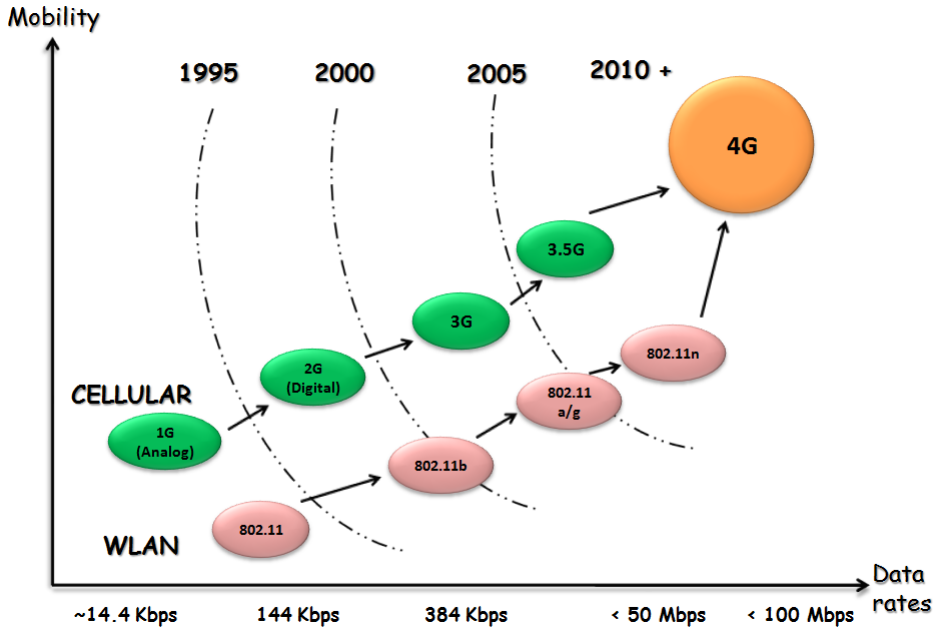

Figure 1.1: Evolution of wireless technologies (after [2]).

wireless transmitter architecture. Bandwidth efficient multi-carrier schemes such as orthogonal frequency division multiplexing (OFDM) are required to cater for the increasing transmission bandwidths. OFDM signals are best amplified by conventional linear RF power amplifiers; however the efficiency is very poor. Switch mode power amplifiers (SMPAs), such as class E amplifiers, are known to be highly nonlinear but attain maximum efficiency if driven by a pulse waveform. The challenge is on the modulation stage to generate the appropriate drive signal which is optimised for efficiency and linearity. Over the years, process technology has improved and it is now possible to directly generate the RF drive signal from a digital source. The replacement of the traditional base station architecture by a digital architecture with the use of SMPAs has many benefits.

1.1 Towards a 'Green' Base Station

At present, the radio interface is the largest power usage component, accounting for approximately 80% of an operator's total power consumption [10]. The generation of large amounts of heat because of high power usage due to inefficient operation leads to higher costs and an unacceptable environmental impact. High energy consuming air conditioning is required to dissipate the heat produced by the linear PAs in order to maintain an acceptable ambient temperature. The change to SMPAs with theoretical efficiencies of 100% will significantly reduce the operating carbon footprint and eventually reduce operational and maintenance expenses.

In many large developing nations, the power supply infrastructure does not cover the entire country. Mobile operators are forced to use diesel power generators for their base stations. The need for a back-up generating set and the logistic effort of supplying diesel to remote places pose a significant economic cost [11]. Furthermore, the use of diesel as fuel is highly polluting. Lowering the power consumed by base stations will easily enable the use of renewable energy sources such as wind, solar or methane. The initial capital expenditure (CAPEX) can be high for 'green' energy solutions, but the operating expenditure (OPEX) is very low as energy is free. Within a few years of operation, green base stations will become an economically viable solution for operators. This is a very important development as it has been predicted that 90% of new subscribers will come from developing or under developed countries where 50%-80% of the population lives in far rural areas [12]. The monthly spending of those subscribers will be significantly lower. Green base stations may

eventually become the service providers' solution to the emerging low income market.

1.2 Social Advantages of a Connected Lifestyle

The advances in transmitter architecture are also driven by the expectation of users to have ubiquitous and broadband access to all their information, communication and entertainment services. It is well documented that access to broadband has positive social impacts on society [12]. A wide broadband network prevents problems associated with urbanisation from occurring. It allows people to open new businesses in rural areas and to have customers from around the world. Broadband also enables office workers to use remote office access and reduce traffic and congestion. Broadband provides reliable video conferencing and hence reduces carbon dioxide emissions by circumventing unnecessary travel. While narrowband access can cater for many services, broadband provides the reliability and quality that is required for applications such as telemedicine. It is indisputable that broadband will continue to improve the quality of life and bridge the socio-economic gap.

1.3 Replacement of Analog Components

The driving force behind the tremendous growth in wireless communications has been the introduction of digital coding and digital signal processing (DSP) in wireless architectures [13]. Moore's law states that the number of transistors on a chip would double every two years [14]. In line with this trend, Intel announced the launch of a chip with two billion transistors in early 2010 [15]. Digital clock frequencies are now in the gigahertz (GHz) region and hence digital processing can now be used to

implement some microwave functions that were previously performed using analog components. There are many significant advantages to this major evolution in circuit design. Some of these are [16]:

1. Digital circuits are not susceptible to changes in temperature and are not subject to ageing.

2. Digital circuits do not require constant tweaking (or factory calibrations) to adapt to manufacturing tolerances.

3. The advancements in digital circuits provide the possibility of integrating both the digital and microwave sections on a single chip.

4. Digital circuits provide reconfigurability enabling the adaptation of architectures to different standards or to changes in system requirements. Consequently, the architectures become more robust, cost-effective and flexible.

5. Digital components are understood to consume less power than analog components [16].

6. Testing of digital circuits is an easier task.

1.4 Towards an All-Digital Transmitter

A traditional transmitter architecture is shown by Fig 1.2(top). Modulated I and Q signals from baseband circuits are modified to minimise the peak power requirements of the following analog circuits. The modification often takes the form of

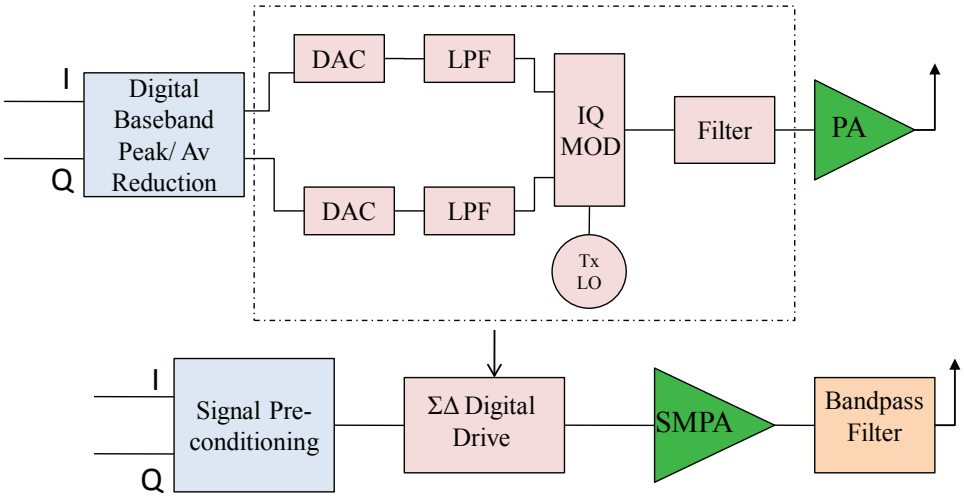

Figure 1.2: Traditional and potential future wireless base station architecture.

clipping and filtering after which the signal passes through digital to analog converters and lowpass reconstruction filters before entering a quadrature modulator for up-conversion to RF. An RF filter after the up-conversion reduces out of band noise from the transmitted signal.

The new architecture (Fig 1.2(bottom)) eliminates many analog components in the transmitter chain and replaces them with a single digital sigma delta ($\Sigma\Delta$) up-conversion circuit. The output of which is a digital representation (0, 1) of the modulated carrier signal. The new circuit trades off the high speed capabilities of modern digital circuits for the elimination of many analog difficulties. Problems such as gain-phase imbalance of the IQ modulator, carrier leak, the need for an analog RF synthesiser and the need for wideband matching of lowpass filters are all eliminated.

The new architecture is not without its problems. $\Sigma\Delta$ noise shaping must be

dealt with using a bandpass filter on the output of the amplifier. Noise and distortions in the signal band must be kept below the specified masks. Some degree of oversampling will be necessary and this can have significant impacts on the maximum usable carrier frequency. Also, the noise shaping associated with the $\Sigma\Delta$ filtering will limit the utilizable bandwidth of the system.

1.5 Research Objectives

The aim of the research program is to study the feasibility of an all-digital RF transmitter architecture with Cartesian inputs and producing a high power RF output using switch mode techniques. The transmitter must have high efficiency and exploit the new advancements in power amplifier technology brought about by the advent of new devices with low parisitic capacitances such as gallium nitride (GaN). These devices are thus more suitable for switching circuits than the traditional silicon laterally diffused metal oxide semiconductor (LDMOS) transistors used in today's quasi-linear class A/B basestation amplifiers. The work was supported by L.M. Ericsson (Sweden), who gave the following three point objectives for the switched transmitter:

1. 100 W output power
2. 100 MHz bandwidth
3. 100% efficiency (as efficient as possible)

The overall goal of the research program is to provide a complete transmitter solution that will fulfill the above objectives as closely as possible. The key architectural blocks include a digital pre-conditioning algorithm (if required), a digital modulator, a digital upconverter and a SMPA with its associated drive circuit.

The work has been split into three PhD research projects represented by the first three blocks in Fig 1.2(bottom). The pre-conditioning algorithm modifies the modulated baseband signal to improve its compatibility with the SMPAs. Typical examples of pre-conditioning include peak power reduction and the minimisation of bandwidth expansion caused by non-linear operations in some switch mode architectures. All the SMPAs to be studied in this work are based on Class E designs. The topologies include envelope elimination and restoration (EER), linear amplification of non-linear components (LINC) and stand-alone Class E. However, the subject of this thesis is the digital modulator and upconverter circuits that produce the drive signals for the SMPAs. The circuit generates pulse-width and pulse-position digital waveforms at the carrier frequency.

For synchronous operation, the pulse edges are constrained to the timing grid of the digital clock. In pulse width modulation (PWM) and pulse position modulation (PPM), the amplitude is represented by the width or marks-space ratio of the pulse and the phase is represented by the position of the pulse. The amplitude (pulse width) and phase (pulse position) will be coarsely quantised. This will generate considerable quantisation error which will need to be shaped. $\Sigma\Delta$ noise shaping is a technique for pushing quantisation noise away from the band of interest such that

it can be filtered out at a later stage.

The research objectives of this thesis are:

1. To propose an appropriate ΣΔ architecture for generating pulse width modulated and pulse position modulated signals.

2. To propose a scheme that is compatible with digital up-conversion techniques and is capable of providing basic tuning across the operating band.

3. To provide a signal with good spectral performance that meets the spectrum mask requirements of the major standards such as WLAN and third generation partnership project (3GPP). Both WLAN and long term evolution (LTE) use channel bandwidths of up to 20 MHz, and any number of channels can be filled within the 100 MHz band. A total of five channels are possible, and each has an adjacent channel power (ACP) specification, which should be met. The ACPs are defined as the noise power in the adjacent channel divided by the signal power. The first and second ACPs for WLAN are ACP(1)= -28 dB and ACP(2)= -40 dB and for 3GPP ACP(1)= -40 dB and ACP(2)= -50 dB.

1.6 Contributions to Knowledge

The following novel contributions have been made in this thesis:

1. A novel all-digital RF transmitter architecture is proposed for generating a digital drive signal for a SMPA. The architecture is referred to as the Cartesian ΣΔ scheme.

2. It is clearly shown that the proposed Cartesian $\Sigma\Delta$ scheme outperforms the polar $\Sigma\Delta$ scheme of [17] by about 10 dB in terms of adjacent channel power in the immediate adjacent channels.

3. The theoretical mean square error (MSE) for a non uniform polar quantiser operating in both stand-alone and feedback modes has been derived.

4. MSE bounds for the $\Sigma\Delta$ modulator with polar quantiser have been derived. The bounds are valid for the high signal region and the low signal region. The bounds show that the slope of MSE vs. input signal power is 1.0 dB/dB in the stand-alone case and 0.5 dB/dB in the feedback mode.

5. The source of unwanted spurs (spectral peaks) in the output spectrum was attributed to the 'polar to PWM/PPM block'. A mathematical derivation was used to predict the size and position of these distortion components. The distortions were shown to increase with offset frequency. A three-level waveform, for push-pull operation, was shown to attenuate and in some cases eliminate many of these spurs. Experimental results verified the analysis.

1.7 List of Publications

From the research accomplished in this thesis, a number of peer-reviewed publications have been obtained.

1. V. Bassoo, L. Linton, and M. Faulkner, "Analysis of distortion in pulse modulation converters for switching radio frequency power amplifiers," *Microwaves,*

Antennas and Propagation, IET, vol.4, no.12, pp.2088-2096, December 2010

2. V. Bassoo, K. Tom, A.K. Mustafa, E. Cijvat, H. Sjoland, and M. Faulkner, "A Potential Transmitter Architecture for Future Generation Green Wireless Base Station," *EURASIP Journal on Wireless Communication and Networking*, Article ID 821846, 8 pages, 2009.

3. V. Bassoo and M. Faulkner, "Sigma Delta Digital Drive Signals for Switch-mode Power Amplifiers", *Electronic Letters*, Vol. 44, Issue 22, pp 1299-1300, October 2008.

4. H. Sjoland, C. Bryant, V.Bassoo and M.Faulkner, "Switched Mode Transmitter Architectures," in *Analog Circuit Design Smart Data Converters, Filters on Chip, Multimode Transmitters*, A.H.M Van Roermund, Ed. Netherlands: Springer, 2009, pp. 325-342.

5. V. Bassoo, A. Mustafa, and M. Faulkner, "Distortion Arising from Polar to PWM/PPM Conversion in an All Digital Upconverter for Switching RF Power Amplifier," *Proc. IEEE IMS Int. Microwave Symposium*, Boston, USA, June 2009, pp. 1533-1536.

6. V. Bassoo, K. Tom, A.K. Mustafa, E. Cijvat, H. Sjoland, and M. Faulkner, "Potential Architecture for Future Generation 'Green' Wireless Base Station", *Proc. IEEE ISWPC Int. Symposium on Wireless and Pervasive Computing*, Melbourne, Australia, February 2009, pp. 1-5.

7. H. Sjoland, C.Bryant, V.Bassoo, M.Faulkner, "Switched Mode Transmitter Architectures," in *Proc. of the 18th Workshop on Advances in Analog Circuit Design (AACD)*, pp. 315-333,Ericsson AB, Lund, Sweden, April 2009.

8. A. K. Mustafa, V. Bassoo, and M. Faulkner, "Reducing the drive signal bandwidths of EER microwave power amplifiers," in Proceedings of the International Microwave Symposium (IMS '09), Boston, Mass, USA, February, 2009.

9. K. Tom, V. Bassoo, M. Faulkner, T. Lejon, "Load Pull Analysis of Outphasing Class E Amplifier," *Proc. IEEE Auswireless*, Sydney, Australia, August 2007.

1.8 Thesis Outline

This thesis is organised as follows:

- Chapter 1 outlines the motivations behind this research. The research objectives of the thesis are presented. Moreover, a list of publications which have directly resulted from the work in this thesis is given.

- Chapter 2 provides background information and a summary of relevant existing literature. The basic concepts of SMPAs are presented in this chapter using Class D and E as examples. The remaining parts of the chapter are dedicated to $\Sigma\Delta$ fundamentals. Key $\Sigma\Delta$ architectures are introduced namely the lowpass $\Sigma\Delta$, bandpass $\Sigma\Delta$ and higher order $\Sigma\Delta$ structures. Existing transmitter architectures are presented such as EER, LINC and the polar $\Sigma\Delta$ scheme.

- Chapter 3 introduces the novel all-digital RF Cartesian-based transmitter architecture which, in this thesis, is referred to as the Cartesian $\Sigma\Delta$ scheme. The main components, which are the $\Sigma\Delta$ filters, the non-uniform polar quantisers and the 'polar to PWM/PPM' converters, are explained. A trade-off between noise performance and efficiency is also discussed. A spectral domain comparison of the polar and the Cartesian architectures shows an improved in-band noise performance for the Cartesian version. The effect of oversampling ratio (OSR) on ACP is studied.

- Chapter 4 gives a quantisation noise analysis of the non-uniform polar quantiser. The polar quantiser uses a circular symmetric Gaussian input signal as input to the system. It is a good approximate of modern communication signals such as OFDM and code division multiple access (CDMA). A generalised mathematical expression is derived for the MSE of a stand-alone polar quantiser. Simulation results of the stand-alone quantiser and the quantiser within the $\Sigma\Delta$ loop are compared. Two major differences between the plots are attributed to the noise enhancement of the $\Sigma\Delta$ loop and the limit cycle behaviour of the loop at low signal powers.

- Chapter 5 investigates the occurrence of the distortions (images and harmonics) in the spectrum when the input signal is offset from the nominal centre frequency. A mathematical analysis shows the distortions are caused by the harmonic content of the square-shaped pulses of the output signal. Simulations

using single sideband tone confirm the analysis. Practical measurements using an OFDM signal and a data timing generator further confirm the analysis.

- Chapter 6 concludes the work and indicates possible future research opportunities. These include a joint amplitude-phase quantisation scheme and the use of predistortion to cancel unwanted images and harmonics generated by the PPM process.

Chapter 2

Background Information

2.1 Introduction

In this chapter, some basic SMPA structures (Section 2.2) are explained, since they are a key component of the next generation green wireless architecture. This is then followed by a review on $\Sigma\Delta$ modulators (Section 2.3), since they provide a possible modulation technique that allows modern communication signals to be embedded into a digital-bit stream. The final section (Section 2.4) reviews recent work in $\Sigma\Delta$ based transmit architectures.

2.2 Switch Mode Power Amplifiers

The development of new power amplifier architectures is essential for the evolution of the mobile wireless system. Modern modulation systems such as OFDM or CDMA suffer from PAPR. Non-linear amplifications will lead to problems with spectral regrowth and inter-tone interference. The non-linearities are generally caused by amplitude variations in the envelope. RF PAs are generally categorised in classes

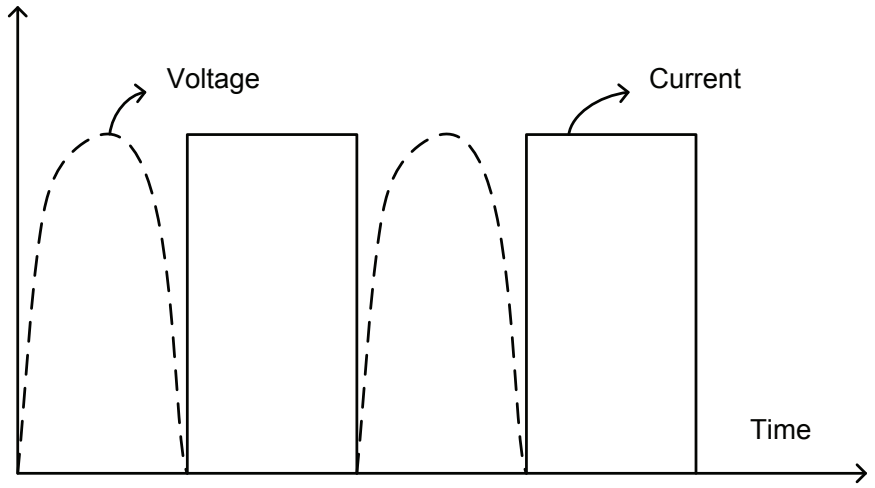

Figure 2.1: Current voltage relationship in the transistor.

A-F. All classes will generate some type of distortion. The classes are usually defined by the input bias, mode of operation and power-output capability of the RF PAs [18]. Current power amplifiers in wireless transmitter architectures are quasi-linear (Class AB) but they are unfortunately bulky and power hungry [19]. Future wireless systems require PAs to provide high efficiency, good linearity and be small in size.

SMPAs have a theoretical efficiency of 100% but are highly non-linear [20]. Higher order modulation schemes such as 64-quadrature amplitude modulation (QAM) are necessary to provide the increasing data rates of modern wireless systems and these schemes requires power amplifiers to exhibit linearity. However, a modulated input signal can be encoded into a pulse train capable of driving the SMPAs at maximum efficiency and by-passing the linearity issue [21, 22]. Unfortunately, there are many practical difficulties in doing this.

2.2.1 Concept of Switch Mode Power Amplifier

As the name indicates, the transistor in a SMPA ideally operates as a switch. The main idea is to operate the transistor in saturation so that at any time, either voltage or current flows. When the switch is open, only voltage is present and when it is closed, current flows through it, as shown by Fig 2.1 [23]. Ideally, current and voltage never overlap and power is not dissipated, hence the 100% theoretical efficiency. Two examples of SMPAs are the Class D and Class E PAs.

2.2.2 Class D Amplifier

A simple class D power amplifier is depicted in Fig. 2.2. The topology consists of two transistors which switch either to supply or to ground creating the pulse waveform. Harmonic power is wasted if the square waveform is applied directly to the load, R_L. Therefore, a series tank network consisting of an inductor, L_0 and a capacitor, C_0 is inserted between the output of the transistor and the load, R_L [24]. The network provides filtering and also impedance transformation which enables the amplifier to deliver sufficient output power at low supply voltages. In practice, the efficiency of the amplifier is not 100%. One of the sources of power loss is due to the hard switching property of the transistor; the switch closes while the voltage is non-zero. Another cause of efficiency degradation relates to the number of 'turn-ons' and 'turn-offs' as they require the device parasitic capacitors to charge and discharge which dissipates energy [25, 26]. In the event both the transistors conduct simultaneously, a shoot-through current may cause the efficiency to further

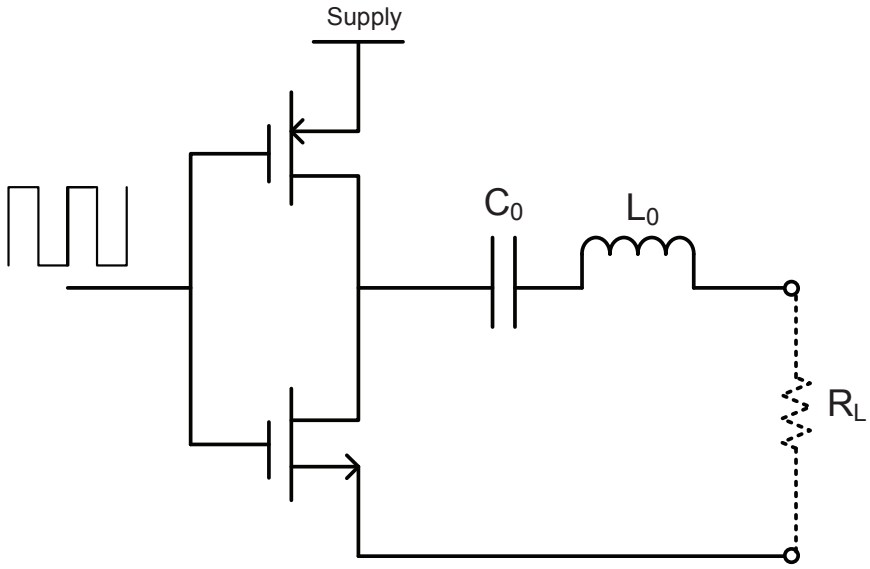

Figure 2.2: Schematic of a Class D PA.

degrade at higher frequencies. However, a class-D amplifier is very robust to changes in load impedance as the output voltage is bounded to the range between ground and supply [27].

2.2.3 Class E Amplifier

Class E amplifier has a very simple circuitry as shown by Fig. 2.3. The key feature of this structure is the addition of inductor, L_x in the output circuit [29]-[32]. The inductance task is to null the effect of the parasitic capacitance, C_1. Therefore when the switch is closed, the voltage across the transistor has already fallen to zero and no switching losses occur. This effect is known as the zero voltage switching (ZVS) or soft switching. The capacitance in the output network helps to improve the high frequency efficiency of the Class E PA compared to a Class D. However under mismatched load conditions, the output voltage can be very high and ZVS ceases to occur.

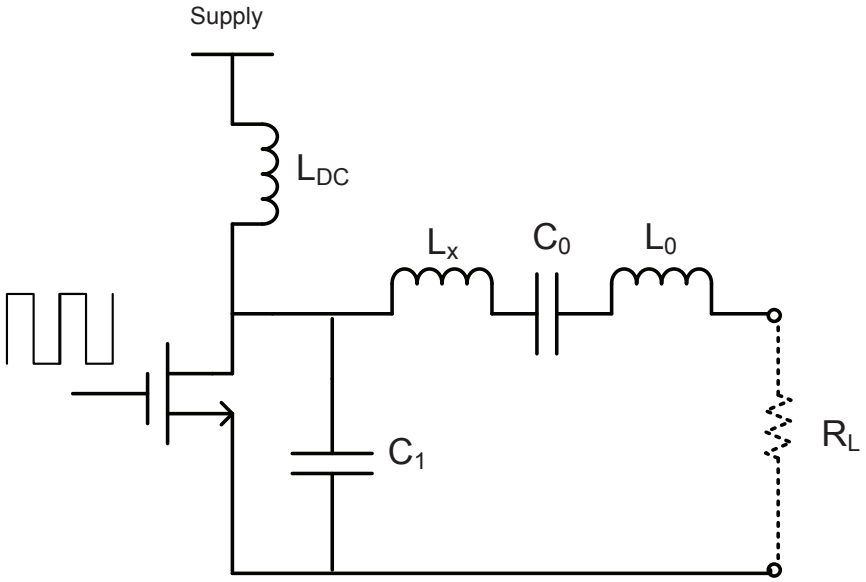

Figure 2.3: Schematic of a Class E PA.

2.2.4 A Practical Amplifier

In this section, practical measurements on GaN amplifier operating in a near switch mode condition (between class C and E) is described. The work in this subsection was performed by a colleague and presented in a joint publication [33].

A simple way to obtain PWM operation is to use a comparator and a triangular drive signal with the reference input controlled by the envelope modulation (Fig. 2.4). In this work, the PWM signal is directly generated in the output power device. The amplifier input is overdriven with sinusoidal carrier signal (V_p), and the gate bias (V_{bias}) is controlled by the envelope component of the modulated signal. Since the device threshold voltage (V_T) is fixed, this has the effect of varying the on/off duty cycle of the amplifier, as illustrated in Fig. 2.5. The method produces two side effects, firstly the pulse width is no longer linear with respect to the envelope signal, $\Delta V = (V_T - V_{bias})$, because of the non-triangular drive signal. Secondly,

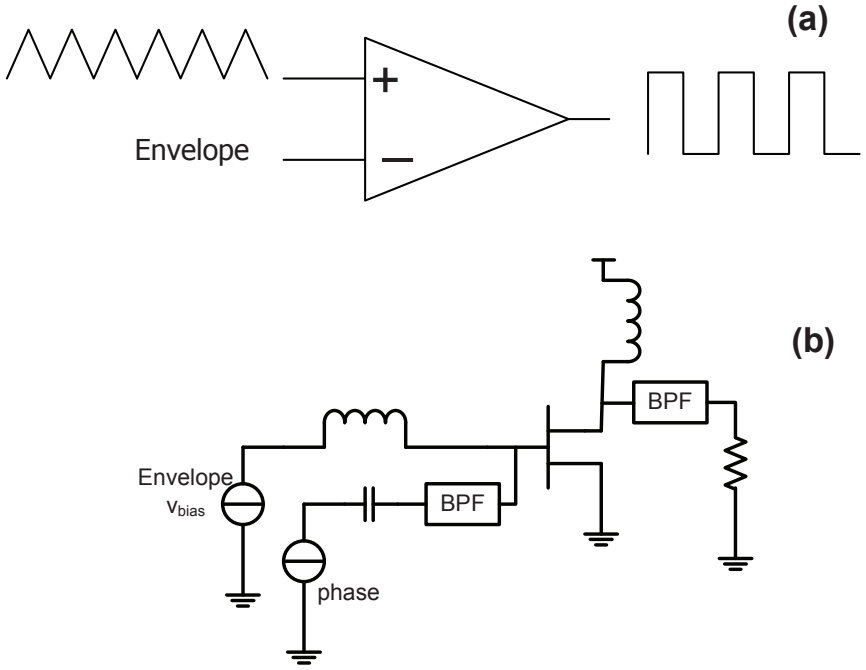

Figure 2.4: PWM generation:(a) ideal, (b) PA schematic

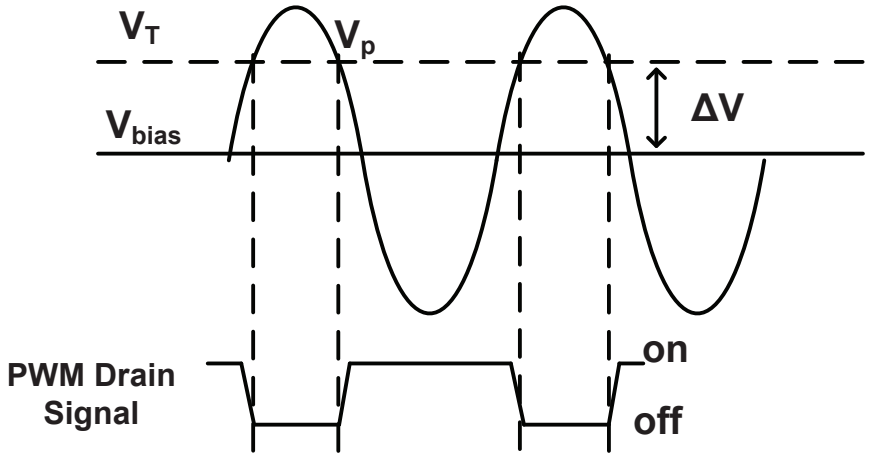

Figure 2.5: Operating principle of the power amplifier. The voltage difference ΔV varies with envelope signal, V_{bias}. The resultant PWM drain signal is illustrated.

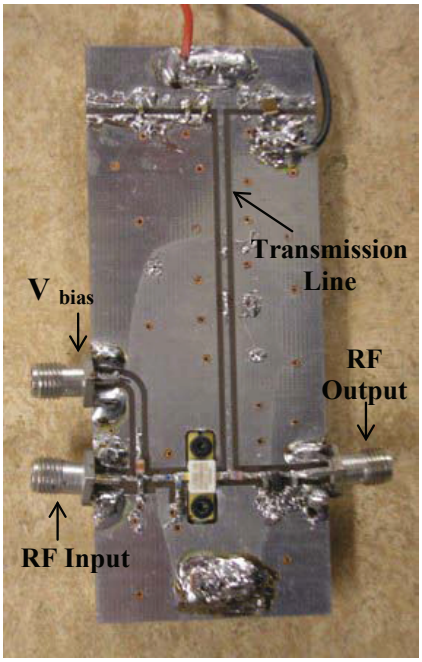

Figure 2.6: The PCB with the transmission line inductance and I/O ports indicated.

the PWM like signal at the drain of the device has a reduced slew rate because of the limited gain of the device. This is particularly so for small conduction angles, when conduction occurs at the peak of the sine wave. The device is operating more like a class C amplifier in this region (conduction angles less than 50%). Efficiency will not be as high as that of (Fig. 2.4).

The full amplifier including matching networks is implemented using surface mount components on a standard FR4 printed circuit board (PCB), with double sided copper layers as illustrated in Fig. 2.6. The inductor at the drain of the device is implemented using a transmission line. The device is a CREE CGH40010 discrete GaN high electron mobility transistor (HEMT) device suitable for high output power (10 W). The carrier frequency was 395 MHz and a high-power input signal was used (23 dBm), since the PA was to operate in switch-mode.

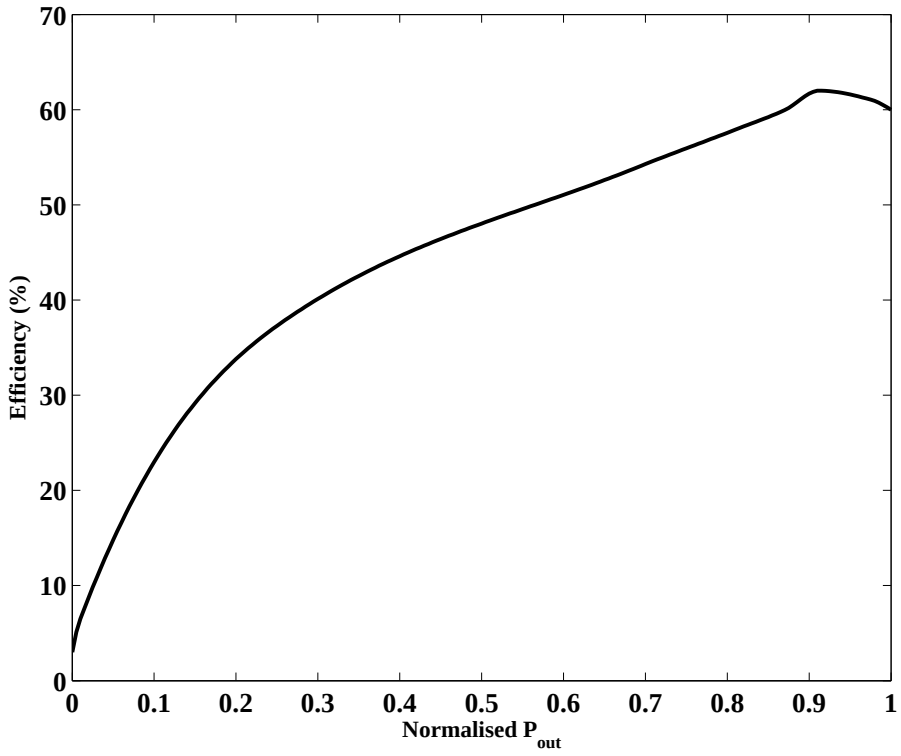

Figure 2.7: Efficiency against power output. PWM curve is for V_{dd}= 30 V. P_{out} is normalised to peak output power of 39.6 dBm.

In Fig. 2.7, the plot shows the efficiency versus normalised output power for both architectures. The power is normalised to the amplifiers peak output power; in this case 39.6 dBm for V_{dd} = 30 V. The loss of efficiency at low output powers is consistent with PWM operation, where slew-rate losses are essentially constant whatever the pulse width (output power).

The peak to average power ratio (PAPR) of modern day modulations (CDMA/ OFDM) is between 6 dB and 8 dB [34] after crest factor reduction. Hence the efficiency of the practical amplifier is much reduced with these signals. The average normalised power is 0.25 for a 6 dB PAPR signal, and this gives an efficiency of

about 35%. This is still a reasonable figure, compared to today's amplifiers, but there is still plenty of room for improvement.

The next sub-section will describe two amplifier architectures that remove the need to modulate the pulse width of the drive signal. The amplifiers can be operated at their highest efficiency all the time

2.2.5 Envelope Elimination and Restoration

A polar transmitter scheme which has been widely investigated over the years is the EER which was first introduced by Kahn [35]. EER using switching amplifiers can achieve high efficiency for complex modulation schemes such as OFDM. A basic structure of EER is shown by Fig. 2.8. The input Cartesian signals are converted to polar equivalents. A limiter is used to eliminate the envelope and produce a constant amplitude phase modulated signal. The RF drive signal of the final output stage contains that phase information. An envelope detector is used to extract the amplitude information which is then amplified by a Class S amplifier and fed to the final stage by means of supply modulation [35]-[37]. A problem associated with the EER scheme is the delay mismatch between the amplitude and phase components which can lead to serious spectral expansion at the output [38]. A possible solution to avoid the time mismatch between the two paths is to delay the phase component [39].

Another major drawback of this scheme is the bandwidth expansion that is produced when the input signal is converted to polar. The Class S amplifiers have difficulties in tracking quickly changing voltages and are normally required to have a switching frequency ten times higher than the modulation bandwidth [40]. Larger

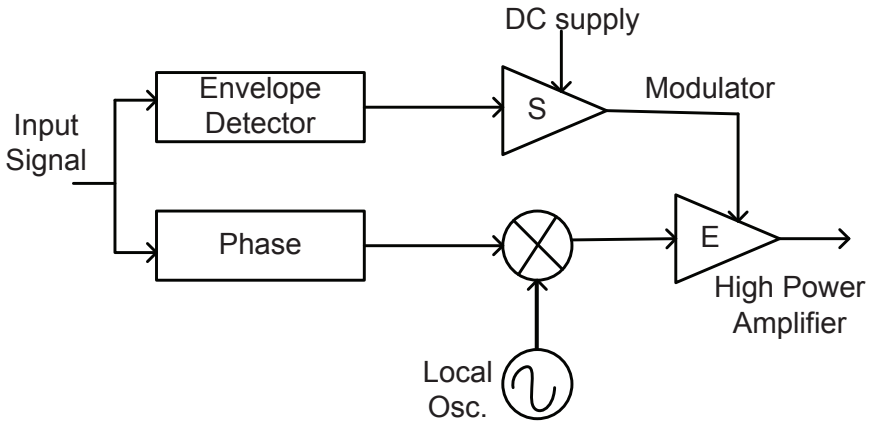

Figure 2.8: An EER transmitter architecture.

bandwidths put immense strain on the supply modulators.

Hole punching has been proposed as a possible solution to the polar bandwidth expansion problem. The idea behind the approach is to prevent the zero crossings of the Cartesian components by establishing a boundary [41]. Thus the phase components do not experience any rapid transition which normally requires a wide bandwidth to capture resulting in bandwidth expansion [27]. The hole punching technique leads to the generation of minimal adjacent channel power. However, substantial in-band distortion is produced leading to degradation in error vector magnitude (EVM). We quantify the trade-off between EVM and bandwidth expansion in [42].

At this stage, EER scheme is appropriate for input signals with limited envelope dynamic range and lesser bandwidth expansion such as $\frac{\pi}{4}$ shift quadrature phase-shift keying (QPSK) or Gaussian minimum shift keying (GMSK) [40]. However, these narrowband modulation schemes are not appropriate for upcoming wireless systems.

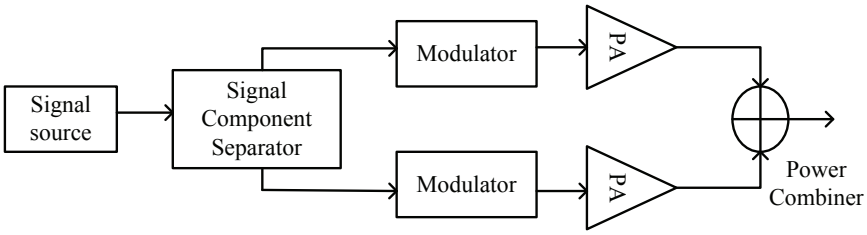

Figure 2.9: A LINC transmitter architecture.

2.2.6 LINC Transmitter Architecture

The amplification of amplitude-varying signals by non-linear SMPAs normally give rise to distortions. The distortions are generally intermodulation components of the signal and the intermodulation products are present both in-band and out-of-band.

Linear amplification of non linear components (LINC) is a method used to amplify signals with varying amplitudes using non-linear amplifiers without degradation by non-linear SMPAs [43]- [49].

Fig. 2.9 shows the operation of the LINC system. The signal component separator decomposes the original signal into two constant amplitude phase varying signals. The two signals are then amplified by highly efficient but non-linear amplifiers such as Class D or E. The last stage is the combining stage where the two signals constructively or destructively interfere to produce an amplified version of the input signal.

In [50], we characterise the LINC performance of a Class E amplifier. Traditional LINC analysis does not apply for a Class E amplifier since Class E is neither an ideal voltage nor current source. We propose a load-pull analysis to obtain its transfer characteristics and its efficiency performance. This load-pull analysis can be used

to characterise any amplifier class in a LINC scheme. Simulations using advanced design system (ADS) showed an efficiency of 81% was achievable when the Class E amplifier was operated in the LINC scheme. It was also found that switching losses account for more that 60% of the total losses.

Moreover, the practical implementation of LINC is not an easy task. The system is very susceptible to disparity in phase, delay and amplitude. It is therefore nearly impossible to achieve a perfect constructive or destructive recombination.

The goal of the thesis is to come up with an all digital drive circuit for SMPAs such as those discussed in this section (Section 2.2). As previously indicated in Section 1.5 synchronous digital circuits will produce quantisation noise. $\Sigma\Delta$ techniques can control the noise spectrum and will be discussed in the next section.

2.3 Sigma Delta Modulators

The $\Sigma\Delta$ technique has been in existence for many years but recent technological advances have made it more widespread. $\Sigma\Delta$ modulators use noise shaping and oversampling techniques to limit quantisation noise in the band of interest. The oversampling ratio of the $\Sigma\Delta$ modulator ($OSR_{\Sigma\Delta}$) needs to be much greater than one. The oversampling technique allows an input signal to be sampled in such a way that two adjacent samples are very similar. The error generated by the coarse quantiser will thus have a high degree of correlation. Hence the quantisation error can be predicted and subtracted from the data through a feedback loop. This process results in the noise shaping characteristics of the $\Sigma\Delta$ modulator [51]-[55]. Fig. 2.10

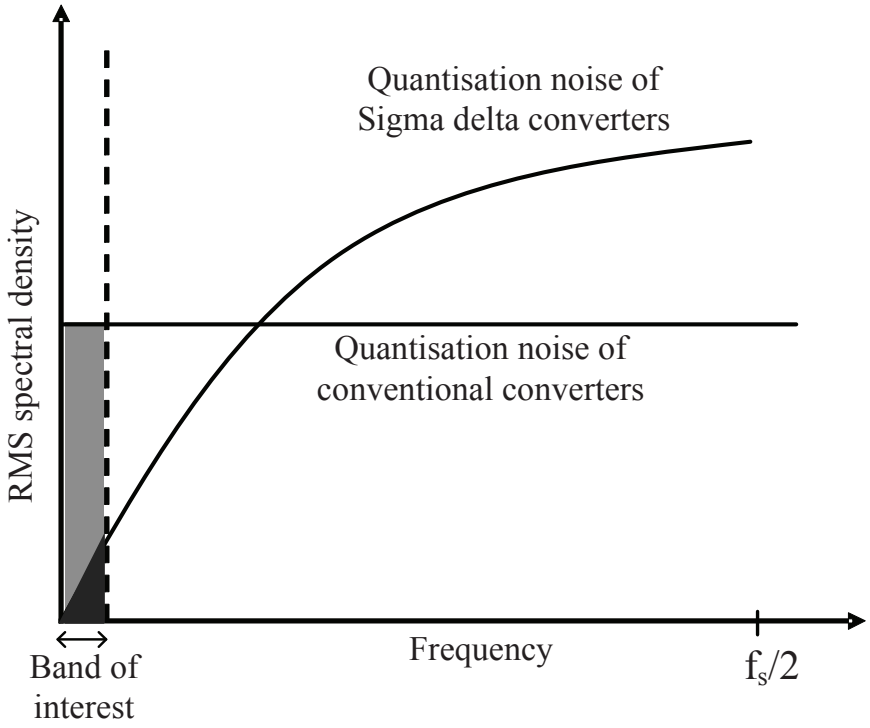

Figure 2.10: Showing the difference between conventional converters and ΣΔ converters. f_s is the ΣΔ sample rate.

shows the reduction in quantisation noise when using a ΣΔ converter compared to a conventional converter. The concept of ΣΔ modulation has contributed to the improvement of many components (such as high performance analog to digital converters (ADCs) and digital to analog converters (DACs)) leading to a higher degree of integration enjoyed by current wireless transceivers.

2.3.1 Linear ΣΔ Model

A basic lowpass ΣΔ model can consist of a subtraction node, a discrete-time integrator and a quantiser as shown in Fig. 2.11. An integrator is used in this architecture as it possesses the appropriate transfer function needed to suppress the quantisation

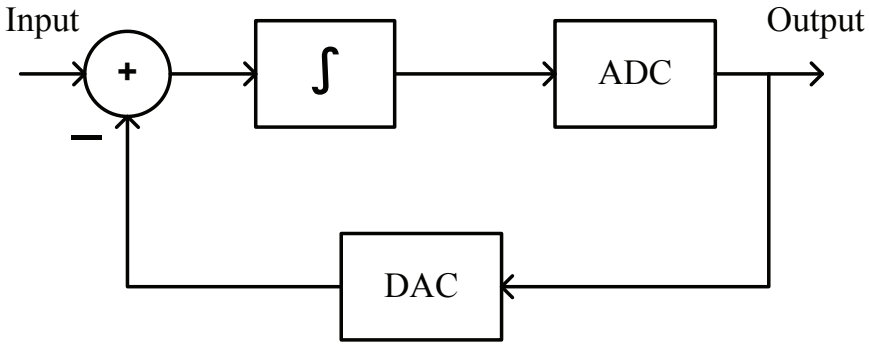

Figure 2.11: A non-linear ΣΔ modulator.

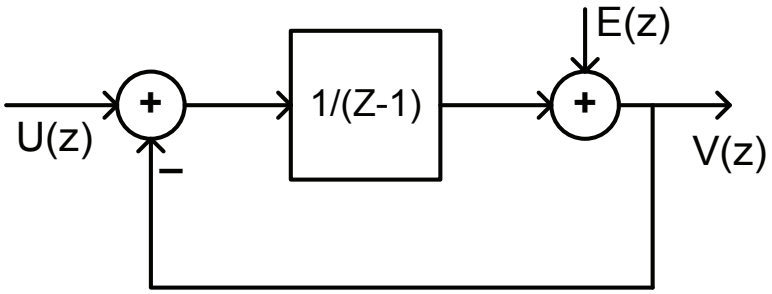

Figure 2.12: A linear z-domain model of a ΣΔ modulator.

noise at baseband. The integrator provides an infinite gain at DC. A ΣΔ modulator is considered to be both non-linear and dynamic because of the presence of the quantiser and the integrator respectively. The ΣΔ modulator is normally linearised to ease the mathematical analysis. The quantiser can be approximated to a white additive noise source, $E(z)$, provided it satisfies a few criteria [54]. One of the most significant criteria is that the input signal needs to be sufficiently small and thus never overloads. A linear z-domain model of the a lowpass ΣΔ is depicted in Fig. 2.12. The linear z-domain model can be further simplified as shown in Fig. 2.13. The integrator which has a transfer function of $\frac{1}{z-1}$ is replaced by a two loop feedback system with simple delays. Equations for the system can be easily derived by

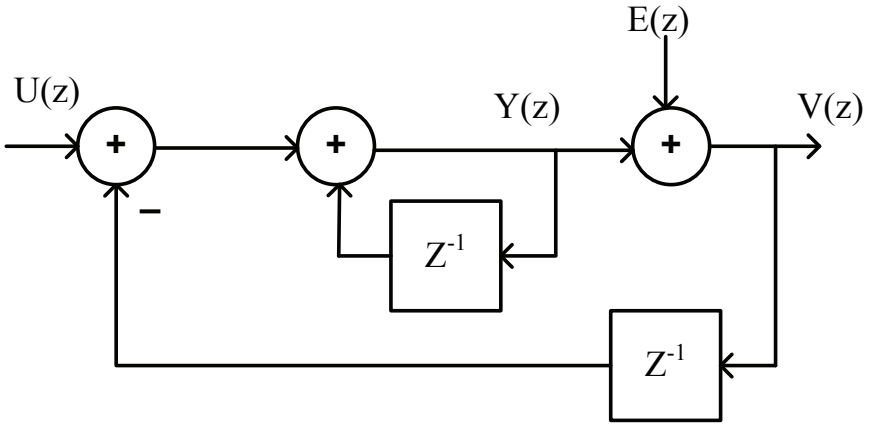

Figure 2.13: A linear z-domain model of a MOD1 [51] ΣΔ modulator.

analysing Fig. 2.13.

$$Y(z) = z^{-1}Y(z) + U(z) - z^{-1}V(z). \tag{2.1}$$

$$\begin{aligned} V(z) &= Y(z) + E(z), \\ &= z^{-1}Y(z) + U(z) - z^{-1}V(z) + E(z), \\ &= U(z) + (1 - z^{-1})E(z). \end{aligned} \tag{2.2}$$

$$V(z) = STF(z)U(z) + NTF(z)E(z). \tag{2.3}$$

For further simplification, the terms signal transfer function (STF) and noise transfer function (NTF) are introduced. The STF is unity and therefore no filtering occurs. The NTF is $1-z^{-1}$ and the noise is high pass filtered. The characteristic of the NTF can be further illustrated by the use of a pole-zero diagram. The zeros of the NTF are located on the unit circle at DC as shown in Fig. 2.14 causing the quantisation noise to be attenuated around that region.

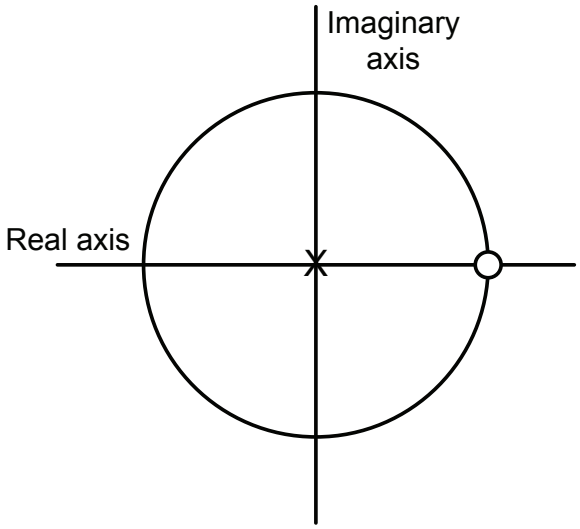

Figure 2.14: Pole/zero diagram of a lowpass ΣΔ modulator.

The square of the magnitude of the NTF in the frequency domain is calculated in order to estimate the in-band power of the quantisation noise as shown below.

$$\begin{aligned} NTF(e^{j\omega}) &= (1 - e^{-j\omega})^2, \\ &= (1 - cos\omega - jsin\omega)^2, \\ &= 2 - 2cos(\omega), \\ &= 4sin^2(\pi f). \end{aligned} \tag{2.4}$$

$$NTF = (2sin^2(\pi f))^2. \tag{2.5}$$

When $f = 0$, the NTF given by (2.5) is also zero. The NTF grows as frequency increases. This causes the noise to increase and is a potential source of interference to adjacent channels. It is quite clear from (2.5) that the quantisation noise is filtered away from DC. This is a highly desirable feature as in a lowpass ΣΔ configuration, the signal is present in the low frequency regions.

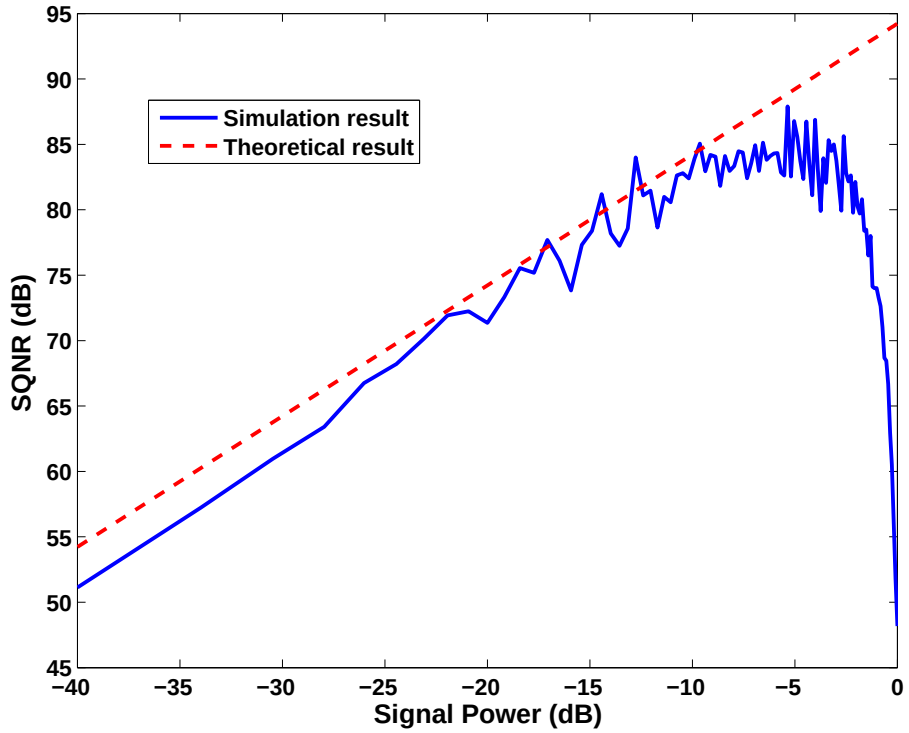

Figure 2.15: A plot showing the SQNR with varying signal power (u_{rms}=1) for MOD-1 ΣΔ with output levels +1,-1. The input signal is a sine wave.

2.3.2 Derivation of Signal to Quantisation Noise Ratio for MOD1 ΣΔ

As mentioned earlier in this chapter, the quantisation error is treated as a white additive noise. The noise power, σ_e^2, is given by $\frac{\Delta^2}{12}$ where Δ is the step size of the linear quantiser [51]. The one-sided power spectral density, $S_e(f)$, is given by $2\sigma_e^2$ (where the sample rate has been normalised to unity). The in-band noise power, σ_q^2, in the output is given by integrating the product of $S_e(f)$ and the NTF given by (2.5). The integration is performed from DC to half the normalised bandwidth

which is given by $\frac{1}{2(OSR_{\Sigma\Delta})}$.

$$\begin{aligned}\sigma_q^2 &= \int_0^{\frac{1}{2(OSR_{\Sigma\Delta})}} (NTF)^2 S_e(f) df, \\ &= \frac{4(\pi)^2 2\Delta^2}{12} \int_0^{\frac{1}{2(OSR_{\Sigma\Delta})}} f^2 df, \\ &= \frac{\pi^2 \Delta^2}{36(OSR_{\Sigma\Delta})^3}. \end{aligned} \tag{2.6}$$

In this derivation, the step-size, Δ, of a 1-bit quantiser is assumed to be 2 [51].

$$\sigma_q^2 = \frac{\pi^2}{9(OSR_{\Sigma\Delta})^3}. \tag{2.7}$$

The peak amplitude of a sine wave is denoted by A_m. Since the STF is unity, the output signal power is given by

$$\sigma_u^2 = \frac{(A_m)^2}{2}. \tag{2.8}$$

The signal to quantisation noise ratio (SQNR) is the relationship between the signal and the quantisation noise. The SQNR for a MOD-1 lowpass $\Sigma\Delta$ is given by

$$SQNR = \frac{\sigma_u^2}{\sigma_q^2} = \frac{9(A_m)^2(OSR_{\Sigma\Delta})^3}{2\pi^2}. \tag{2.9}$$

Fig. 2.15 shows plots of input power against SQNR. The figure contains a theoretical plot obtained from (2.9) and a simulated plot. The simulated curve follows the theoretical curve except for large values of input power. When the input power lies near the quantiser range boundary or is excessively high, the quantiser overloads. This results in the generation of spurious tones and a degradation in the SQNR [54]. An

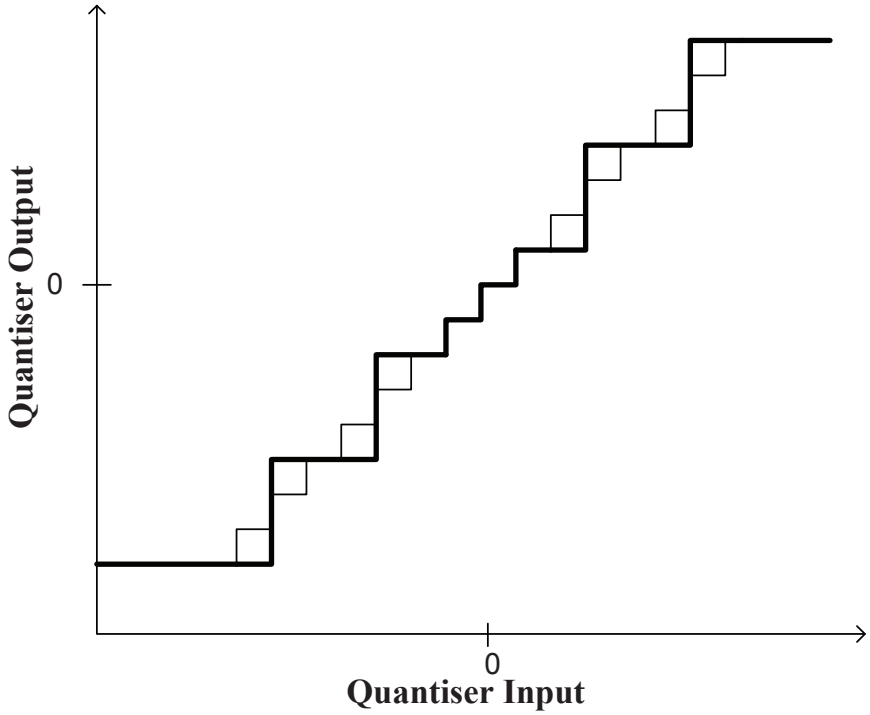

Figure 2.16: Quantiser input and output of a 4-bit uniform quantiser (thin lines) and a 3-bit non-uniform quantiser (thick lines).

increase in the difference between the theoretical and simulated SQNR is expected.

2.3.3 Non-Uniform Quantisation

A uniform quantiser is appropriate for signals with uniform distribution. However, signals with non-uniform probability density function (PDFs) require non-uniform quantisers for optimum quantisation. The input range is divided in unequal intervals. Depending on the PDF of the input signal, the threshold levels of the quantiser can be more densely located for some values of the input signals and more coarsely for others.

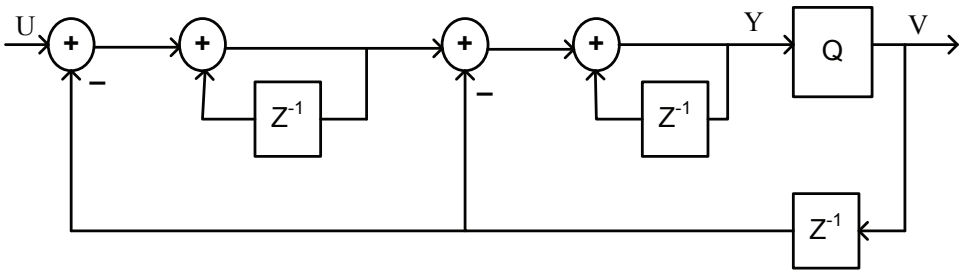

Figure 2.17: A linear z-domain model of a MOD-2 ΣΔ modulator.

In [56]-[58], non-uniform quantisers are used for input signals which can be approximated to Gaussian signals. Since such a signal is more likely to have small amplitudes, the quantiser is designed to have smaller quantisation steps around that region. For uncommon larger input values, the quantisation steps are larger. Fig 2.16 shows a non-uniform quantiser (3-bit) superimposed on a uniform one (4-bit). SQNR results in [56] show that the 3-bit non-uniform quantiser outperforms the 3-bit uniform quantiser. It is also shown that the 3-bit non-uniform quantiser and a 4-bit uniform quantiser produce similar SQNR results.

2.3.4 Higher Order ΣΔ Converters

Higher order converters can be used to obtain a better noise shaping effect. They are designed by cascading the MOD-1 architectures discussed in earlier paragraphs. Fig. 2.17 shows a second order ΣΔ modulator(MOD-2 [51]) which is essentially a MOD-1 ΣΔ with an additional integrator and another feedback path.

The SQNR is improved by the new NTF. However, the improved noise shaping characteristics of the higher order ΣΔ are achieved at the expense of increased complexity, instability and a steeper increase in the noise spectrum which puts

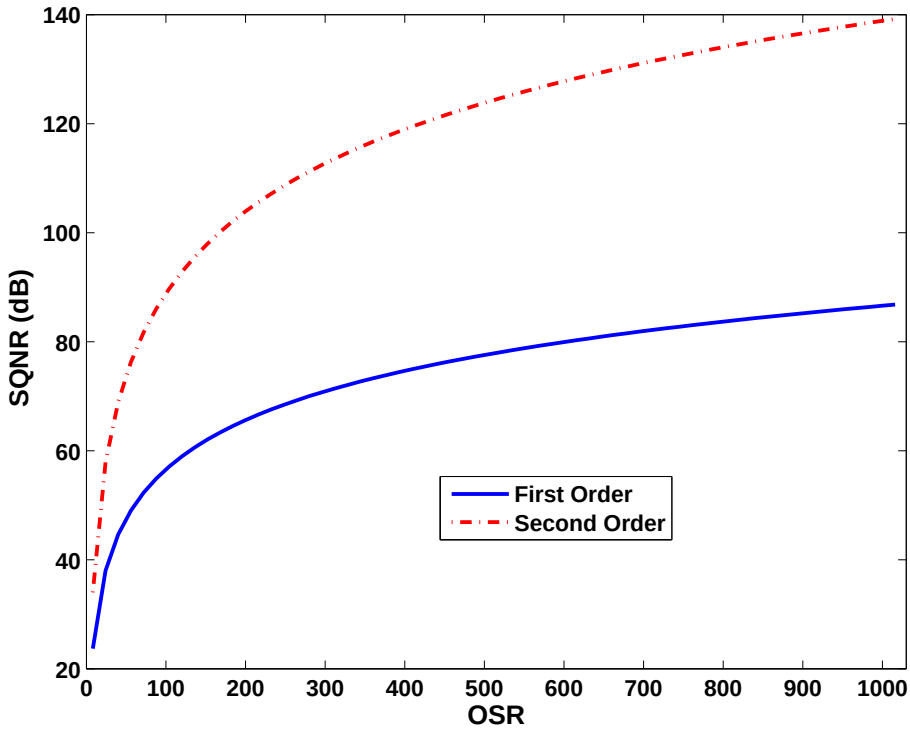

Figure 2.18: The effect of $OSR_{\Sigma\Delta}$ on SQNR for MOD-1 and MOD-2 $\Sigma\Delta$ modulators.

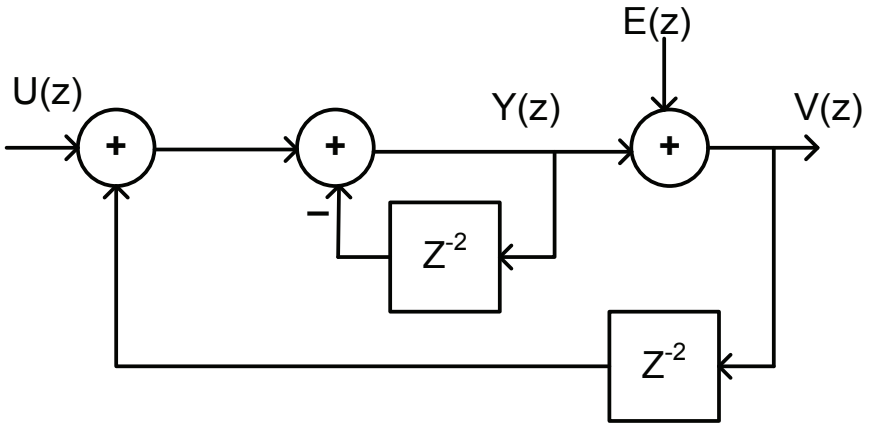

Figure 2.19: A linear z-domain model of a bandpass ΣΔ modulator.

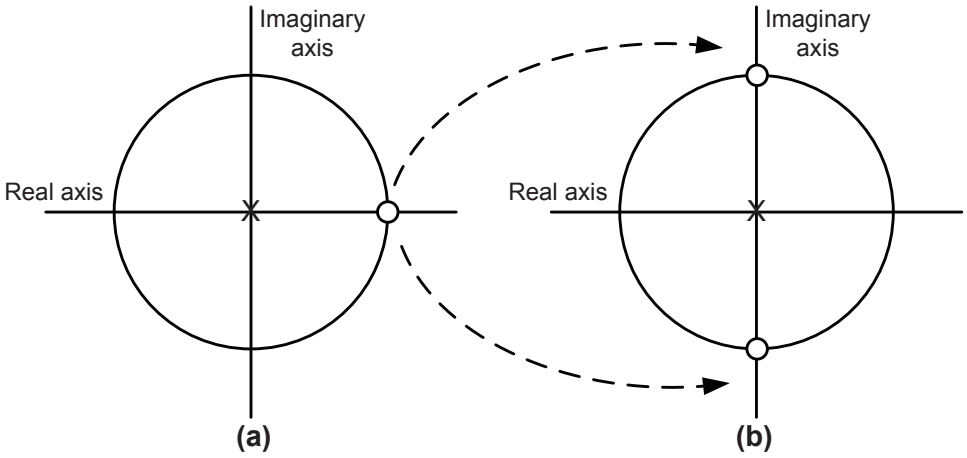

Figure 2.20: Pole/zero diagram of the NTF of (a) first-order lowpass and (b) second-order bandpass ΣΔ modulator.

additional pressure on the output bandpass filters.

The SQNR can also be further increased by increasing $OSR_{\Sigma\Delta}$. Fig. 2.18 shows the improvement in SQNR as $OSR_{\Sigma\Delta}$ increases for MOD-1 and a MOD-2 architectures. It can be observed that a higher $OSR_{\Sigma\Delta}$ is needed to achieve the same SQNR in MOD-1 compared to MOD-2, making MOD-2 a more practical choice as the sampling frequency is lower.

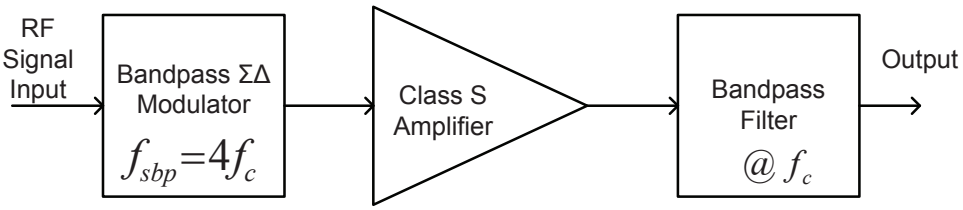

Figure 2.21: A bandpass ΣΔ architecture.

2.3.5 Bandpass ΣΔ Modulators

Analysing lowpass ΣΔ is essential to understand the concept of ΣΔ. However, lowpass ΣΔ applies to signals at DC. Signals at radio frequencies are needed for most communication systems. For a bandpass modulator, the highpass characteristic of the NTF has to be replaced by the bandstop transfer function [59]-[61]. The most common method to design a bandpass ΣΔ modulator is to perform a simple mathematical transformation on a suitable lowpass ΣΔ. It is called a DC to $f_{sbp}/4$ transformation and it requires the z^{-1} in the transfer function to be replaced by $-z^{-2}$ [51]. f_{sbp} is the sampling rate of the bandpass ΣΔ. Fig. 2.19 shows the linear z-model of a MOD-2 bandpass ΣΔ.

The number of zeros in the NTF of the lowpass ΣΔ is doubled and the zeros are rotated in the z-plane from $z = 1$ to $z = j$ as illustrated by Fig. 2.20. In the frequency domain, the noise suppression region shifts from DC to $f_{sbp}/4$. The system block diagram of a bandpass ΣΔ is shown in Fig. 2.21.

Fig. 2.22 shows the spectrum plot of a 20 MHz OFDM signal after it has been modulated by a fourth-order bandpass ΣΔ converter. The null is no longer at DC, it is now situated at $f_{sbp}/4$. A blow-up of the same spectrum is shown in Fig. 2.23. The

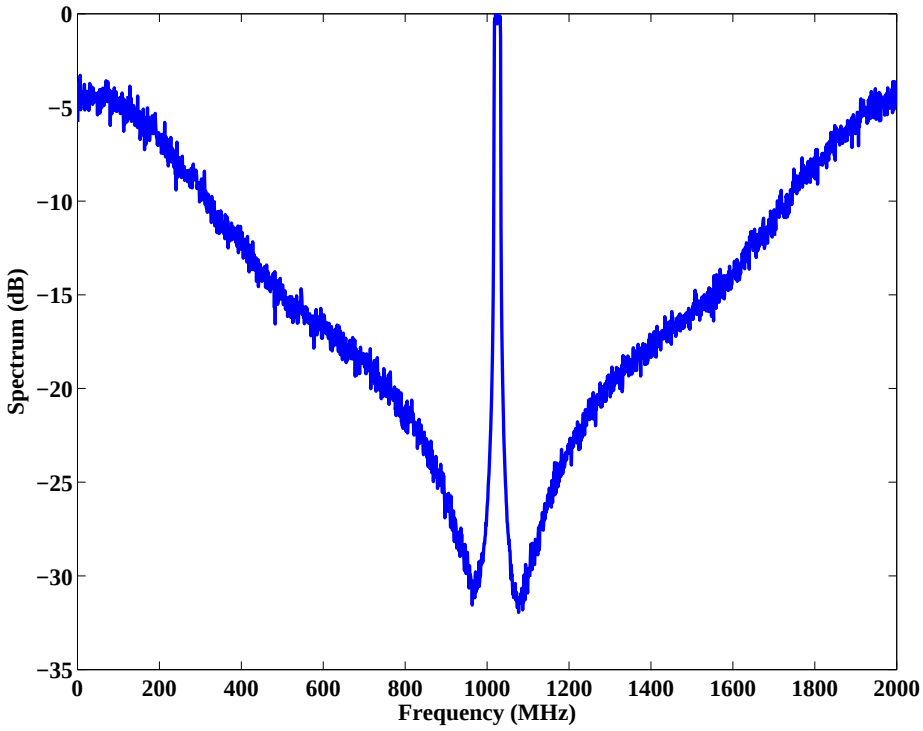

Figure 2.22: Spectrum of the output of a bandpass ΣΔ. f_{sbp}=4 GHz, f_c= 1.024 GHz, OFDM input signal level= -12 dB (u_{rms}=1).

noise in the two immediate adjacent channels are calculated and given by ACP(1) which is -23.7 dB and ACP(2) which is -30.4 dB. The ACPs are defined as the noise power in the adjacent channel divided by the signal power. This bandpass ΣΔ is a few dB short of the WLAN specification.

The next section will show how ΣΔ can be used in upconverter circuits for SMPAs.

2.4 Sigma Delta-Based Transmitter Architectures

ΣΔ waveforms are generally of the 'on'/'off' type. Such signals can be used to control the amplifier operation. There are two major approaches, burst mode and

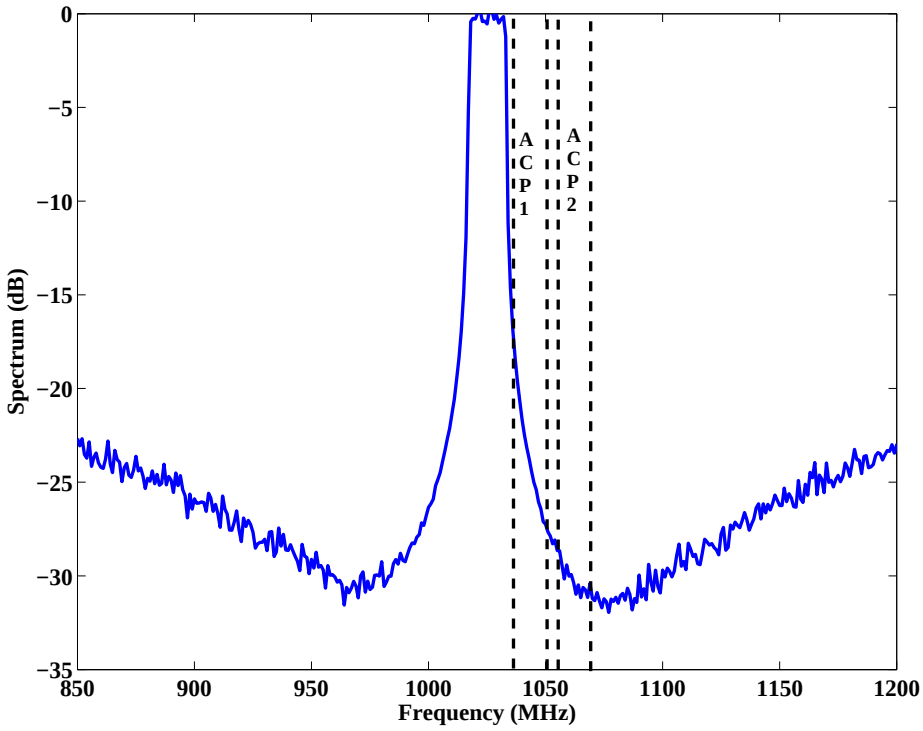

Figure 2.23: Zoom-in view of spectrum ((u_{rms}=1)) (Fig. 2.22) of the output of a bandpass ΣΔ. ACP(1) and ACP(2) are shown.

cycle mode.

2.4.1 Burst Mode Operation

Burst mode was first used in the early 1970s in a ultra high frequency (UHF) rescue radio. This mode produces a series of 'on' and 'off' bursts as shown by Fig 2.24. The amplitude of the signal is determined by the burst width. The bursts need to be an integer number of carrier cycles. The smallest burst size is 1 period (or $1/f_c$ seconds, equal to 1 ns at 1 GHz carrier frequency). To achieve an amplitude control range (CR) of 40 dB, the number of blank cycles, B_L, between each burst would

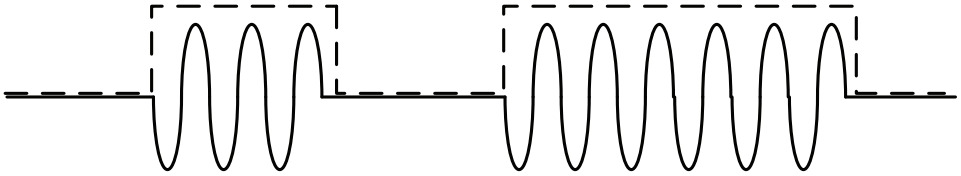

Figure 2.24: Diagram showing burst mode operation.

need to be

$$B_L = 10^{\frac{CR}{20}} - 1, \text{here } (=99). \tag{2.10}$$

Hence causing the minimum burst rate, $Burst_{min}$ of

$$Burst_{min} = \frac{f_c}{(B_L + 1)}, \text{here } (=10 \text{ Mbursts/s}), \tag{2.11}$$

that would limit the modulation bandwidth << 10 MHz. The scheme is therefore unlikely to meet the whole of band requirements of 100 MHz, but could meet the 20 MHz channel bandwidth particularly for the higher frequency cellular bands. The advantage of the scheme is that the $\Sigma\Delta$ clock frequency is at or below the carrier frequency.

An example of burst mode operation is given in [70]. After the $\Sigma\Delta$ filtering process, the outputs are discretised and converted to polar. The outputs are a one-bit amplitude signal and two modulated phase signal as shown in Fig 2.25(a). The one-bit amplitude signal is used to turn the switching power amplifier 'on' or 'off' through drain supply or gate control. The modulated phase signals control the phase modulator to perform constant envelope phase modulations as shown in Fig 2.25(b). An RF carrier input is still required and therefore the scheme does not fully eliminate the need for analog components such as the IQ modulator and the RF local oscillator.

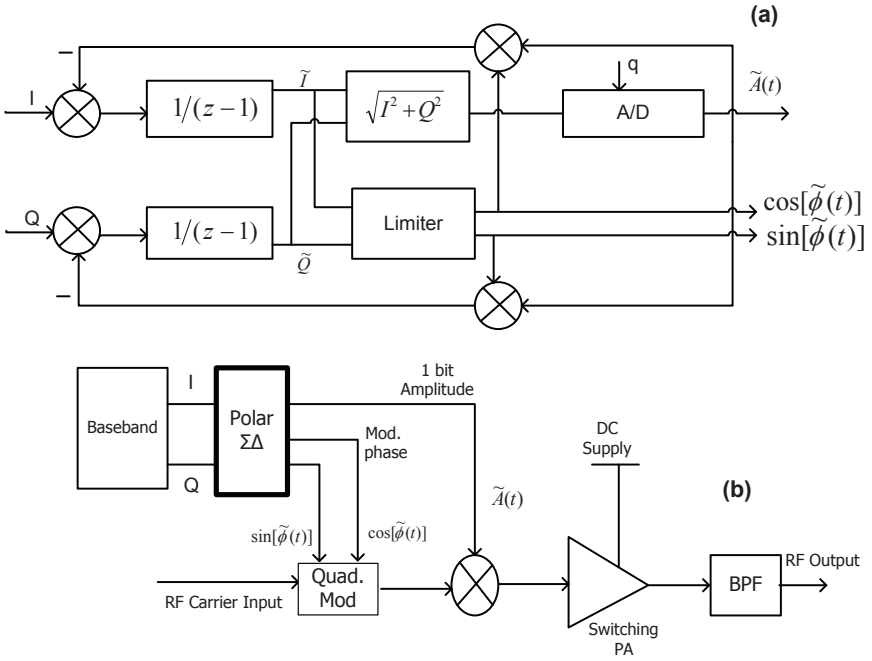

Figure 2.25: (a)Block diagram of the polar ΣΔ modulator of [70] (b)The transmitter architecture [70].

2.4.2 Cycle Mode Operation

Cycle mode architectures control each individual cycle of the RF signal. If an all-digital transmitter is to be developed, the clock frequency must be higher than the carrier frequency to enable different pulse widths.

In the late 90s, bandpass ΣΔ modulators were proposed as a possible solution to enable the use of SMPAs [62]-[65]. As seen from the block diagram in Fig. 2.21, an RF signal is converted to a digital pulse train by the bandpass ΣΔ modulator. The binary signal is then fed to the non-linear but efficient Class-S PA. The bandpass ΣΔ modulators also shape the quantisation noise and hence ease the requirements of the bandpass filter at the output of the Class-S amplifier. This system was a good solution as it provided high efficiency and high linearity with minimum analog

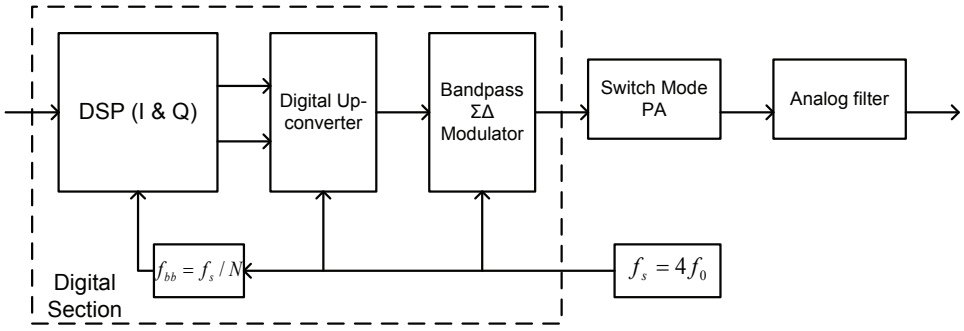

Figure 2.26: The bandpass ΣΔ proposed in [66].

components. In [66], a digital method to generate the RF signals is proposed as shown in Fig. 2.26. The baseband frequency used is a sub-multiple of the sampling frequency. If the sampling frequency is four times the carrier frequency, the up-conversion operation is performed by multiplying the baseband I and Q signals by the pulse sequences $1, 1, -1, -1 \ldots$ and by $-1, 1, 1, -1 \ldots$ respectively.[1] The two resulting signals are summed. The net effect is the DSP equivalent of a quadrature modulator. The output of which can be fed directly into bandpass ΣΔ filters. This is an all-digital process.

However, the up-conversion and bandpass ΣΔ modulators are operating at a very high sampling frequency (typically four times the RF carrier frequency). At present, DSP circuits operating at such high clock rate require substantial power consumption leading to a degradation in efficiency [67].

In an attempt to lower the clock frequencies, researchers in [68, 69], moved the up-conversion to after the ΣΔ modulation, effectively replacing the bandpass ΣΔ with two lowpass ΣΔs. The sample rate reduction in [69] was more aggressive

[1] These sequences represent sampled versions of $\cos(2\pi \frac{f_c}{4f_s} n)$ and $\sin(2\pi \frac{f_c}{4f_s} n)$ respectively where n is the sample number.

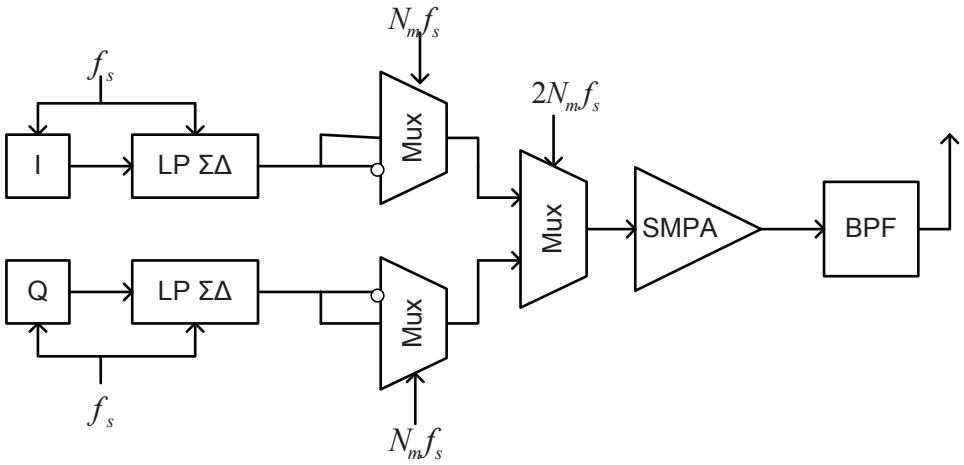

Figure 2.27: The proposed transmitter architecture of [69].

leading to a continuous burst mode operation and the DSP load was further reduced (Fig. 2.27). The quantised output from the lowpass ΣΔs is effectively multiplied by a square-wave in the first set of multiplexers. The final multiplexer interleaves the two waveforms.[2] Only the multiplexers are operating at high sample rates while the ΣΔ operating frequency has been reduced by a factor $2N_m$ (Fig. 2.27).

However, lowering the sample rate also reduces the signal bandwidth by the same ratio. The bandwidth reduction was partially compensated for by increasing the effective order of the ΣΔ filters to produce multiple nulls in the band of interest. In the methods described in [68, 69], switching activity occurs at least once per RF period, even if the input signal is small or absent leading to an increase in SMPA switching activity.

Keyser et al. proposed a technique which reduces switching activity [17]. The technique is referred to as the polar ΣΔ throughout this thesis. The polar ΣΔ

[2]This is an alternative method to [69] for getting the cosine and sine functions by using the sequence 0,1,0,-1... and 1,0,-1,0... respectively.

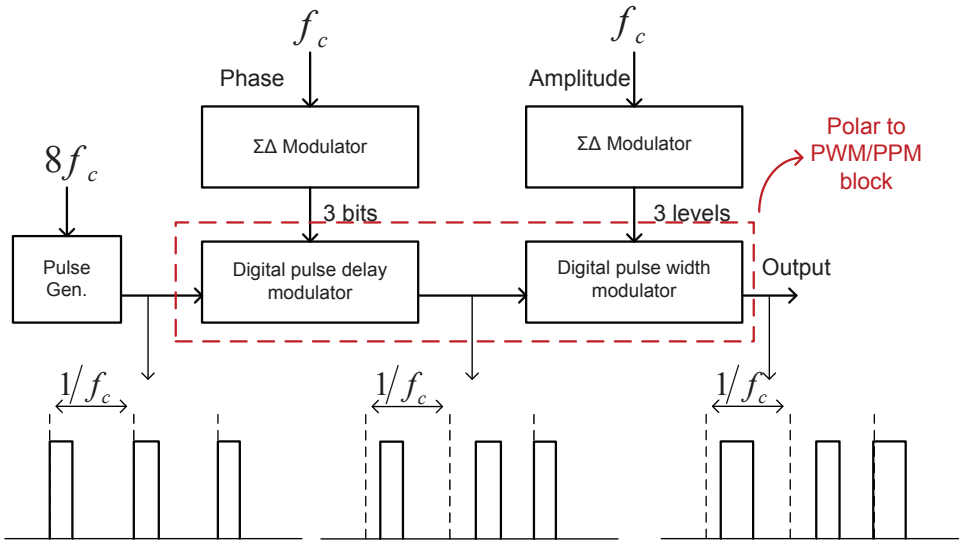

Figure 2.28: The polar ΣΔ transmitter architecture [17] showing the pulse train, pulse train with phase and pulse train with phase and amplitude.

consists of two lowpass ΣΔs operating on polar representations of the baseband signal, followed by an up-conversion block which performs polar to PWM and PPM operation. As shown in Fig 2.28, the phase is quantised into eight levels and the amplitude is quantised into three levels. The digital pulse delay modulator outputs a periodic pulse train positioned at one of the eight possible values. It is then fed to a digital pulsewidth modulator which selects a pulsewidth of $\frac{1}{8f_c}$, $\frac{3}{8f_c}$ or zero depending on the amplitude output of the ΣΔ. Moreover, this scheme limits the number of pulses to a maximum of one pulse per period of the RF carrier. Often there are no switching pulses when the input signal is small, thus limiting the power loss in the amplifier. Since this technique is an all-digital one, it opens the possibility for the direct generation of RF signals using a DSP-based structure and the integration of the entire architecture onto a single chip. Unfortunately, the input signal needs to be polar which is a bandwidth expanded signal because of the non-linear Cartesian to

polar transform, $R = \sqrt{I^2 + Q^2}$ and $\theta = tan^{-1}(\frac{Q}{I})$. The non-linear process causes some of the quantisation noise to fold back into the band of interest and hence cannot be filtered out. Moreover, since the $\Sigma\Delta$ filtering is performed on bandwidth expanded signals, the effective oversampling rate is reduced. Degradation of the signal to noise ratio (SNR) is observed leading to a limitation in the possible range of applications for this technique. This is one of the problems that will be addressed in the following chapters.

2.5 Summary

In this chapter, introductory material is proposed on SMPAs namely on Class D and on Class E PAs and measurement results are given for a GaN amplifier operating in an overdriven (switch-mode) state. The operation of switching amplifiers in LINC and EER is briefly discussed. EER has problems in meeting the bandwidth requirement on the envelope signal and LINC has many implementation problems in balancing the two branches as well as combining the two outputs. Next, the concept of $\Sigma\Delta$ modulators is explained and the equations for the STF and NTF are derived. The derivation of SQNR for a MOD-1 $\Sigma\Delta$ is also given. Higher order converters and bandpass $\Sigma\Delta$ converters are explained. Finally bandpass, polar and Cartesian $\Sigma\Delta$-based transmitter architectures from the literature are evaluated. The advantages and disadvantages of the different schemes are discussed. Bandpass $\Sigma\Delta$-based architectures are always switching, even when the signal is not present.

They generally require a clock frequency four times the carrier frequency. Polar architectures suffer from bandwidth expansion issues. Cartesian-based schemes, either have high switching activity, low bandwidth or need analog components to give a phase modulated RF carrier.

In the next chapter, a novel Cartesian $\Sigma\Delta$ scheme is presented. The aim of the proposed architecture is to provide a fully digital solution, ease the bandwidth expansion problems and reduce switching activity.

Chapter 3

Cartesian Sigma Delta Architecture

3.1 Introduction

After analysing different existing transmitter structures, the novel Cartesian ΣΔ architecture is proposed as a potential candidate for future wireless base stations [72]. It provides a power efficient all-digital solution and tackles the bandwidth expansion problem. It also converts multi-carrier input signals into RF pulse train waveforms which can drive SMPAs at maximum efficiency. The phase and amplitude information of the signal is embedded in the edges of the pulse train as shown by Fig 3.1. The output of the architecture produces a three-level waveform (1, 0, -1) with low

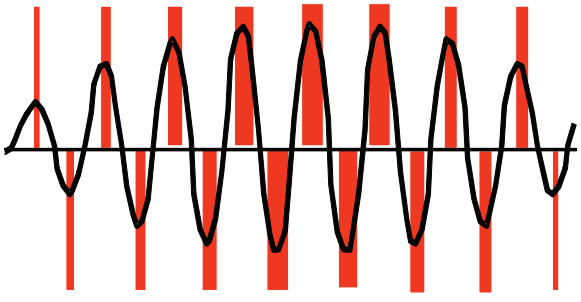

Figure 3.1: Three-level waveform with phase and amplitude information embedded in the edges of the pulse train.

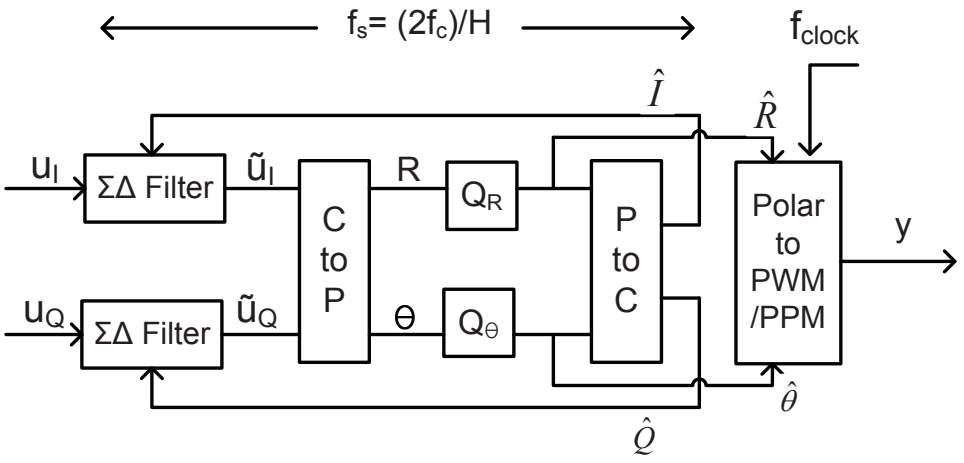

Figure 3.2: The proposed Cartesian ΣΔ architecture. 'C to P' refers to Cartesian to polar conversion and 'P to C' refers to polar to Cartesian conversion.

switching activity thus reducing the power loss in SMPAs. The Cartesian ΣΔ architecture is introduced in *IET Electronics Letters* titled 'Sigma-Delta Digital Drive Signals for Switch Mode Power Amplifiers' [72]. Additional work presented in this chapter has been published in the *EURASIP Journal on Wireless Communication and Networking* titled 'A Potential Transmitter Architecture for Future Generation Green Wireless Base Station' [33]. In this chapter, Section 3.2 describes the proposed architecture and the sub-blocks are examined thoroughly. The effect of a gain term on efficiency and noise performance of the Cartesian ΣΔ is investigated in Section 3.3. A comparison of the spectrum and the effect of oversampling factor on the Cartesian and polar ΣΔ is presented in Section 3.4.

3.2 The Cartesian Sigma-Delta Architecture

The Cartesian ΣΔ architecture shown by Fig. 3.2 is an improvement over the polar ΣΔ modulator of [17] which was discussed in Section 2.4. The main objective is to

eliminate the bandwidth expanded signals from the ΣΔ process. This is achieved by moving the non-linear Cartesian to polar conversion of [17] to the output of the ΣΔ filters. This Cartesian structure performs ΣΔ filtering on individual u_I and u_Q Cartesian signals. After ΣΔ filtering, the $\tilde{u}_I$ and $\tilde{u}_Q$ signals are then converted to polar coordinates $[R, \theta]$ and separately quantised in blocks Q_R and Q_θ. The output of the quantisers $[\hat{R}, \hat{\theta}]$ are converted to pulse widths and pulse positions in the 'polar to PWM/PPM' block. Moreover, the output of the quantisers $[\hat{R}, \hat{\theta}]$ is converted back to Cartesian coordinates $[\hat{I}, \hat{Q}]$(removing bandwidth expansion) [28] and fed as feedback to the ΣΔ filters. The output of the 'polar to PWM/PPM' block is a pulse train to be fed directly to the SMPA and band-pass filtered to remove the quantisation and out-of-band distortion products. The three main blocks in the Cartesian ΣΔ design are discussed in detail below, starting from the output.

3.2.1 Polar to PWM/PPM Converters

The 'polar to PWM/PPM' block is responsible for upconverting the output of the quantisers to RF. Fig. 3.3 demonstrates the principle of pulse width and pulse position modulation. The quantised phase, $\hat{\theta}$, determines the pulse position. A change in phase is represented by a change in position and the pulse edges must occur on the digital timing grid. This method helps to maintain the synchronous nature of this all-digital architecture. The quantised amplitude, $\hat{R}$, determines the pulse duration [17].

Fig. 3.4 explains the process employed in this work to convert $\hat{R}$ to pulsewidth.

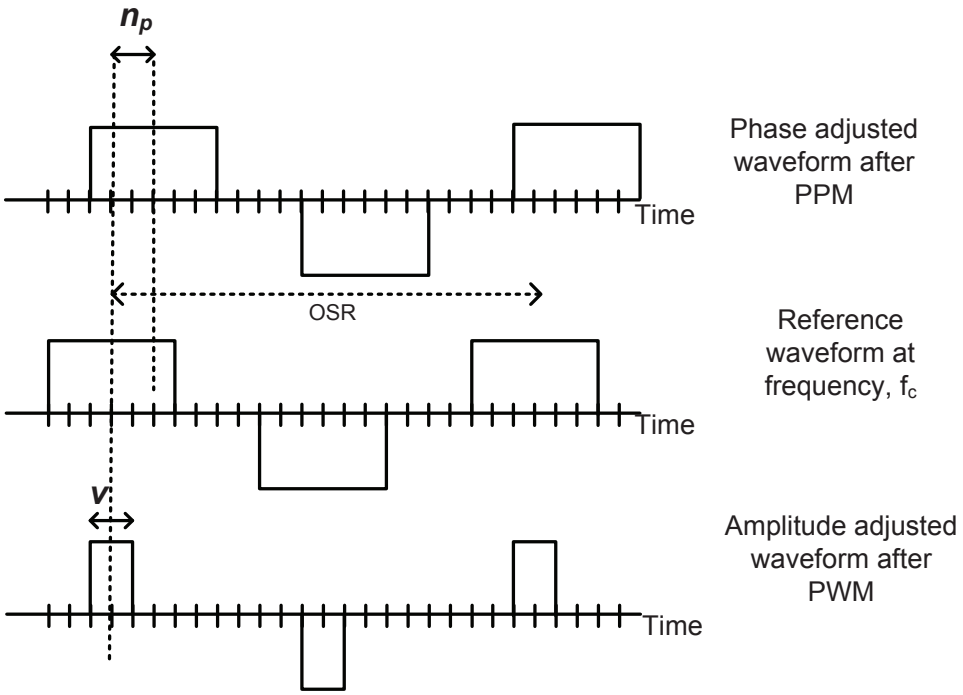

Figure 3.3: Demonstrating PWM (amplitude modulation) and PPM (phase modulation) concept. Edges occur on the digital timing grid. v is the pulse width. n_p refers to the time delay or advance. $f_c = \frac{f_s}{OSR}$.

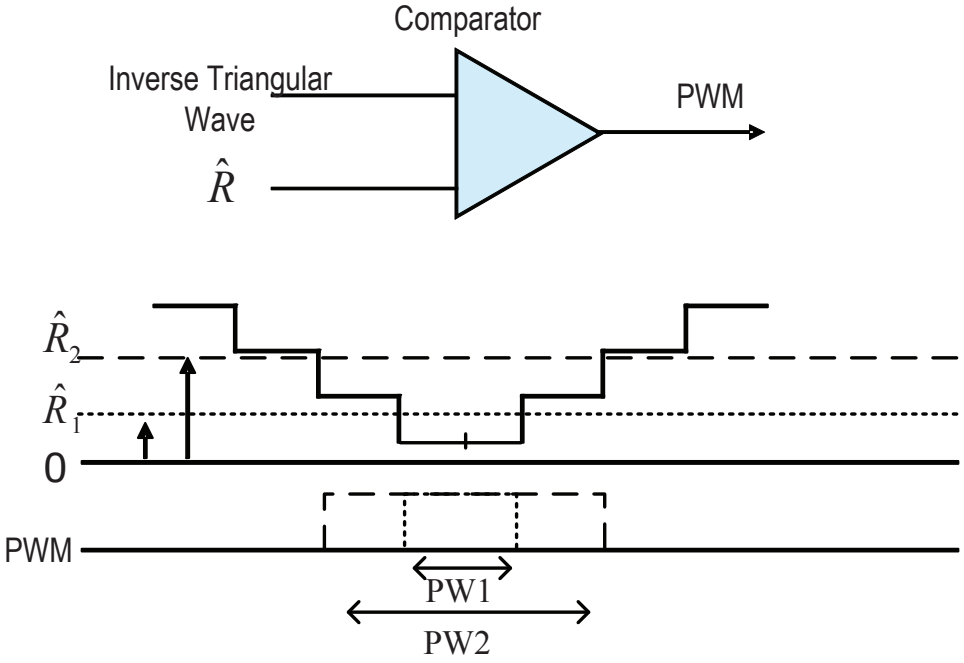

Figure 3.4: Illustrating PWM generation.

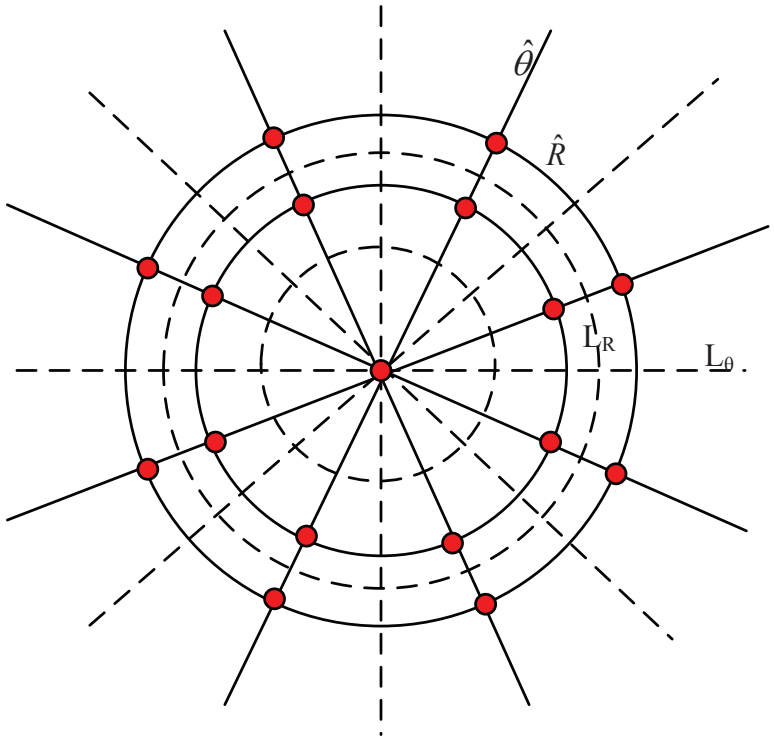

Figure 3.5: An example of the polar quantisation plane with N_A=3 and N_P=8.

Two examples are shown: quantised amplitude $\hat{R}_1$ and $\hat{R}_2$. The quantised amplitudes are compared to an inverted stepped triangular wave. The output pulsewidths, $PW1$ and $PW2$, are of the same width as that of the stepped triangular wave corresponding to comparator inputs of $\hat{R}_1$ and $\hat{R}_2$ respectively. The pulsewidths have two sample increments in order to decouple the amplitude response from the phase response, avoiding an amplitude modulation (AM) to phase modulation (PM) conversion, and so simplifying the quantisation process.

3.2.2 Non-uniform Polar Quantisers

As mentioned before, the filtered u_I and u_Q signals are converted to polar and quantised in block Q_R and Q_θ. The polar amplitude levels corresponding to the

permitted pulse widths are not linearly spaced. They need to be computed. In [73] the n^{th} harmonic amplitude of a two-level (1,0) repeating pulse waveform is given by

$$A_{\text{\_twolevel}}(n) = \frac{4}{n\pi} sin(nd_r\pi). \tag{3.1}$$

where d_r refers to the duty ratio of the pulse. However, in this work, a three-level waveform (Fig. 3.6) is used as it has many advantages and these will be discussed in Section 3.3. The method for calculating the amplitude of the first harmonic is explained in the next sub-section.

The quantiser of the proposed Cartesian $\Sigma\Delta$ architecture is shown by Fig. 3.5. The quantisation points are represented by the red dots. The dashed lines and circles represent the threshold levels of the quantisation points. The phase is uniformly quantised into N_P phase increments from zero to 2π. The quantised phase,

$$\hat{\theta} = n_p \frac{2\pi}{N_p} \quad \text{(rad)} \tag{3.2}$$

where $n_p = 0 \ldots N_p - 1$ and represents the PPM delay in clock periods. This quantisation process requires the system digital clock (f_{clock}) to oversample the nominal carrier frequency (f_c) by a factor of OSR (There are OSR clock periods in one cycle of f_c and OSR is equal to N_p.).

$$f_{clock} = OSR \times f_c. \tag{3.3}$$

$$OSR = N_P. \tag{3.4}$$

The amplitude, R, is quantised into N_A levels,

$$N_A = \left(\frac{OSR}{4} + 1 \right), \tag{3.5}$$

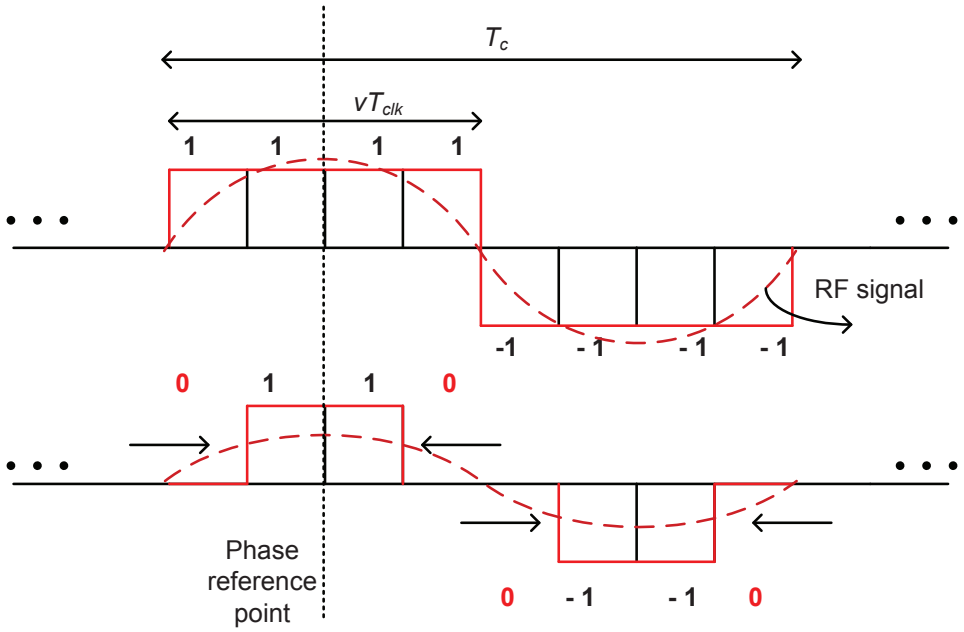

Figure 3.6: Quantisation amplitude level calculation. T_{clk} corresponds to the time period of system digital clock.

corresponding to pulsewidths having an even number of clock periods,

$$\left(0, \frac{2}{OSR}, \frac{4}{OSR}, \frac{6}{OSR} \cdots \frac{OSR/2}{2}\right) \frac{1}{f_c}.$$

3.2.2.1 Calculation of Threshold Levels and Quantisation Levels of the Amplitude Component

The amplitude and threshold levels are calculated by evaluating the fundamental spectral component of the repeating three-level waveform, $y(v, n_p)$ as shown in Fig 3.6. v is the pulsewidth in number of clock cycles and n_p is the pulse position (3.3). The pulse width is varied (by changing the pulsewidth in increment of two clock periods) to calculate the different RF envelope values, $\hat{R}$. The three-level pulse wave can be mathematically represented by

$$y_n(v, n_p) = \sum_{\alpha=-\infty}^{\infty} \text{rect}\left(\frac{(n_p + \alpha N_p)T_{clk}}{vT_{clk}}\right) - \text{rect}\left(\frac{(n_p + \alpha N_p - \frac{N_p}{2})T_{clk}}{vT_{clk}}\right) \quad (3.6)$$

where

$$\text{rect}\left(\frac{t_r}{\tau}\right) = u\left(t_r + \frac{\tau}{2}\right) - u\left(t_r - \frac{\tau}{2}\right) \tag{3.7}$$

and where $u(...)$ is a step function of amplitude 1.

Since $y(v, n_p)$ is a repeating waveform, the amplitude of the fundamental can be calculated from one period only using the discrete fourier transform (DFT).

$$Y_k(v, n_p) = \frac{1}{N_p}\text{DFT}(y_n(v, n_p)). \tag{3.8}$$

The amplitude of the fundamental of the pulse wave is given by

$$\hat{R}\left(\frac{v}{2}\right) = 2[|Y_k(v, n_p)|], \tag{3.9}$$

when $k = 1$. $(\frac{v}{2})$ is the index for the different pulse widths.

The decision threshold levels for the quantiser are given by the midpoint of two quantised levels,

$$L_R\left(\frac{v}{2}, \frac{v}{2} + 1\right) = \frac{R(\frac{v}{2}) + R(\frac{v}{2} + 1)}{2}. \tag{3.10}$$

3.2.2.2 Calculation of Threshold Levels for the Phase Component

The phase is uniformly quantised into OSR phase increments. The threshold level is midway between these increments. The threshold for the quantised phase is given by

$$L_\theta(n_p, n_p + 1) = (n_p + 0.5)\frac{2\pi}{OSR}. \tag{3.11}$$

3.2.3 Sigma Delta Filters

In this work, the $\Sigma\Delta$ filters used are second order lowpass $\Sigma\Delta$ filters (Fig. 3.7). This type of filter is generally referred to as MOD-2 [51] filters and they are simple to

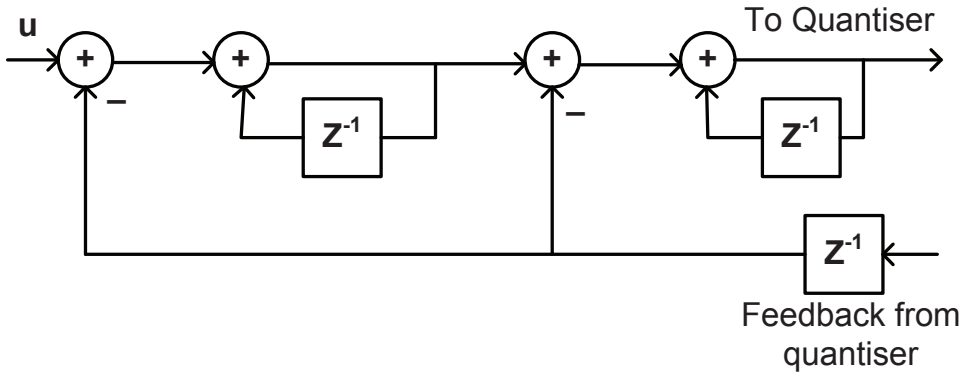

Figure 3.7: Second order lowpass ΣΔ modulator.

implement. In the Cartesian ΣΔ architecture, u_I and u_Q signals are each filtered by a MOD-2 filter. The feedback to the MOD-2 filters are obtained from the output of the polar quantisers after they are converted to Cartesian as shown by Fig. 3.2.

The ΣΔ filters operate at a sample rate, f_s, and it is common to define the ΣΔ oversampling rate, $OSR_{\Sigma\Delta}$ as

$$OSR_{\Sigma\Delta} = \frac{f_s}{BW} \tag{3.12}$$

where BW is the modulation bandwidth of the signal.

3.3 Output of the System

The output of the 'polar to PWM/PPM' block is a pulse train to be fed to the SMPA and band-pass filtered to eliminate quantisation noise and out-of-band distortion products. A second pulse train delayed by π (or OSR/2 clock cycles) on the first pulse train can be used for push/pull or bridge SMPA structures (Fig. 3.8). This gives an effective three-level waveform (1, 0, -1) at the amplifier output (Fig. 3.9). The pulse position and pulse width can therefore be updated for each half cycle of

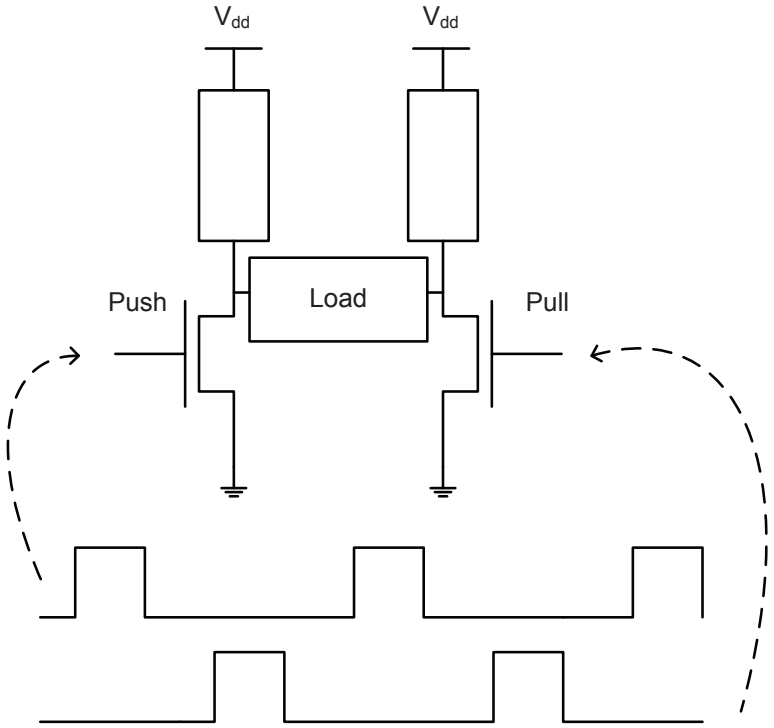

Figure 3.8: A push-pull amplifier structure.

the RF carrier, which sets the sampling rate of the ΣΔ circuits (f_s) at

$$f_s = 2\frac{fc}{H}, \tag{3.13}$$

where H is the number of half periods between each update of the ΣΔ circuits. The maximum sample rate occurs when H=1. Substituting (3.13) in (3.12),

$$OSR_{\Sigma\Delta} = \frac{2f_c}{BW \times H}. \tag{3.14}$$

Substituting (3.3) in (3.14),

$$OSR_{\Sigma\Delta} = \frac{2f_{clock}}{BW \times H \times OSR}. \tag{3.15}$$

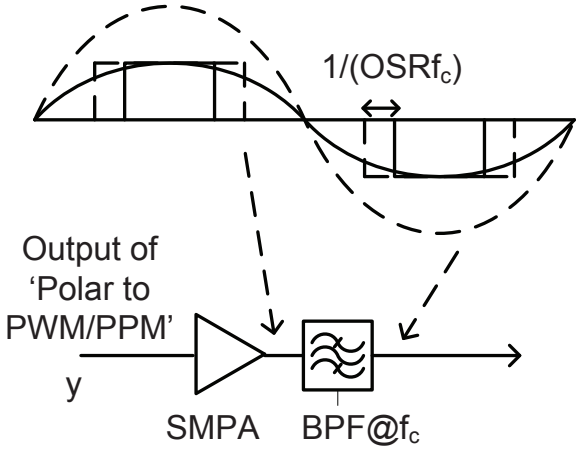

Figure 3.9: Output of system: PWM/PPM output of the SMPA is filtered to select the first harmonic (fundamental) at f_c.

3.3.1 Effect of Gain and Amplitude on Waveform and SMPA Efficiency

The 'polar to PWM/PPM' block is also responsible for producing an output drive signal with at most one pulse per half cycle. This highly desirable feature of the drive signal reduces the number of switchings in the SMPA compared to the bandpass $\Sigma\Delta$ structure. The transistor in a SMPA operates as a switch. When the switch is closed, current flows through the transistor and when the switch is open, voltage is present. In ideal conditions, the current and voltage never overlap in time. This assumption leads to a theoretical efficiency of a 100% [24]. However, in reality transistors cannot be modelled as ideal switches. Each switching of the transistor results in losses, and the 'on' state normally involves a finite resistance $R_{ds}(on)$. Therefore, the number of switchings in the drive signal for the SMPA needs to be minimised.

In this section, the activity of the amplifier is measured by using the utility factor. The utility factor is defined as the average number of samples per half

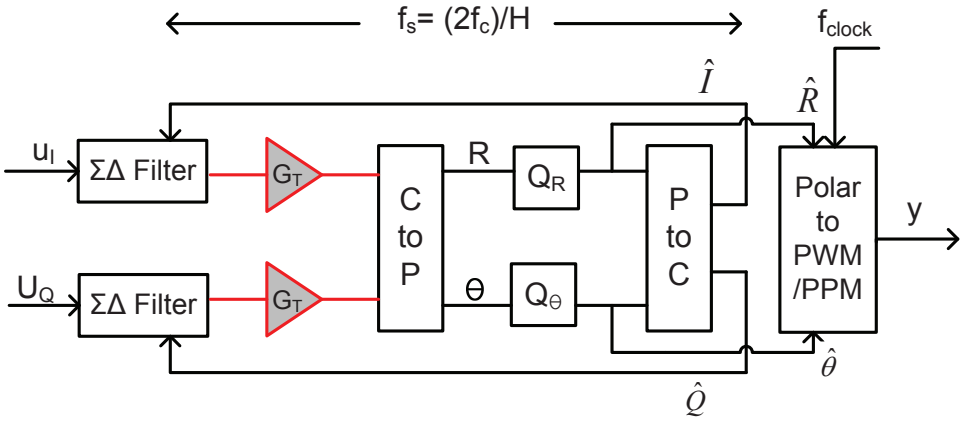

Figure 3.10: Block diagram of the Cartesian ΣΔ with a gain term, G_T.

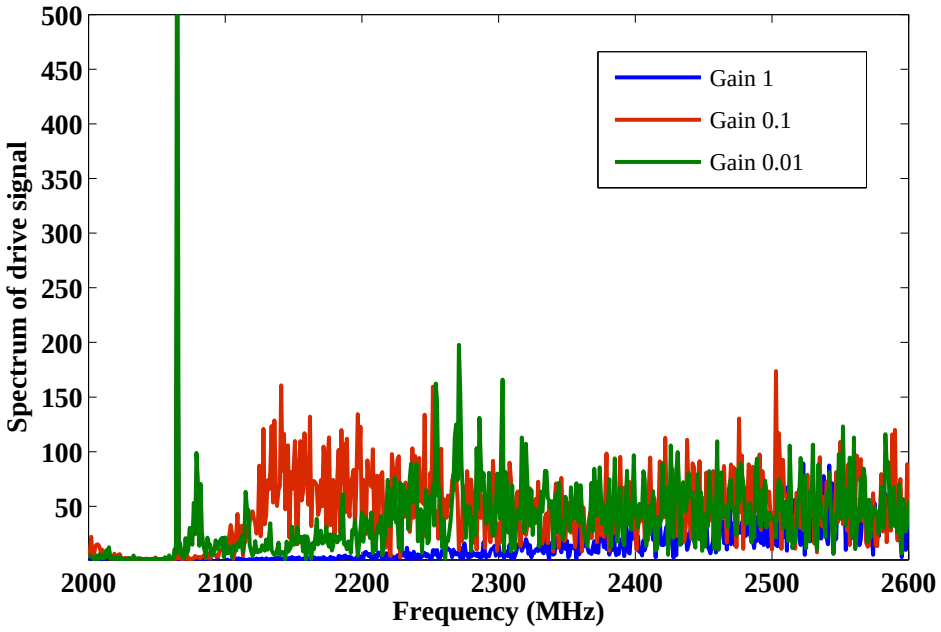

Figure 3.11: Spectrum of RF PWM waveform for a SSB input and 3 different gains. OSR=32, f_c=2048 MHz and SSB at 2066 MHz.

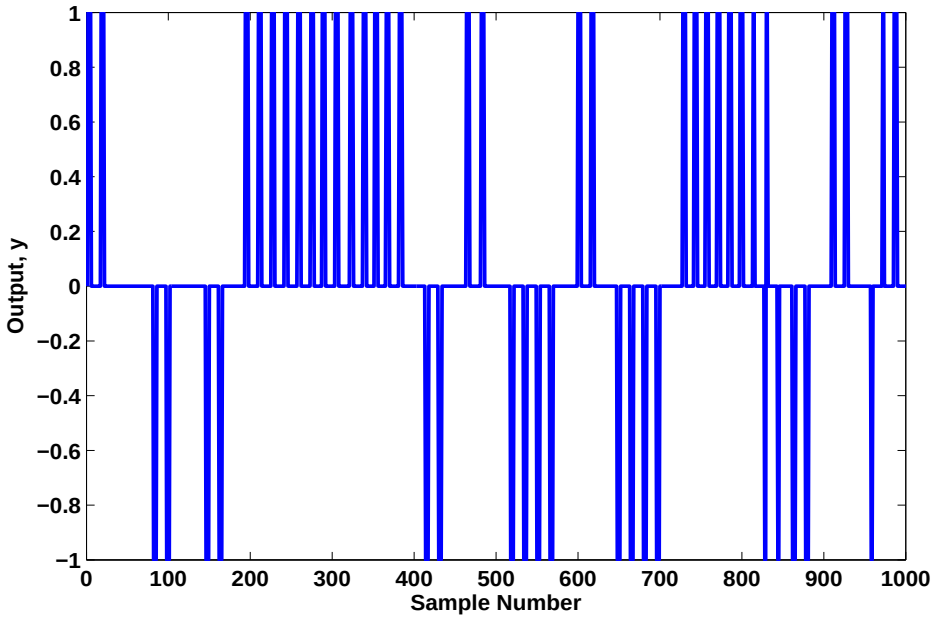

Figure 3.12: Time snapshots of the normalised PWM RF output,y. 1 is the high logic level of the particular technology. Amplitude=0.01, Gain=1, Utility=5.2744 and OSR=32.

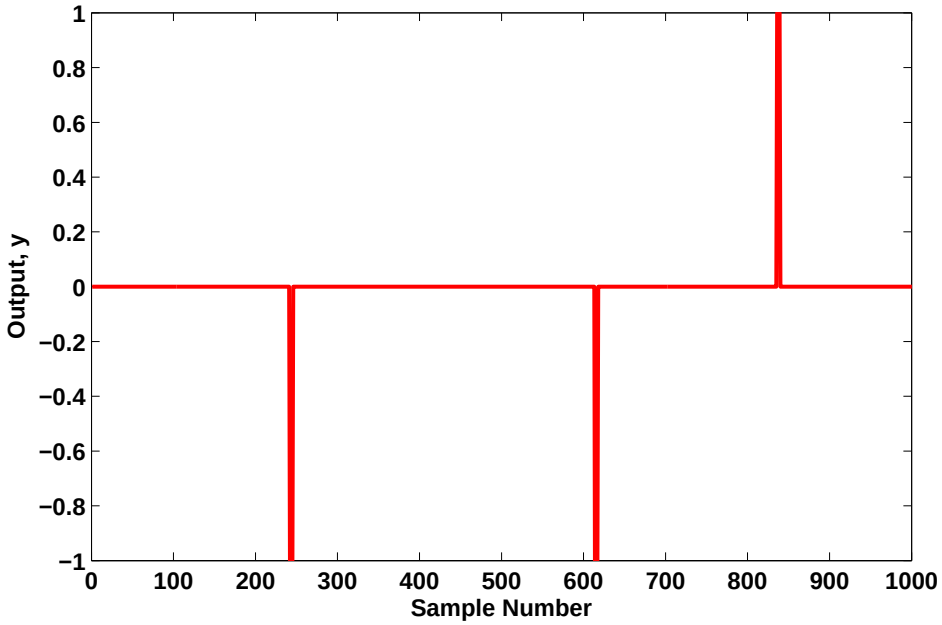

Figure 3.13: Time snapshots of the normalised PWM RF output,y. 1 is the high logic level of the particular technology. Amplitude=0.01, Gain=0.1, Utility=0.4453 and OSR=32.

period that the amplifier is in the 'on' state. It is a rough measure that determines the efficiency of the amplifier since the 'on' periods represent energy loss conditions through conducting losses. The maximum value of the utility factor is therefore $\frac{OSR}{2}$, which also corresponds to the worse value. A gain term, G_T, was introduced to the Cartesian $\Sigma\Delta$ architecture to attempt to reduce the activity (Fig. 3.10). A single side band (SSB) tone was used to test the architecture in Matlab®.

Fig. 3.11 shows the spectrum of the transmit signal of 0.01 V situated at 16 MHz from the carrier. It was found that varying G_T traded off the utility factor (efficiency) with noise performance. The different time waveforms and utility values are shown in Fig. 3.12 and Fig. 3.13. The utility factor of the amplifier drops by an order of magnitude by reducing G_T from 1 to 0.1, indicating higher efficiency. The cost is an inward movement of the quantisation noise (red trace of Fig. 3.11) thus reducing the bandwidth. It can be noted that the blue trace of Fig. 3.11 (G_T=1) has a much greater bandwidth for the same noise build-up. The power spectral denisty (PSD) of noise increases as you move away from the centre frequency. G_T should therefore be kept as small as possible while still meeting any out-of-band spectrum mask requirements.

3.4 Analysis of Polar $\Sigma\Delta$ and Cartesian $\Sigma\Delta$

3.4.1 Test Signal Characteristics

The polar $\Sigma\Delta$ [17] (Fig. 2.28) which was discussed in Section 2.4 was simulated for comparison with our proposed structure. A QPSK-modulated OFDM input

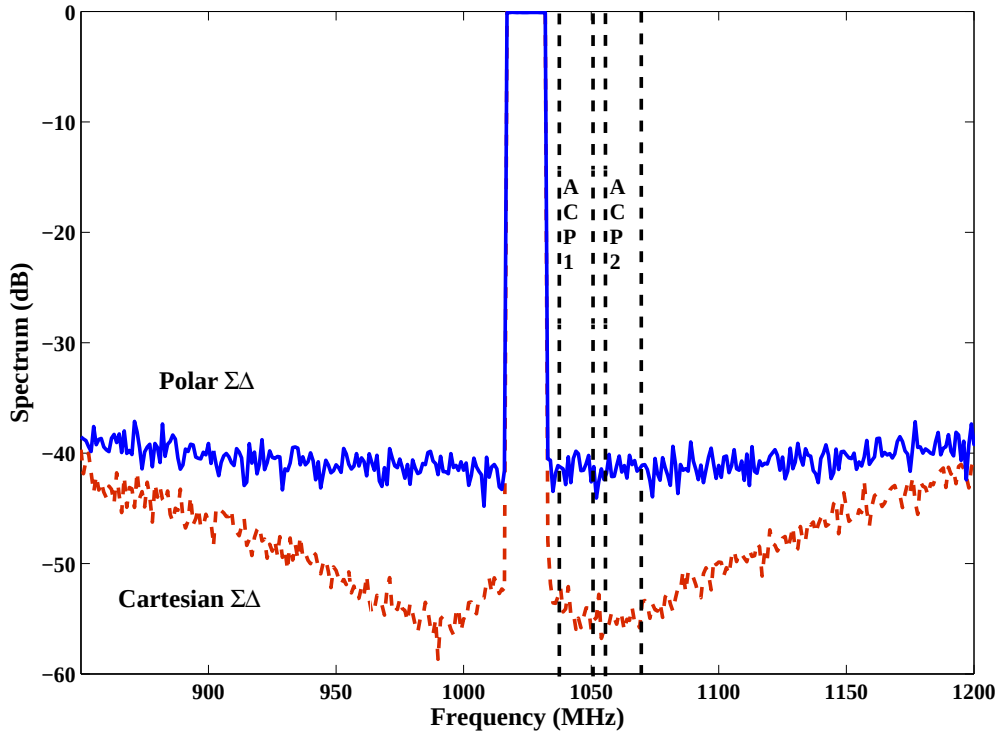

Figure 3.14: Normalised spectrum of OFDM signal with f_c=1024 MHz and $B_{ofdm} = \frac{f_c}{64}$ at input signal level of -12 dB ($u_{rms} = 1$ at 0 dB), OSR=32, G_T=1, $OSR_{\Sigma\Delta} = 128$, MOD-2 ΣΔ architecture.

signal with a worst case peak to average power level of 12 dB was used to test both blocks. The OFDM bandwidth (B_{ofdm}) was set at $\frac{f_c}{64}$ (an $OSR_{\Sigma\Delta}$ of 128 with H=1). The number of subcarriers in the OFDM system is 16. All simulations were performed in Matlab®; the sub-blocks for each structure were identical for a meaningful comparison.

3.4.2 Spectrum Analysis of Cartesian and Polar Sigma Delta

In the spectral domain, the noise in the adjacent channels needs to be below an acceptable level. ACP(1) indicates the first adjacent channel and ACP(2) indicates the second adjacent channel. Fig. 3.14 shows spectrum plots for Cartesian ΣΔ and

polar ΣΔ at an input signal level of -12 dB (which is about a 5 dB back-off from the optimum dynamic range input level of -7 dB occurring at the base of the distortion wall which corresponds to saturation, see Fig. 3.15). The root mean square (RMS) of the input signal, u_{rms}, is equal to one at 0 dB. There is a guard band between adjacent channels of $0.25B_{ofdm}$. It can be easily observed from Fig. 3.14 that there is more noise in the polar ΣΔ architecture. This phenomenon occurs because the bandwidth expanded polar signals pick up more quantisation noise which is not removed when the signal is later reconstructed. The noise fills up the null around the signal band. Fig. 3.14 also shows that the noise shaping is more prominent in the Cartesian ΣΔ scheme as a better null is observed around the signal band. Both noise curves eventually merge and follow the expected ΣΔ noise shaping when the frequency axis of Fig. 3.14 is extended. The scheme can maintain a noise floor of better than -50 dB with respect to signal power over a bandwidth of $f_c = \pm\frac{0.15f_c}{2}$ beyond which the output band-pass filter must take over responsibility for spectrum control.

3.4.3 Adjacent Channel Power Analysis of Cartesian and Polar Sigma Delta

The out-of-band distortions for both schemes are compared by calculating their ACPs. Fig. 3.15 shows that Cartesian ΣΔ has at least 10 dB less ACP than the polar ΣΔ. The improvement holds over a wide dynamic range of input signal levels. The polar ΣΔ scheme washes out the noise shaping for signal levels greater than -25 dB as indicated by the small differences between ACP(1) and ACP(2). The

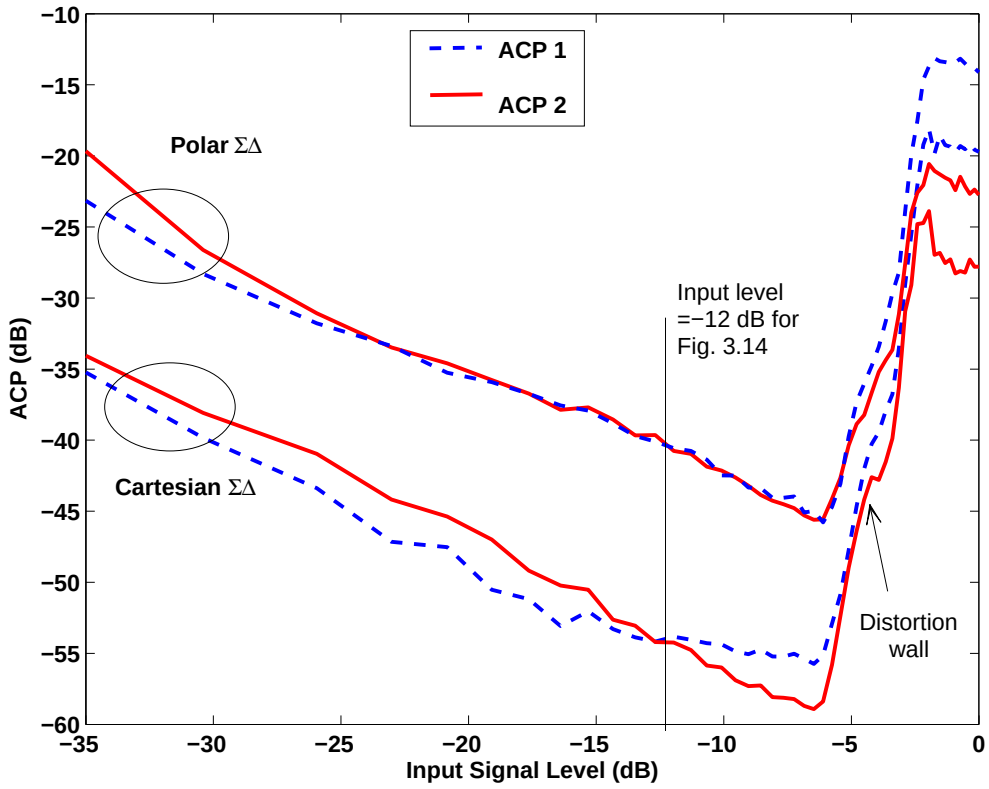

Figure 3.15: ACP for Cartesian and polar ΣΔ scheme against input signal level ($u_{rms} = 1$ at 0 dB).

improved noise shaping of the Cartesian ΣΔ architecture can be observed by the clear separation between ACP(1) and ACP(2). Clipping of the OFDM signal shows up in the proposed scheme as a skirt around the signal spectrum of the Cartesian ΣΔ plot of Fig. 3.14. The onset of this effect is evident in Fig. 3.14 and dominates the Cartesian ΣΔ performance for average input signal levels greater than -12 dB as shown by Fig. 3.15.

3.4.4 Effect of Oversampling Factor on Adjacent Channel Power in Polar and Cartesian Sigma Delta

The OSR has a direct impact on f_{clock} as shown by equation (3.3). Since the maximum value of f_{clock} is restricted by today's digital technology, it can be deduced from equation (3.3) that higher OSR limits the maximum value of f_c. It is therefore crucial to keep the OSR as low as possible. Fig. 3.16 shows a plot of ACP vs OSR. The Cartesian $\Sigma\Delta$ clearly outperforms the polar $\Sigma\Delta$, leading to a lower OSR requirement for the same ACP. Even the traditional bandpass $\Sigma\Delta$ with an OSR=4 outperforms the polar $\Sigma\Delta$ with OSR=8.

The results shown here for the Cartesian architecture with an OSR of 8 are reasonable for the WLAN standard (ACP<-40 dB). However, a higher oversampling rate of OSR=20 is required to meet the tougher -50 dB 3GPP spectrum mask, limiting carrier frequencies, f_c, to about 200 MHz (very high frequency (VHF) band) using current digital technology (f_{clock}=4 GHz). Clock rates must further improve before carrier frequencies in the cellphone bands can be handled.

3.5 Summary

In this chapter, a novel all-digital drive for SMPAs in wireless transmitter architecture is proposed. It outputs two 1-bit drive signal for SMPAs operating in push-pull giving an effective three-level waveform. It shows a better adjacent channel noise performance compared to a polar $\Sigma\Delta$ architecture based on the structure of [17]. This is achieved by swapping the order of the Cartesian to polar conversion and the

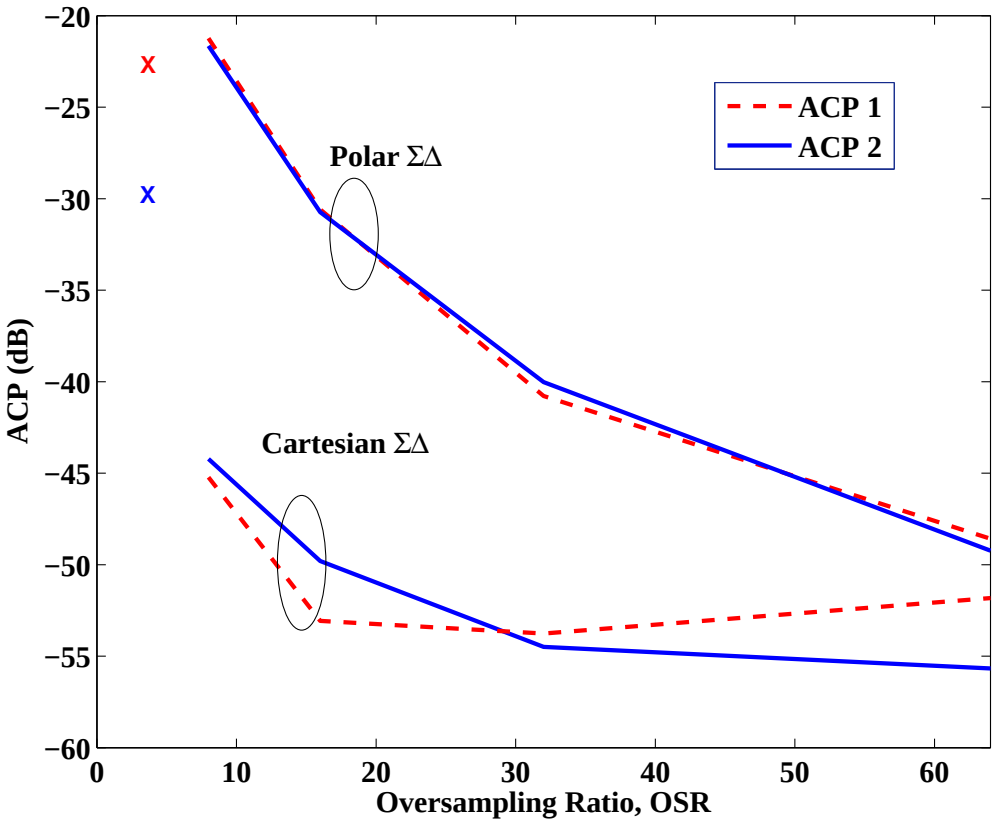

Figure 3.16: Plot of ACP (dB) against oversampling rate, *OSR*. The first and second adjacent channels are shown. Other conditions as per Fig. 3.14. The crosses show the performance of the bandpass ΣΔ of Sub-section 2.3.5 (The red cross refers to ACP1 and the blue cross refers to ACP2).

ΣΔ filtering. The ΣΔs can then act on non-bandwidth expanded signals. The developed scheme gives an improvement of at least 10 dB in signal to adjacent channel noise over the previous scheme. In addition:

1. Equations are developed showing the basic relationship between the system digital clock, f_{clock}, the carrier frequency, f_c, the ΣΔ sampling frequency, f_s, and the modulation bandwidth of the signal, BW.

2. A trade-off between the gain factor, G_T, the utility and the quantisation noise

is presented. A gain of 1 provides a greater bandwidth but gives a utility of 5.274. A gain of 0.1 reduces utility by a factor of ten but also reduces the bandwidth. G_T should only be reduced from unity if the spectrum requirement allows it; which is not the case in the wireless applications discussed here.

3. It is shown that for two adjacent channels an OSR of eight is required to meet ACP requirements of -40 dB (WLAN specifications) and an OSR of 20 is needed to meet the ACP of -50 dB (3GPP specifications).

4. It is shown that a Cartesian $\Sigma\Delta$ with MOD-2 filters operating at $2f_c$ enables an operating bandwidth of $0.15f_c$. The implied 150 MHz bandwidth at f_c=1.024 GHz would exceed the project goal (Section 1.5) if an OSR value of 20 could be accommodated (f_c = 20 GHz!).

5. It is shown that carrier frequencies in the high frequency (HF)(3-30 MHz) and VHF range (30-300 MHz) can be easily accommodated with achievable sample rates (4 GHz). Current digital technology still needs to advance if the requirements of the cellular bands are to be met. Note that the maximum sampling rate of the $\Sigma\Delta$ is $2f_c$ (two updates per period), and so the only section that needs to be operating at a higher speed is the 'polar to PWM/PPM' circuit block and it is the oversampling requirements on this block that limits the maximum f_c.

In the next chapter, the MSE performance of the system will be discussed taking into account the non-linearity of the quantiser.

Chapter 4

Polar quantisation plane

4.1 Introduction

There have been many papers describing the quantisation noise associated with $\Sigma\Delta$ modulators. The main performance of the $\Sigma\Delta$ ADCs and DACs is well understood and the traditional analysis models the quantisation noise as a white error process which is fed into the $\Sigma\Delta$ loop. The quantisers are generally linear and the noise power is given by $\frac{\Delta^2}{12}$ where Δ represents the step-size as described in Section 2.3 [51]. However, there has been no analysis of a non-uniform polar quantiser with an input circular symmetric Gaussian signal having Rayleigh envelope. The latter is a good approximation for many signal modulation formats such as such as OFDM and CDMA [74]. In this chapter, the MSE of the non-uniform polar quantiser with such a signal is derived in sub-section 4.3. Section 4.4 compares the theoretical and simulated MSE results for a stand-alone quantiser. In Section 4.5, the polar quantiser is embedded in the $\Sigma\Delta$ modulator. The MSE curves are analysed and compared to the ones produced by the stand-alone quantiser. The differences are investigated and mathematical derivations are provided to explain and substantiate

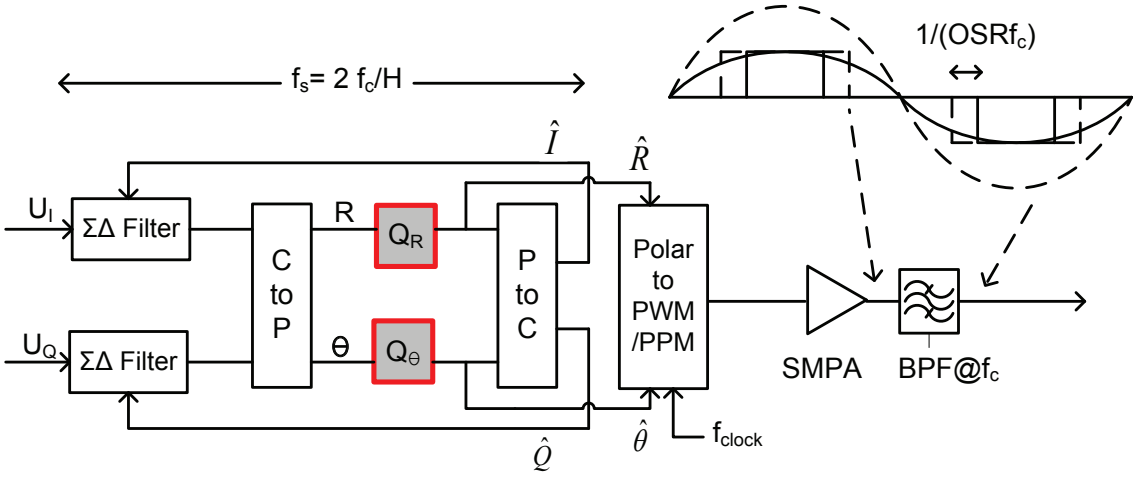

Figure 4.1: Cartesian ΣΔ modulator (polar quantiser blocks are highlighted).

the findings.

4.2 Polar Quantisation Plane

The 'polar to PWM/PPM' block has been previously discussed in Section 3.2.1. The quantised phase is used to determine the pulse position and the quantised amplitude is used to determine the pulsewidth.

The quantisation phase plane of Fig. 3.5 illustrates the functions carried out by blocks Q_R and Q_θ. It shows a series of concentric circles sliced at equal angles. The circles represent the quantised amplitude and the slices represent the quantised phases. The dots at the intersection of the circles and the slices represent the quantisation points. The dotted circles and dotted lines represent the threshold levels used in the quantiser. The number of quantised steps (N_A, N_P) can be increased or decreased depending on the accuracy requirement. However, it must also be noted

Table 4.1: $\hat{R}$ values for OSR = 4, 8, 16 and 32.

OSR	**4**	**8**	**16**	**32**
$\hat{R}_0$	0	0	0	0
$\hat{R}_1$	1.4142	0.9238	0.4904	0.2488
$\hat{R}_2$	-	1.3066	0.9062	0.4880
$\hat{R}_3$	-	-	1.1840	0.7086
$\hat{R}_4$	-	-	1.2814	0.9018
$\hat{R}_5$	-	-	-	1.0604
$\hat{R}_6$	-	-	-	1.1782
$\hat{R}_7$	-	-	-	1.2508
$\hat{R}_8$	-	-	-	1.2752

that increasing the number of levels implies a higher OSR which eventually constrains the maximum f_c, because of technology limitation on the maximum f_{clock} (3.3).

4.2.1 Non-Linear Amplitude Quantisation Levels

$\hat{R}_{\frac{v}{2}}$ is the RF carrier amplitude for a repeating binary pulse sequence with pulsewidths of v clock cycles as per Fig. 3.6. Table 4.1 lists the amplitude quantisation levels, $\hat{R}$, for a quantiser with OSR of 4, 8 (Fig. 3.5), 16 and 32. The uneven separation between the quantised levels indicates that increasing the pulsewidth has less effect on the RF carrier magnitude when the pulsewidths are already large. The pulse extremities contribute less to the signal amplitude compared to the pulse central sections.

Rayleigh distributed signals have amplitude probability density functions (PDFs) that are concentrated around the lower signal levels. It can be noted from Table 4.1 that the low amplitude levels are coarsely quantised and higher amplitudes are

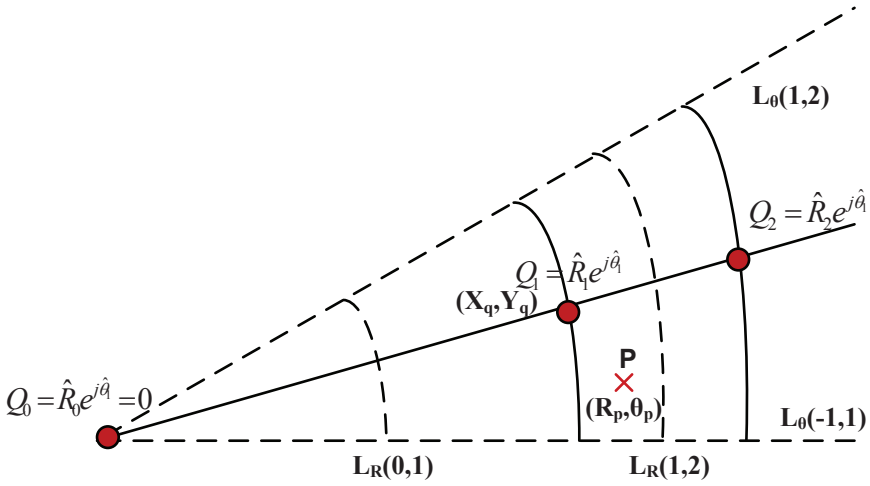

Figure 4.2: An expanded view of a slice of the polar quantisation plane. OSR=8.

more finely quantised. Therefore, the quantisation noise is larger for such signals than would be normally expected using a linear quantiser. Signals whose PDFs are concentrated at medium to high amplitude levels (such as $\frac{\pi}{4}$QPSK and enhanced data rates for GSM evolution (EDGE) modulation) are more suited to this type of non-linear quantiser.

However the phase error behaves in an opposite way; increasing the amplitude produces a bigger MSE for the same phase error. To some extent, this neutralises the non-linear quantisation of the magnitude error. These effects will now be quantified in the next sections.

4.3 Derivation of Polar Quantiser MSE

In this section, an expression is derived for the MSE for the non-linear polar quantiser with a circular symmetric Gaussian input signal of arbitrary power. The MSE

contribution for each of the amplitude quantisation levels has to be calculated separately as the area associated with each quantisation level is not uniform. However, the MSE contribution of only one slice (one phase quantisation level) needs to be calculated due to the phase symmetry. This procedure helps to minimise mathematical complexity. The MSEs contributions obtained for each of the amplitude quantisation levels are summed. The resulting value represents the MSE for one angular slice and must be multiplied by the number of slices, N_p.

Point P is represented by the polar coordinates R_p and θ_p in Fig. 4.2. There are three MSE calculation zones corresponding to the quantisation point Q_0, Q_1 and Q_2. Q_0 is selected when P lies between the amplitude limits 0 and $L_R(0,1)$ and phase limits $L_\theta(-1,1)$ and $L_\theta(1,2)$. Q_1 is selected when P lies between the amplitude limits of $L_R(0,1)$ and $L_R(1,2)$ and the phase limits of $L_\theta(-1,1)$ and $L_\theta(1,2)$. Q_2 is selected when P lies between the amplitude limits of $L_R(1,2)$ and infinity and the phase limits of $L_\theta(-1,1)$ and $L_\theta(1,2)$. The MSE contributions are summed and multiplied by N_p which corresponds to eight in the example of Fig. 3.5.

Assuming the input signal has a Rayleigh envelope, the MSE of the non-uniform polar quantiser is derived. The derivation process starts by finding the probability of occurence in a small area about point P, between amplitude R_p and $R_p + \delta R_p$ and between phase θ_p and $\theta_p + \delta\theta_p$.

Assuming the signal is Rayleigh, the PDF of the envelope is given by

$$P(R_p) = \frac{R_p}{\sigma^2} e^{\frac{-R_p^2}{2\sigma^2}}, \tag{4.1}$$

where $2\sigma^2$ is the average power of the input signal.

The PDF of θ_p is given by

$$P(\theta_p) = \frac{1}{2\pi}. \tag{4.2}$$

Therefore, the MSE contribution from the zone containing point P with polar coordinates (R_p, θ_p) with respect to the nearest quantisation point $Q_{\frac{v}{2}}$ with Cartesian coordinates ($X_{\frac{v}{2}} = \hat{R_{\frac{v}{2}}}\cos\hat{\theta_1}$, $Y_{\frac{v}{2}} = \hat{R_{\frac{v}{2}}}\sin\hat{\theta_1}$) is given by

$$\begin{aligned} MSE\left(Q_{\frac{v}{2}}\right) =& \frac{1}{2\pi}\int_{L_\theta(-1,1)}^{L_\theta(1,2)}\int_{L_R\left(\frac{v}{2}-1,\frac{v}{2}\right)}^{L_R\left(\frac{v}{2},\frac{v}{2}+1\right)}[(X_q - R_p cos\theta_p)^2 + (Y_q - R_p sin\theta_p)^2] \\ & \times \frac{R_p}{\sigma^2} e^{\frac{-R_p^2}{2\sigma^2}} dR_p d\theta_p. \end{aligned} \tag{4.3}$$

Solving and simplifying the integral gives the MSE for a given amplitude quantisation region (with boundaries $L_R(\frac{v}{2}-1, \frac{v}{2})$ and $L_R(\frac{v}{2}, \frac{v}{2}+1)$) and a phase quantisation region (with boundaries by $L_\theta(-1,1)$ and $L_\theta(1,2)$). The boundary limits have previously been defined by the threshold equations (3.10) and (3.11) and they are midway between the quantisation points. The MSE of different quantisation regions can be calculated by altering the limits of equation (4.3).

$$\begin{aligned} MSE\left(Q_{\frac{v}{2}}\right) =& \frac{1}{2\pi\sigma^2}\left[-\sigma^2 e^{\frac{-R_p^2}{2\sigma^2}}(X_q^2 + Y_q^2) - \sigma^2(2\sigma^2 + R_p^2)e^{\frac{-R_p^2}{2\sigma^2}}\right]_{L_R(\frac{v}{2}-1,\frac{v}{2})}^{L_R(\frac{v}{2},\frac{v}{2}+1)} \\ & \times \Big[\theta_p\Big]_{L_\theta(-1,1)}^{L_\theta(1,2)} + \frac{1}{2\pi\sigma^2}\Big[-X_q^2 sin\theta_p + Y_q^2 cos\theta_p\Big]_{L_\theta(-1,1)}^{L_\theta(1,2)} \\ & \times \left[-R_p\sigma^2 e^{\frac{-R_p^2}{2\sigma^2}} + \frac{1}{2}\sigma^3\sqrt{\pi}\sqrt{2}\mathrm{erf}\frac{\sqrt{2}R_p}{2\sigma}\right]_{L_R(\frac{v}{2}-1,\frac{v}{2})}^{L_R(\frac{v}{2},\frac{v}{2}+1)} \end{aligned} \tag{4.4}$$

The final MSE of the quantised signal covering the whole phase plane is given by

$$MSE_{final} = N_p \sum_{\frac{v}{2}=0}^{N_A} MSE\left(Q_{\frac{v}{2}}\right), \tag{4.5}$$

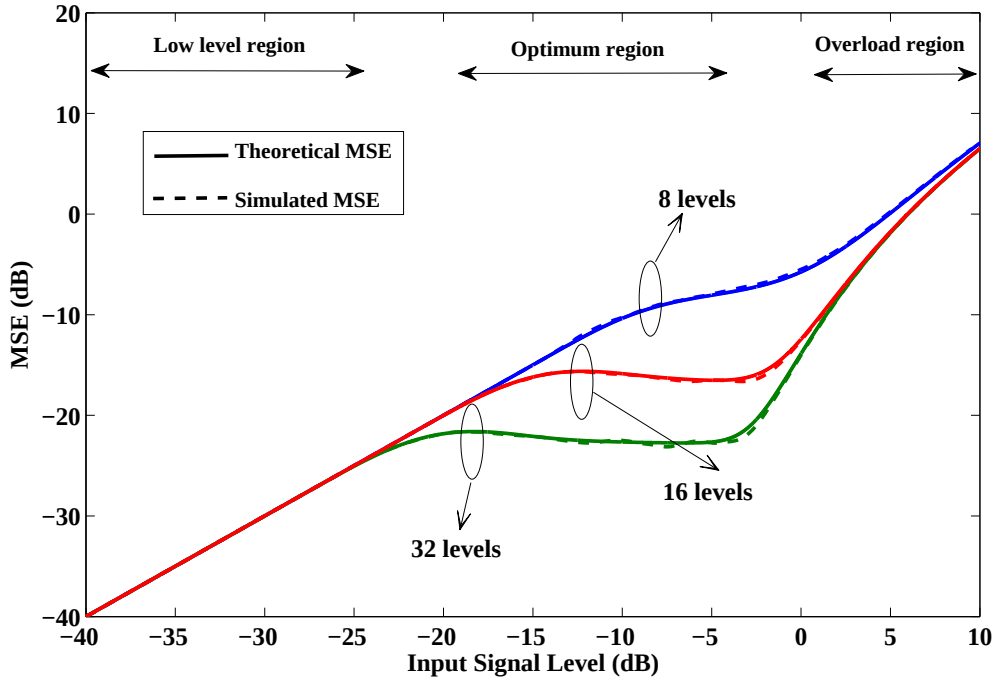

Figure 4.3: Theoretical and simulated results of MSE for a stand-alone polar quantiser with three OSR levels ($\overline{|\tilde{u}|^2}$ =1 at 0 dB).

where N_P and N_A are the number of amplitude and phase levels which are related to OSR through equations (3.5) and (3.4). Equation (4.5) gives the total MSE as a function of the average input power ($2\sigma^2$) and the OSR.

4.4 Theoretical and Simulated Results of Stand-Alone Polar Quantiser

The non-uniform polar quantiser is simulated to verify the validity of the derived MSE equation. A QPSK-modulated OFDM signal was chosen as input to the simulated quantiser as it approximates a Rayleigh envelope and hence satisfies the assumption made during the derivation of the MSE equation.

Fig. 4.3 shows plots of MSE against input signal level for the theoretical and

simulated quantisers with three different OSR values. It can be observed that the simulated MSE and the theoretical MSE curves are almost indistinguishable.

The MSE is exactly equal to the signal power at low signal levels for all three plots. When the input signal is increased and crosses the first threshold level ($L_{R(0,1)}$), the MSE plateaus. The plot with the highest OSR (32 levels) plateaus sooner as its first threshold level is closest to zero. The average MSE is also less for this plot as it has more quantisation levels (N_A and N_P). For the two higher OSR curves (16 and 32), the plateaus have a slightly reducing MSE with increasing signal power: caused by the clustering of the amplitude quantisation levels at larger magnitudes (see Table 4.1). The plateau section of the plot is referred to as the optimum region.

As the signal power is increased beyond the largest quantisation level, the MSE errors again increase. This region is known as the overload. The final quantisation level represents the maximum pulsewidth corresponding to a square wave and is therefore the same for all OSR values. At very high signal levels, the MSE will eventually equal the signal power again as shown by the asymptotic curve shape (top right of Fig. 4.3).

4.5 Analysis of Polar Quantiser with and without $\Sigma\Delta$ Modulators

In this section, the MSE of the combined $\Sigma\Delta$ and the polar quantiser is studied. The simulations are carried out on both the polar $\Sigma\Delta$ architecture (Section 2.4) and the Cartesian $\Sigma\Delta$ architecture (Section 3.2). The MSE is measured between the input

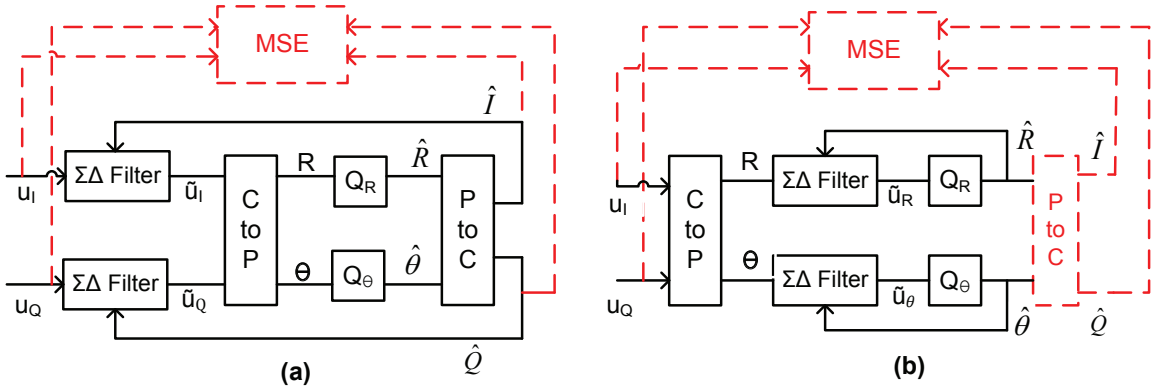

Figure 4.4: Block diagrams showing the MSE calculation steps for the Cartesian ΣΔ architecture (a) and the polar one (b).

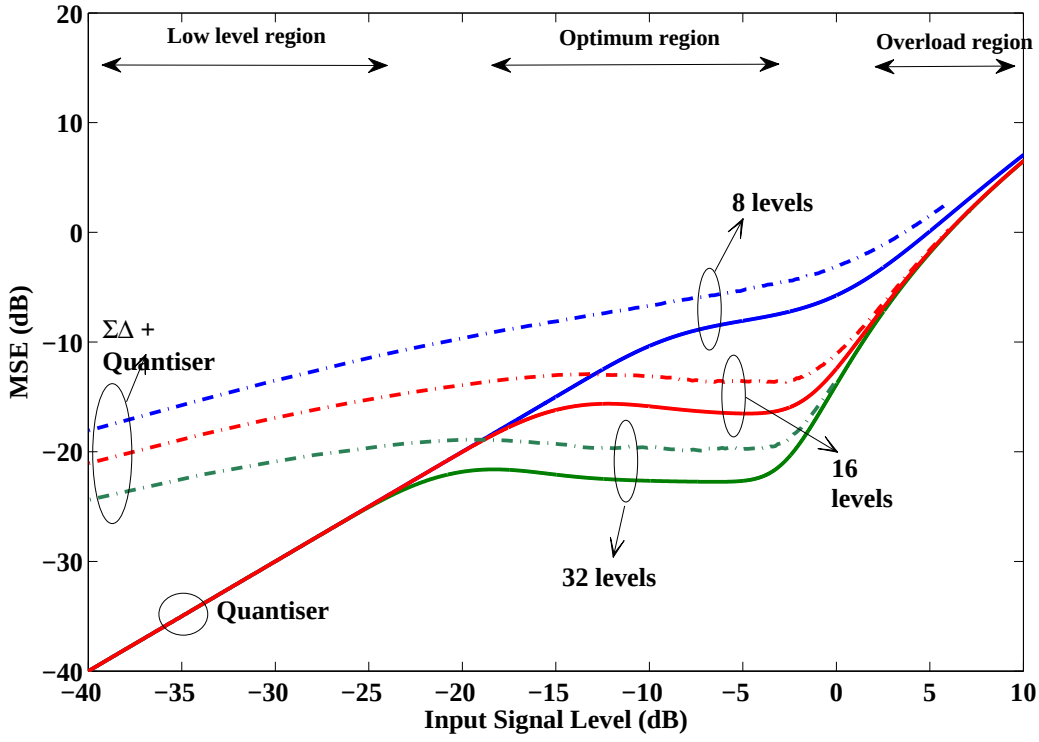

Figure 4.5: Simulated results of polar quantiser with and without ΣΔ modulators - Polar ΣΔ architecture. ($\overline{|\tilde{u}, u|^2}$ =1 at 0 dB)

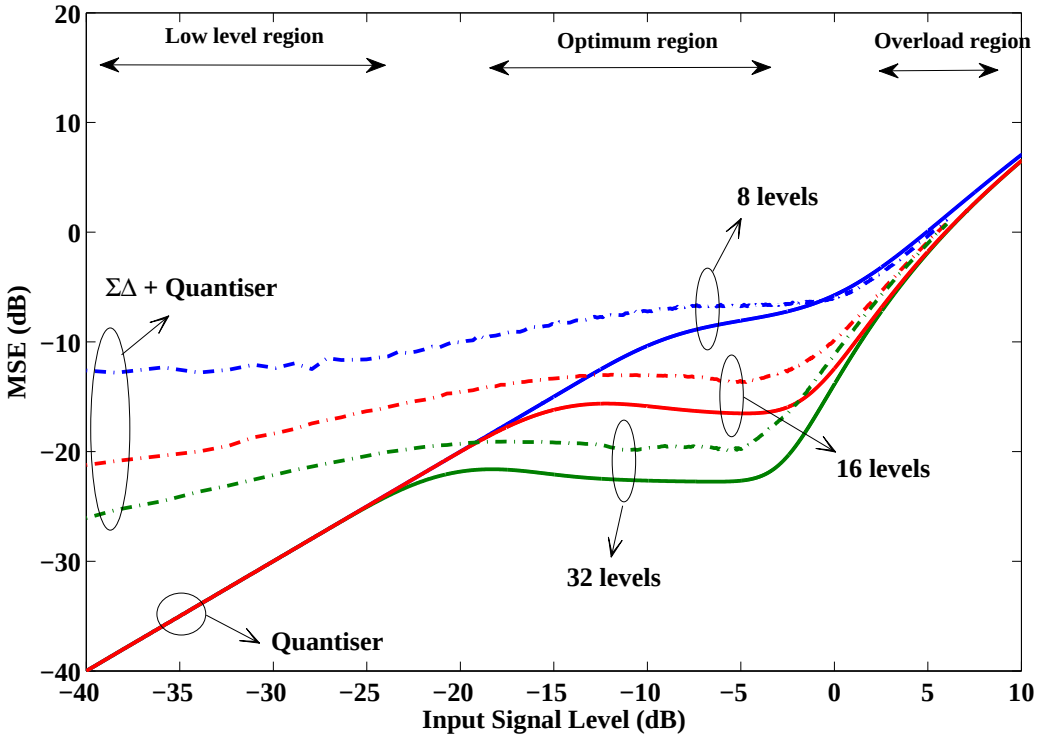

Figure 4.6: Simulated results of polar quantiser with and without ΣΔ modulators - Cartesian ΣΔ architecture. ($\overline{|\tilde{u}, u|^2}$ =1 at 0 dB)

signal and the quantised output signal as shown in Fig. 4.4. The simulations are performed for three different OSR levels (8, 16 and 32) and the results obtained from the polar and Cartesian ΣΔ architectures are shown in Fig. 4.5 and Fig. 4.6 respectively. The ΣΔ filters used in both architectures are first order (MOD-1 [51]). The optimum SQNR is obtained at the end of the plateau region (just before the overload region) where the MSE steeply ramps up.

The MSE plots also plateau but at a level 3 dB higher than stand-alone quantiser. This trend can be observed for all the three OSR levels but is more evident for the plot with an OSR of 32 as the plateau covers a wider range of signal power. Plots

with higher OSR cover a wider range of signal power at a lower MSE. Additionally, the performance at low signal levels is significantly different. The MSE drops at a lower rate as the signal power is reduced. The result is a significant increase in MSE at very low signal levels compared to the stand-alone quantiser. The phenomena are analysed in the following subsections.

4.5.1 Mathematical Derivation of Noise Associated with ΣΔ Modulator

The 3 dB noise increase over the plateau region can be explained from the NTF of the ΣΔ modulator. The NTF of a first order lowpass ΣΔ modulator is given by $(1 - z^{-1})$ (Section 2.3.1) and its power gain is:

$$\begin{aligned} |NTF|^2 = &\left(1 - e^{j2\pi\frac{f}{f_s}}\right)\left(1 - e^{-j2\pi\frac{f}{f_s}}\right), \\ =&2\left(1 - cos\left(2\pi\frac{f}{f_s}\right)\right). \end{aligned} \tag{4.6}$$

Following the traditional analysis for ΣΔ ADCs, we make the assumption that the quantisation noise is spectrally white. The MSE can then be calculated by integrating the $|NTF|^2$ over the range of $-\frac{f_s}{2}$ to $\frac{f_s}{2}$. The noise due to the ΣΔ modulators is given by

$$MSE_{\Sigma\Delta} = 2\int_0^{\frac{f_s}{2}} N_o(f) \times 2\left(1 - cos\left(2\pi\frac{f}{f_s}\right)\right)df, \tag{4.7}$$

where $N_o(f)$ is the quantisation noise power spectral density introduced by the quantiser (4.5)

$$N_o(f) = \frac{MSE_{final}}{f_s}. \tag{4.8}$$

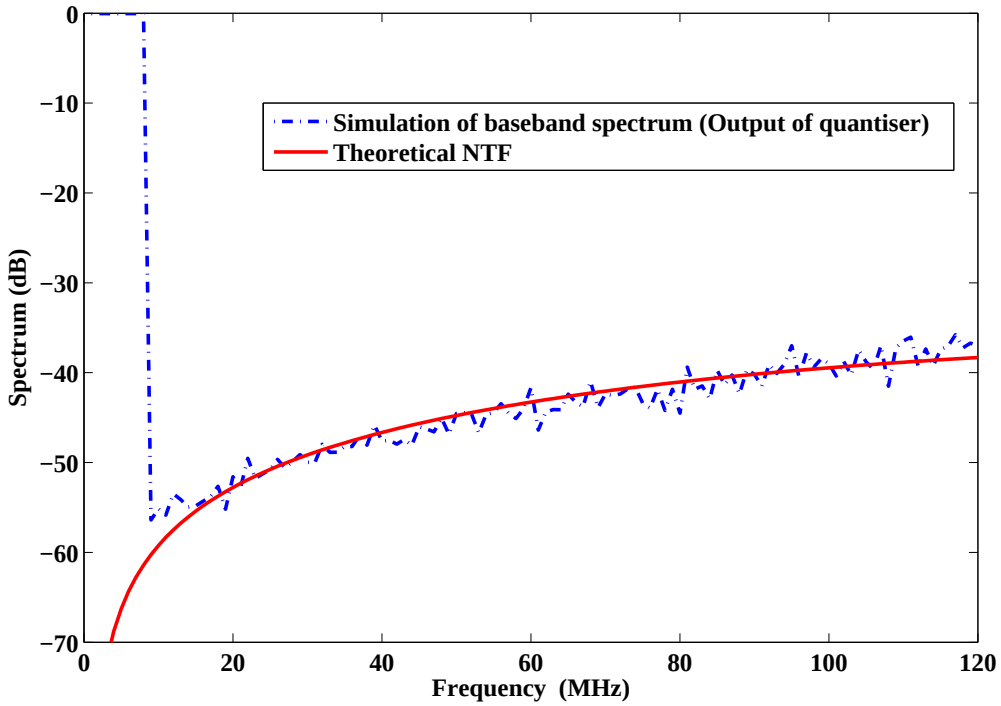

Figure 4.7: Simulated output spectrum of the Cartesian ΣΔ modulators superimposed on a theoretical NTF plot of a first order ΣΔ modulator. ($\overline{|u|^2}$ =1 at 0 dB)

Substituting (4.8) in (4.7) and evaluating the integral gives

$$MSE_{\Sigma\Delta} = \frac{MSE_{final}}{f_s} \times 4 \times \left[f - \frac{f_s}{2\pi} sin(2\pi \frac{f}{f_s}) \right]_0^{0.5f_s}, \tag{4.9}$$
$$= MSE_{final} \times 2.$$

The spectrum output of the quantiser is plotted at an input signal level of -10 dB ($\overline{|u|^2}$ =1 at 0 dB) for the Cartesian ΣΔ architecture. The first order lowpass ΣΔ NTF is superimposed on the simulation plot and agreement between the theoretical and simulation plots is observed as shown in Fig. 4.7. The analysis clearly predicts the correct performance of the ΣΔ modulator when the signal power is in the plateau region. However, the 3 dB MSE increase derived in (4.9) does not forecast the

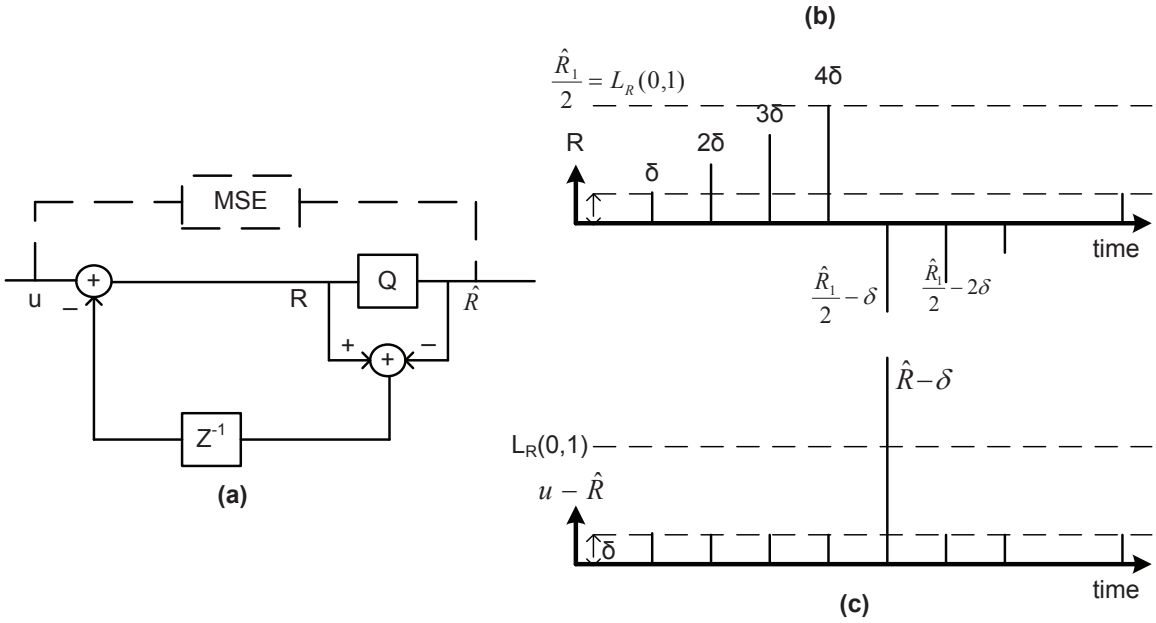

Figure 4.8: (a) shows a simplified first order ΣΔ modulator. (b) shows a plot of the input, R, to the quantiser and (c) plots the difference between u and the quantiser output, $\hat{R}$.

operation of the ΣΔ in the low signal region as shown in Fig. 4.5 and Fig. 4.6. A different analysis is required for that section of the graph and is given in the next subsection.

4.5.2 Low Signal Behaviour of ΣΔ Modulators

At low signal levels, the output of the ΣΔ modulator is characterised by a string of zero valued samples, $\hat{R}_0$, followed by an occasional jump to $\hat{R}_1$. It is the jump to $\hat{R}_1$ that causes the higher than expected MSE. This jump can be attributed to the integrator loop inside the ΣΔ modulator. This phenomenon is known as the limit cycle behaviour. The operation can be explained by just considering the magnitude component of the polar ΣΔ (Fig. 2.28). Consider a first order ΣΔ with a constant input signal, $u = \delta$; $\delta \ll L_R(0,1)$ as shown in Fig. 4.8. The error across the quantiser

$(R - \hat{R})$ is fed back in to the $\Sigma\Delta$ causing the quantiser input signal, R, to ramp up in steps of δ. When the first threshold is reached, the output changes from $\hat{R_0}(= 0)$ to $\hat{R_1}$ causing a large pulse in the quantiser output, resetting R to a value close to $\frac{\hat{R_1}}{2}$. The system works like a relaxation oscillator. The output pulse occurs every $N_T = \frac{\hat{R_1}}{\delta}$ samples. The error between the analog input and the quantised output $(u - \hat{R})$ is also shown in the Fig. 4.8. The MSE is therefore given by:

$$MSE(\delta) = \frac{N_T\delta^2 + (\hat{R_1} - \delta)}{N_T + 1}. \tag{4.10}$$

When the input signal is replaced by a Rayleigh distributed envelope signal, the amplitude, δ, can be replaced by the mean signal level, $\sigma\sqrt{\frac{\pi}{2}}$, and the power of the signal, δ^2, is replaced by $2\sigma^2$. This gives:

$$N_T = \frac{\hat{R_1}}{\sigma\sqrt{\frac{\pi}{2}}}, \tag{4.11}$$

$$MSE(\sigma) = \frac{N_T(2 \times \sigma^2) + (\hat{R_1} - \sigma\sqrt{\frac{\pi}{2}})^2}{N_T + 1}. \tag{4.12}$$

The plots obtained from theoretical equation (4.12) are superimposed over the simulated plots of MSE of the polar $\Sigma\Delta$ modulator as shown in Fig. 4.9. The signal power axis of the simulated values is extended to -60 dB to observe the low signal behaviour of the $\Sigma\Delta$ modulators. The plots show that the derived equation is in accordance with the simulation results for low signal level range and the value of the gradient of the plots is 0.5. The simulation results start to deviate from the theoretical analysis when the first threshold level is reached and in Fig. 4.9 this phenomenon is more evident with an OSR of 32 as the threshold level is attained at a lower signal power.

It should be noted that phase quantisation effects have almost no contribution to the MSE at low signal levels. This is because the dominant contribution to MSE is the $(\hat{R_1} - \delta)^2$ term. If the phase of $\hat{R_1}$ changes the resultant power variation is small since δ is very small.

Equation (4.12) can be simplified when σ is much less than $\hat{R_1}$. The numerator can be approximated with $\hat{R_1}^2$ and the unity term can be neglected in the denominator giving

$$\begin{aligned} MSE &= \frac{\hat{R_1}^2}{\frac{\hat{R_1}}{\sigma\sqrt{\frac{\pi}{2}}}}, \\ &= \hat{R_1}\sigma\sqrt{\frac{\pi}{2}}, \end{aligned} \tag{4.13}$$

$$\begin{aligned} 10\log(MSE) &= 10\log(\sigma) + 10\log\left(\hat{R_1}\sqrt{\frac{\pi}{2}}\right), \\ &= 5\log(2\sigma^2) + 5\log(0.5) + 10\log\left(\hat{R_1}\sqrt{\frac{\pi}{2}}\right), \\ &= 0.5(10\log(2\sigma^2)) + 5\log(0.5) + 10\log\left(\hat{R_1}\sqrt{\frac{\pi}{2}}\right), \end{aligned} \tag{4.14}$$

$$MSE(dB) = 0.5 \times SignalPower(dB) + C. \tag{4.15}$$

Equation (4.15) indicates a straight line with gradient of 0.5 as shown in Fig. 4.9. This gradient is less than the stand-alone quantiser and indicates that the $\Sigma\Delta$ process boosts noise beyond that predicted by traditional $\Sigma\Delta$ analysis. The boosted noise will lead to degrading SNR values at very low signal power and could have implications on transmitters with a wide power control range, such as those found on W-CDMA handsets.

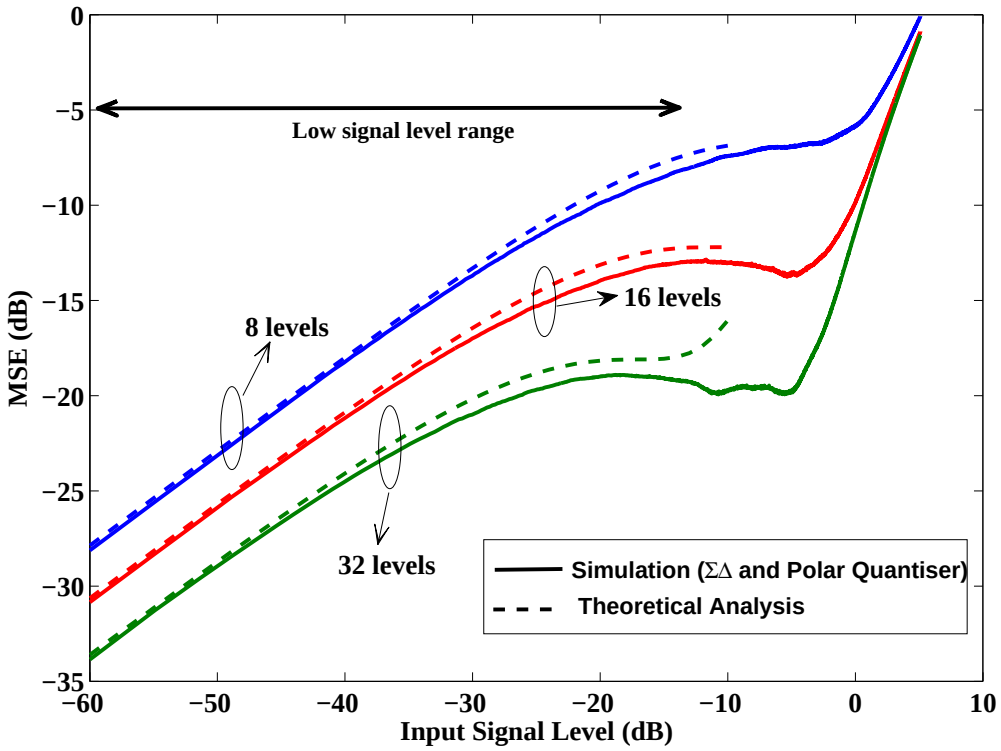

Figure 4.9: Simulated and theoretical analysis of low-signal behaviour of ΣΔ modulators on MSE ($\overline{|u|^2}$ =1 at 0 dB).

4.6 Summary

In this chapter, the polar quantisation blocks of the transmitter architecture is explained. A general expression for the MSE is derived for a circular symmetric Gaussian input signal with Rayleigh envelope. The expression is validated by simulation results of a stand-alone quantiser. The results are further substantiated by plotting MSE curves for different OSR values (note that the OSR determines the number of quantisation levels). Near perfect agreement between the simulated and theoretical curves is observed.

The MSE of the ΣΔ with the polar quantiser is also simulated for both the polar

and Cartesian $\Sigma\Delta$ scheme. Over the plateau (quantisation range), it was found that the $\Sigma\Delta$ introduces an additional 3 dB of noise. A mathematical derivation is performed to confirm that the noise introduced by the first order lowpass $\Sigma\Delta$ modulators is indeed 3 dB. At low signal level range, it was found that the MSE plots of the $\Sigma\Delta$ with the polar quantiser have a gradient of 0.5 whereas the MSE plots of the stand-alone quantiser have a gradient of one. This divergence was investigated and attributed to limit cycle behaviour, leading to the derivation of a theoretical expression which approximates the MSE for low signal levels in the presence of $\Sigma\Delta$ modulators.

The next chapter considers the operation of the PWM/PPM block that converts the polar outputs into a pulse sequence suitable for driving SMPAs. It is shown that the PPM operation produces some in-band distortions which explain the low-level skirts on the main signal in Fig. 3.14.

Chapter 5

Analysis of Distortion in Pulse Modulation Converters

5.1 Introduction

The generation of pulse width modulated signals and pulse position modulated signals by the 'polar to PWM/PPM' converter proposed in Chapter 3 can introduce unwanted spectral components. Spurious tones are observed when PWM/PPM is used to upconvert polar signals to RF. This phenomenon was first observed in [17]. In this chapter, it is shown that the presence of the spurious tones is due to the PPM process. Third order and image components are the dominant distortions generated in the pulse position modulation circuit and they fold in from other harmonic zones. Fig. 5.1 shows the output spectrum of a PWM/PPM signal that consists of a SSB tone offset from the nominal carrier frequency by 40 MHz, the image and third order distortion products are clearly visible.

Part of the work in this chapter has been presented as a conference paper titled 'Distortion Arising from Polar to PWM/PPM Conversion in an All Digital Upconverter for Switching RF Power Amplifier' at the *IEEE International Microwave*

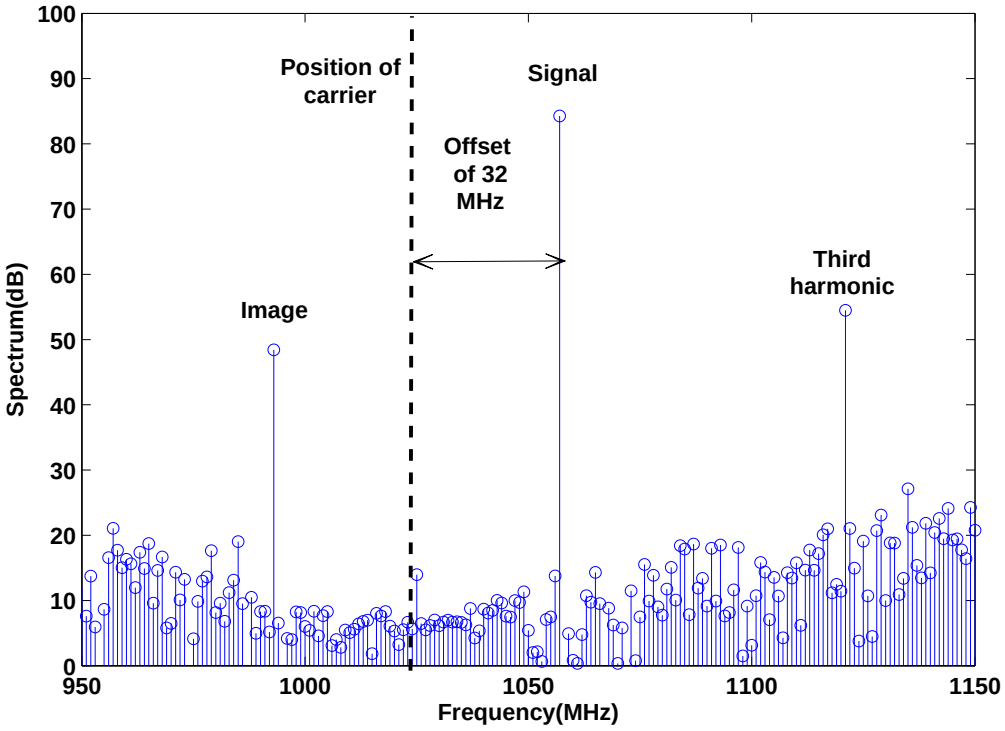

Figure 5.1: Upper SSB output spectrum from a Cartesian $\Sigma\Delta$. The distortions are from the PWM/PPM image and third harmonic.(f_c=1024 MHz and f_{ssb}= 32 MHz)

Symposium 2009 [75]. The rest of the work has been accepted for publication by the *IET journal on Microwave, Antennas and Propagation* [76].

Section 5.2 explains the process leading to the formation of the distortions. A mathematical analysis to quantify the distortion is presented in Section 5.3. Simulations and measurements results obtained in a single-carrier environment are shown in Section 5.4. Furthermore, the effect of the distortion on multi-carrier signals is presented through simulations and measurements results in Section 5.5.

5.2 Phase Modulation to Amplitude Modulation Distortion

The phase modulation operates by swallowing or stuffing a pulse whenever $\hat{\theta}$ moves from one phase quantisation level to another. The loss or gain of a pulse affects the mark-space ratio which represents the amplitude of the signal. It can thus be deduced that PM leads to AM distortion. The distortion is more significant when a 'high' pulse (logic '1') is affected. The phase advance causes the high pulse at the end of the carrier period to wrap around to the beginning in the next period. The result is a doubling in the pulse width $v = 2$ whenever this occurs (5.2(i)). The phenomenon manifests itself in the spectral domain as images and harmonic components when the baseband input signal is a phase ramp or SSB tone in the RF domain.

Fig. 5.2 shows the pulse extension effect. For illustrative purposes, the repeating pulse train is divided into sections of two periods. Waveform (a) shows the original reference waveform at f_c. At the $(n+1)$ period of waveform (b), there is a change in phase compared to the n^{th} period. The change in phase is represented by a change in position. In the remaining waveforms, the phase is incremented at every second period to produce a SSB signal at $f_c + f_{ssb}$. A change in phase causes a change in the mark-space ratio between two consecutive pulses. At some stage, the high pulses will join to form a wider high pulse ($v = 2$ for waveform(i)). Hence, the signal is no longer one pulsewidth wide.

Since the 'polar to PWM/PPM' block is located outside the $\Sigma\Delta$ loop, the error

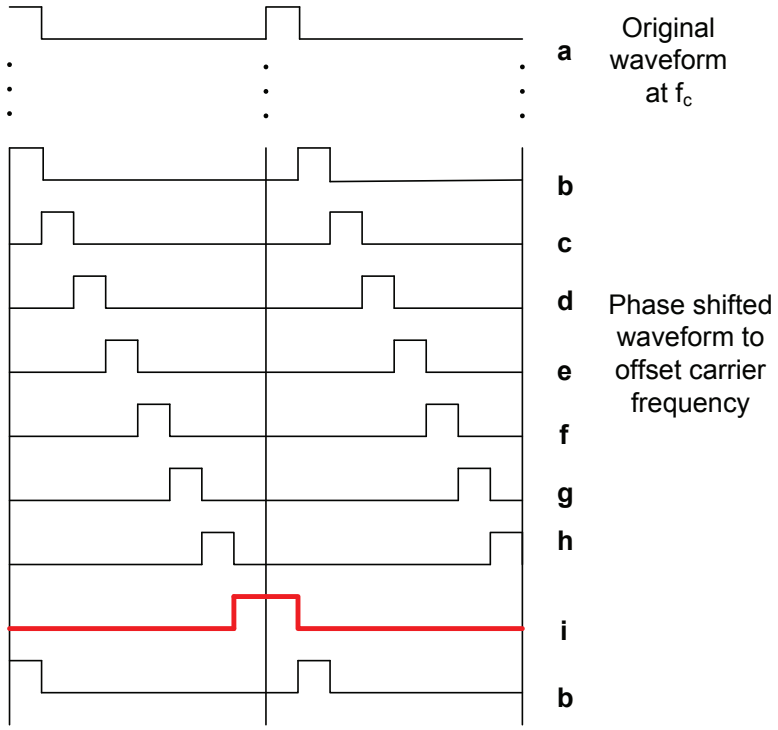

Figure 5.2: Illustrating the pulse stuffing effect required to cause a change in phase of the RF signal. (a) carrier reference signal, (b) to (i) signal with phase advanced transient. Here the phase is quantised into 8 increments.

cannot be corrected by the feedback mechanism. The situation is undesirable since the harmonics produced are often in-band and cannot be filtered out.

5.3 Mathematical Analysis of Harmonic Distortion

In this section, expressions are derived for the distortion caused in the 'polar to PWM/PPM block'. In particular, the previous section shows PM to AM distortion is attributed to changes between different phase quantisation levels. Therefore, we analyse the distortions produced by an input single sideband tone. This signal has constant amplitude and a phase that linearly increases (or decreases) with time to produce an upper (or lower) sideband signal with carrier frequency, $(f_c + f_{ssb})$ or $(f_c - f_{ssb})$ Hz respectively. The phase slope $\frac{d\theta}{dt}$ determines the side band frequency,

$$f_{ssb} = \frac{1}{2\pi}\frac{d\theta}{dt}. \tag{5.1}$$

After quantisation, the linear phase ramp turns into a staircase signal with OSR steps in 2π radians. Therefore, the step size is,

$$\Delta\theta = \frac{2\pi}{OSR}. \tag{5.2}$$

In the digital domain, the PWM operation holds the pulse width constant while the PPM operation slowly increments (or decrements) the pulse position by one clock period, T_{clk}, as each quantised phase level is passed. There are OSR clock periods in each carrier signal period ($T_c = T_{clk}OSR$). It is the action of switching between two quantised phases that causes the period of the waveform to be extended or shortened

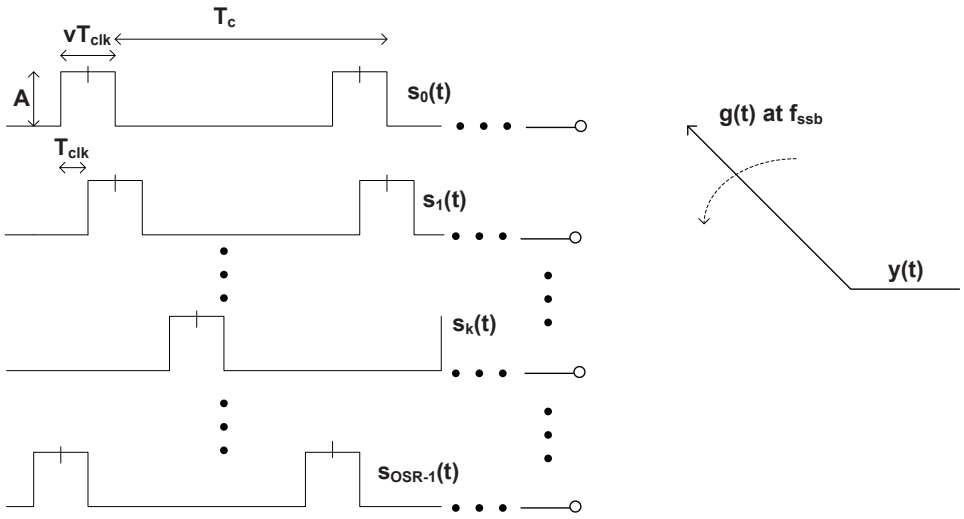

Figure 5.3: SSB generation from a bank of phase shifted oscillators.

by a clock cycle, introducing unwanted amplitude modulation as already illustrated in Fig.5.2.

Mathematically, the output $y(t)$ coming from a switch that selects one oscillator from a bank of OSR oscillators is considered. The k^{th} oscillator has an output signal $s_k(t)$ with quantised phase shift of $k\Delta\theta$ $(k = 0, \ldots, OSR - 1)$, caused by a pulse delay of kT_{clk} seconds as shown in Fig. 5.3,

$$s_k(t) = s(t + kT_{clk}). \tag{5.3}$$

All oscillators have the same pulse width, vT_{clk}, and frequency, f_c. Each anti-clockwise rotation of the switch will delay the signal by 2π radians, or reduce the number of transmitted periods by one. Therefore, the direction and rotational speed (revolutions per second) of the switch equates to the offset frequency, f_{ssb}. Hence the time for a complete switch revolution is

$$T_{ssb} = \frac{1}{f_{ssb}}, \tag{5.4}$$

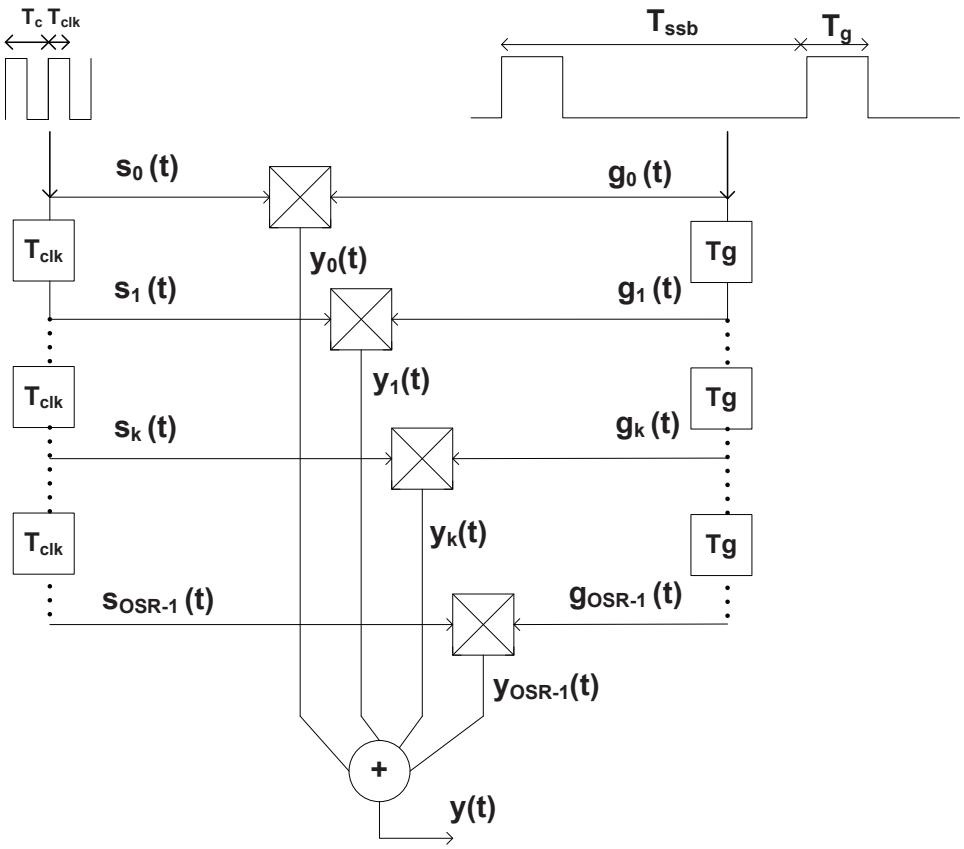

Figure 5.4: SSB generation for mathematical analysis.

and therefore the duration period that each of the OSR oscillators is connected (or gated) to the output is

$$T_g = \frac{T_{ssb}}{OSR}. \tag{5.5}$$

Based on the above discussion, the circuit can be further refined to that of Fig. 5.4. A tapped delay line generates all OSR phases from a single reference oscillator, $s_0(t)$. Each tap has a delay of T_{clk} seconds. Each oscillator signal is then gated to the output using a multiplier and gating waveform, $g_k(t)$, which has a period of T_{ssb}, an 'on time' of T_g, and a delay of kT_g. The output from the k^{th} gate is given by

$$y_k(t) = s_k(t)g_k(t), \tag{5.6}$$

and the total output is given by

$$y(t) = \sum_{k=0}^{OSR-1} y_k(t). \tag{5.7}$$

It is now possible to calculate the spectrum of the final output signal. First the spectra of the oscillator signal $\tilde{S}_k(f) = F\{s_k(t)\}$ and the gate signal $\tilde{G}_k(f) = F\{g_k(t)\}$ are calculated. The operator F is the Fourier transform. Next, the fact that multiplication in the time domain is equivalent to convolution in the frequency domain is used to get the output spectrum, $\tilde{Y}_k(f)$. For simplicity, the derivation has been broken down into three distinct sections which are the derivations of $\tilde{S}_k(f)$, the derivation of $\tilde{G}_k(f)$ and the convolution of $\tilde{S}_k(f)$ with $\tilde{G}_k(f)$ to obtain a general expression for the output spectral components.

The oscillator signal, $s_0(t)$, is a repeating pulse signal and therefore Fourier Series is used to calculate its spectrum. Its pulse width is given by, vT_{clk}, its pulse amplitude is A, its period is T_c and its spectrum is well known [77].

$$\tilde{S}_0(f) = \sum_{n=-\infty}^{\infty} S_0(n)\delta(f - nf_c), \tag{5.8}$$

where

$$S_0(n) = \frac{AvT_{clk}}{T_c}\text{Sinc}\left(\frac{nvT_{clk}}{T_c}\right). \tag{5.9}$$

Since ($T_c = T_{clk}OSR$), $S_0(n)$ can be re-written as

$$S_0(n) = \frac{Av}{OSR}\text{Sinc}\left(\frac{nv}{OSR}\right). \tag{5.10}$$

This is a series of delta functions at the harmonics of f_c and with amplitude controlled by the Sinc function which gradually decays in an oscillatory fashion as

$|n|$ increases. In the model a change in phase is represented by a change (delay or advance) in pulse position, so the time shifting property of the Fourier Transform is invoked. Hence,

$$\tilde{S}_k(f) = \sum_{n=-\infty}^{\infty} S_k(n)\delta(f - nf_c), \tag{5.11}$$

$$S_k(n) = \frac{AvT_{clk}}{T_c}\text{Sinc}\left(\frac{nvT_{clk}}{T_c}\right)e^{\frac{j2\pi nk}{OSR}}, \tag{5.12}$$

and $k = 0, 1, \ldots, (OSR - 1)$,

$$S_k(n) = S_0(n)e^{\frac{j2\pi nk}{OSR}}. \tag{5.13}$$

The gate signal, $g_k(t)$ is a repetitive pulse train which has a period of T_{ssb}. The 'on period' of this pulse train is given by $\frac{T_{ssb}}{OSR}$.

$$\tilde{G}_0(f) = \sum_{m=-\infty}^{\infty} G_0(m)\delta(f - mf_{ssb}), \tag{5.14}$$

where

$$G_0(m) = \frac{1}{OSR}\text{Sinc}\left(\frac{m}{OSR}\right). \tag{5.15}$$

The delayed version $\tilde{G}_k(f)$ by kT_{clk} is given by

$$\tilde{G}_k(f) = \sum_{m=-\infty}^{\infty} G_k(m)\delta(f - mf_{ssb}), \tag{5.16}$$

$$G_k(m) = G_0(m)e^{\pm\frac{j2\pi mk}{OSR}}. \tag{5.17}$$

The convolution of $\tilde{S}_k(f)$ and $\tilde{G}_k(f)$ gives $\tilde{Y}_k(f)$,

$$\tilde{Y}_k(f) = \sum_{n=-\infty}^{\infty} S_k(n)\delta(f - nf_c) \otimes \sum_{m=-\infty}^{\infty} G_k(m)\delta(f - mf_{ssb}). \tag{5.18}$$

Convolution of delta functions effectively imprints the G spectrum on each harmonic of f_c. After substituting for $S_k(n)$ (5.13) and $G_k(m)$ (5.17),

$$\tilde{Y}_k(f) = \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} S_0(n)G_0(m)e^{\frac{j2\pi(m+n)k}{OSR}} \times \delta(f - nf_c - mf_{ssb}). \tag{5.19}$$

The total $\tilde{Y}(f)$ spectrum is the sum of each gated phase spectrum, $\tilde{Y}_k(f)$,

$$\tilde{Y}(f) = \sum_{K=0}^{OSR-1} \tilde{Y}_k(f), \tag{5.20}$$

$$= \sum_{K=0}^{OSR-1} \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} S_0(n)G_0(m)e^{\frac{j2\pi(m+n)k}{OSR}} \times \delta(f - nf_c - mf_{ssb}). \tag{5.21}$$

The above equation can be simplified if the summation of k is implemented first. It can be seen that a harmonic is produced only when $m + n =$ integer $\times$ (OSR). The exponential term sums to zero for all other combinations of m and n, when $m = i(OSR) - n$ and i is any integer, the output becomes

$$\tilde{Y}(f) = OSR \sum_{n=-\infty}^{\infty} \sum_{m=-\infty}^{\infty} S_0(n)G_0(m)\delta(f - nf_c - mf_{ssb}). \tag{5.22}$$

The amplitude of the harmonic is given by $S_0(n)G_0(m)OSR$ and the delta function gives its position in the spectrum. Any increase in OSR reduces the amplitude by similar amount since both $S_0(n)$ and $G_0(n)$ are proportional to $\frac{1}{OSR}$. Sometimes many harmonics have the same frequency and their contributions must be summed. However those with large m values will have small amplitudes because of the decay of the Sinc function. For this reason, spectra from the closest carrier frequency harmonics (small n) need only be considered. As an example, we set OSR=16 and $v = 2$ and $f_{ssb} = \frac{f_c}{16}$. The spectrum consists of a spur at DC ($m = 0, n = 0$) of amplitude $\frac{AvT_{clk}}{T_c} = \frac{2}{OSR}$. The desired SSB signal occurs about the first harmonic

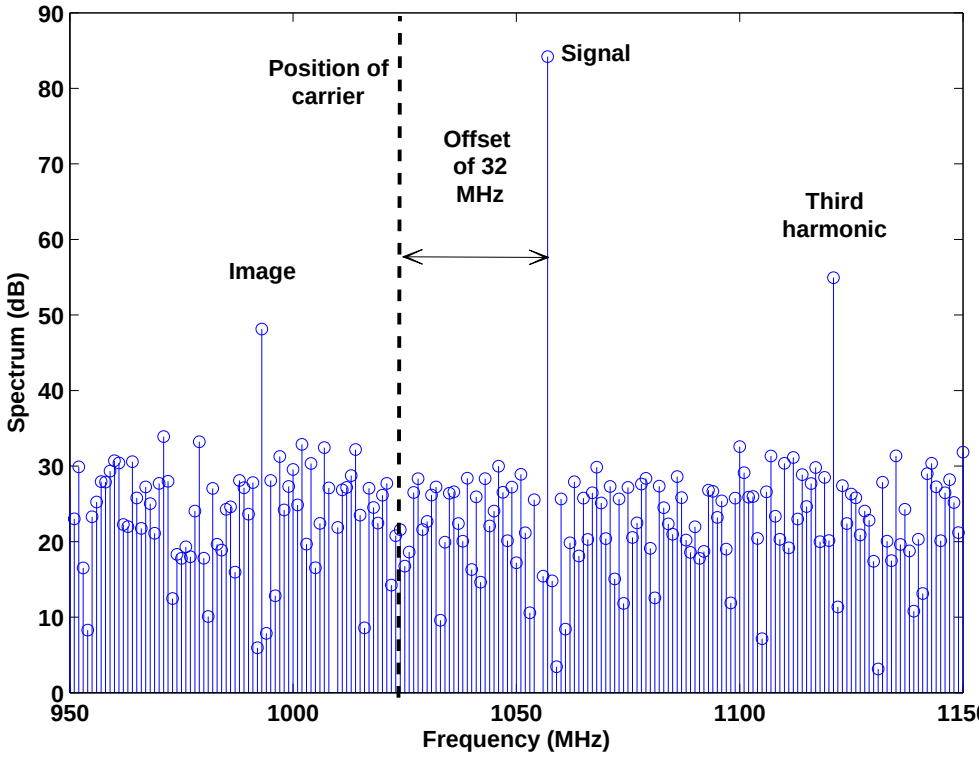

Figure 5.5: Upper SSB output spectrum from a Polar $\Sigma\Delta$. The distortions are from the PWM/PPM image and third harmonic. (f_c=1024 MHz and f_{ssb}= 32 MHz)

zone(f_c) with $n = 1, i = 0$ and $m = -1$ giving the lower side band at $f = f_c - f_{ssb}$. The undesired second harmonic (of f_{ssb}) occurring at $f = f_c - 2f_{ssb}$ folds back from the second harmonic zone at $2f_c$ ($n = 2, i = -1$ and $m = -16 - 2$). The third harmonic at $f = f_c - 3f_{ssb}$ folds back from the third harmonic zone at $3f_c$ ($n = 3, i = -2$ and $m = -32 - 3$ and the signal image at $f_c + f_{ssb}$ comes from the negative harmonic zone at $-f_c(n = -1, i = 2, m = 32 + 1)$. The upper side band signal can be obtained by changing the sign of the exponent of 5.17 which then reverses the sign of m in all the subsequent equations.

The current formulation is for a single ended (two state, 0 and A) signal only.

The above analysis can be extended to include the tri-state signal of Fig. 3.9 by modifying the expression for $s_k(t)$ in (5.3) to

$$s_k(t) = s(t + kT_{clk}) - s\left(t + kT_{clk} - \frac{T_c}{2}\right). \tag{5.23}$$

The spectrum of this signal can be obtained by the normal time shifting property. The result of adding this term is to double the signal level for all odd harmonics of f_c and to zero all even harmonics of f_c. This effectively eliminates the folded spectrum from the even harmonic zones (n, even) which include the DC term and the even harmonics of f_{ssb} as shown in Fig. 5.1.

5.4 Distortion Analysis in a Single Carrier Environment

In this section, the phenomenon is simulated and measured in a single carrier environment. All simulations were performed in $Matlab^{®}$. This section also presents a plot showing calculated, simulated and measured results in agreement.

5.4.1 Simulation Results

Here, the test signal is a SSB tone, offset by 32 MHz from f_c which is 1024 MHz. The $OSR_{\Sigma\Delta}$ is 128. Fig. 5.1 shows the spectrum plot of the SSB signal obtained at the output of the 'polar to PWM/PPM' block for the Cartesian $\Sigma\Delta$ structure. The position of the reference carrier is drawn for illustrative purposes. The signal can be observed (32 MHz offset from f_c). The image (-32 MHz from f_c) and the third harmonic (96 MHz from f_c) can be seen rising far above the noise floor. It can also be noted that the average noise floor is much lower compared to the similar

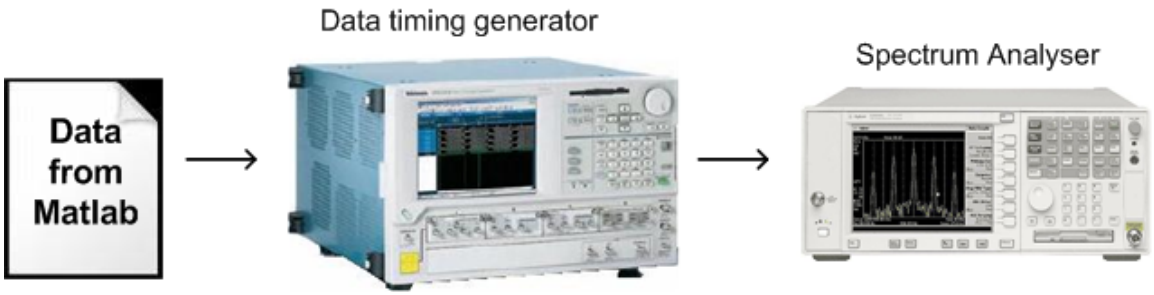

Figure 5.6: Experimental setup for measurement of a two-level waveform.

spectrum plot in Fig. 5.5 where the $\Sigma\Delta$ filtering was performed on polar signals [75]. The noise shaping in Fig. 5.5 is also less evident compared to Fig. 5.1.

5.4.2 Experimental Setup And Measurements

The *Tektronix*® data timing generator can output an arbitrary sequence of pulses and can be used with a spectrum analyser for the practical measurement of a 2-level waveform (Fig. 5.6). A SSB tone is simulated in *Matlab*® and the output PWM/PPM data are stored to a file. The data are programmed in the data timing generator and a suitable f_{clock} (less than 2.4 GHz in this case) is chosen. (Note: All frequencies are scaled to f_{clock} and therefore reducing f_{clock} will reduce both f_c and the signal bandwidth by the same fraction.) The data timing generator is then connected to a spectrum analyser to obtain the spectrum. A SSB signal is simulated in such a way that it exactly repeats after a fixed number of clock periods (equal to the size of the data file). The *Tektronix*® data timing generator can then loop through the memory without causing signal discontinuity. Fig. 5.7 shows a plot of simulated, calculated and measured values of the image, the second harmonic and the third harmonic against varying offset frequency, f_{ssb}. The OSR is kept to 32

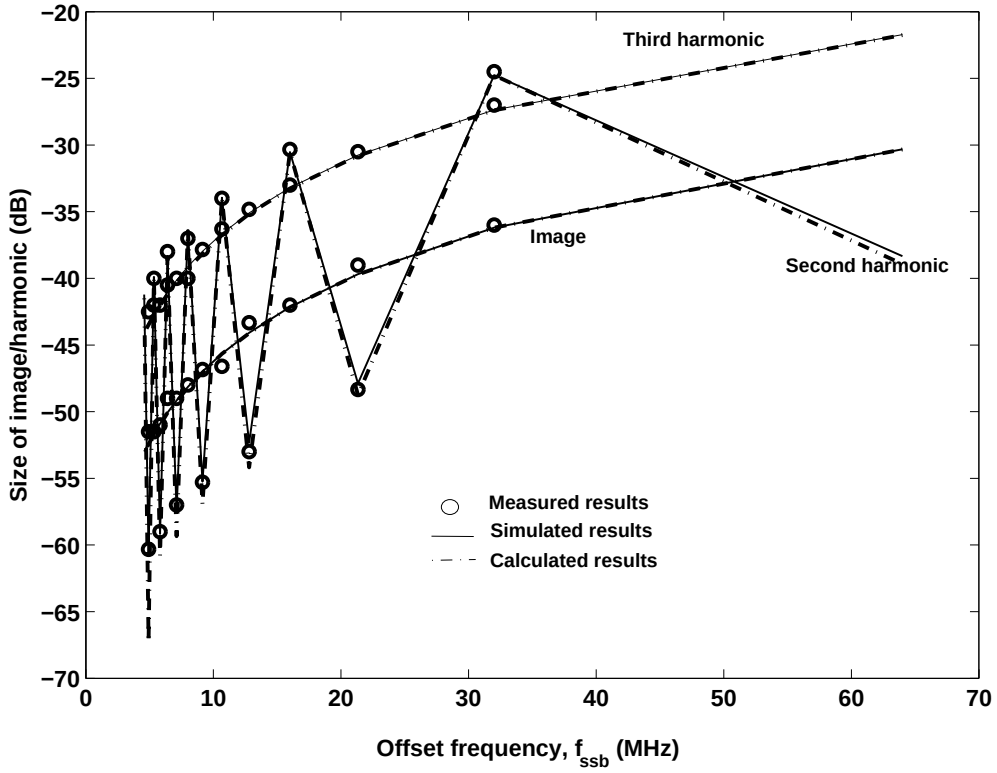

Figure 5.7: SSB harmonics and image. Amplitude (relative to desired signals) vs. f_{ssb}. (OSR=32, f_c=1024 MHz)

and f_{ssb} varied up to $\frac{f_c}{16}$. The higher the value of f_{ssb}, the larger the distortion, because the switching transients occur more often. A doubling of f_{ssb} increases the distortion products by approximately 6 dB. The size of the second harmonic oscillates between a lower and an upper limit depending on the ratio of f_c and f_{ssb}. An even ratio produces the upper limit while an odd ratio produces the lower boundary (Fig. 5.7). The second harmonic curve does not exist for the three-state signal (Fig. 3.9), but does if only a two-state signal is used. The close proximity to the desired signal and the dominant nature of the second order distortion justifies the additional expense associated with the implementation of a bridge amplifier

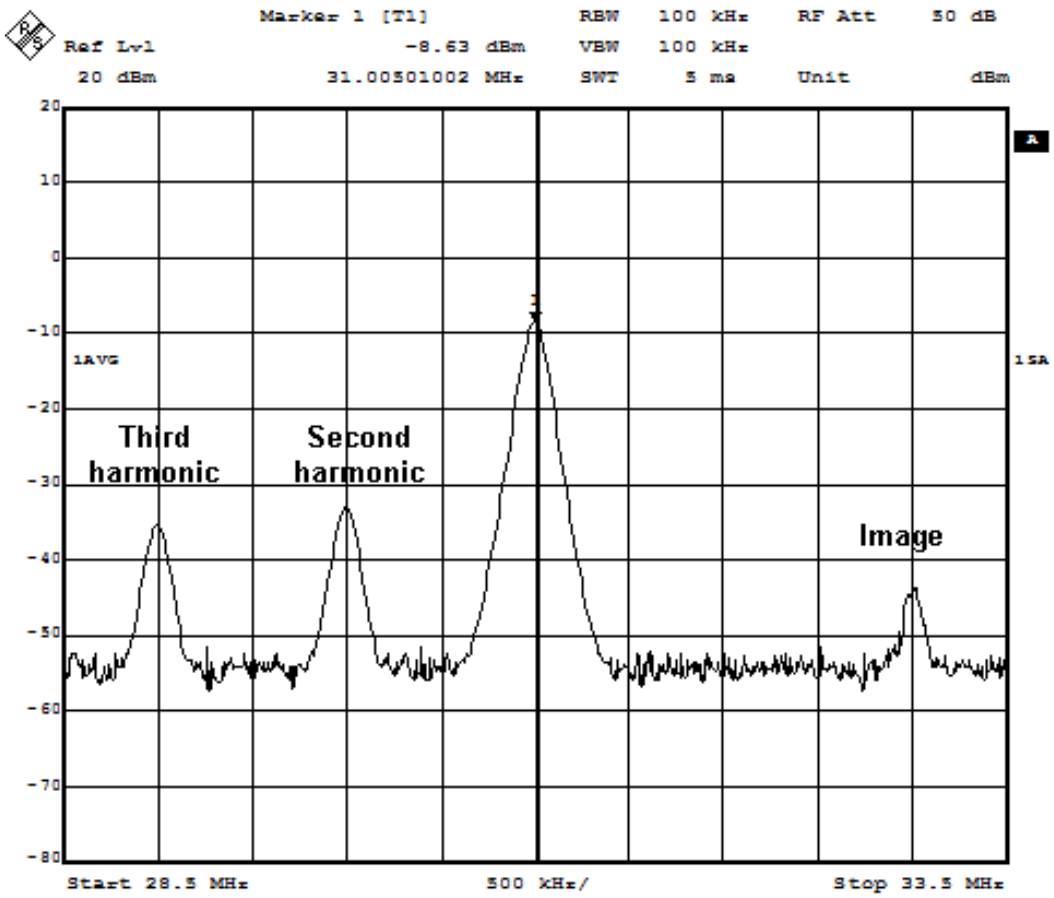

Figure 5.8: Measurement spectrum of lower SSB tone. (f_{clk}= 1024 MHz, f_c= 32 MHz, f_{ssb}=1 MHz ($\frac{f_c}{32}$), OSR=32)

structure to make the three-state signal. The dotted lines on Fig. 5.7 show the evaluated results from equation (5.22). The markers on Fig. 5.7 show the measured results. Close agreement between the simulated, calculated and measured values is observed. A spectrum plot showing the second harmonic, third harmonic and image is shown in Fig. 5.8.

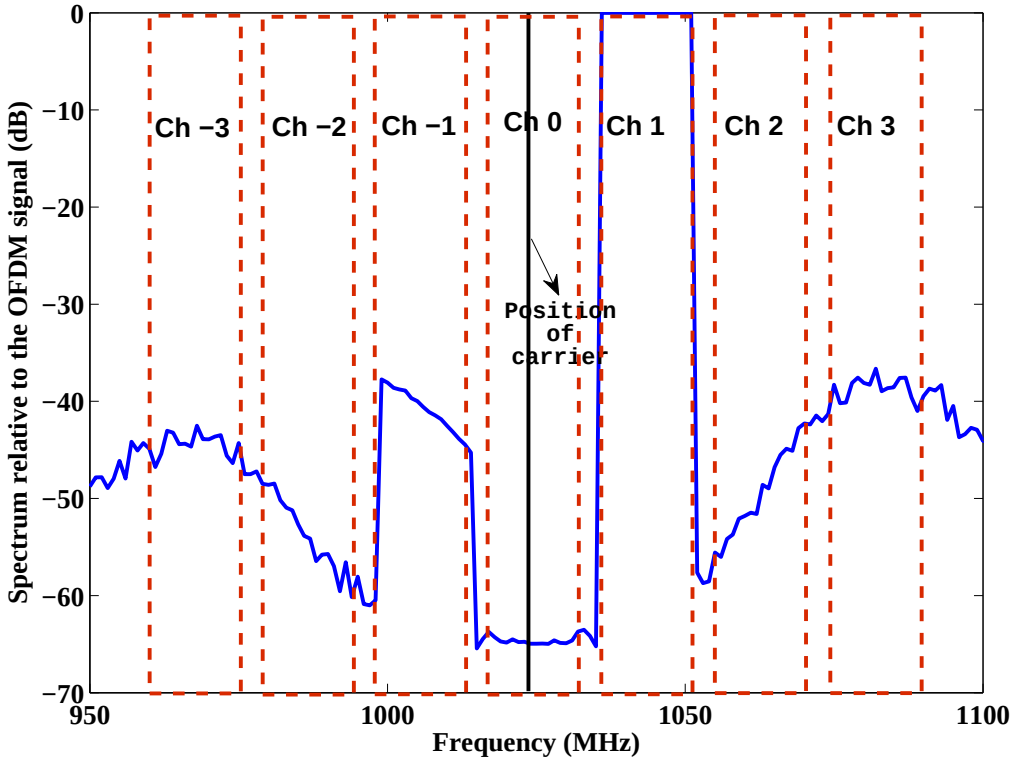

Figure 5.9: Spectrum plot of Cartesian ΣΔ scheme with offset OFDM signal. (OSR=64, f_c=1024 MHz and Offset= 20 MHz (1 channel))

5.5 Distortion Analysis in a Multi-Carrier Environment

5.5.1 Simulation Results

A QPSK-modulated OFDM input signal with a worst case peak to average power level of 8 dB was used to test the architecture. The $OSR_{\Sigma\Delta}$ is 128 and defines the sampling frequency of the ΣΔ. The OFDM bandwidth (B_{ofdm}) was set at $\frac{f_c}{64}$ equivalent to a B_{ofdm} of 16 MHz (similar bandwidth to 802.11g, LTE and WIMAX) with f_c=1024 MHz. The OFDM signal has 16 subcarriers. There is a guard band between adjacent channels of $0.25B_{ofdm}$. The signal was shifted one channel to the

right to examine the resultant spectral images. The ACPs which are defined as the noise power in the adjacent channel divided by the signal power, were calculated. The noise power includes quantisation noise as well as distortions arising from PPM. The simulations were performed on both polar and Cartesian $\Sigma\Delta$ architectures.

A spectrum plot of a pulse waveform with an RF carrier OSR of 64 and an input signal level, u=-7 dB (with respect to $u_{rms} = 1$) obtained at the output of the Cartesian $\Sigma\Delta$ architecture is shown in Fig. 5.9. The six adjacent channels and the position of the carrier are drawn on the figure to facilitate the understanding of the plot. The signal is present in channel 1. The image is present in channel -1 and the third harmonic is situated in channel 3 with the highest noise. The noise is lowest in channel 0 as the NTF of the $\Sigma\Delta$ operates from f_c and maximum attenuation of quantisation noise occurs around that region. This figure will be more elaborately discussed in Section 5.5.2.

Fig. 5.10 shows a plot of input level (dB) against ACP (dB) for the six adjacent channels obtained after simulating the Cartesian $\Sigma\Delta$ scheme. Again, it can be observed that channel 3 which represents the third harmonic has the highest noise. Channel -1 representing the image has the second highest noise. Channel 0 has lower noise than channel 2 as channel 0 is centered at f_c. This plot further validates the conclusions drawn from Fig. 5.9.

Fig. 5.11 shows a plot similar to that of Fig. 5.10 but for a polar $\Sigma\Delta$ architecture. The characteristics of the input test signals and the OSR for both architectures are kept the same. The overall performance of the polar $\Sigma\Delta$ is worse than the Cartesian

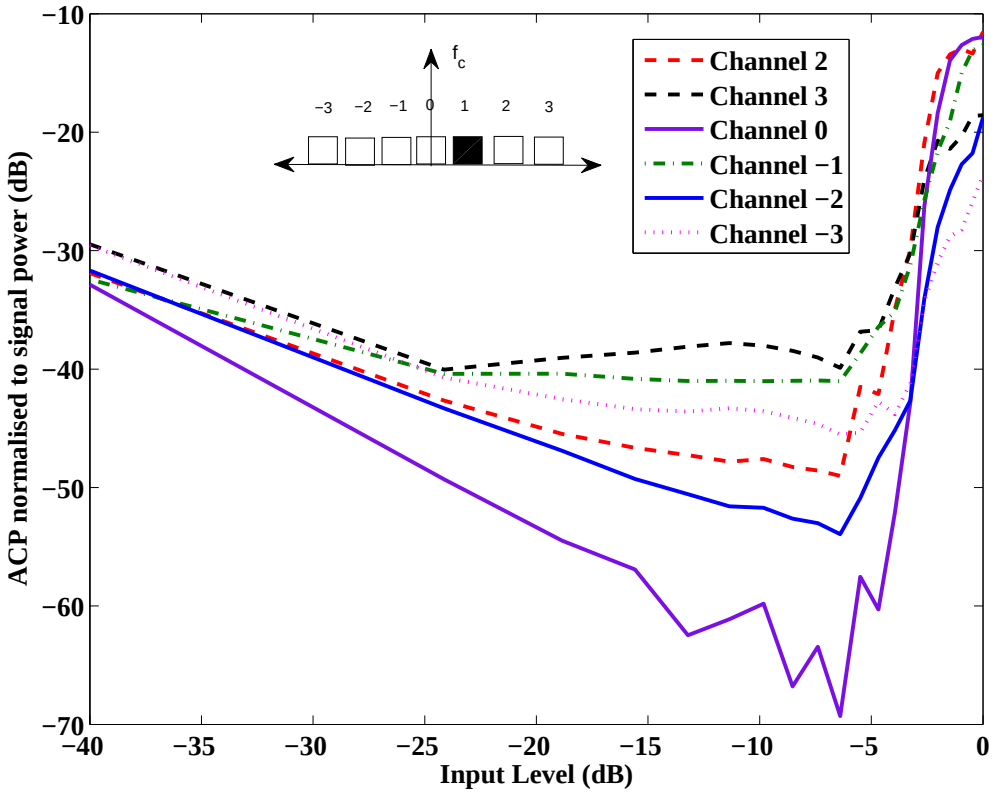

Figure 5.10: Cartesian ΣΔ scheme - ACP in adjacent channels vs. input level. The signal is in channel 1 (OSR=64).

structure as the polar one has an inherently higher noise floor. Once more, it can be observed that the third harmonic is the biggest noise contributor followed by the image.

Table 5.1 helps to further illustrate the effect of offset on ACP. It gives a comparison of ACP values for both polar and Cartesian ΣΔ with offset and without offset. The values were obtained at an input level of -7 dB ($u_{rms} = 1$). Shifting the signal to channel 1 increases the noise in all channels. Those channels containing the odd harmonics are particularly affected with noise. Increases of 20 dB (channel 3), 15 dB (channel -1) and 13 dB (channel -3) are observed for the Cartesian ΣΔ scheme.

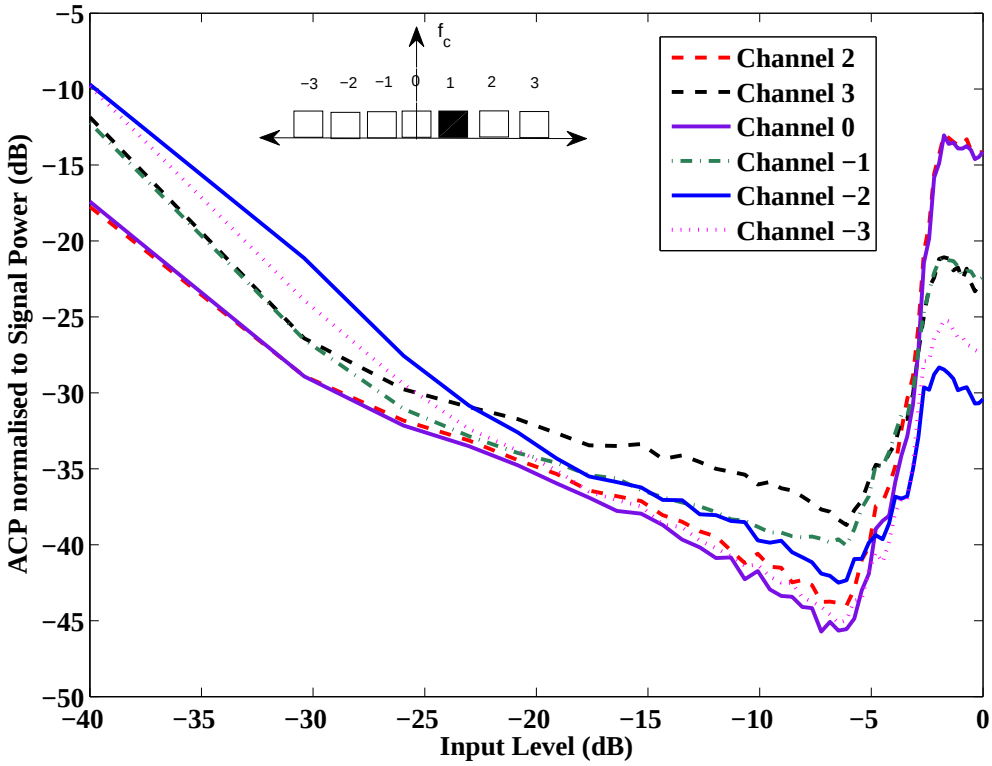

Figure 5.11: Polar ΣΔ scheme - ACP in adjacent channels vs. input level. The signal is in channel 1 (OSR=64).

In the polar ΣΔ, increases of 7 dB (channel 3) and 6 dB (channel -1) of noise are observed. A reduction in the noise can be seen in the channel 0 as the NTF of the ΣΔ operates from f_c.

Even though the noise increase in the channels of the polar ΣΔ due to the offset is lower than the Cartesian scheme, the overall ACP performance is significantly worse.

However, even the Cartesian scheme will require a higher oversampling rate to meet the WLAN standard (ACP <-40 dB) or f_c can be increased to reduce the relative offset frequency. Increasing f_c by 2.5 will reduce the main interference

Table 5.1: ACP for Cartesian and polar ΣΔ with offset and without offset.

Channels	-3	-2	-1	0	1	2	3
Cart ΣΔ ACP no offset (dB)	-57	-59	-54	Data	-55	-59	-57
Cart ΣΔ ACP 1 channel offset (dB)	-44	-50	-39	-69	Data	-47	-37
Polar ΣΔ ACP no offset (dB)	-45	-45	-45	Data	-45	-45	-45
Polar ΣΔ ACP 1 channel offset (dB)	-44	-42	-39	-46	Data	-44	-38

channels by 8 dB which should then meet the WLAN specification (Equation 5.22). Alternatively, the WLAN standard is easily met if the signal is not shifted to the adjacent channels. In fact, in this case the OSR can even be reduced from 64 to a value as low as eight [33].

5.5.2 Experimental Setup and Measurements.

In this thesis, a three-step waveform is used for the multi-carrier measurements. Since the data timing generator can only produce two-level waveforms, a combiner circuit is needed. The two channels of the data timing generator are set to output two streams of data simultaneously. The data of one of the channels is inverted and is out of phase by π radians. The combiner circuit uses the two streams of data to produce a three-level waveform. The combiner circuit is then connected to a spectrum analyser as shown by Fig. 5.12. Spectrum measurement was performed using multi-carrier signals to further substantiate our findings. The Cartesian architecture was used as it has a lower noise floor making the harmonics and images more visible. An OFDM signal with an input level of -7 dB ($u_{rms} = 1$) was programmed into the data timing

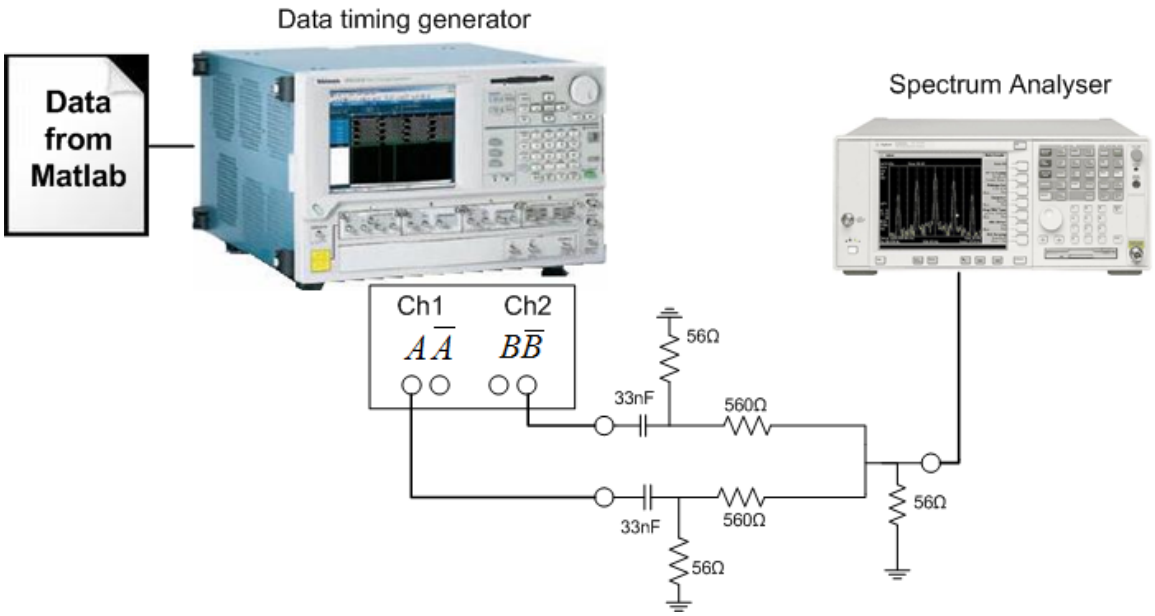

Figure 5.12: Experimental setup for measurement of a three-level waveform.

generator. A three-level waveform (Fig. 3.9) was used as it suppresses the even harmonics. Fig. 5.13 shows the spectrum analyser display for a pulse waveform with an OSR of 64. The images and harmonics which arise as a result of the offset are clearly visible. The measured result agrees with simulations (Fig. 5.9), except for some small artifacts in channel 0 of the measured signal. The discrepancies can be attributed to the limitation in the slew rate capability of the experimental setup and the mismatches in the positive and negative going waveforms. The negative slope of the signal image in channel -1 can be explained by the fact that OFDM is made up of many individual tones. As the offset between the tones and f_c increases, the size of the distortions of each tone image increases as shown by Fig. 5.7. The third harmonic and the image of the third harmonic are smeared over a number of channels, but most of the energy is concentrated within channel 3 and -3 respectively.

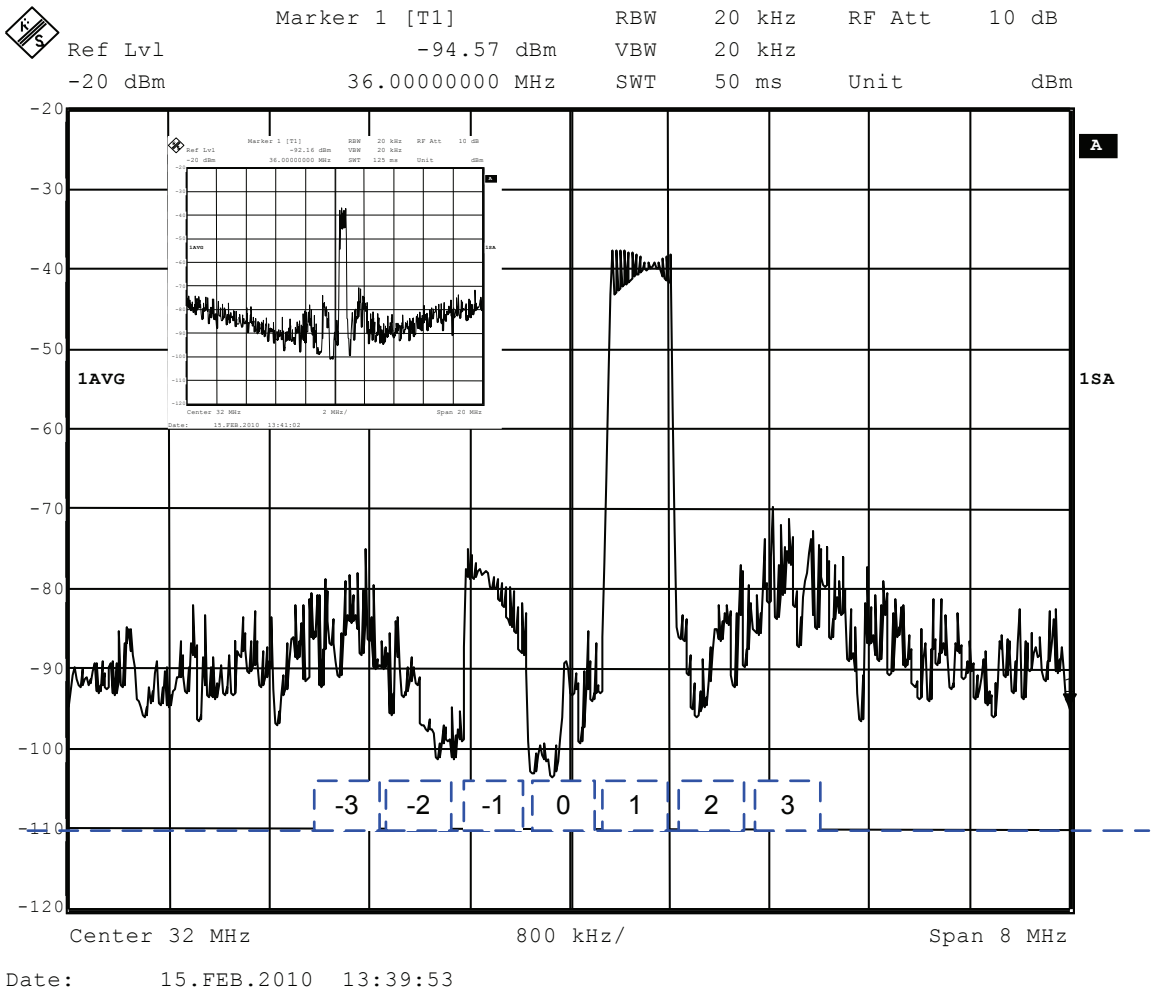

Figure 5.13: Spectrum measurements. f_c=32 MHz and an OSR=64. The channels are shown. The insert displays a wider spectrum view of the same signal.

It is quite evident that the inband noise is dominated by the distortions as a result of the 'polar to PWM/PPM' conversion whereas the out-of-band noise is dictated by the noise shaping effect of the $\Sigma\Delta$. This is illustrated by the gradual rise in the noise level at the extremities of the spectrum as shown by the wide span view (Fig. 5.13).

5.6 Summary

This section has identified a problem occurring when quantised phase shifts are converted to pulse positions in a digital 'polar to PWM/PPM' block. The quantisation in phase causes significant distortion. This chapter proposes a mathematical expression (Equation 5.22) to predict the amplitude and frequency of the distortion products generated from an SSB input signal. It also demonstrates that the distortion increases with increasing offset frequency by almost 6 dB/octave. In this senario, the offset frequency must be less than 0.6 % of f_c to keep distortions less than -40 dB for narrowband signals (Fig. 5.7). Increasing the OSR helps to alleviate the problem (-6 dB/octave), but it also reduces the maximum carrier frequency. The use of higher order $\Sigma\Delta$ structures will not be effective either, since the PPM distortion dominates the in-band spectrum. (Note: The 'polar to PWM/PPM' block is not enclosed in the $\Sigma\Delta$ feedback loop.) A potential solution is to avoid quantising the phase by using analog techniques [70] but this removes many of the advantages of this all-digital structure.

In a multi-carrier environment, measurements and simulations show that it is best to avoid changing channels by offsetting the carrier frequency because of increasing adjacent channel interference in odd harmonics channels. Some of the distortions can be cancelled by using a bridge amplifier structure to give a three-level signal. In order to meet the WLAN standard, it is preferable to accommodate any channel change by altering the system clock frequency, f_{clock}, in which case WLAN specifications can be met with a much reduced OSR.

Chapter 6

Conclusion and Further Research

This work forms part of a concept design of a new 'green' digital base station transmitter utilising efficient SMPAs. The program goal was to see how close a switching architecture could get to a bandwidth of 100 MHz, a maximum power of 100 W and 100% efficiency while meeting spectrum requirements of popular standards such as WLAN and 3GPP. The work in this thesis concentrates on the up-conversion structure, where the challenge was to obtain the bandwidth requirement using an all-digital architecture. A 100 MHz bandwidth could be reached with a clock frequency of 32 GHz. This is well beyond current technology at high power levels.

In the literature review, the SMPAs are studied first as they are the main component of the new architecture. The concept of $\Sigma\Delta$ modulators is explained. A list of the known transmitter architectures are also evaluated.

A new $\Sigma\Delta$-based transmitter architecture is proposed in Chapter 3. The output is a pulse train with a maximum of one pulse per half period, thus limiting the number of switching cycle to boost efficiency. It is shown that the new Cartesian $\Sigma\Delta$ scheme outperforms its polar counterpart giving an additional 10 dB reduction

in ACP(1). In order to meet the original bandwidth requirement of 100 MHz, at least the first and second adjacent channels should be below the specified transmission mask (assuming 20 MHz channel). An OSR of eight is sufficient to meet the WLAN specifications and an OSR of 20 is needed for the more stringent 3GPP specifications. These figures imply clock frequencies of 8 and 20 GHz respectively. These values are not possible using today's technology particularly at high power.

Next, the MSE of the non-uniform polar quantisers is analysed. A closed-form equation is derived for the MSE for a circular symmetric Gaussian input signal. Simulation results of the MSE with different OSR values corroborate the theoretical analysis. Simulations are also performed for the non-uniform polar quantiser embedded in the $\Sigma\Delta$ modulator. The presence of $\Sigma\Delta$ modulators boosts the overall quantisation noise, while minimising it in the band of interest. Mathematical derivations were used to analyse this phenomenon at both low signal levels and high signal levels. The low signal range is particularly interesting, since the slope of the MSE vs. input level drops from 1 dB/dB for the raw quantisation to 0.5 dB/dB when the quantiser is combined in a $\Sigma\Delta$ loop.

In chapter 5, the spurious tones present in the output spectrum of the 'polar to PWM/PPM' block are attributed to the PPM process. The adoption of a three-level waveform (push-pull amplifier architecture) can reduce or even eliminate many of the distortions. The chapter presents a mathematical analysis of the distortions predicting the size and position of the unwanted spurs. Simulation and measurement results support the findings. It was observed that the size of the distortions grows

by 6dB/octave with increasing offset frequency and so the latter must be less than 0.6% of f_c to guarantee distortions under -40 dB transmission mask of the WLAN standard. This eliminates the possibility of offset carrier operation from the same nominal carrier frequency. Simulations and measurements were also conducted using an input multi-carrier signal (OFDM). It was found that offsetting the carrier frequency increases adjacent channel interference in odd channels. If the OFDM signal is centered about the nominal carrier frequency, then the distortions show up as intermodulation skirts on the OFDM spectrum (Fig.3.14). Sometimes, this makes ACP(1) slightly larger than ACP(2), however the skirts are still well below the 3GPP specifications.

6.1 Further Research

6.1.1 Improving Amplitude Quantisation for Low Signal Levels

The quantised amplitude levels, $\hat{R}$ and the threshold levels are calculated by evaluating the fundamental spectral component of the repeating three-level waveform. The different values of $\hat{R}$ are calculated by changing the pulsewidth in increments of two clock periods. This leads to coarse quantisation at low signal levels. Since Rayleigh distributed signals have PDFs in the low signal levels, MSE values would improve if the quantisation levels are lower. Therefore in future work, it is possible to reduce the pulsewidths by one cycle while still having a constant phase reference ((1, 3, 5,...) instead of (2,4,6,...)) as marked by crosses on Fig 6.1. This new scheme will target the lower signal levels. Further, we can extend this to include both even

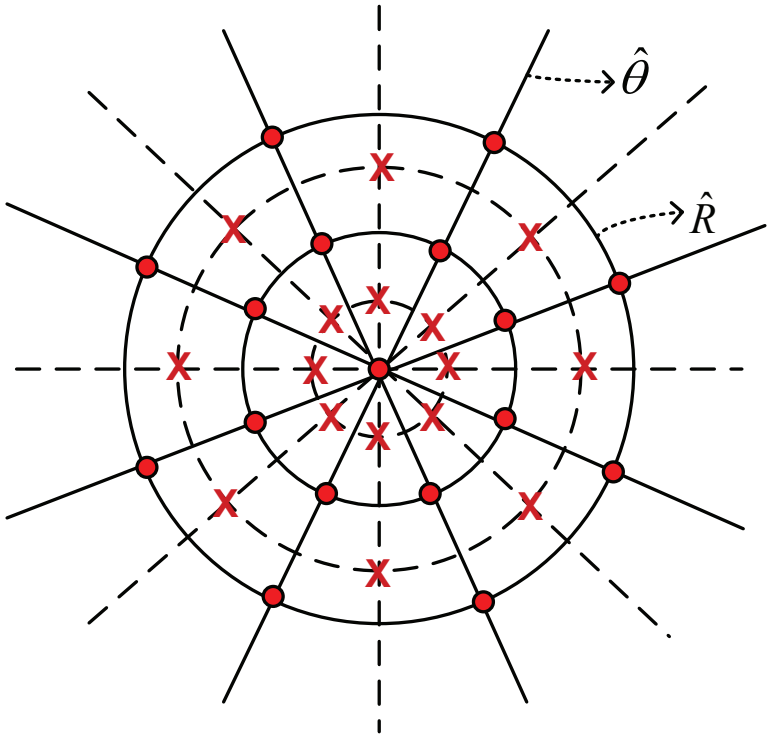

Figure 6.1: Quantisation plane showing joint quantisation. Circle - even pulsewidths and crosses - odd pulsewidths.

and odd quantisation as shown in Fig 6.1. This will however increase quantiser complexity since the phase reference changes for even and odd pulsewidths.

6.1.2 Pre-distortion

In Chapter 5, simulation and measurement results show the in-band noise is dominated by the distortions as a result of the 'polar to PWM/PPM' conversion. The distortions are mainly images and harmonics. In a multi-carrier environment, the shape of the distortions are distinct (particularly the image components) and their positions are known as shown in Fig 5.13. Since the distortions are in-band, they cannot be filtered out. Digital pre-distortion of the input multi-carrier signal can help to cancel most of the spurious tones since the mechanism by which they are

generated is known. The spectrum will improve leading to a better ACP which will help to eventually meet the WLAN standard with offset carrier.

6.1.3 Addressing High Clock Frequencies

The research shows that to obtain acceptable performance in WLAN and cellular bands, the f_{clock} must be 8 or 20 times f_c. Currently f_c is 2 GHz for cellular bands and 5 GHz for WLAN, therefore f_{clock} needs to be at least 40 GHz. Such clock frequencies are not possible using today's technology. The sampling frequency would have to be increased by a factor of ten if operation at cellular frequencies is to be achieved. Today's digital transistors have an Ft (cut-off frequency) beyond 218 GHz (Intel 32-nm process [78]). Therefore, there is a potential to use controlled digital delay lines and phase locked loop techniques to generate oversampled clocking edges typically between 1/8 or 1/16 of the sampling period. This can be done on-chip. Future research would investigate the matching requirements of the delay elements given typical process variations to see if the required timing accuracy can be met.

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