VICTORIA UNIVERSITY OF TECHNOLOGY

THE DESIGN OF AN H_∞ VOLTAGE REGULATOR FOR A PREDICTIVE CURRENT CONTROLLED THREE PHASE PWM POWER CONVERTER

A Thesis Submitted for Examination for the Degree of Master of Engineering in Electrical and Electronic Engineering

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DECLARATION

This thesis contains no material which has been accepted for the award of any other degree or diploma in any university or other institution. To the best of my knowledge the material is original and has not been previously written or published by any other person, except where due reference is made in the text of the thesis.

Ming YU

30th June 1999

ABSTRACT

In this project, an H_∞ controller is proposed as a DC voltage regulator for the predictive current controlled pulse width modulated (PWM) three-phase power converter to compensate the uncertainty caused by the predictive current controller. The H_∞ theory has its unique approach to the uncertainty issue, its design method allows both the stability robustness and performance robustness to be considered at the design stage.

The design of the H_∞ voltage regulator is based on the worst case scenario where the converter is subject to a load disturbance and its operation mode is changed from the rectifying to the regeneration, consequently, parameters and structure of the original plant transfer function derived, vary significantly. The proposed H_∞ (DC) voltage regulator is to overcome the uncertainty problem and to work with the predictive current controller to achieve robust control of the entire system.

The combined control scheme is simulated using MatLab/SIMULINK environment. The simulation results show that the closed-loop system is capable of achieving performance robustness and stability robustness for the worst case scenario. The output DC link voltage is stable and nearly sinusoidal, while the line currents are delivered with a unity power factor.

A computer controlled three-phase PWM converter of 10kVA is developed and tested in the open-loop condition, and the performance of the power converter is examined. An INTEL industrial PC-486 single chip computer is used as a digital controller. For a given modulation index and output frequency, switching intervals are calculated using the space vector PWM algorithm, and are down loaded to a PWM generator board which synthesizes gating pulse to six switching devices (IGBT). There is a on-board synchronizing unit which synchronizes the fundamental frequency of the gating pulses with the mains. A computer program is developed in Borland C++ to perform the modulation process. The experimental results show that the developed converter system is ready to be used as a test

bed for conducting experimental research in the area of converter control and machine control.

To summarize the work accomplished by the author for this project:

1. The introduction of the H_∞ control theory into the application of converter control and theoretical design of the H_∞ voltage regulator;

2. The simulation of the entire closed-loop controlled power converter with the combination of a predictive current control and a H_∞ voltage regulator;

3. The development of a computer controlled three-phase PWM power converter as a test bed.

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INTRODUCTION AND LITERATURE REVIEW

1.1 INTRODUCTION

Over the last three decades, there have been considerable advances in the design of variable frequency drivers. Most power converters on the market today are link type converters in which an uncontrolled rectifier with a stiff DC voltage supplies an insulated gate bipolar transistor (IGBT) or bipolar junction transistor (BJT) inverter bridge. A fairly large capacitor is required in the DC link.

The uncontrolled converter with a large capacitor has a slow dynamic response of DC voltage output and a very poor line current waveform with a large harmonic component which is fed back into the supply network that causes harmonic pollution [1-2]. The supply authorities intend to draw up more restrictive regulations to inhibit such harmonic pollution. In order to satisfy such new regulations, the AC drives may be redesigned to use controlled converters. One approach is to replace the uncontrolled diodes with transistors such as GTO (Gate Turn Off) or IGBT (Insulated Gate Bipolar Transistor). By controlling the gating signals to these transistors, it is possible to produce sinusoidal current waveforms with a unity power factor at the utility side. This permits a substantial reduction in the size of the DC link capacitor and bidirection power flow between the utility and the load [3-12].

Intensive research work has been carried out in the area of converter control. The work can be divided into two major tasks, the design of a controller (or compensator) and a modulator. Their functions are explained respectively as follows.

(1) The controller is designed based on the specifications such as fast dynamic response of DC voltage, unit power factor and stability of the entire system. The control outputs are in the form of voltage modulating waveforms, which are fed into the pulse width modulator.

(2) The pulse width modulator generates gating signals to each transistor of the power converter in terms of the reference inputs from the controller. The switching strategy is selected based on specifications of harmonic performance of the line current, electro-magnetic interference (EMI) and the efficiency of the converter. For a given switching strategy, the modulator calculates switching pulses in terms of modulation signal, and then outputs them to switching devices of the converter. Within the linear modulation range, the fundamental component of the switching pattern should be proportional to the sinusoidal modulating waveform.

1.2 REVIEW OF THE MODULATOR SCHEME

It is possible, by surveying the literature over the last decade, to trace the historical development of pulse width modulator (PWM) techniques and relate these developments to the changes in technology. The delta current regulator, hysteresis current controller, ramp comparison regulator and natural sampled PWM regulator have been widely used because of their ease of implementation using analogue techniques. More recently, a switching strategy referred to as 'Regular' sampling, has been proposed which is considered to have a number of advantage when implemented using digital or microprocessor techniques. The approach uses the so-called 'Space Vector' and has drawn attention because space vector modulation is able to lead to a reduced harmonic current ripple compared to other modulation strategies.

1.2.1 DELTA CURRENT REGULATOR

Among the various well-known current regulated PWM (CRPWM) algorithms, the delta current regulator has an extremely simple and robust structure, and excellent dynamic performance [3]. The switching frequency is bounded by the sampling frequency (T_s). However, the steady state performance of the regulator is very poor. The harmonic content is large. The wide harmonic spectrum includes frequencies from the subsynchronous range to the sampling frequency range. The regulator can not effectively utilize the converter

zero states and requires high sampling frequency, hence high average switching frequency as shown in Fig. 1.1. S1 and S2 are drive signals.

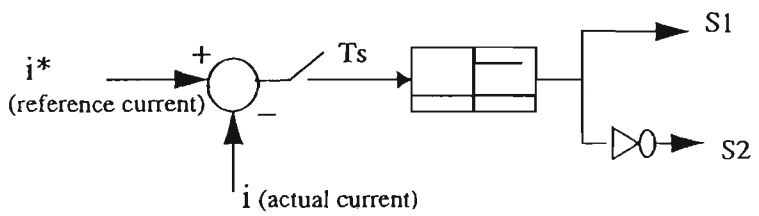

Fig. 1.1 Per Phase Delta Current Regulator Structure

1.2.2 HYSTERESIS CURRENT CONTROLLER

The hysteresis current controller is an important PWM technique that is applicable to voltage source converter and inverter [13-14]. A simplified diagram of a typical hysteresis current controller is shown in Fig. 1.2.

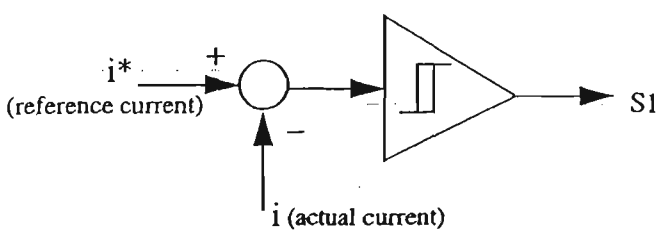

Fig. 1.2 Hysteresis Current Regulator

It can be seen from Fig. 1.2 that the current is detected and compared to the current reference using independent hysteresis comparator which has a hysteresis band, with comparator output signal being used to produce the drive signal (S1) for phase leg power switches. When the phase leg current becomes greater (or less) than the target current by an amount equal to the hysteresis band, the phase leg is switched in the negative (or positive) direction. This provides an instantaneous current limit and forces the actual current to track the reference current within the hysteresis band by toggling the upper and lower phase leg switches. The hysteresis current controller is simple to implement by hardware, the peak to peak current ripple is directly controlled and response time of the current controller is fast. However, the switching frequency will vary over a fundamental period since the hysteresis band specifies the current ripple and the load current harmonic ripple can be substantial.

1.2.3 STATIONARY FRAME RAMP COMPARISON REGULATOR

The stationary frame ramp comparison regulator (SFRC) is one of CRPWM strategies [3] as shown in Fig. 1.3. The SFRC has a simple structure and provides well-defined harmonic spectrum. The regulator has nonzero steady state error because it operates on AC signals. If the controller gain K_p is not changed in the proper direction, the phase and magnitude error of the regulator degrades the performance as the operating point is varied.

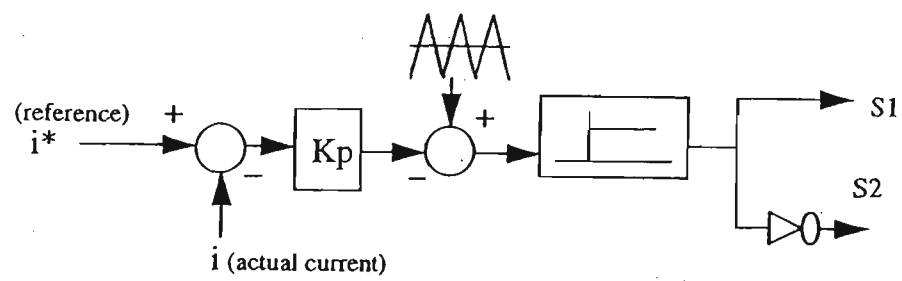

Fig. 1.3 Phase SFRC Current Regulator Structure

1.2.4 NATURAL SAMPLED PWM

Most analogue implemented PWM schemes employ natural sampling technique [5]. It can be seen that a triangular carrier wave is compared directly with a sinusoidal modulating wave to determine the resultant pulse widths, which are illustrated in Fig. 1.4. It is important to note that, because of the instantaneous intersection of two waves, the resultant pulse width is proportional to the amplitude of the modulating wave at the instant that switching occurs. This has two important consequences: the first is that the centers of the pulses in the resultant PWM wave are not uniformly spaced, secondly, it is not possible to define the widths of the pulses using analytic expressions. It is not possible to calculate the widths of the modulated pulses directly, because of the transcendental relationship exiting between the switching time.

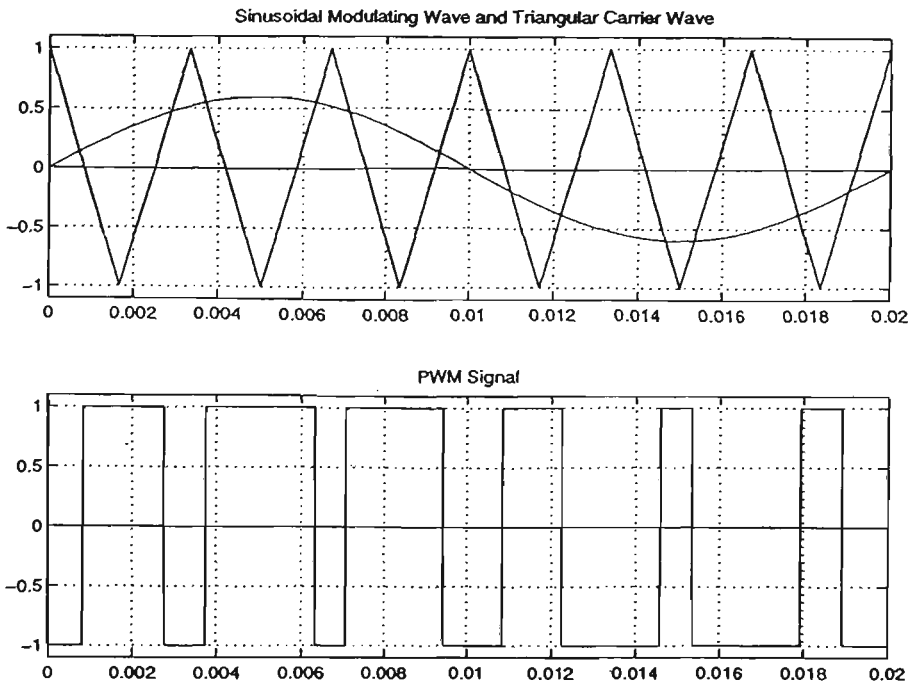

Fig. 1.4 Natural Sampled PWM

1.2.5 REGULAR SAMPLED PWM

Regular sampled PWM is recognized to have certain advantages when implemented using digital or microprocessor techniques [5]. The amplitude of the modulating signal at the sample instant is stored by a sample and hold circuit and is maintained at a constant level during the intersample period until the next sample is taken. This produces a sample hold version of the modulating signal. Comparison of sample hold signal with the carrier signal defines the points of intersection used to determine the switching instants of the width-modulated pulses as shown in Fig. 1.5. As a result of this process, the modulating wave has constant amplitude while each sample is being taken, and consequently the widths of the pulses are proportional to the amplitude of the modulating wave at uniformly spaced sampling time. It is an important characteristic of regular sampling that the sampling positions and sampled values can be defined unambiguously, such that the pulses produced are predictable both in width and position. It should be noted that this was not the case in the natural sampled process, as discussed previously. Because of this ability to define precisely the pulse configuration, it is possible to derive a simple trigonometric function to calculate the pulse widths.

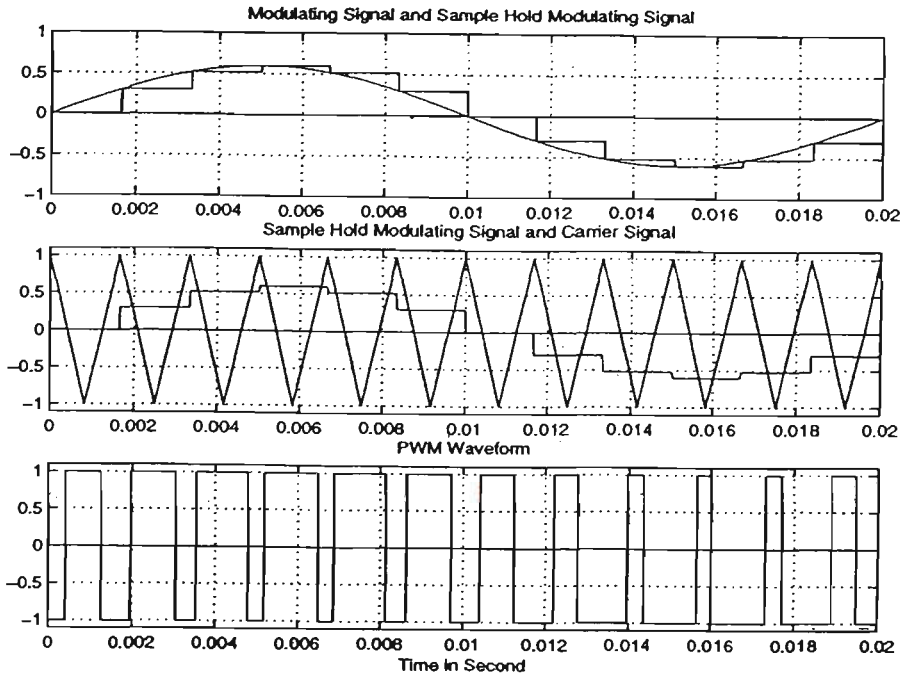

Fig. 1.5 Regular Sampled PWM

1.2.6 SPACE VECTOR PWM

The traditional triangular carrier method has been largely superseded by the 'space vector' representation more suitable for digital implementation. In this paragraph some basic features of this method will be reviewed and the relation with the traditional sine triangle method will be emphasized [4][10-11].

In order to understand space vector PWM, once again look closely at Fig. 1.5 to see what happens inside one switching period in the case of a single carrier and sinusoidal voltage reference 120-degree apart. If the signal is high, the top switch of the selected leg is closed. On the other hand, if the signal is low, the bottom switch is closed instead. The three phase converter is constituted by six switches and there are eight possible configurations, as shown in Fig. 1.6 (a). In correspondence of each configuration, the six switches have a well-defined state: on or off. As a consequence, all the possible rectifier configurations can be identified. When the switch on the top is on, the top bit is 1 and the bottom bit is 0, and vice versa, for example, switching state S_4 in Fig. 1.6 (a) is 011, S_5 is 001 and so on.

In a three-phase system, the three sinusoidal voltages, 120 degree apart, can be represented by a rotating vector, V, whose projections on the three-phase axis are, instant by instant, the three sinusoidal values.

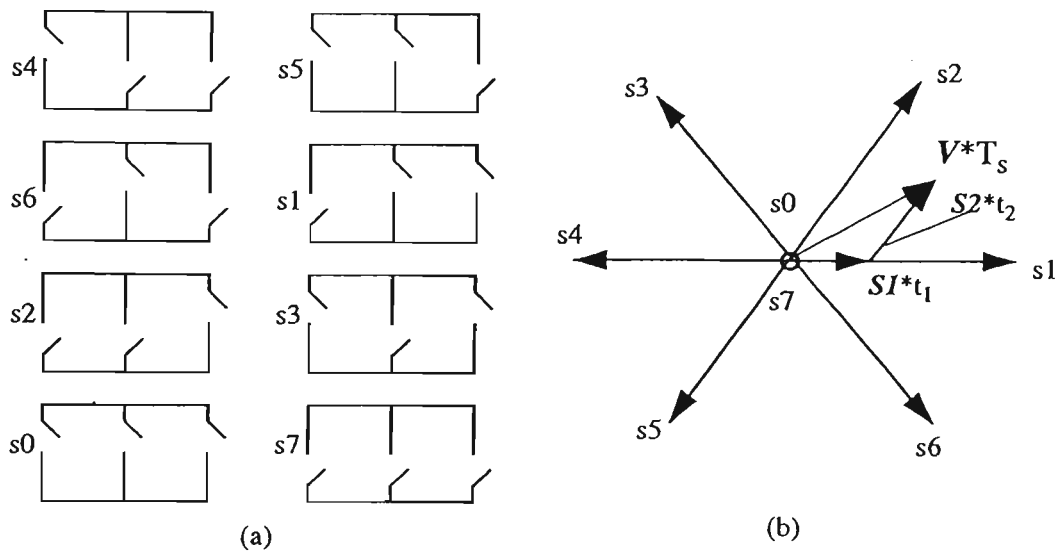

Fig. 1.6 Switch configuration and Target Phase from Space Vector

The voltage reference vector can be synthesized by a combination of three eight states as shown in Fig. 1.6 (b). If the modulating signal frequency is much lower than the switching frequency, then the reference voltage vector can be considered constant during one switching period, T_s. As a consequence, in a 'time average' sense, the voltage reference vector in a switching period can be approximated by two active switching states, each for a certain amount of time. In other words, the reference voltage vector is realized, in an average sense, by computing the fraction of the switching period for the two voltage vectors, which are adjacent to V. In Fig. 1.6 (b), t_1 and t_2 are the amount of time spent on S_1 and S_2, respectively. Then, in order to keep the switching frequency constant, the remainder of the switching period is spent on the zero switching state, t_0. There is $t_0 + t_1 + t_2 = T_s$.

To obtain the minimum switching frequency of each converter leg, it is necessary to arrange the switching sequence in such a way, that the transition from one state to the next is performed by switching only one rectifier leg. In order to match these rules in the case represented in Fig.1.6 (b), the switching sequence has to be 02177120.... These results in a definite switching order as shown in Fig.1.7, which shows exactly, the same symmetry as

derived for sinusoidal modulation. Refer to Section 5.3 for calculation details of m_1, m_3 and m_5 respectively.

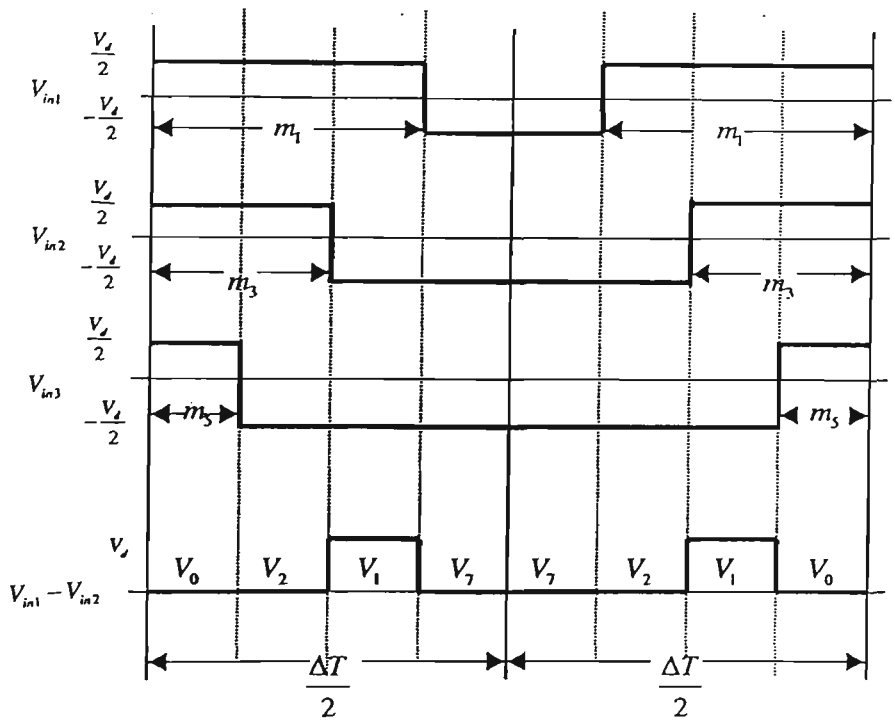

Fig. 1.7 Space Vector PWM Waveform in One Switching Period

The space vector representation is quite useful in digital systems because the microcontroller can calculate the t_k, t_{k+1} and T_s and transfer them to a "hardware modulator'.

1.2.7 OVERMODULATION

If a sine wave reference (reference modulating signal) is used, and if the peak of the reference waveform is less than peaks of the carrier waveform, it is referred to as linear modulation range, where the fundamental component of the switching pattern is equal to the modulating waveform. A problem arises when the peak of the reference waveform exceeds the peaks of the carrier waveform (modulation index >1). This is referred to as 'overmodulation'. The relationship between the reference amplitude and the fundamental voltage output becomes non-linear, and also harmonics become large causing degradation of the waveform quality. When the overmodulation is in extreme case, it produces a square wave output, which has the highest possible fundamental component because only two cross-over points occur in the fundamental period.

1.3 REVIEW OF THE CONTROL SCHEME

Up to now, AC/DC conversion has been dominated by uncontrolled rectifiers or phase controlled rectifiers. Such rectifiers have the inherent drawbacks that their power factor decreases when the firing angle increases and that harmonics of the line current are relatively high. Meanwhile, more and more applications require that the AC/DC converters have both rectifying and regenerating abilities with fast response to improve the dynamic performance of the whole system. These bidirectional power flow and response requirements have drawn more attention to PWM AC/DC converters. Converters using hysteresis current control (HCC), current controlled voltage regulated converter in stationary and rotating frame and predicted current control with fixed switching frequency (PCFF) have been very popular. They are capable of delivering nearly sinusoidal current waveforms with a unity power factor. By adding DC voltage feedback, they can be made into stand-along regulated DC voltage supplies with fast response to bidirectional power demand.

1.3.1 HYSTERESIS CURRENT CONTROL STRATEGY

The hysteresis current control (HCC) configuration is shown in Fig.1.8. It looks like an usual converter including a bridge and a tank capacitor in the DC link [12-14]. Owing to the scheme symmetry, bidirectional power control is possible. The bridge, connected to the supply line e_k, is operated so as to absorb sinusoidal currents in phase with the line voltage source. The bridge is controlled by a Hysteresis technique in order to obtain accurate waveform shaping and fast dynamic response. The tank capacitor stores the amount of energy needed to keep the DC voltage ripple below a suitable limit, while converter control keeps constant the DC voltage. To minimize the tank capacitor, the converter must provide fast control of the energy exchange between line and storage capacitor. In fact, any input or output power unbalance causes a variation of the stored energy and, if the capacitor is small, the DC voltage may vary widely.

In order to obtain fast response of the power converter, a hysteresis current control technique can be adopted, which keeps each current close to its reference, ensuring good accuracy and small delay time. In any case, some DC voltage variations are unavoidable, but they should not affect the output performance.

In order to keep constant link voltage, V_d, a closed-loop control is introduced. Voltage V_d is compared with reference V_{d_ref}, and the resulting error signal is fed to a PI regulator, which provides correcting term. The load current is low-pass filtered to obtain average value. As shown in Fig.1.8, the current reference amplitude I^* is the sum of the correcting term and load current. In theory, the voltage control loop can work alone. However, sensing the load current I_d ensures a feed-forward action, which speeds up the response of V_d.

The switching frequency of HCC control varies with the DC load current, at heavy loads the frequency increases substantially. The switching frequency pattern is uneven and random. This presents a major problem for HCC control, in that the instantaneous switching frequency can be even higher than the average switching frequency, causing excessive stress on switching devices.

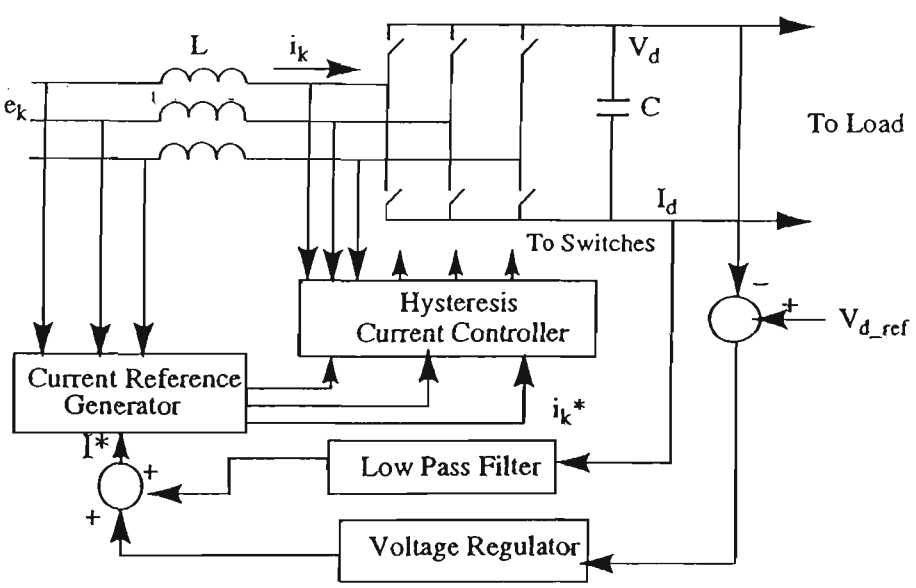

Fig. 1.8 Hysteresis Current Control

1.3.2 CURRENT-CONTROLLED CONVERTER IN STATIONARY AND ROTATING FRAMES

A current controlled PWM rectifier provides near sinusoidal input currents with a unity power factor and a low output voltage ripple. Moreover, it produces a well-defined input current harmonic spectrum, exhibits fast transient response to load voltage variations, and is capable of regenerative operation. PWM pattern generation is based on a carrier technique and the current controller that is implemented in the stationary and rotating frames [15].

1.3.2.1 Stationary Frame Controller

The complete rectifier system includes a voltage source PWM converter, a current controller loop and a DC voltage loop as shown in Fig. 1.9. The amplitude of the current reference is obtained from the DC voltage loop. The output DC voltage is compared with a voltage reference and the error is fed to a PI (proportional and integral) regulator to reduce the steady state voltage error. The output of the PI regulator is then multiplied by input voltage waveforms to provide the three AC current references with the desirable input power factor and proper phase shift. The stationary frame controller has the obvious advantage of simplicity since it can be implemented using simple analog circuit. However, the stationary controller regulates AC signals and the integrator has a finite gain at fundamental frequency. Therefore, there is an inherent amplitude and phase error. The error depends on the input frequency.

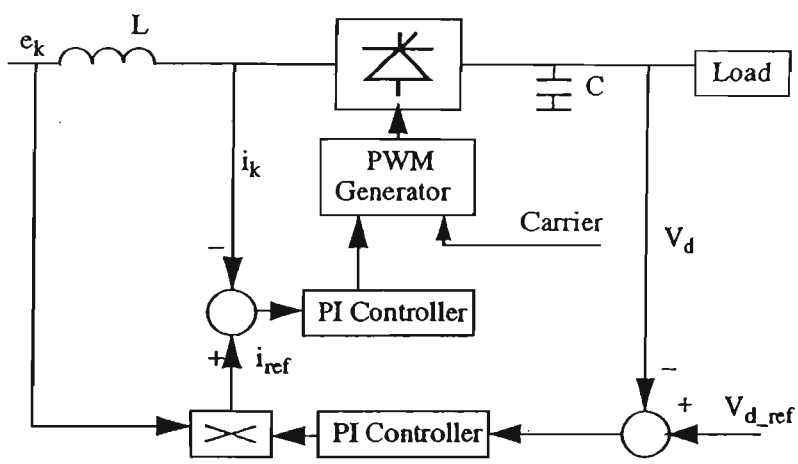

Fig. 1.9 Current Control in Stationary Frame

1.3.2.2 Rotating Frame Controller

The rotating frame controller is depicted in Fig. 1.10. The three line currents are transferred to (dqo) frame. The magnitudes of the reference currents in the rotating frame I_{d_ref} and I_{q_ref} are dictated by the voltage feedback loop. Any arbitrarily rotating frame can be chosen as the reference frame. However, if the q-axis is in phase with the phase a, in order to achieve unity power factor operation, the reference signals for the dq axis currents must satisfy I_{d_ref}=0 and I_{q_ref}=I_d.

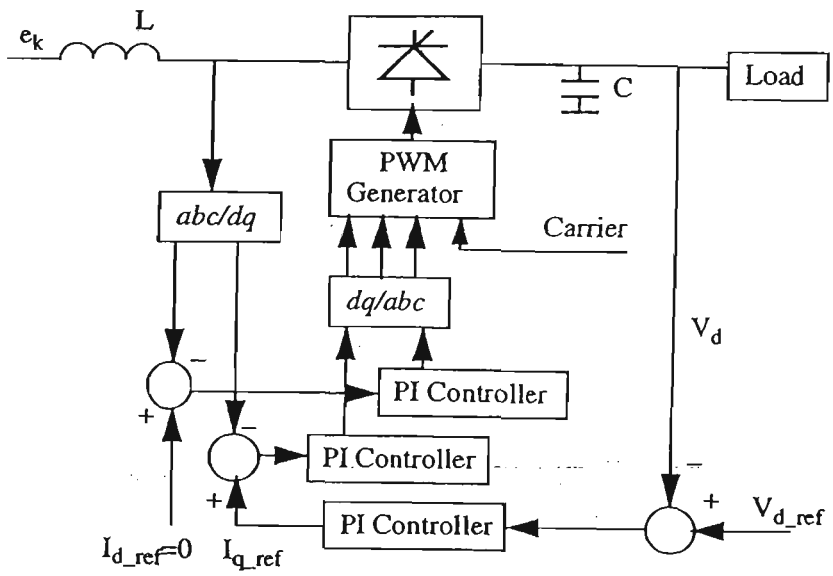

Fig. 1.10 Current Control in Rotating Frame

The rotating frame controller eliminates the steady state error, since it operates on DC quantities and the integrator has an infinite gain at zero frequency. A lot of digital calculations are required for the rotating frame controller, so that the implementation is more complicated. However, for applications which require high accuracy, the rotating frame controller is the preferred solution.

1.3.3 Predicted Current Control with a Fixed Switching Frequency (PCFF)

The PCFF control system keeps the bidirectional high speed dynamic features but operates at a fixed switching frequency. It is able to produce nearly sinusoidal line current waveform with a unity power factor. By adding a DC voltage feedback, it can be made into a stand-alone regulated DC voltage supply with fast response to bidirection power demand [18-19].

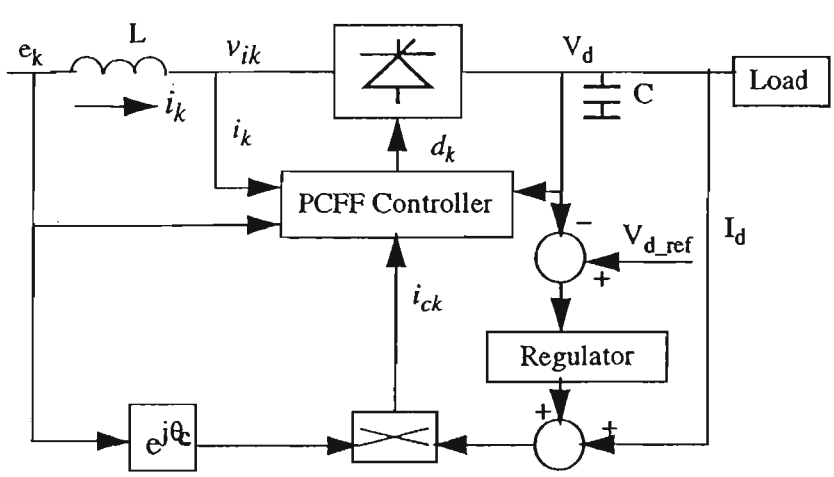

Fig. 1.11 Block Diagram of the PCFF Control

Fig. 1.11 shows the block diagram of PCFF control. The amplitudes of the current reference i_{ck} $(k = 1,2,3)$, are produced by a DC voltage feedback and a load current feedforward to regulate the DC output voltage V_d. After the regulator, the current references are modulated by the three-phase source voltage e_k with a $e^{j\theta_c}$, where θ_c is an adjustable phase angle for the leading phase shift. The angle of the current reference is taken from the angle of the source voltage e_k, plus a phase shift θ_c, which compensates for the time delay of the PCFF control. Thus the line current is forced to vary in phase with e_k, and a unity power factor is obtained. The use of load feedforward eliminates the steady-state error that exists when using only proportional DC output voltage feedback. If the proportional plus integral (PI) action is used to control the DC output voltage, the PI regulator can eliminate the steady-state error in the DC output voltage and the load feedforward significantly improves the dynamic response of the DC output voltage due to the load changes.

The detail of the PCFF controlled power converter is shown in the next chapter. In this technique, the modulating voltage V_{ck} required for controlling the line current is calculated based on the parameters of the power circuit and the switching frequency, this voltage is then compared to a carrier wave to generate a switching pattern to regulate the line current. The major shortcoming of the PCFF control is that its control principle is parameter sensitive. The power circuit parameters are required to implement the control algorithm. In practice, the difference between a real system model and its mathematical model caused by the variations of these design inputs is the source of system uncertainty and may deteriorate the system performance.

1.4 SUMMARY OF LITERATURE REVIEW

The comparison of the preceding control schemes, the predictive current control with a fixed switching frequency (PCFF) combines many of the advantages, such as a fast dynamic response, a well-defined switching pattern, and low complexity [18-19]. However, the PCFF scheme is sensitivity to parameter variations of the system, i.e. the system performance may deteriorate when operating conditions of the system have been

changed from its set point, or when the system is subject to load disturbances [26-27]. The difference between a real system and its mathematical model is a source of uncertainty. The requirement of coping with uncertainty for the PCFF scheme is a robust control problem, and is explored in this thesis.

1.5 OBJECTIVES OF THE THESIS

Having reviewed the literature of the current development in the converter control including both controllers and modulators, the following objectives of this thesis were considered:

1. The development of a computer controlled three-phase pulse width modulated (PWM) AC/DC IGBT power converter (10kVA) as an experimental system, where a single board 486 computer is used as a digital controller and a PWM generator board as a modulator device.

2. Experimental implementation of the space vector PWM algorithm as the modulation strategy. Software is to be developed in Borland C++ code, where the switching intervals are calculated according to given modulation index and output frequency. The results are downloaded to the PWM generator board for the switching pattern to be synthesized before output to six switching devices of the power converter respectively.

3. Theoretical design and simulation of an advanced H_∞ controller as a DC voltage regulator to compensate the uncertainty problem of the PCFF scheme. The PCFF control combined with the H_∞ voltage regulator is capable of achieving both the performance robustness and stability robustness for the output DC link voltage of the AC/DC power converter, and nearly sinusoidal line currents with a unity power factor.

The research work carried out to achieve these objectives is reported in this thesis.

1.6 OVERVIEW OF THE THESIS

Chapter 2 reviews the control principle of the predicted current control with a fixed switching frequency (PCFF). The plant transfer function of a PCFF controlled PWM power converter is derived, based on which the H_∞ voltage regulator is designed.

Chapter 3 introduces the fundamentals of the H_∞ control theory, the design principle and optimal design process. An advanced H_∞ controller is proposed and designed as a DC voltage regulator to compensate the uncertainty problem of the PCFF scheme. The stability analysis of the designed H_∞ control system is also given in this Chapter.

Chapter 4 describes the simulation work for the performance of the three-phase predictive pulse-width modulated AC/DC power converter with the proposed H_∞ voltage regulator, using MATLAB/SIMULINK. Simulation results for the output DC voltage and AC line currents are also presented in this Chapter 4.

Chapter 5 describes the development of an experimental system, which includes a 10kVA IGBT voltage source converter, a single chip PC-486 controller, a PWM generator board, a data acquisition and conversion board. The Chapter gives a detailed description of each component of the system and explains their functionality. The development of a software in Borland C++ code to implement the space vector PWM algorithm and to interface the PC-486 controller with the PWM generator board is detailed in this Chapter.

The hardware and software developed in Chapter 5 are tested and verified experimentally, results are presented in Chapter 6. The measured performance agrees well with the theoretical and simulation results.

The final Chapter 7 is the conclusions of the thesis, which highlights the achievements throughout the thesis and the significance of the study. Suggestions for further work are also given.

The thesis has three appendices. Appendix A shows the schematics of the circuit developed for the experimental system. Appendix B gives the listings of simulation and computer programs for the analysis and implementation of the PWM AC/DC power converter. Appendix C gives the publications by the author during his candidature.

Chapter 2

THE PRINCIPLE OF PCFF CONTROL

Reference: [18-19]

2.1 INTRODUCTION

The principle of the predicted current control with a fixed switching frequency (PCFF) has been proposed previously [18-19]. Since the PCFF control is to be used in this project, its comprehensive analysis is detailed in this Chapter. The analysis starts from the establishment of a PWM AC/DC converter model, from which the PCFF control law is derived. The original model of the PCFF controlled converter is nonlinear and time-variant, it is then transformed to a rotating reference frame to become a nonlinear and time-invariant model, where it is linearized about a set point. The transfer function of the PCFF controlled converter is derived based on the resulting linear and time-invariant model and is used for the design of the H_∞ voltage regulator in this study.

2.2 THE MODEL OF THE PWM AC/DC CONVERTER

The basic structure of the PWM AC/DC converter is shown in Fig. 2.1, where the three phase power supplies are connected to the three phase legs of the converter, which employs six fully controlled IGBT switches, S_1 through S_3 and S_1' through S_3'. Both the AC line inductance, L, and the DC link capacitor, C, act as the low pass filter to smooth the line current and the DC output voltage respectively. For phase one, the voltage equation on the AC side of the converter is:

$$L(\frac{di_1}{dt}) + R_L i_1 = e_1 - (V_{DN} + V_{NO}) \qquad (2.2\text{-}1)$$

Where R_L is the line resistance. When switch S_1 is on and switch S_1' is off, the switching function is d_1=1, d_1' = 0 and $V_{DN} = i_1 R_s + V_d$ where R_s is the equivalent resistance of a switching device. When switch S_1 is off and S_1' is on, d_1=0, d_1'=1 and $V_{DN} = i_1 R_s$. Equation (2.2-1) becomes:

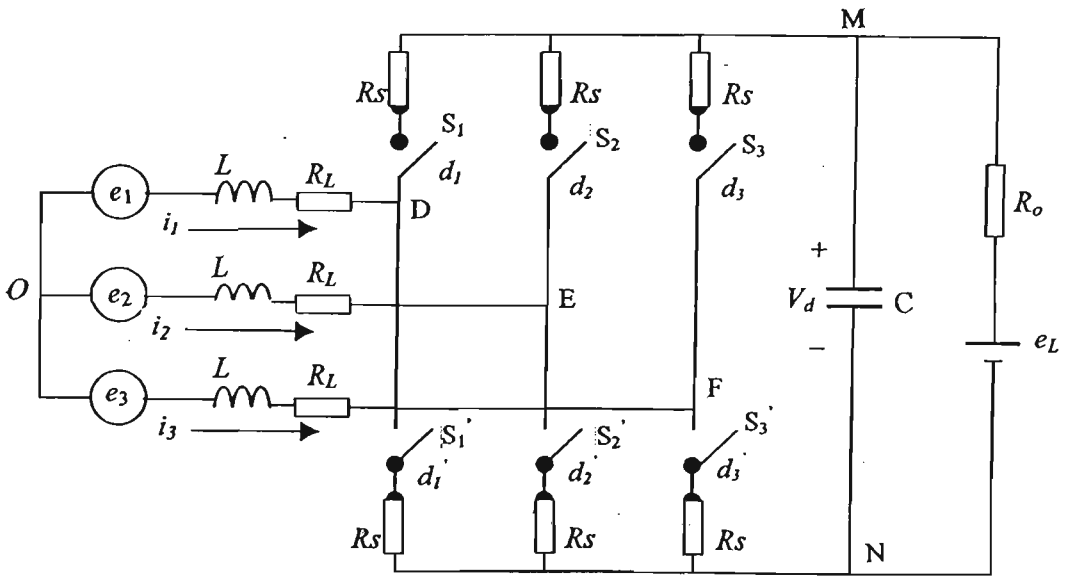

Fig. 2.1 The Circuit of PWM AC/DC Converter

$$L(\frac{di_1}{dt}) + R_L i_1 = e_1 - [(i_1 R_s + V_d)d_1 + (i_1 R_s)d_1' + V_{NO}] \qquad (2.2\text{-}2)$$

Because either S_1 or S_1' is conducting and only one of them is allowed to conduct at any moment, $d_1 + d_1' = 1$. The equation (2.2-2) can be expressed as:

$$L(\frac{di_1}{dt}) = -Ri_1 - (V_d d_1 + V_{NO}) + e_1 \qquad (2.2\text{-}3)$$

Where $R=R_L+R_s$, the total series resistance in one phase. Similarly, for phase two and three:

$$L(\frac{di_2}{dt}) = -Ri_2 - (V_d d_2 + V_{NO}) + e_2 \qquad (2.2\text{-}4)$$

$$L(\frac{di_3}{dt}) = -Ri_3 - (V_d d_3 + V_{NO}) + e_3 \qquad (2.2\text{-}5)$$

For a three-phase system without neutral line, three phase AC current relationship is:

$$i_1 + i_2 + i_3 = 0 \qquad (2.2\text{-}6)$$

If the AC supply is a balanced source, equation (2.2-7) is obtained:

$$e_1 + e_2 + e_3 = 0 \qquad (2.2\text{-}7)$$

The voltage V_{NO} can be obtained by adding (2.2-3) to (2.2-5) together:

$$V_{NO} = \frac{-V_d}{3}\sum_{k=1}^{3} d_k \qquad (2.2\text{-}8)$$

For the circuitry of Fig. 2.1, another differential equation can be written by inspection:

$$C\frac{dV_d}{dt} = i_1 d_1 + i_2 d_2 + i_3 d_3 - \frac{(V_d - e_L)}{R_o} \qquad (2.2\text{-}9)$$

Equations from (2.2-3) to (2.2-5) and (2.2-9) comprise a complete differential equation set to describe the converter. In the frequency range much lower than the switching frequency, the switching function d_k can be replaced by its average value or duty ratio. Therefore, the converter can be represented by the matrix-form differential equation:

$$\begin{bmatrix} L & 0 & 0 & 0 \\ 0 & L & 0 & 0 \\ 0 & 0 & L & 0 \\ 0 & 0 & 0 & C \end{bmatrix} \begin{bmatrix} \dot{i}_1 \\ \dot{i}_2 \\ \dot{i}_3 \\ \dot{V}_d \end{bmatrix} = \begin{bmatrix} -R & 0 & 0 & -(d_1 - \frac{1}{3}\sum_{k=1}^{3} d_k) \\ 0 & -R & 0 & -(d_2 - \frac{1}{3}\sum_{k=1}^{3} d_k) \\ 0 & 0 & -R & -(d_3 - \frac{1}{3}\sum_{k=1}^{3} d_k) \\ d_1 & d_2 & d_3 & -\frac{1}{R_o} \end{bmatrix} \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ V_d \end{bmatrix} + \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & \frac{1}{R_o} \end{bmatrix} \begin{bmatrix} e_1 \\ e_2 \\ e_3 \\ e_L \end{bmatrix} \qquad (2.2\text{-}10)$$

2.3 PCFF CONTROL SYSTEM

Fig. 2.2 shows the block diagram of PCFF control. The amplitudes of the current reference i_{ck} $(K = 1,2,3)$, are produced by a DC voltage feedback and a load current feedforward to regulate the DC output voltage V_d. After the regulator, the current references are modulated by the three-phase source voltage e_k with a $e^{j\theta_c}$, where θ_c is an adjustable phase angle for the leading phase shift. The angle of the current reference is taken from the angle of the source voltage e_k, plus a phase shift θ_c, which compensates for the time delay of the PCFF control. Thus the line current is forced to vary in phase with e_k, and a unity power factor is obtained. The regulator can eliminate the steady-state error in the DC output voltage and the load feedforward can increase the dynamic response of the DC output voltage due to the load changes.

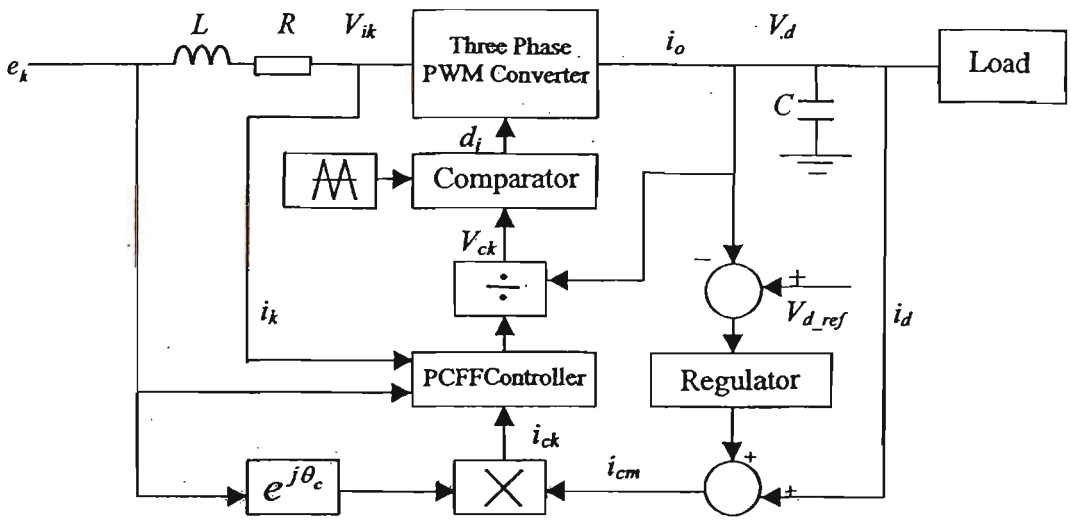

Fig. 2.2 Block Diagram of the PCFF Control System

2.3.1 PCFF CONTROL LAW

From (2.2-10), it is seen that the state variables i_1, i_2, i_3 and V_d are controlled by the duty ratio d_1, d_2 and d_3. For the PCFF control, the duty ratio d_k, k=1, 2 and 3, is derived from source voltage e_k, line current i_k, DC output voltage V_d, and a current reference i_{ck} as follows, where T is the switching period.

$$d_k = \frac{1}{V_d}\left[e_k - (R - \frac{L}{T})i_k - \frac{L}{T}i_{ck}\right] + \frac{1}{2} \qquad (2.3\text{-}1)$$

If the duty ratio is produced by this equation, the line current would be forced to reach a "predicted" value at the end of a defined switching period. For a three-phase balance system, (2.2-6) and (2.2-7) apply. The current reference i_{ck} are modulated by the source voltage e_k. Their sum equals to zero: $\sum_{k=1}^{3} i_{ck} = 0$. Therefore

$$\sum_{k=1}^{3} d_k = \frac{3}{2} \qquad (2.3\text{-}2)$$

Substituting (2.3-1) and (2.3-2) into (2.2-10), the relationship between current reference and actual current can be derived:

$$\frac{di_k}{dt} = \frac{1}{T}(i_{ck} - i_k) \qquad (2.3\text{-}3)$$

This means that the line current i_k will follow the reference current i_{ck} with only one switching period T delay.

From Fig. 2.2, it can be seen that the voltage V_{ck}, necessary for controlling the line current, is created by a combination of e_k, i_k, V_d, and the current reference i_{ck}, as

$$V_{ck} = \frac{2V_s}{V_d}\left[e_k - (R - \frac{L}{T})i_k - \frac{L}{T}i_{ck}\right] \qquad (2.3\text{-}4)$$

This voltage is transferred to a voltage/trigger converter, where it is compared with a triangle waveform. The intersections determine the switching pattern of Fig. 2.3. If the switching frequency is high enough, the voltage V_{ck} can be treated as a constant within the switching period, and the trigger duty ratio d_k will have the following relationship to V_{ck}, where M is modulation index.

$$d_k = \frac{t_{on}}{T} = \frac{V_{ck}}{2V_s} + \frac{1}{2} = \frac{1}{2}(M+1) \qquad (2.3\text{-}5)$$

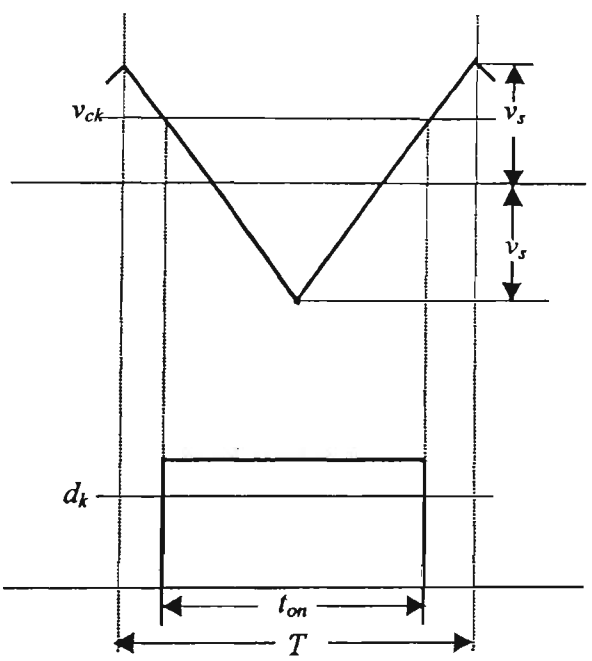

Fig. 2.3 The Waveform of Voltage Trigger Converter

Thus combining the relation of (2.3-4) and (2.3-5) the required PCFF control law of (2.3-1) is realized. If V_{ik} is AC terminal voltage of converter, V_{ik} can be expressed by:

$$V_{ik} = e_k - L\frac{di_k}{dt} - Ri_k = (d_k - \frac{1}{3}\sum_{k=1}^{3} d_k)V_d = \frac{V_d}{(2/M)} \qquad (2.3\text{-}6)$$

The DC output current of the converter will be:

$$i_o = \sum_{k=1}^{3} d_k i_k = \frac{1}{2V_s} \sum_{k=1}^{3} i_k V_{ck} \qquad (2.3\text{-}7)$$

2.3.2 PCFF CONTROL SYSTEM IN ROTATING FRAME OF REFERENCE [19]

The PCFF control system is nonlinear and time-variant system. Therefore, analysis and design of PCFF system is quite complex. The PCFF AC/DC voltage source converter in a stationary frame of reference has been derived, rewritten from (2.2-10) and (2.3-1).

$$Z\dot{X} = AX + Be \qquad (2.3\text{-}8)$$

where:

$$Z = \begin{bmatrix} L & 0 & 0 & 0 \\ 0 & L & 0 & 0 \\ 0 & 0 & L & 0 \\ 0 & 0 & 0 & C \end{bmatrix} \qquad X = \begin{bmatrix} i_1 \\ i_2 \\ i_3 \\ V_d \end{bmatrix} \qquad A = \begin{bmatrix} -R & 0 & 0 & -(d_1 - \frac{1}{3}\sum_{k=1}^{3} d_k) \\ 0 & -R & 0 & -(d_2 - \frac{1}{3}\sum_{k=1}^{3} d_k) \\ 0 & 0 & -R & -(d_3 - \frac{1}{3}\sum_{k=1}^{3} d_k) \\ d_1 & d_2 & d_3 & -\frac{1}{R_o} \end{bmatrix}$$

$$B = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & \frac{1}{R_o} \end{bmatrix} \qquad e = \begin{bmatrix} e_1 \\ e_2 \\ e_3 \\ e_L \end{bmatrix}$$

$$d_k = \frac{1}{V_d}\left[e_k - (R - \frac{L}{T})i_k - \frac{L}{T} i_{ck} \right] + \frac{1}{2} \qquad (2.3\text{-}9)$$

If a sinusoidal line current is required, the reference current should have the form:

$$i_{ck} = i_{cm} \cos\left[\omega t + \theta_c - (k-1)\frac{2\pi}{3} \right] \qquad (2.3\text{-}10)$$

The i_{cm} is the reference current amplitude control. The switching duty ratio is created by the PCFF control (2.3-9) as a function of time. Therefore, the matrix is time variant. This difficulty can be overcome by applying a transformation to a rotating frame of reference

synchronized with the utility frequency ω [19]. The transformation matrix T and its inverse matrix T^{-1} are:

$$T=\frac{1}{\sqrt{3}}\begin{bmatrix}1 & e^{-j\omega t} & e^{j\omega t} & 0\\ 1 & e^{-j(\omega t-\frac{2\pi}{3})} & e^{j(\omega t-\frac{2\pi}{3})} & 0\\ 1 & e^{-j(\omega t+\frac{2\pi}{3})} & e^{j(\omega t+\frac{2\pi}{3})} & 0\\ 0 & 0 & 0 & \sqrt{3}\end{bmatrix} \qquad T^{-1}=\frac{1}{\sqrt{3}}\begin{bmatrix}1 & 1 & 1 & 0\\ e^{j\omega t} & e^{j(\omega t-\frac{2\pi}{3})} & e^{j(\omega t+\frac{2\pi}{3})} & 0\\ e^{-j\omega t} & e^{-j(\omega t-\frac{2\pi}{3})} & e^{-j(\omega t+\frac{2\pi}{3})} & 0\\ 0 & 0 & 0 & \sqrt{3}\end{bmatrix}$$

Thus, the state variable vector in the rotating frame X_r and the vector in the stationary frame X have the relation:

$$X=TX_r \tag{2.3-11}$$

Where $X_r=\begin{bmatrix}i_o\\ i_f\\ i_b\\ V_d\end{bmatrix}$ and its differentiation:

$$\dot{X}=T\dot{X}_r+\dot{T}X_r \tag{2.3-12}$$

Where i_o, i_f and i_b are zero sequence current, forward current and backward current relatively. Pre-multiplying by T^{-1} on both sides of (2.3-8) yields:

$$(T^{-1}ZT)\dot{X}_r=(T^{-1}AT-T^{-1}\dot{Z}T)X_r+T^{-1}Be \tag{2.3-13}$$

By substituting (2.3-8) and (2.3-9) into (2.3-13), the following time-invariant state space equation in the rotating frame of reference can be obtained:

$$\begin{bmatrix}L\dot{i}_o\\ L\dot{i}_f\\ L\dot{i}_b\\ C\dot{V}_d\end{bmatrix}=\begin{bmatrix}-R & 0 & 0 & 0\\ 0 & j\omega L-\frac{L}{T_s} & 0 & 0\\ 0 & 0 & -j\omega L-\frac{L}{T_s} & 0\\ \frac{\sqrt{3}}{2} & a_{42} & a_{43} & -\frac{1}{R_o}\end{bmatrix}\begin{bmatrix}i_o\\ i_f\\ i_b\\ V_d\end{bmatrix}+\begin{bmatrix}0\\ \frac{\sqrt{3}Le^{-j\theta}}{2T_s}i_{cm}\\ \frac{\sqrt{3}Le^{j\theta}}{2T_s}i_{cm}\\ \frac{e_L}{R_o}\end{bmatrix} \tag{2.3-14}$$

where $$a_{42}=\frac{1}{V_d}\left[\frac{\sqrt{3}e_m}{2}-(R-\frac{L}{T_s})i_b-\frac{\sqrt{3}Li_{cm}}{2T_s}e^{j\theta}\right]$$

$$a_{43} = \frac{1}{V_d}\left[\frac{\sqrt{3}e_m}{2} - (R - \frac{L}{T_s})i_f - \frac{\sqrt{3}Li_{cm}}{2T_s}e^{j\theta}\right]$$

For a three-phase system without neutral line, the zero sequence current i_o is equal to zero. The equation (2.3-14) can be simplified to its reduced form:

$$\begin{bmatrix} \dot{L}i_f \\ \dot{L}i_b \\ \dot{C}V_d \end{bmatrix} = \begin{bmatrix} j\omega L - \frac{L}{T_s} & 0 & 0 \\ 0 & -j\omega L - \frac{L}{T_s} & 0 \\ a_{42} & a_{43} & -\frac{1}{R_o} \end{bmatrix} \begin{bmatrix} i_f \\ i_b \\ V_d \end{bmatrix} + \begin{bmatrix} \frac{\sqrt{3}Le^{-j\theta}}{2T_s} i_{cm} \\ \frac{\sqrt{3}Le^{j\theta}}{2T_s} i_{cm} \\ \frac{e_L}{R_o} \end{bmatrix} \qquad (2.3\text{-}15)$$

2.4 THE MODEL OF PCFF CONTROL SYSTEM

One of the most important tasks in the analysis and design of control system is mathematical model of the system. The differential equation (2.3-15) is a nonlinear equation. It can be approximately linearized within a small area around the DC operating points.

2.4.1 DC MODEL

Let the state variables be expressed as:

$$\begin{bmatrix} i_f \\ i_b \\ V_d \end{bmatrix} = \begin{bmatrix} I_f \\ I_b \\ V_d \end{bmatrix} + \begin{bmatrix} \Delta i_f \\ \Delta i_b \\ \Delta V_d \end{bmatrix} \qquad (2.4\text{-}1)$$

the inputs $e_m = E_m + \Delta e_m$, $\omega = \Omega + \Delta\omega$

the load $R_o = R_o + \Delta r_o$, $e_L = E_L + \Delta e_L$

the control $i_{cm} = I_{cm} + \Delta i_{cm}$

By substituting the equation (2.4-1), the inputs, load and control into (2.3-15), omitting second-order terms and separating the DC component from the AC variation, the steady-state DC model can be derived. The steady-state DC model is

$$\begin{bmatrix} j\Omega L-\frac{L}{T_s} & 0 & 0 \\ 0 & -j\Omega L-\frac{L}{T_s} & 0 \\ A_{42} & A_{43} & -\frac{1}{R_o} \end{bmatrix} \begin{bmatrix} I_f \\ I_b \\ V_d \end{bmatrix} + \begin{bmatrix} \frac{\sqrt{3}Le^{-j\theta_c}}{2T_s} I_{cm} \\ \frac{\sqrt{3}Le^{j\theta_c}}{2T_s} I_{cm} \\ \frac{E_L}{R_o} \end{bmatrix} = 0 \qquad (2.4\text{-}2)$$

where

$$A_{42}=\frac{1}{V_d}\left[\frac{\sqrt{3}E_m}{2}-(R-\frac{L}{T_s})I_b-\frac{\sqrt{3}LI_{cm}}{2T_s}e^{j\theta_c}\right], \quad A_{43}=\frac{1}{V_d}\left[\frac{\sqrt{3}E_m}{2}-(R-\frac{L}{T_s})I_f-\frac{\sqrt{3}LI_{cm}}{2T_s}e^{-j\theta_c}\right]$$

The steady-state solutions can be obtained directly from the DC model. From the first row of (2.4-2), the steady-state forward current component I_f can be obtained as

$$I_f=\frac{\sqrt{3}I_{cm}e^{-j\theta_c}}{2(1-j\Omega T_s)} \qquad (2.4\text{-}3)$$

If $$\theta_s=\tan^{-1}(\Omega T_s) \qquad (2.4\text{-}4)$$

And $$K_T=\sqrt{1+(\Omega T_s)^2} \qquad (2.4\text{-}5)$$

Then $$I_f=\frac{\sqrt{3}I_{cm}e^{-j(\theta_c-\theta_s)}}{2K_T} \qquad (2.4\text{-}6)$$

Similarly, the steady-state backward current component I_b can be obtained from (2.4-2) as

$$I_b=\frac{\sqrt{3}I_{cm}e^{j(\theta_c-\theta_s)}}{2K_T} \qquad (2.4\text{-}7)$$

The steady-state DC output V_d can be calculated from the third row of (2.4-2) as

$$V_d=\frac{1}{2}\left\{E_L+\sqrt{E_L^2+\frac{6I_{cm}R_o}{K_T^2}[E_m K_T\cos(\theta_c-\theta_s)-RI_{cm}]}\right\} \qquad (2.4\text{-}8)$$

If the leading compensation angle θ_c is adjusted to be equal to θ_s, then

$$I_f=\frac{\sqrt{3}I_{cm}}{2K_T} \qquad (2.4\text{-}9)$$

$$I_b=\frac{\sqrt{3}I_{cm}}{2K_T} \qquad (2.4\text{-}10)$$

$$V_d = \frac{1}{2}\left\{E_L + \sqrt{E_L^2 + \frac{6I_{cm}R_o}{K_T^2}[E_m K_T - RI_{cm}]}\right\} \qquad (2.4\text{-}11)$$

The steady-state current solution I_f, I_b are the components of the line current in the rotating frame of reference, but the variables of greatest concern are the steady-state peak current I_m and the power factor Φ. They can be derived as follows:

$$I_m = \frac{2}{\sqrt{3}}|I_f| = \frac{I_{cm}}{K_T} \qquad (2.4\text{-}12)$$

$$\Phi = Arg(I_f) = (\theta_s - \theta_c) \qquad (2.4\text{-}13)$$

The approximation $K_T = \sqrt{1+(\Omega T_s)^2} \approx 1$ is generally valid, because the switching frequency of the converter is usually much higher than the supply frequency. The steady-state peak current I_m is approximately equal to the control current I_{cm}, and the power factor angle Φ is equal to 0^o if the leading compensation angle is adjusted to be $\theta_c = \theta_s = \tan^{-1}(\Omega T_s)$. Therefore, one advantage of the PCFF control is its input power factor, which is automatically maintained at unity if $\theta_c = \theta_s$. The only control variable i_{cm} can be used to regulate the DC output voltage. The PWM converter under the PCFF control becomes a single-input signal-output system.

2.4.2 AC Model

The AC model of the converter under PCFF control can be derived by substituting the equation (2.4-1), the inputs, load and control into (2.3-15).

$$Z_r \dot{\Delta X}_r = A_x \Delta X_r + A_c \Delta i_{cm} + A_\omega \Delta\omega + A_e \Delta e_m + A_r \Delta r_o + A_L \Delta e_L \qquad (2.4\text{-}14)$$

$A_c\Delta i_{cm}$, $(A_\omega\Delta\omega + A_e\Delta e_m)$ and $(A_r\Delta r_o + A_L\Delta e_L)$ are control, input disturbances and load disturbances terms respectively, where

$$Z_r = \begin{bmatrix} L & 0 & 0 \\ 0 & L & 0 \\ 0 & 0 & C \end{bmatrix} \quad \Delta X_r = \begin{bmatrix} \Delta i_f \\ \Delta i_b \\ \Delta V_d \end{bmatrix} \quad A_\omega = \begin{bmatrix} jLI_f \\ -jLI_b \\ 0 \end{bmatrix} \quad A_L = \begin{bmatrix} 0 \\ 0 \\ \frac{1}{R_o} \end{bmatrix}$$

$$A_x = \begin{bmatrix} j\Omega L - \frac{L}{T_s} & 0 & 0 \\ 0 & -j\Omega L - \frac{L}{T_s} & 0 \\ A_{42} - \frac{1}{V_d}(R - \frac{L}{T_s})I_b & A_{43} - \frac{1}{V_d}(R - \frac{L}{T_s})I_f & -\frac{1}{V_d}(A_{42}I_f + A_{43}I_b) - \frac{1}{R_o} \end{bmatrix}$$

$$A_c = \begin{bmatrix} \frac{\sqrt{3}L}{2T_s}e^{-j\theta_c} \\ \frac{\sqrt{3}L}{2T_s}e^{j\theta_c} \\ -\frac{1}{V_d}(\frac{\sqrt{3}L}{2T_s})(e^{j\theta_c}I_f + e^{-j\theta_c}I_b) \end{bmatrix} \qquad A_e = \begin{bmatrix} 0 \\ 0 \\ \frac{\sqrt{3}}{2V_d}(I_f + I_b) \end{bmatrix} \qquad A_r = \begin{bmatrix} 0 \\ 0 \\ \frac{(V_d - E_L)}{R_o{}^2} \end{bmatrix}$$

From the AC model derived in (2.4-14), the Laplace transformation of the variable vector $\Delta X_r(s)$ can be written as

$$\Delta X_r(s) = (sZ_r - A_x)^{-1}(A_c\Delta i_{cm} + A_\omega\Delta\omega + A_e\Delta e_m + A_r\Delta r_o + A_L\Delta e_L) \qquad (2.4\text{-}15)$$

Equation (2.4-15) gives all the transfer functions between the state variables Δi_f, Δi_b, ΔV_d and the control Δi_{cm}, input disturbance $\Delta\omega$, Δe_m or load disturbance Δr_o, Δe_L, and the small signal transfer function from any disturbance or control to any state variable can be derived from them.

The transfer function $\frac{\Delta V_d(s)}{\Delta i_{cm}(s)}$ can be obtained by setting $\Delta\omega = \Delta e_m = \Delta r_o = \Delta e_L = 0$ in (2.4-15). Then,

$$\Delta X_r(s) = \begin{bmatrix} \Delta i_f(s) \\ \Delta i_b(s) \\ \Delta V_d(s) \end{bmatrix} = (sZ_r - A_x)^{-1} A_c\Delta i_{cm}(s) \qquad (2.4\text{-}16)$$

The third row of this equation gives the transfer function $\frac{\Delta V_d(s)}{\Delta i_{cm}(s)}$. It has two zeros and three poles, but since the converter usually works at the condition of $K_T = \sqrt{1 + (\Omega T_s)^2} \approx 1$ and $\theta_c = \theta_s = \tan^{-1}(\Omega T_s) \approx 0$, thus $\cos\theta_c = \cos\theta_s \approx 1$. This transfer function can be simplified as follows

$$\frac{\Delta V_d(s)}{\Delta i_{cm}(S)} \approx \frac{3(E_m - 2I_{cm}R - LI_{cm}s)(1+sT_s)}{2V_d(1+sT_s)^2\left[\left(\frac{\left(2-\frac{E_L}{V_d}\right)}{R_o}\right)+sC\right]} = \frac{3(E_m - 2I_{cm}R)}{2V_d\left(\frac{2-\frac{E_L}{V_d}}{R_o}\right)} \frac{\left[1-s\left(\frac{LI_{cm}}{E_m-2I_{cm}R}\right)\right]}{(1+sT_s)\left[1+s\frac{CR_o}{2-\left(\frac{E_L}{V_d}\right)}\right]} \quad (2.4\text{-}17)$$

It is seen that one pole and one zero are canceled. This is another advantage of PCFF control. The transfer function has a lower order and can be rewritten as

$$\frac{\Delta V_d(s)}{\Delta i_{cm}(s)} = K_p \frac{\left(1-\frac{s}{\omega_o}\right)}{\left(1+\frac{s}{\omega_{p1}}\right)\left(1+\frac{s}{\omega_{p2}}\right)} \quad (2.4\text{-}18)$$

where

$$K_p = \frac{3(E_m - 2I_{cm}R)}{2V_d\left(\frac{\left(2-\frac{E_L}{V_d}\right)}{R_o}\right)} \qquad \omega_o = \frac{E_m - 2I_{cm}R}{LI_{cm}} \qquad \omega_{p1} = \frac{2-\frac{E_L}{V_d}}{R_oC} \qquad \omega_{p2} = \frac{1}{T_s}$$

It can been seen from (2.4-18) that, there is a zero in the right-half s plane. Hence, the transfer function is of the non-minimum phase type.

2.4.3 TRANSFER FUNCTION BETWEEN PEAK LINE CURRENT AND CONTROL SIGNAL

Since peak link current Δi_m is not one of the variables in the rotating frame of reference, it is necessary to find the relation between the variables Δi_f, Δi_b, and control Δi_{cm} first. It is known that

$$i_m = \frac{2}{\sqrt{3}}\sqrt{i_f \cdot i_b} \quad (2.4\text{-}19)$$

since

$$i_m = I_m + \Delta i_m, \qquad i_f = I_f + \Delta i_f, \qquad i_b = I_b + \Delta i_b$$

and the first order approximation of a function $f(x,y)$ about $x = x_o$, $y = y_o$ is

$$f(x,y) \approx f(x_o, y_o) + \frac{\partial f}{\partial x}(x - x_o) + \frac{\partial f}{\partial y}(y - y_o)$$

Therefore

$$I_m = \frac{2}{\sqrt{3}}\sqrt{I_f \cdot I_b} \qquad (2.4\text{-}20)$$

and

$$\Delta i_m = \frac{1}{\sqrt{3}}\left(\sqrt{\frac{I_b}{I_f}}\Delta i_f + \sqrt{\frac{I_f}{I_b}}\Delta i_b\right) \qquad (2.4\text{-}21)$$

From (2.4-6) and (2.4-7), it is seen that

$$\sqrt{\frac{I_b}{I_f}} = e^{j(\theta_c - \theta_s)}, \qquad \sqrt{\frac{I_f}{I_b}} = e^{-j(\theta_c - \theta_s)}$$

and

$$\frac{\Delta i_m(s)}{\Delta i_{cm}(s)} = \frac{1}{\sqrt{3}}\left[e^{j(\theta_c-\theta_s)}\frac{\Delta i_f(s)}{\Delta i_{cm}(s)} + e^{-j(\theta_c-\theta_s)}\frac{\Delta i_b(s)}{\Delta i_{cm}(s)}\right] \qquad (2.4\text{-}22)$$

The two functions $\frac{\Delta i_f(s)}{\Delta i_{cm}(s)}$ and $\frac{\Delta i_b(s)}{\Delta i_{cm}(s)}$ can be derived from the first and second rows of (2.4-16) as

$$\frac{\Delta i_f(s)}{\Delta i_{cm}(s)} = \frac{\sqrt{3}}{2}\cdot\frac{e^{-j\theta_c}}{(sT_s - j\Omega T_s + 1)}, \qquad \frac{\Delta i_b(s)}{\Delta i_{cm}(s)} = \frac{\sqrt{3}}{2}\cdot\frac{e^{j\theta_c}}{(sT_s - j\Omega T_s + 1)}$$

Substitution of these into (2.4-22) yields

$$\frac{\Delta i_m(s)}{\Delta i_{cm}(s)} = \frac{\cos\left[\theta_s - \tan^{-1}\dfrac{\Omega T_s}{(1+sT_s)}\right]}{\sqrt{(1+sT_s)^2 + (\Omega T_s)^2}} \qquad (2.4\text{-}23)$$

For the frequency range $\omega << \frac{1}{T_s}$

$$\tan^{-1}\frac{\Omega T_s}{(1+sT_s)} \approx \tan^{-1}\Omega T_s = \theta_s, \qquad \cos\left[\theta_s - \tan^{-1}\frac{\Omega T_s}{(1-sT_s)}\right] \approx 1.$$

Meanwhile, $K_T = \sqrt{1+(\Omega T_s)^2} \approx 1$; therefore

$$\frac{\Delta i_m(s)}{\Delta i_{cm}(s)} \approx \frac{1}{1+sT_s} \qquad (2.4\text{-}24)$$

From this transfer function and the steady-state solution with $I_m \approx I_{cm}$, it is concluded that the peak line current i_m would follow the control i_{cm} with a nearly first-order lag depending only on the switching frequency $F_s = \frac{1}{T_s}$. Because the switching frequency usually is rather high, the phase lag is negligible in the frequency range of interest.

2.5 SUMMARY

1. A comprehensive analysis of the PCFF control is provided, including a steady-state analysis, a dynamic response analysis and their solutions.

2. The derived solutions show that the line current follows the control signal closely with a nearly first-order lag, depending on the switching frequency. Because the switching frequency usually is rather high, the system has a rather good dynamic response.

3. The PCFF control only has one control variable. The power factor is maintained at unity if the leading compensation angle is appropriately adjusted. The control signal can be then used to regulate the DC output voltage. Therefore, the converter under PCFF control becomes a single-input, single-output system.

4. From the derivation of transfer function relating DC output voltage to control signal, it is seen that one pole has been cancelled by a zero. Hence, the system has a low order and there is a right half plane zero in system. Therefore, the system is a non-minimum phase system.

Chapter 3

THE DESIGN OF H∞ CONTROLLER

3.1 INTRODUCTION

The model of the PCFF control system is derived, and the comprehensive analysis is given in Chapter 2. The PCFF control scheme has a fast dynamic response, a well-defined switching pattern, and low complexity. However, the major problem with the PCFF scheme is its sensitivity to parameter variations of the system. Hence, the system performance may deteriorate when operating conditions of the system are changed. For example, from the rectifying mode to the regenerating mode, or when the system is subject to load disturbances. The difference between a real system and its mathematical model is a source of uncertainty, which directly degrades the performance of the PCFF controlled system. The requirement of coping with uncertainty for the PCFF scheme is a robustness problem and can only be compensated by a properly designed DC voltage regulator.

The conventional design approach to the DC voltage stabilisation utilises a proportional and integral (PI) controller operating on an error signal $V_{d\_ref} - V_d$. Although theoretically a PI controller is comparable to any other controller for a single-input single-output system, its design method is based on a trial and error procedure, and the optimal solution is not easy to be obtained.

In this project, an advanced H_∞ controller is proposed in the place of a PI voltage regulator. Not only the H_∞ theory has its unique approach to the uncertainty issue, but also its design method allows both the stability robustness and performance robustness to be considered at the design stage [29-34]. The H_∞ voltage regulator is to work with the PCFF current control to compensate uncertainty problem. The successful introduction of H_∞ control into this engineering application is demonstrated in this chapter.

3.2 THE PRELIMINARY OF H_∞ CONTROL THEORY

Control theory is concerned with the control of processes with inputs and outputs. How can a desired goal be achieved for outputs of a plant by choosing a control input?

The first step is to find a mathematical model describing the behavior of the real plant. Since the mathematical model should be simple enough for the mathematical tools, the model is not able to describe exactly a real plant. Because of this, the real-time behavior might differ significantly from the mathematically predicted behavior. Therefore, it is extremely important that a control method is chosen for the mathematical model, which deviates from the real plant. This leads to the so-called robustness analysis of the mathematical model and a robust controller is to be designed to cope with this deviation. Robustness of a system says nothing more than that the stability of the system will stand against perturbation.

Since the last decade, the H_∞ norm as a measure system has been thoroughly embedded in control theory, and there has been a gigantic surge in research efforts towards the minimization of the H_∞ norm for a closed-loop system to cope with model uncertainty. A fairly complete solution is now available.

3.2.1 SINGULAR VALUES

The singular values of a rank r matrix A, denoted $\sqrt{\lambda_i}$ are the non-negative square-roots of the eigenvalues of A^*A [29], such that

$$\sigma_i = \sqrt{\lambda_i} \qquad (i=1,2,\ldots r) \qquad (3.2\text{-}1)$$

The greatest singular value σ_i is denoted by $\bar{\sigma}$, and least singular value is denoted by $\underline{\sigma}$.

The properties of singular values are:

(1) $\bar{\sigma}(A) = \max_{x\neq 0} \dfrac{\|Ax\|}{\|x\|} = \max_{\substack{x\neq 0 \\ \|x\|=1}} \|Ax\|$ $\qquad$ $\underline{\sigma}(A) = \min_{x\neq 0} \dfrac{\|Ax\|}{\|x\|} = \min_{\substack{x\neq 0 \\ \|x\|=1}} \|Ax\|$ $\qquad$ where $\|x\| = \sqrt{x^* x}$

(2) $\underline{\sigma}(A) = \dfrac{1}{\bar{\sigma}(A^{-1})}$

(3) $\bar{\sigma}(AB) \le \bar{\sigma}(A)\bar{\sigma}(B)$

(4) $\bar{\sigma}(A+B) \le \bar{\sigma}(A) + \sigma(\bar{B})$

(5) $\underline{\sigma}(A) + \bar{\sigma}(\Delta A) \ge \underline{\sigma}(A+\Delta A) \ge \underline{\sigma}(A) - \bar{\sigma}(\Delta A)$

3.2.2 Spaces, H_2 and H_∞ Norms

The H_∞ space is the class of matrix-valued functions which are analytic and bounded in the open right half-plane, the H_∞ norm of such a function, say $F(s)$, being defined as

$$\|F\|_\infty := \sup \bar{\sigma}[F(s)] \qquad (3.2\text{-}2)$$

Here $\bar{\sigma}[F(s)]$ denotes the greatest singular value and the supremum is over all s in the open right half-plane, $R_e s > 0$ [30]. For such a function the boundary value

$$F(j\omega) := \lim_{\xi \to 0} F(\xi + j\omega) \qquad (3.2\text{-}3)$$

exists for almost all ω and the boundary function is of L_∞ space. As a consequence of the maximum modulus principle the H_∞ norm of $F(s)$ equals the L_∞ norm of the boundary function, i.e.,

$$\|F\|_\infty := ess \sup_\omega \bar{\sigma}[F(j\omega)] \qquad (3.2\text{-}4)$$

For example, suppose $F(s)$ is scalar-valued, analytic and bounded in $R_e s > 0$, and continuous on the imaginary axis, then $\|F\|_\infty$ equals the distance in the complex plane from the origin to the farthest point on the Nyquist plot of F. The space $L_2[0,\infty]$ is the class of vector-valued square-integrable functions. The norm on $L_2[0,\infty]$ is

$$\|X\|_2 := \left[\int_0^\infty x(t)^* x(t) dt\right]^{\frac{1}{2}} \qquad (3.2\text{-}5)$$

Where * denotes complex-conjugate transpose. The Laplace transform of $x(t)$ in $L_2[0,\infty]$, denoted by $x(s)$, belongs to the H_2 space of functions analytic in $R_e s > 0$ and H_2 norm is

$$\|X\|_2 := (2\pi)^{-1}\left[\int_0^\infty x(j\omega)^* x(j\omega)d\omega\right]^{\frac{1}{2}} \qquad (3.2\text{-}6)$$

Suppose $F \in H_\infty$. Then $Fx \in H_2$ whenever $x \in H_2$ and moreover

$$\|F\|_\infty = \sup\{\|Fx\|_2 : x \in H_2, \|x\|_2 = 1\} \qquad (3.2\text{-}7)$$

Therefor it can be concluded that

1. The space H_∞ is the class of all stable matrix-values functions.
2. The space H_2 is the class of Laplace transform of bounded input and bounded output signals.
3. H_∞ norm represents the energy gain.

3.2.3 STANDARD REPRESENTATION FOR H_∞ PROBLEM

The standard configuration for H_∞ optimal design [34] is shown in Fig. 3.1, where (v) is an 'external inputs' vector of all the signals entering the system, including load disturbance, sensor noise, reference input and so on. (z) is an 'error' vector of all the signals required to characterize the behaviour of the closed-loop system, for example, it can be error signals, weighted control output and so on. Both these vectors may contain elements which are abstract in the sense that they may be defined mathematically, but do not represent signals which actually exist at any point in the system. (u) is a control vectors, and (y) is the vector of measured outputs. The matrix $K(s)$ is the controller to be designed.

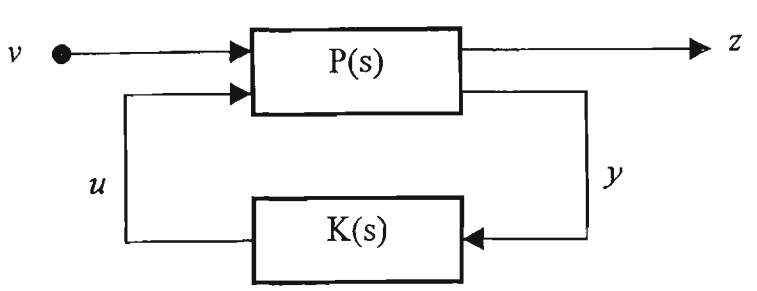

Fig. 3.1 Standard Configuration

$P(s)$ is a transfer matrix derived from the nominal plant model. However, it may also include weighting functions which depend on design problems to be solved. Suppose that $P(s)$ is partitioned as

$$P(s) = \begin{bmatrix} p_{11}(s) & p_{12}(s) \\ p_{21}(s) & p_{22}(s) \end{bmatrix} \tag{3.2-8}$$

So the equations corresponding to the system of Fig. 3.1 can be derived as follows:

$$\begin{aligned} z &= p_{11}v + p_{12}u \\ y &= p_{21}v + p_{22}u \\ u &= Ky \end{aligned} \tag{3.2-9}$$

The transfer matrix from v to z is denoted as $M(s)$, which can be obtained from the last equation where p_{22} is strictly proper and real rational.

$$M(s) = p_{11} + p_{12}K(I - p_{22}K)^{-1}p_{21} \tag{3.2-10}$$

The objective of H_∞ design is to determine a proper and real rational controller K, which can not only stabilize the closed-loop but also minimize the H_∞ norm of $M(S)$. In other words, H_∞ design is to solve the following optimal problem.

$$\min_{k\,stabilizing} \|M(s)\|_\infty \tag{3.2-11}$$

This is known as the H_∞ optimization problem. In the design, weighting functions are introduced to normalize $M(s)$. The weighting function expresses the relative importance of different frequencies (it is bigger for frequencies whose presence is more disturbing). By adjusting the weighting function, better performance at frequencies concerned can be obtained.

3.2.4 THE H_∞ PROBLEM FORMULATION

- ***CONDITION OF STABILITY ROBUSTNESS***

When the uncertainty $\Delta_M(s)$ is expressed in the multiplication form as shown in Fig. 3.2. The true plant transfer function is written as [34]:

$$G(s) = [1 + \Delta_M(s)]G_o(s) \tag{3.2-12}$$

Where, the effect of $\Delta_M(s)$ on the performance of a closed-loop system over the high frequency range, which corresponds to the stability robustness of the system is most concerned. Let $s = j\omega$

$$|\Delta_M(j\omega)| < I_m(\omega) \qquad (3.2\text{-}13)$$

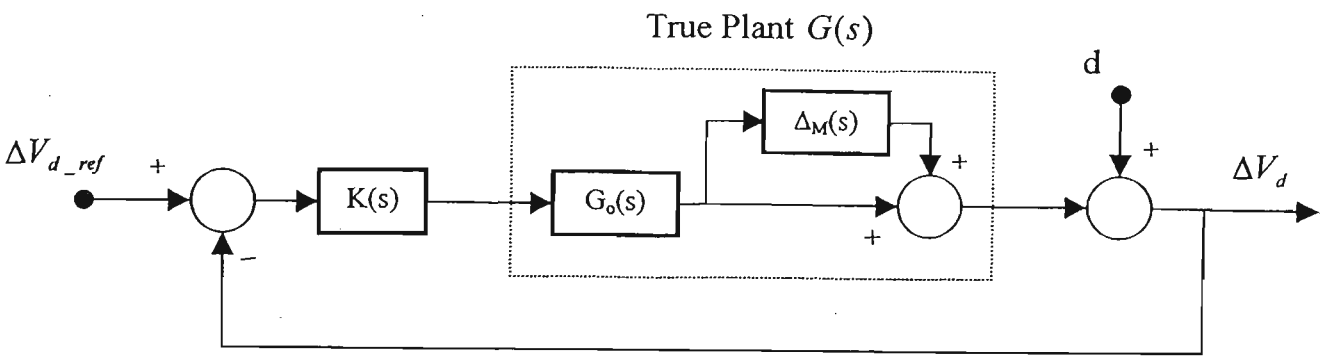

Fig. 3.2 Multiplicative Unstructured Uncertainty

$I_m(\omega)$ represents the boundary of the relative value in which the physical plant $G(j\omega)$ deviates from the plant mathematical model $G_o(j\omega)$. Assume the original system is stable (i.e. the locus of $1+G_o(j\omega)K(j\omega)$ meets the Nyquist stability criterion). Now in order to keep the system stable, it requires that when $G_o(j\omega)$ changes into $G(j\omega)$, the locus of $1+G(j\omega)K(j\omega)$ still meets the Nyquist stability criterion. The condition of the stability robustness is

$$|1+[1+\Delta_M(j\omega)]G_o(j\omega)K(j\omega)| > 0 \qquad (3.2\text{-}14)$$

From equation (3.2-14), the condition of the stability robustness can be written

$$\left|\frac{G_oK}{1+G_0K}\right| < \frac{1}{I_m} \qquad (|\Delta_M(j\omega)| < I_m(\omega)) \qquad (3.2.15)$$

This condition means that when the value of the uncertainty I_m increases the gain of the loop should decrease, otherwise the physical system may not be stable.

- ***CONDITION OF PERFORMANCE ROBUSTNESS***

The voltage error signal can be obtained from Fig. 3.2,

$$e = \Delta V_{d\_ref} - \Delta V_d = \frac{1}{1+(1+\Delta_M)G_oK}\Delta V_{d\_ref} - \frac{1}{1+(1+\Delta_M)G_oK}d \qquad (3.2\text{-}16)$$

It can be seen from the last equation that, when the gain of loop $G_o(j\omega)K(j\omega)$ increases,

the voltage error e would decrease. Therefore the condition of the performance robustness is given as

$$|G_o(j\omega)K(j\omega)| \geq ps(\omega) \qquad \forall \omega \leq \omega_{ps} \qquad (3.2\text{-}17)$$

Where $ps(\omega)$ is the performance specification, ω_{ps} represents the spectrum width of exogenous signals.

Based on the preceding discussion, it is shown that H_∞ theory allows for both stability robustness and performance robustness to be considered at the design stage. The design principles of the controller can be summarized as follows:

1. The nominal system should be stable.
2. The gain at low frequencies should be higher than the performance boundary $ps(\omega)$ as shown in Fig. 3.3 that is specified according to the requirements for the tracking error or attenuation of disturbance.
3. The gain at high frequencies should be lower than the boundary $\frac{1}{I_m}$ as shown in Fig. 3.3 that is specified according to the requirements for the noise or uncertainty.

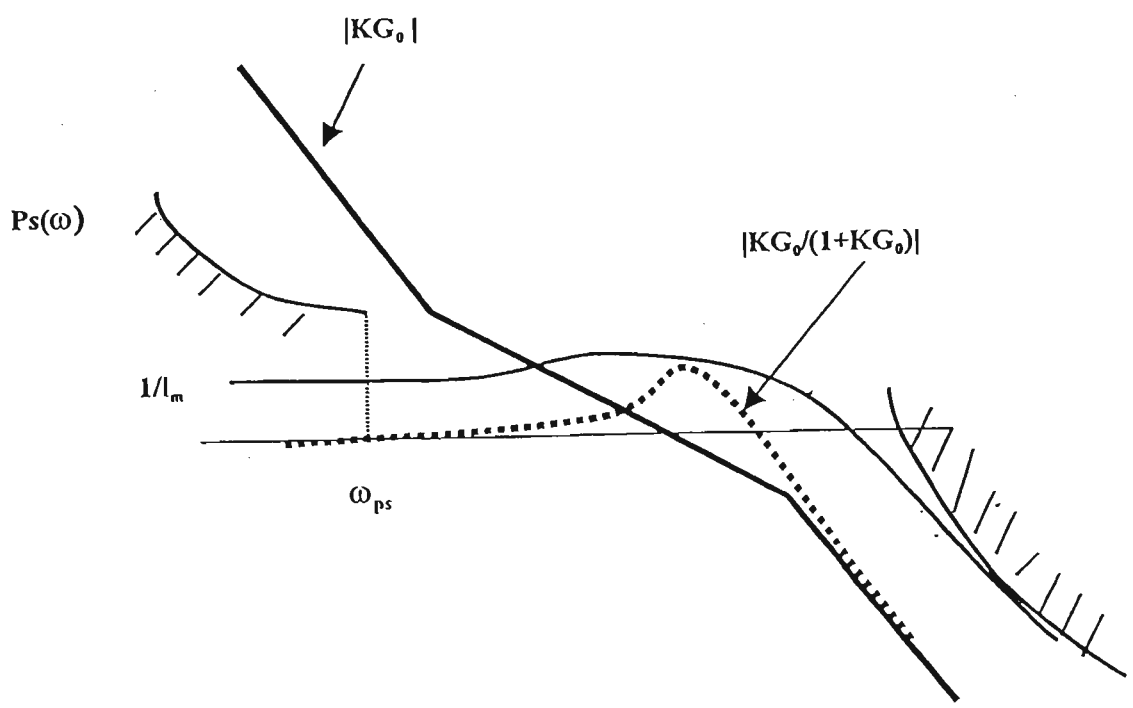

Fig. 3.3 The Bode Plot of Design Principles

3.3 DESIGN OF THE H∞ CONTROLLER

The H_∞ controller is proposed as a DC voltage regulator, which is to work with the PCFF current control to compensate for uncertainty problem. The H_∞ voltage regulator is designed in the frequency domain based on the worst case scenario: the sudden change of the operating condition from rectifying to regeneration. This load disturbance causes uncertainty problem as the original plant transfer function experiences a significant change due to the shift of the operating point, and should be dealt with by the H_∞ voltage regulator.

3.3.1 A 10KVA MODEL POWER CONVERTER

The plant model used for the design is derived based on the experimental system (a 10 kVA IGBT voltage source converter) available in out control laboratory. The schematic circuit of the voltage source converter is shown in Fig. 2.1 of Chapter 2. The three-phase bridge is connected to the power grid supplying e_1, e_2 and e_3 via a set of line reactances, L. The output DC voltage, V_d, is delivered across the DC link capacitor, C. The DC load is modeled by a Thevenin equivalent circuit with a load resistance R_o and a back EMF, E_L. The parameters of the entire model system are given as follows.

Utility supply phase voltage $e_m = 60$ volts; Line inductance $L = 10$ mH

Line resistance $R = 1\ \Omega$; Load resistance $R_o = 40\ \Omega$;

DC link voltage capacitor $C = 200\ \mu$F; DC link voltage reference $V_{d\_ref} = 150$ volts;

Switching frequency $f_{sw} = 1250$ Hz; Sampling frequency $f_{sm} = 2500$ Hz;

In the design of the DC voltage regulator, $K(s)$, the PCFF controller, together with the power converter of Fig. 2.2 is treated as one plant. The transfer function of the plant from the current reference, Δi_{cm}, to the DC link voltage output, ΔV_d, is given as equation (2.4-18) and is rewritten here:

$$G_o(s) = \frac{\Delta V_d(s)}{\Delta i_{cm}(s)} = K_p \frac{\left(1 - \frac{s}{\omega_o}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right)\left(1 + \frac{s}{\omega_{p2}}\right)} \qquad (3.3\text{-}1)$$

The expressions of K_p, ω_o, ω_{p1} and ω_{p2} depend on the parameters of the PWM power converter and operating point as shown:

$$K_p = \frac{3(E_m - 2I_{cm}R)}{2V_d\left(\frac{\left(2-\frac{E_L}{V_d}\right)}{R_o}\right)} \qquad \omega_o = \frac{E_m - 2I_{cm}R}{LI_{cm}} \qquad \omega_{p1} = \frac{2-\frac{E_L}{V_d}}{R_oC} \qquad \omega_{p2} = \frac{1}{T_s}$$

The block diagram of the H_∞ controlled system is formed as shown in Fig. 3.4, where d represents disturbances and the H_∞ controller, $K(s)$, is to be designed.

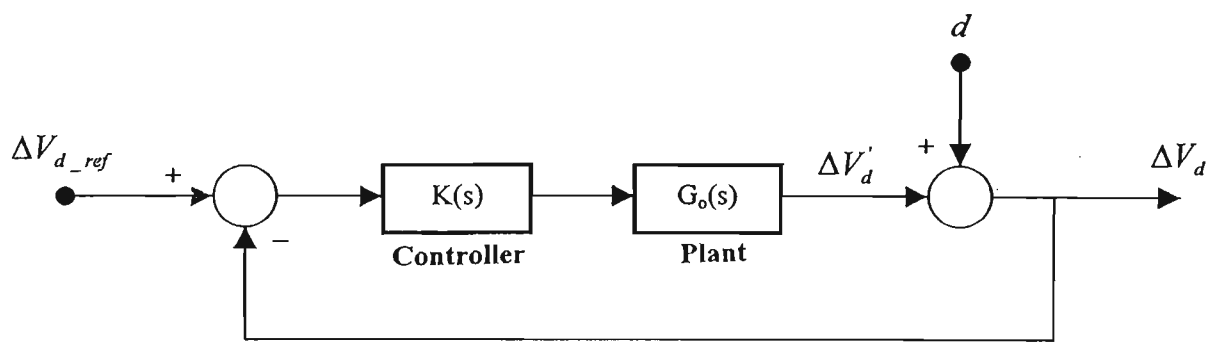

Fig. 3.4 The H_∞ Controlled PCFF Converter

The H_∞ voltage regulator is designed in the frequency domain based on the worst possible scenario: the sudden change of the operating condition from rectifying to regeneration. That is, the system is first operated in a rectifying mode with a zero back EMF, then a 290-volt step change in back EMF voltage is suddenly applied, forcing the load current to change its direction by flowing into the power converter. This disturbance causes the plant transfer function to change from $G_{o1}(s)$ of the rectifying mode to $G_{o2}(s)$ of the regeneration mode as given in equations (3.3-2) and (3.3-3) respectively.

$$G_{o1}(s) = \frac{\Delta V_d(s)}{\Delta i_{cm}(s)} = 9.16\frac{\left(1-\frac{s}{645.07}\right)}{\left(1+\frac{s}{250}\right)\left(1+\frac{s}{1250}\right)} \qquad (3.3\text{-}2)$$

$$G_{o2}(s) = \frac{\Delta V_d(s)}{\Delta i_{cm}(s)} = 295.8 \frac{\left(1 - \frac{s}{921.5}\right)}{\left(1 + \frac{s}{8.33}\right)\left(1 + \frac{s}{1250}\right)} \qquad (3.3\text{-}3)$$

Comparing the last two equations, the variations in their corresponding pole, zero and DC gain are significant.

3.3.2 DESIGN OF THE H_∞ VOLTAGE REGULATOR

Referring to the H_∞ controlled PCFF power converter of Fig. 3.4, the design of the H_∞ voltage regulator is treated as the problem of mixed sensitivity and the complementary sensitivity minimization. Denoted S and $I - S$ as the sensitivity function and complementary sensitivity function respectively, they are reflected in the transfer matrix $M(s)$ as

$$M(s) = \begin{bmatrix} W_1 S \\ W_2(I - S) \end{bmatrix} \qquad (3.3\text{-}4)$$

where $$S = (I + G_o K)^{-1} \qquad (3.3\text{-}5)$$

$$I - S = G_o K (I + G_o K)^{-1} \qquad (3.3\text{-}6)$$

W_1 and W_2 are frequency-dependent weighting functions, they are introduced to normalize $M(s)$. The weighting function expresses the relative importance of different frequencies (it is bigger for frequencies whose presence is more disturbing). The design process is basically adjusting the gain of the weighting function W_1 to obtain optimal performance at frequencies concerned.

The system performance requirement is reflected in the weighted sensitivity function

$$W_1 S = W_1 (I + G_o K)^{-1} = W_1 [I - G_o K (I + G_o K)^{-1}] \qquad (3.3\text{-}7)$$

While the stability robustness of the system is reflected in the weighted complementary sensitivity function.

$$W_2 (I - S) = W_2 G_o K (I + G_o K)^{-1} \qquad (3.3\text{-}8)$$

Relations between weighting functions and error signals in Fig. 3.4 can be found by substituting (3.3-7) and (3.3-8) in (3.3-4), and then comparing the resulting equation with (3.2-10), we have p_{11}, p_{12}, p_{21} and p_{22} as

$$p_{11}=\begin{bmatrix} W_1 \\ 0 \end{bmatrix}, \quad p_{12}=\begin{bmatrix} -W_1 G_o \\ W_2 G_o \end{bmatrix}, \quad p_{21}=I, \quad p_{22}=-G_o \qquad (3.3\text{-}9)$$

This is equivalent to choosing vectors $v=\begin{bmatrix} v_1 \\ v_2 \end{bmatrix}$ and $z=\begin{bmatrix} z_1 \\ z_2 \end{bmatrix}$ with $v_1=d$, $v_2=\Delta V_{d-ref}$, $z_1=W_1\Delta V_d$, $z_2=W_2\Delta V_d'$. Referring to Fig. 3.4, d, ΔV_{d_ref}, ΔV_d and $\Delta V_d'$ are the disturbance, reference input and variations of outputs respectively.

The optimal design of the H_∞ voltage regulator is realized by formulating a cost function, based on which, the H_∞ norm of the transfer matrix $M(s)$ of (3.3-7) is minimized. Note that $M(s)$ combines specifications of performance robustness and stability robustness. The design criterion is thus given by

$$\min_{k\_stabilizing} \|M(s)\|_\infty = \min_{k\_stabilizing} \left\| \begin{matrix} W_1 S \\ W_2(I-S) \end{matrix} \right\|_\infty \qquad (3.3\text{-}10)$$

Where the H_∞ voltage regulator, $K(s)$ is to be designed by solving the criterion for W_1 and W_2 so that the H_∞ norm of $M(s)$ is minimized. Steps taken for the optimal design of $K(s)$ can be summarized as follows:

1. To define an initial weighting function $W_2(s)$ according to $I_m(s)$;
2. To define an initial weighting function $W_1(s)$ according to $ps(s)$;
3. To satisfy the following criterion for final $W_1(s)$ and $W_2(s)$;

$$\gamma := \min_{k\_stabilizing} \left\| \begin{matrix} W_1 S \\ W_2(I-S) \end{matrix} \right\|_\infty \qquad \gamma \approx 1;$$

4. If $\gamma \geq 1+\varepsilon$, then to reshape $W_1(s)$ and go to step 3;
5. If $\gamma < 1$, then to increase the gain of $W_1(s)$ and go to step 3;
6. When γ approaches one, $W_1(s)$ and $W_2(s)$ can be used to calculate $K(s)$.

- ***DESIGN SPECIFICATIONS***

In this design, $G_{o1}(s)$ is chosen as the nominal model, based on which the H_∞ voltage regulator is designed. The worst case scenario is considered when the system is suddenly changes its operation mode from rectifying to the regeneration. The most important design specification is that the system must be stable under such a substantial change of operating condition. This requires the transition time to be as fast as possible and confined to one cycle of the line frequency (50 Hz). This means that the bandwidth of the closed-loop system should be as narrower than 50Hz as possible to attenuate line noises. The following frequency domain specifications are defined:

Gain crossover frequency ≤ 125 rad/sec;

Phase margin P_m > 45 deg;

Gain margin G_m > 8 db;

A reasonably damped responses

Where the gain crossover frequency of 125 rad/sec corresponds to a bandwidth of 20 Hz. The selection of phase margin > 45° and gain margin > 8 dB is a common design practice to insure sufficient damping of a transient response. With this design objective, it is expected that the maximum singular value of S, $\sup\bar{\sigma}[S]$, decreases sharply over the frequency range below 125 rad/sec, whereas the maximum singular value of the complementary sensitivity function, $\sup\bar{\sigma}[I-S]$ attenuates quickly over the frequency range above 125 rad/sec. In order to achieve this, the mixed performance and robustness problem defined in equation (3.3-10) should be solved.

- ***DESIGN RESULTS***

The selection of weighting function $W_2(s)$ is based on $I_m(s)$, the boundary of the relative value in which the physical plant is deviates from the plant mathematical model due to uncertainties. Assume $I_m(s)$ is a time delay in nature, viz.

$$I_m(s) = e^{-\varpi} - 1 \qquad (3.3\text{-}11)$$

The Taylor series expansion of a function $f(x)$ around operating value $x = x_0$ is

$$f(x) = f(x_0) + \left.\frac{df(x)}{dx}\right|_{x=x_0} (x - x_0) + \cdots \qquad (3.3\text{-}12)$$

Applying the Taylor expansion to $I_m(s)$ around $t = 0$ and ignoring the higher order terms, the initial weighing function $W_2^{-1}(s)$ is therefore chosen to be

$$W_2^{-1}(s) = \frac{1}{\tau_1 s + 0.01} \qquad (3.3\text{-}13)$$

Where, τ_1 is a constant value in terms of the delay uncertainty.

The selection of initial weighting function $W_1(s)$ is based on $ps(s)$, the performance specifications for error tracking. An integral controller is commonly used for this purpose. Thus

$$W_1(s) = \frac{1}{s + 0.01} \qquad (3.3\text{-}14)$$

Where the location of pole is selected at –0.01 instead of at the origin to meet algorithm requirements. By following the design procedure given in the preceding discussion, the final weights $W_1(s)$ and $W_2(s)$ are determined according to the optimization procedure. It can be seen that in the following expression of final $W_1(s)$ and $W_2(s)$, more poles and zeros are added to shape the frequency response of $M(s)$ as specified.

$$W_2^{-1}(s) = \frac{3(T_1 s + 1)}{(T_2 s + 1)} \qquad (3.3\text{-}15)$$

$$W_1(s) = \frac{\rho(T_5 s + 1)(T_6 s + 1)}{(T_3 s + 1)(T_4 s + 1)} \qquad (3.3\text{-}16)$$

where $T_1 = \frac{1}{5000}$, $T_2 = \frac{1}{500}$, $T_3 = 100$, $T_4 = \frac{1}{20}$, $T_5 = \frac{1}{100}$, $T_6 = \frac{1}{105}$ and $\rho = 1750$.

In H_∞ optimal design, ρ of equation (3.3-16) should be as large as possible to obtain the maximum attenuation of disturbance and the H_∞ optimal design is obtained at ρ=1750. The resulting H_∞ voltage regulator, $K(s)$ has its poles and zeros at:

Gain:	0.146;			
Poles:	0,	-2,	-321.2,	-1960;
Zeros:	-35.32,	-49.98,	-199.74;	-6061.2;

This raw controller is of 4th order, and can be order-reduced to a 3rd order one by simply ignoring the insignificant zero and pole at -1960 and –6061.2 respectively. Thus the expression of the final H_∞ voltage regulator, $K(s)$ is obtained:

$$K(s) = 0.146\frac{(s+35.32)(s+49.98)(s+199.74)}{s(s+2)(s+321.2)} = 80\frac{\left(1+\frac{s}{35.32}\right)\left(1+\frac{s}{49.98}\right)\left(1+\frac{s}{199.74}\right)}{s\left(1+\frac{s}{2}\right)\left(1+\frac{s}{321.2}\right)} \tag{3.3-17}$$

The Bode plot for W_1, W_2^{-1}, KG_{o1} and KG_{o2} is shown in Fig. 3.5.

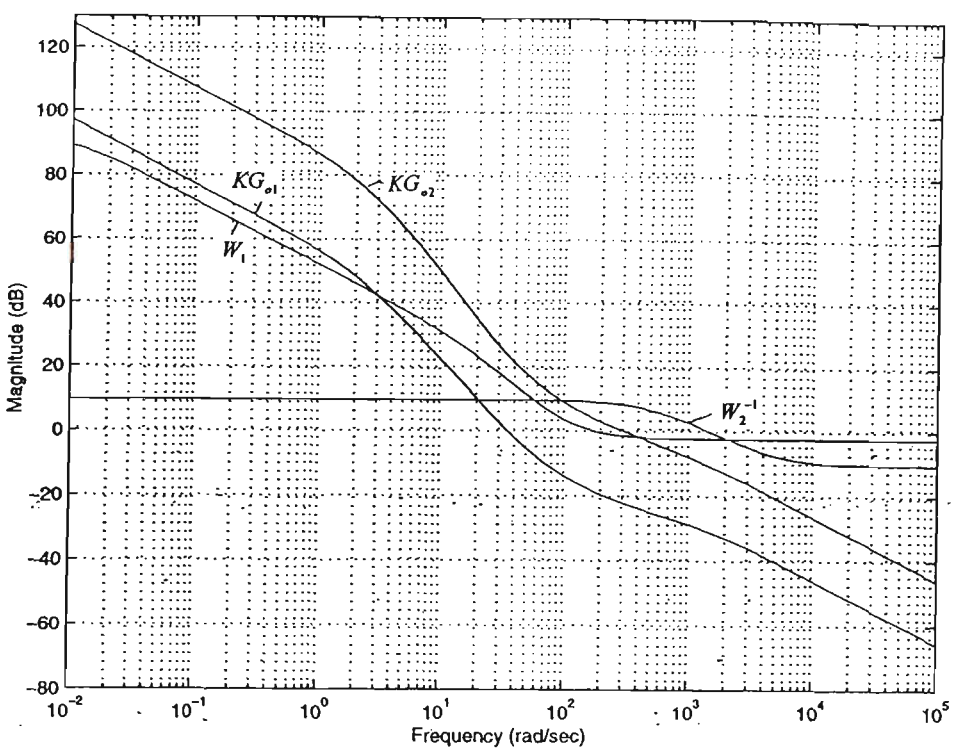

Fig. 3.5 Bode Plot of W_1, W_2^{-1}, KG_{o1} and KG_{o2}

The robustness of the proposed H_∞ voltage regulator is illustrated in Fig. 3.5, where $W_1(\omega)$ and $W_2(\omega)$ represent $ps(\omega)$ and $I_m(\omega)$ respectively. By comparing Fig. 3.3 with Fig. 3.5, it can be seen that gains of KG_{o1} and KG_{o2} are higher than the performance boundary $W_1(\omega)$ at low frequencies and are lower than the stability boundary $W_2^{-1}(\omega)$ at

high frequencies. This means that the designed H_∞ voltage regulator satisfies the robustness requirement.

The optimal design result is illustrated in Fig. 3.6, where the solution of the gain of the optimal transfer matrix $M(s)$ is plotted. It can be seen that for frequencies below the specified gain crossover frequency of 125 rad/sec, the gain of $M(s)$ is very close to 0dB, corresponding to $\gamma \approx 1$. Hence the H_∞ optimal design is obtained.

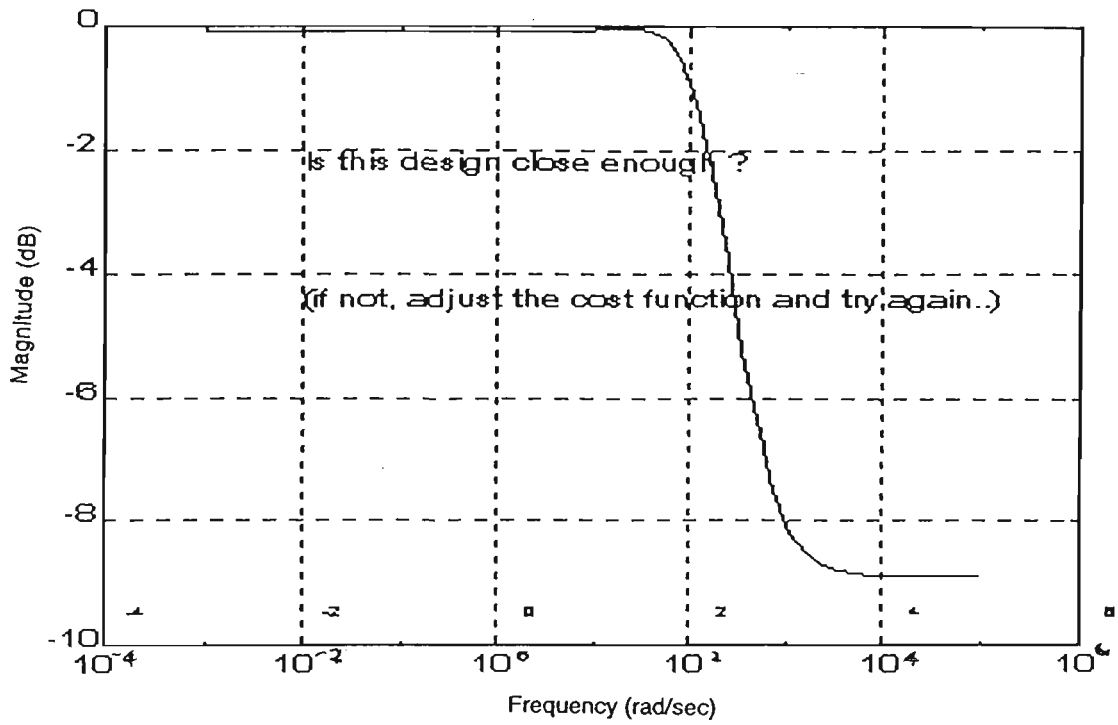

Fig. 3.6 The Gain Plot of the Optimal M(s)

The author uses programs in the Robust control Toolbox of MATLAB 5.1 to get the solutions[29].

3.4 THE PERFORMANCE OF THE H$_\infty$ CONTROL SYSTEM

Absolute stability, relative stability and discrete-time stability of the system under the proposed control strategy are analysed. The absolute stability refers to the condition of whether the system is stable or not, while the degree of the stability is measured by the relative stability. Stability analysis of discrete-time system in the z plane is to be carried out for implementation [35].

3.4.1 THE ABSOLUTE STABILITY OF THE SYSTEM

The Routh-Hurwitz criterion represents a method of determining the location of zeros of a polynomial with constant real coefficients with respect to the left and right half of s plane, without actually solving for the zeros. The characteristic equation of the designed system is:

$$1 + G_n(s)K(s) = 0 \qquad (3.4\text{-}1)$$

From (3.4-1), the characteristic equation for rectifying operation can be derived:

$$s^5 + 1175.3s^4 + 1031195s^3 + 208905970s^2 + 7830537497.2s + 147359014089 = 0 \qquad (3.4\text{-}2)$$

Since the equation (3.4-2) has no missing terms and the coefficients are all of the same sign, the Routh-Hurwitz criterion is used. Routh's tabulation is formed as follows:

s^5	1	1031195	7830537497.2
s^4	1175.3	208905970	147359014089
s^3	853448	7705157582.2	0
s^2	198295046.1	147359014089	0
s^1	7070934699	0	0
s^0	147359014089	0	0

Since there is no change in sign in the first column of the tabulation, the equation has no root in the right half of s-plane. The designed system is stable.

The characteristic equation for regeneration operation and Routh's tabulation are:

$$s^5 + 1355.58s^4 + 546831.95s^3 + 54952994.24s^2 + 3723609368.17s + 71250683947 = 0 \qquad (3.4\text{-}3)$$

s^5	1	546831.95	3723609368.17
s^4	1355.58	54952994.24	71250683947
s^3	506293.58	3671021255.21	0
s^2	45123987.53	712506833947	0
s^1	2871584728.7	0	0
s^0	71250683947	0	0

The system is stable under regeneration operation.

3.4.2 THE RELATIVE STABILITY OF THE SYSTEM

The relative stability measures how stable the system is. The Bode plot of the loop transfer function of the system is a very useful graphical tool for the analysis of the relative stability. The gain margin (GM) and phase margin (PM) which are used as the relative stability measures, are more easily determined on the Bode plot.

The loop transfer function of the closed-loop system under the rectifying operation can be derived from the characteristic equation in (3.4-2).

$$L_{01}(s) = G_{01}(s)K(s) = 647.87\frac{(-s+645.07)(s+35.32)(s+49.98)(s+199.74)}{s(s+2)(s+250)(s+321.2)(s+1250)} \qquad (3.4\text{-}4)$$

The Bode plot of $L_{01}(j\omega)$ is shown in Fig. 3.7, which indicates:

Gain-crossover frequency $\omega_g = 106.89$ rad/sec; Gain Margin GM=13.43dB;

Phase Margin PM=68.25deg;

The loop transfer function of the system under the regeneration operation is:

$$L_{02}(s) = G_{02}(s)K(s) = 219.29\frac{(-s+921.5)(s+35.32)(s+49.98)(s+199.74)}{s(s+2)(s+8.33)(s+321.2)(s+1250)} \qquad (3.4\text{-}5)$$

The Bode plot of $L_{02}(j\omega)$ is given in Fig. 3.8. The plot illustrates a conditionally stable system. There are three phase crossovers at 2.1rad/sec, 38.16rad/sec and 1150rad/sec respectively. The phase characteristics indicate that the system would be stable if the gain crossover lies between the frequency range of 38.16rad/sec and 1150rad/sec. The following results are obtained:

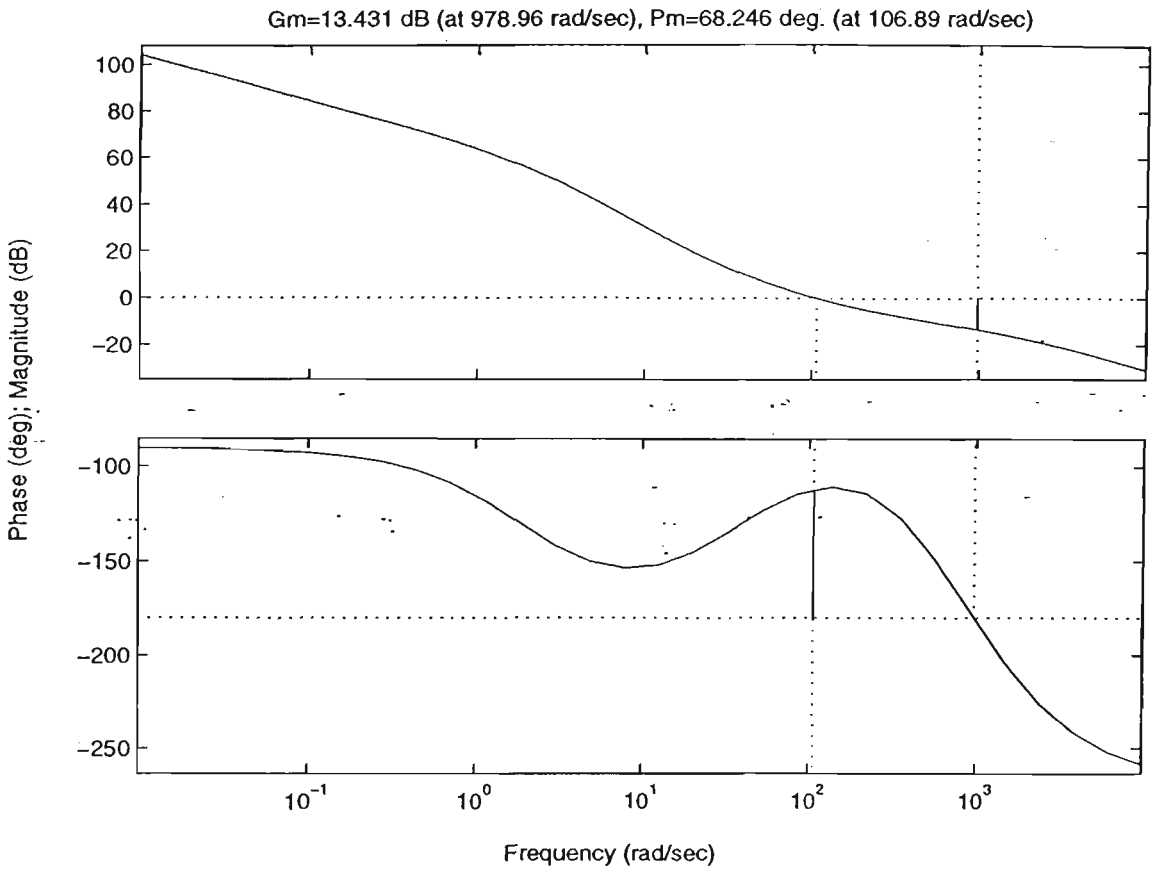

Fig. 3.7 Determination of Gain Margin and Phase Margin on the Bode Plot of $L_{01}(s)$

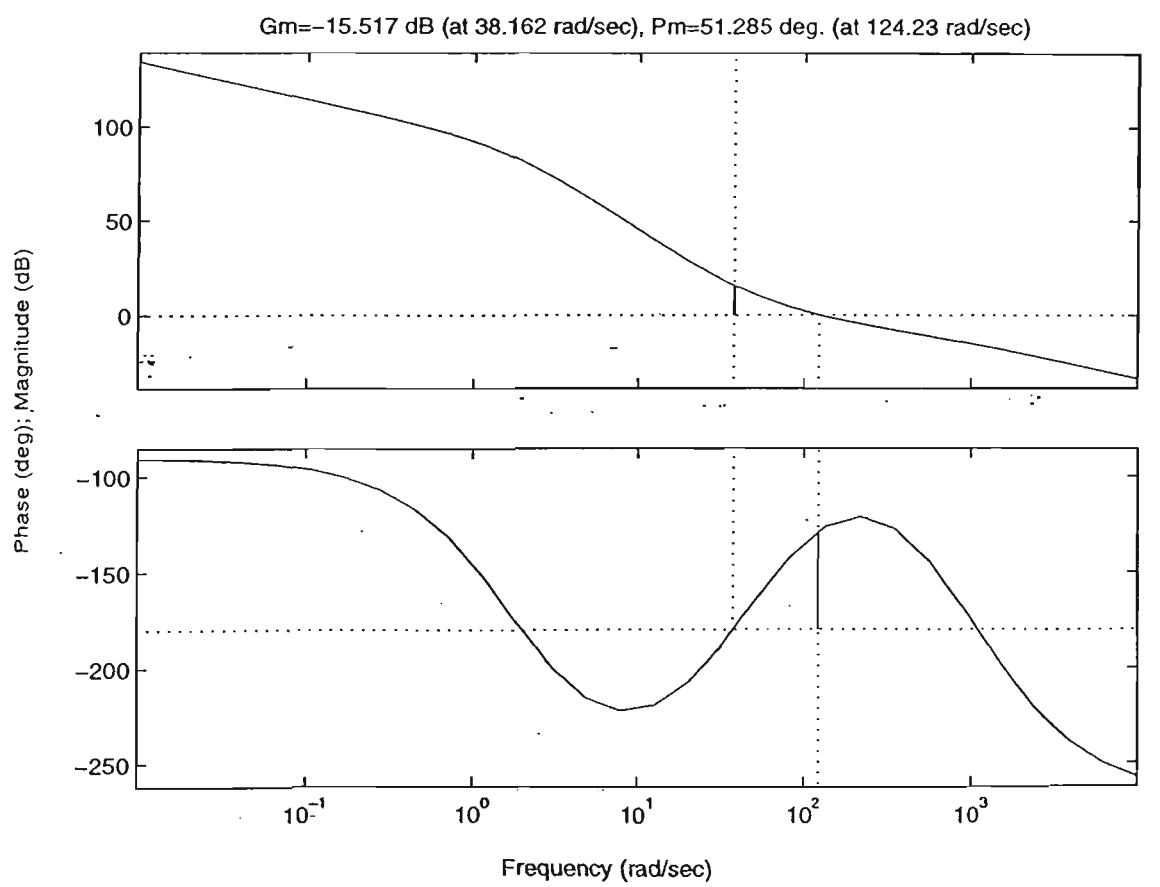

Fig. 3.8 Determination of Gain Margin and Phase Margin on the Bode Plot of $L_{02}(s)$

Gain-crossover frequency $\omega_g = 124.23$ rad/sec; Phase Margin PM=51.285deg;

Gain Margin GM_1=15.52dB, GM_2=16.20dB;

It can be seen from Fig. 3.8 that $GM_1 \approx GM_2$, which demonstrates that an optimal design of the controller has been obtained.

From the Bode plot for the rectifying model and the regeneration model, the design of predictive PWM power converter with an H_∞ voltage regulator meets all design specifications.

3.4.3 STABILITY ANALYSIS IN THE Z PLANE

Discrete-time system arises in this project due to a computer-controlled converter is used as an experimental system. It is necessary to investigate the stability of discrete-time system in the z plane. A linear dynamic system is stable if all poles of the transfer function lie in the left-half s plane. In the z plane, the left-half s plane corresponds to the unit circle centred at the origin, or the left-half s plane maps into the inside of the unit circle in the z plane. The discrete-time PCFF controlled system with H_∞ DC voltage regulator is shown in Fig. 3.9. The sampling frequency is 2500Hz.

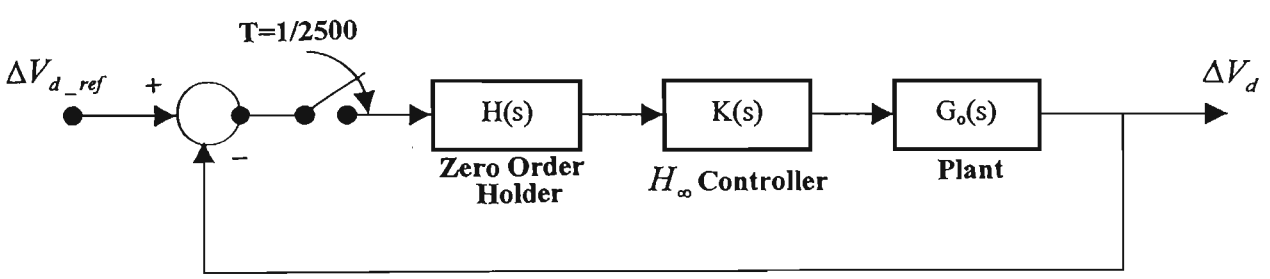

Fig. 3.9 The Discrete-Time PCFF Control System with H_∞ Controller

The open-loop transfer function of the system under the rectifying operation can be obtained from (3.4-4). The z transform of $L_{01}(s)$ is

$$L_{01}(z) = \frac{-0.164z^4 + 0.688z^3 - 1.074z^2 + 0.741z - 0.190}{z^5 - 4.389z^4 + 7.657z^3 - 6.626z^2 + 2.841z - 0.482} \qquad (3.4\text{-}6)$$

The characteristic equation becomes

$$z^5 - 4.554z^4 + 8.344z^3 - 7.700z^2 + 3.582z - 0.673 = 0 \qquad (3.4\text{-}7)$$

from which the roots are found to be

$$z_{1,2} = 0.825 \pm j0.2499; \qquad z_{3,4} = 0.901 \pm j0.008; \qquad z_5 = 0.918;$$

Thus, no root of the characteristic equation has a magnitude greater than unity, and the system is stable.

The loop transfer function of the system under the regeneration operation is derived from (3.4-5). Its z transform is $L_{02}(s)$

$$L_{02}(z) = \frac{-0.055z^4 + 0.238z^3 - 0.383z^2 + 0.271z - 0.071}{z^5 - 4.482z^4 + 7.977z^3 - 7.040z^2 + 3.076z - 0.531} \qquad (3.4\text{-}8)$$

The characteristic equation is

$$z^5 - 4.537z^4 + 8.215z^3 - 7.423z^2 + 3.348z - 0.603 = 0 \qquad (3.4\text{-}9)$$

from the characteristic equation, the roots are found to be

$$z_{1,2} = 0.905 \pm j0.093; \qquad z_{3,4} = 0.828 \pm j0.100; \qquad z_5 = 0.776;$$

There is no root of characteristic equation which has a magnitude greater than unity. The system is stable.

3.5 SUMMARY

In this chapter, the H_∞ controller is proposed and designed as the DC voltage regulator, which is to work with the PCFF controller and compensate its uncertainty problem. The method of the mixed sensitivity and complementary sensitivity functions is used in this study. The advantage of this method is that it allows for both the stability robustness and performance robustness to be considered at the design stage, and problem caused by the system uncertainties are dealt with regardless of whether they are structured or unstructured uncertainties [29]. The design specifications are reflected in the selection of initial weighting functions $W_1(s)$ and $W_2(s)$ respectively, then a cost function is formulated based on the disturbance transfer function $M(s)$. The H_∞ norm of $M(s)$ is then minimized to find the final value of $W_1(s)$ and $W_2(s)$ by following a systematic optimal design approach. The H_∞ controller $K(s)$ is finally determined based on the results of $W_1(s)$ and $W_2(s)$. From the simulation results, it can be seen that the characteristics of the designed system satisfy the design specifications. It optimizes the disturbance transfer matrix in such a way that the maximum loop gain is obtained. The performance of the H_∞ voltage regulator combined with PCFF control is simulated using the MatLab in next Chapter.

Chapter 4

SIMULATION AND SIMULATION RESULTS

4.1 INTRODUCTION

In Chapter 2 and 3, the principles, models and designs of the predictive current controller and the H_∞ voltage regulator for the three-phase PWM power converter are presented. The mathematical analysis of these control strategies show respectively that the former is capable of delivering nearly sinusoidal current waveform with a unity power factor, while the latter can achieve stability robustness and performance robustness for the output DC link voltage.

In this Chapter the digital simulation of the entire closed-loop system is presented, using MatLab/SIMULINK environment, running on a Unix machine. In the simulation, the steady state responses of the system under both rectifying and regeneration operations are studied. The transient responses of the system are simulated for cases of step change in DC voltage reference, as well as the worst load variation from the rectifying to the regeneration. The results obtained are in good agreement with the theoretical prediction.

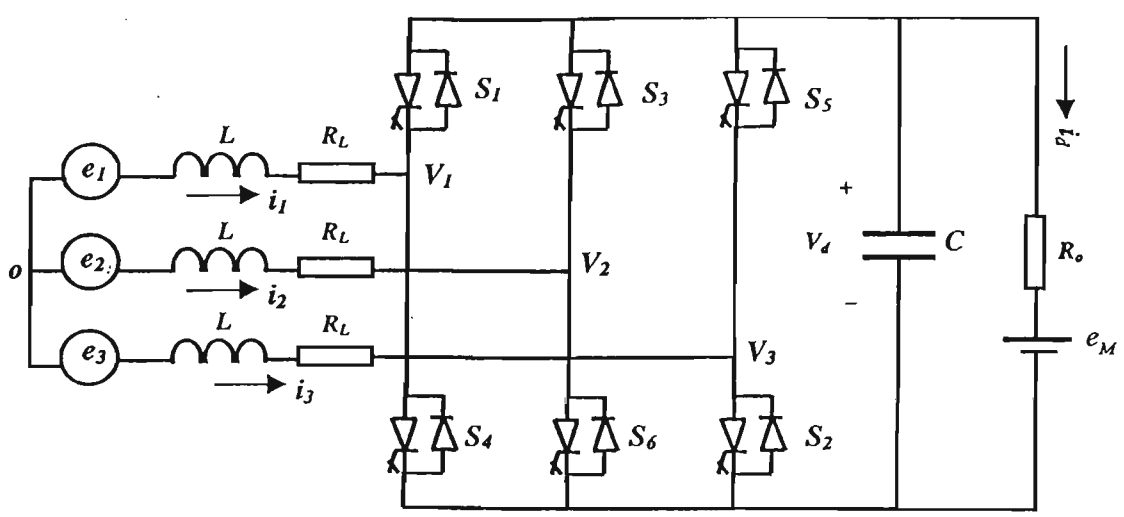

Fig. 4.1 Three Phase PWM AC/DC Power Converter

The simulation is based on the experimental system of the 10kVA voltage source converter as shown Fig. 4.1. All parameters of the system are given in section 3.3.1 of Chapter 3 and are specified in a MatLab set up file (see Appendix B).

4.2 THE SIMULATION PACKAGE USED

MatLab environment is a high-performance interactive software package used for scientific and engineering numeric computations. It integrates numerical analysis, matrix computation, signal processing, and graphics in an easy-to-use environment where problems and solutions are expressed just as they are written mathematically, without requiring traditional programming.

As an extension of the popular MatLab environment, SIMULINK is more flexible and faster than Matlab while retaining all of Matlab's general-purpose functionality. SIMULINK uses block diagrams to represent dynamic systems, and defining a system is much like drawing a block diagram. Furthermore, instead of drawing every individual block, block can be copied from libraries, either using the standard block library supplied with SIMULINK or block libraries built by the user.

It is extremely convenient to use SIMULINK for a system simulation, since using several blocks with appropriate interconnections can simulate the real control system.

4.3 SIMULATION CONFIGURATION

The simulation structure of the entire system is given in Fig. 4.2, where only one phase is shown in detail. Other two phases are shown in subsystem blocks **Phase Two** and **Phase Three** respectively. There are also six subsystems shown as black blocks in Fig. 4.2, being the **Step Signal Generator**, **Phase Lead**, **H_∞ Controller**, **PCFF Controller**, **PWM Modulator** and **Crossover Delay**. The details of each subsystem are discussed in following sections.

In this simulation, the DC voltage reference, V_{d_ref}, and load back EMF, E_M, are generated by using **Step** blocks (V_{d_ref}, BackEMF). The **Repeating Sequence** block is used as a

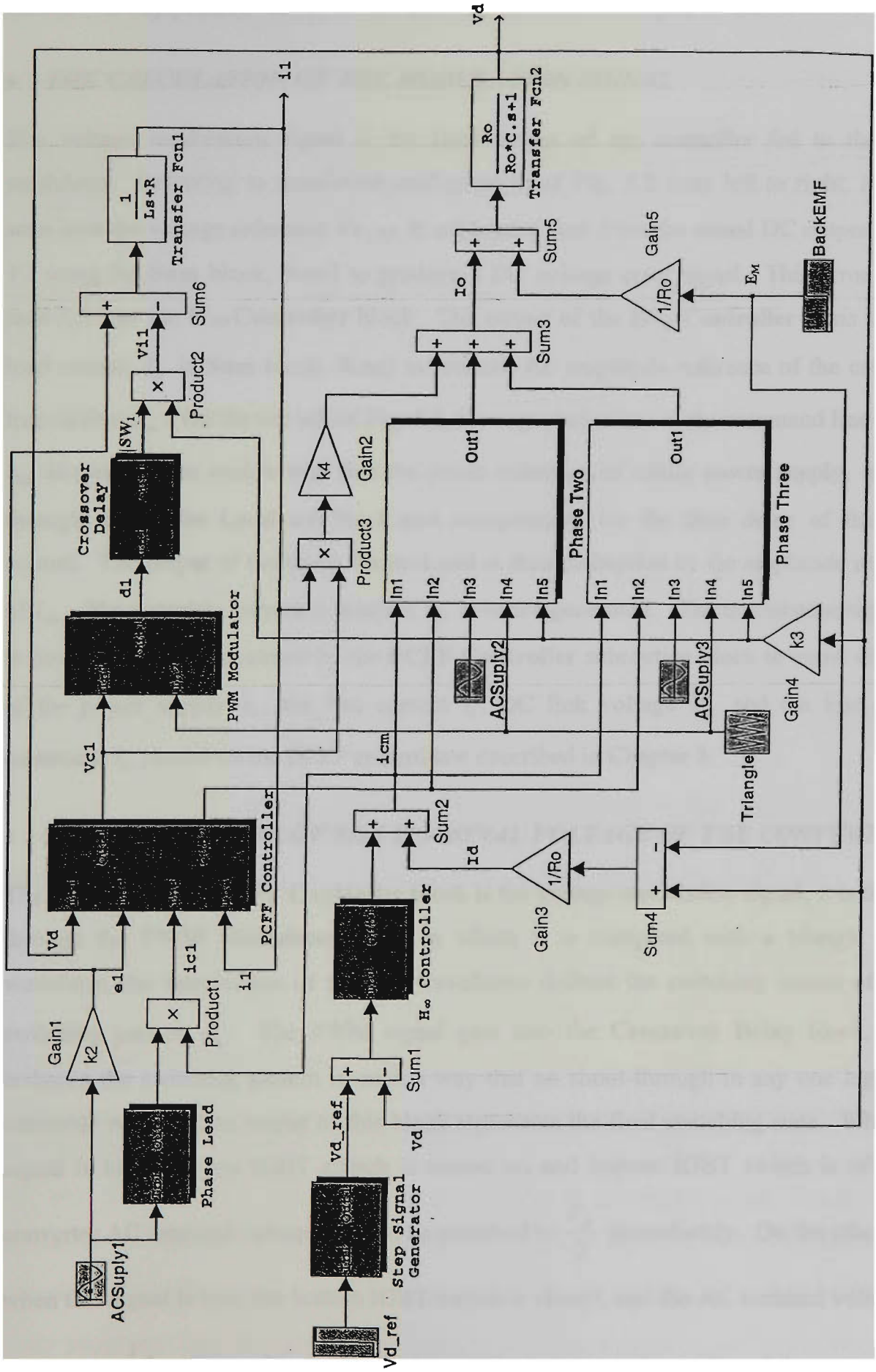

Fig. 4.2 Simulation Block Diagram of Three Phase Predictive PWM AC to DC Converter with H_∞ Controller

triangle carrier generator. Three-phase power supplies are generated by three **Sine Wave** blocks (ACSuply1,2,3). These blocks generate independent signal to the simulated system.

- ***THE CALCULATION OF THE MODULATION SIGNAL***

The voltage modulation signal is the final output of the controller fed to the PWM modulator. Referring to simulation configuration of Fig. 4.2 from left to right, it can be seen how the voltage reference V_{d_ref} is subtracted first from the actual DC output voltage V_d using the **Sum** block, Sum1 to produce a DC voltage error signal. This error term is then fed into the **H∞ Controller** block. The output of the **H∞ Controller** sums with the load current I_d in **Sum** block, Sum2 to produce the amplitude reference of the command line current i_{cm}. On the top left of Fig. 4.2, the angle reference of the command line current i_{cm} is produced in such a way that the phase reference of utility power supply, e_1, goes through the **Phase Lead** sub-block and compensates for the time delay of the PCFF control. The output of the block **Phase Lead** is then multiplied by the amplitude reference of i_{cm}. The complete current command, i_{c1} is hence generated. The modulation signal V_{c1} is now ready to be calculated by the **PCFF Controller** subroutine block in terms of inputs of the power supply e_1, the line current i_1, DC link voltage V_d and the line current command i_{c1}, based on the PCFF control law described in Chapter 3.

- ***THE CALCULATION OF THE TERMINAL VOLTAGE OF THE CONVERTER***

The output from the **PCFF Controller** block is the voltage modulation signal, it is then fed through the **PWM Modulator** block in which it is compared with a triangle carrier waveform, the intersection of the two waveforms defines the switching instant of PWM switching pattern d_1. The PWM signal gets into the **Crossover Delay** block, which reshapes the switching pattern in such a way that no shoot-through in any one leg of the converter occurs. The output of this block represents the final switching state. When this signal is high, the top IGBT switch is turned on and bottom IGBT switch is off. The converter AC terminal voltage V_{i1} will be switched to $\frac{V_d}{2}$ immediately. On the other hand, when this signal is low, the bottom IGBT switch is closed, and the AC terminal voltage V_{i1} becomes $-\frac{V_d}{2}$. From this analysis, the terminal phase voltage V_{i1} of the converter is

obtained by multiplying the switching pattern, i.e. the output of the **Crossover Delay** block, by $K_3 * V_d$ (using **Gain** block, Gain4 and **Product** block, Product2).

- *THE CALCULATION OF THE AC LINE CURRENT*

With the knowledge of the AC terminal voltage of the converter, the AC line current can be calculated using Ohm's law in the frequency domain. In Fig. 4.2, the line impedance is modeled by the **Transfer Fcn** block (Transfer Fcn1), to which the voltage difference between the voltage supply e_1 and the terminal voltage V_{i1} is applied. Please note that the line current i_1 obtained is fed into the **PCFF Controller** subroutine.

- *THE CALCULATION OF THE DC LINK VOLTAGE*

Referring to Fig. 4.1, the DC link voltage can be calculated from the back EMF voltage, converter's output DC current, I_o, and impedance in the frequency domain as follows:

$$V_d = (I_0 + \frac{E_M}{R_0}) \frac{R_0}{R_0 Cs + 1} \qquad (4.3\text{-}1)$$

where the DC current, I_o, is determined by $\sum_{k=1}^{3} i_k d_k$ based on equation (2.3-7) of Chapter 2.

Currents I_o and $\frac{E_M}{R_o}$ are summed using **Sum5** block before feeding into **Transfer Fcn2** block to generate V_d, which is then fed back for error calculation at **Sum1** block.

The **BackEMF block** shown in Fig. 4.2 is only used to model the sudden change in operation mode of the converter from the rectifying mode, when E_M is zero, to the regeneration mode, when E_M is 290 Volts.

4.3.1 THE PCFF CONTROLLER SUBBLOCK

The **PCFF Controller** subroutine is simulated in a subsystem block, based on the mathematical expression of this function given by equation (2.3-4) in the Chapter 2. This subsystem block for phase one is shown in Fig. 4.3, where the DC output voltage V_d, utility supply voltage e_1, reference current i_{c1} and line current i_1 are input parameters, which are passed on to the subroutine **PCFF Controller** respectively.

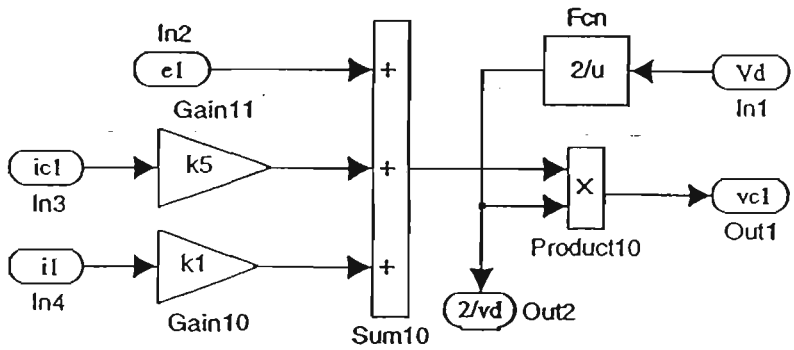

Fig. 4.3 The Configuration of the PCFF Controller Subroutine

In Fig. 4.3, i_{c1}, scaled by K_5 (using **Gain** block, Gain11), i_1, scaled by K_1 (using **Gain** block, Gain10) and e_1 are summed using **Sum** block, Sum10. V_d is inverted by the **Fcn** block. The product of the two results in the modulation signal V_{c1}, which is one of the two outputs of the **PCFF Controller** block. The other output of the block is the inverted V_d, which is fed to **Phase Two** and **Phase Three** subroutine respectively to perform calculations of V_{c2} and V_{c3} similar to V_{c1}.

4.3.2 THE PWM MODULATOR SUBBLOCK

Details of the black block **PWM Modulator** of Fig. 4.2 is given in Fig. 4.4 below. The PWM modulator subroutine is simulated based on the regular sampled PWM. One input to the modulator block is the modulation signal V_{c1}, which is fed to a sample and hold block (using **Zero-Order Hold** block, Zero-Order Hold3) first to produce a staircase waveform of V_{c1}. The other input to the block is a triangle carrier waveform, which is compared with the discretized V_{c1} via the summer, **Sum11** block. The output of the summer is processed by the **Sign** block, if it is positive, the **Sign** block generates a positive unit signal, otherwise, a zero signal is generated, in this way the original switching pattern is synthesized.

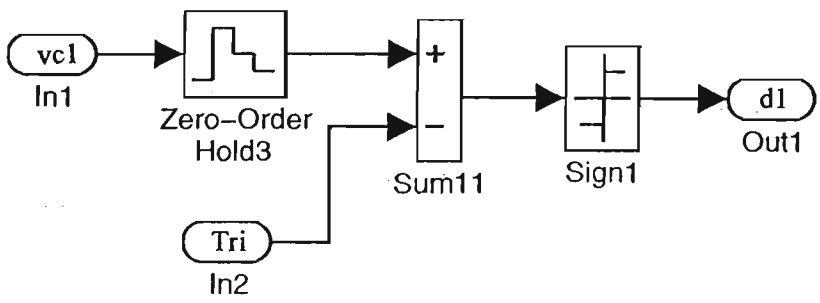

Fig. 4.4 The Configuration of the PWM Modulator Subroutine

4.3.3 THE CROSSOVER DELAY SUBBLOCK

The original PWM switching pattern assumes that the switching device is ideal, and that it changes instantaneously from on-state to off-state or vice versa. The crossover delay is introduced to take into account of the fact that in practice there is always a turn-on and turn-off delay, which results in shoot-through of upper and lower devices of the same phase leg for the voltage source type converter. Introduction of the crossover delay ensures no shoot-through in any leg of converter.

In Fig. 4.5, simulation structure of the crossover delay block is given. It involves two **Transport Delay** blocks, six **Logical Operator** blocks, one **Constant** block and two **Sum** blocks. The function of each block can be best explained by waveforms as shown in Fig.4.6, where waveform (**Error! Not a valid embedded object.Error! Not a valid embedded object.**) presents an ideal PWM switching signal without any crossover delay which is the primary input to the subblock.

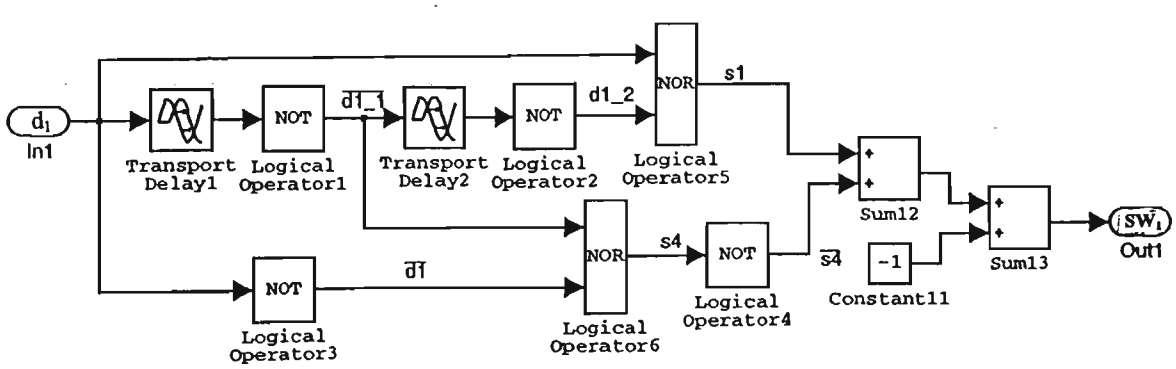

Fig. 4.5 The Simulation Structure of Crossover Delay Subroutine

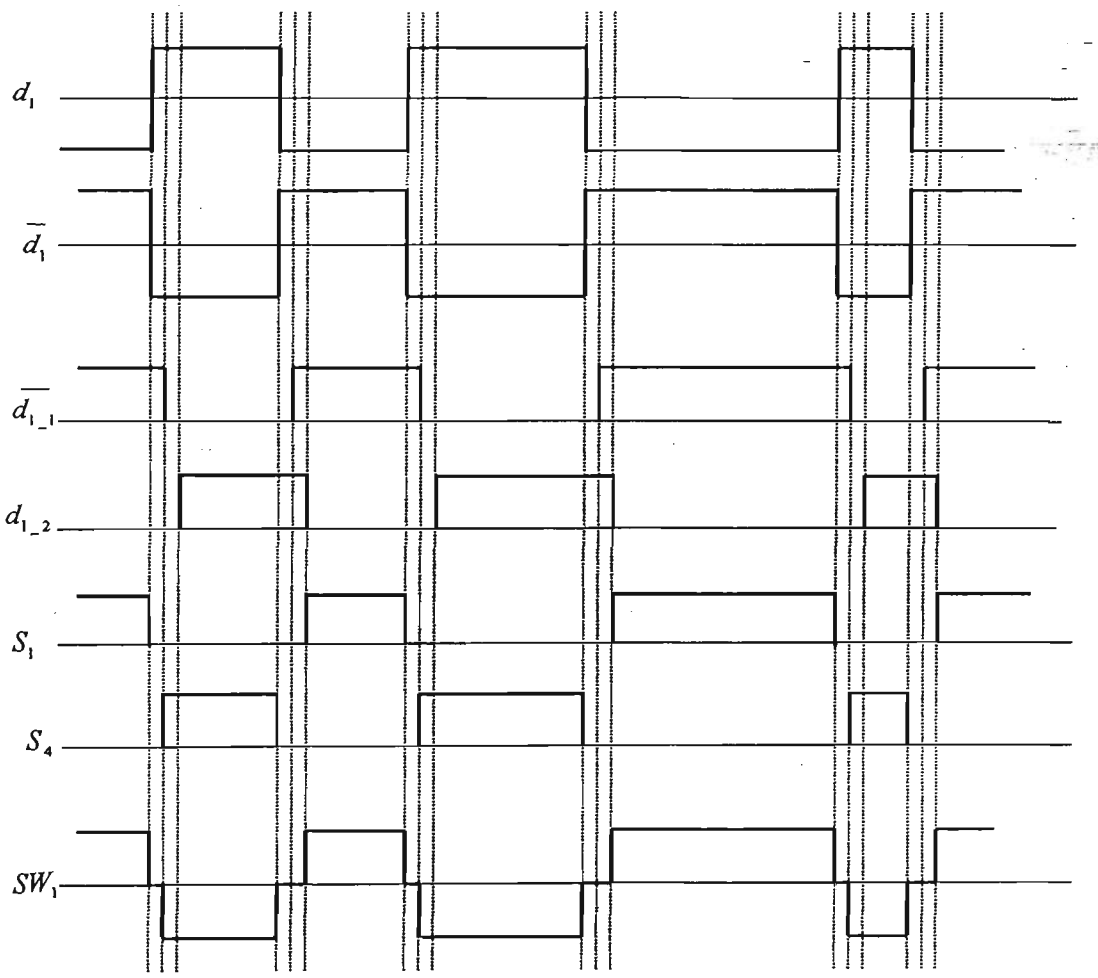

Fig. 4.6 The Simulation Results of Gating Signals.

In Fig. 4.5, the **Logical Operator 3** block is used to invert PWM waveform as shown in Fig. 4.5 ($\overline{d_1}$). The **Transport Delay 1, 2** blocks and **Logical Operator 1, 2** blocks are used to produce delayed and inverted PWM waveform shown in Fig. 4.6 as $\overline{d_{1\_1}}$, and d_{1_2} respectively, where the subscripts _1 indicates one step delay, while _2 indicates two-step delay, one step represents the time duration between two vertically dotted lines of Fig. 4.6.

The **Logical Operator 5, 6** blocks perform logic nor operation with d_1 and d_{1_2}, and with $\overline{d_1}$ and $\overline{d_{1\_1}}$ to produce the upper and lower switching patterns depicted in Fig. 4.6 as S_1, S_4 respectively. The **Constant11** block and two **Sum** blocks, Sum12, Sum13 are used to generate the real switching signal as shown in Fig. 4.6 (SW_1), which, if scaled by $K_3 * V_d$, is the same waveform as that of the converter's phase voltage.

4.3.4 The H_∞ Controller Subblock

The simulation configuration of the H_∞ **Controller** block is given in Fig. 4.7, which is based on the mathematical expression of equation (3.3-17) of Chapter 3. The DC voltage error signal, $V_{d-ref} - V_d$ is fed into the **Transfer Fcn10** block, which is the transfer function of the H_∞ voltage regulator. The output of the block is scaled by the coefficient k6 of the **Gain** block (using Gain12) as shown in Fig. 4.7.

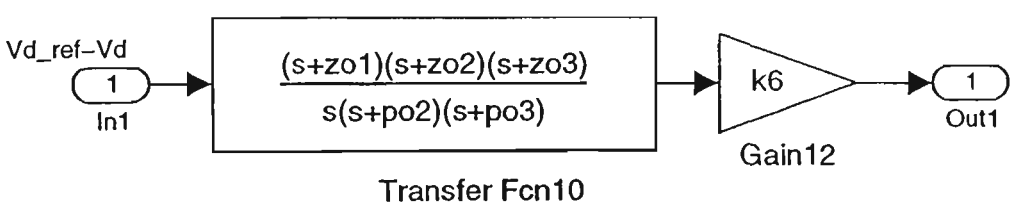

Fig. 4.7 The Configuration of the H_∞ Controller Subroutine

4.3.5 The Phase Lead Subblock

The black block **Phase Lead** of Fig. 4.2 is detailed in Fig. 4.8. Its function is to compensate for the time delay of PCFF controller. As can be seen from Fig. 4.8, a **Gain** block and a **Transfer Fcn** block are used to produce a phase lead signal. The calculation of k7, zo4 and po4 is dependent on the switching frequency f_{sw}. In this study, $f_{sw} = 1250Hz$, which corresponds to a phase angle delay of 14^o for one switching cycle. Hence in the phase lead compensator, zo4=23.3 and po4=107.22 are selected to obtain the required phase angle compensation for the 50Hz power input ($\tan^{-1}\frac{314}{23.3} - \tan^{-1}\frac{314}{107.22} \approx 14^o$). To compensate for the attenuation due to the phase lead block, the gain is increased by a factor of k7=1.05.

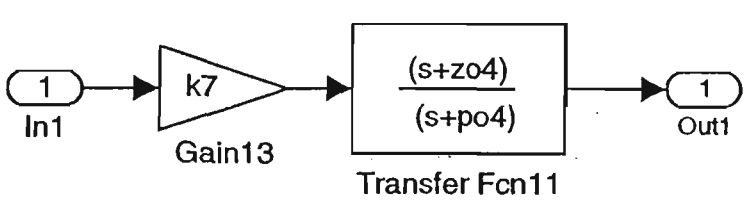

Fig. 4.8 The Configuration of Phase Lead Subroutine

4.3.6 THE STEP SIGNAL GENERATOR SUBBLOCK

The simulation configuration of the black block **Step Signal Generator** of Fig. 4.2 is shown in Fig.4.9. Its purpose is to model the step change in DC voltage reference for analyzing the transient behavior of the system.

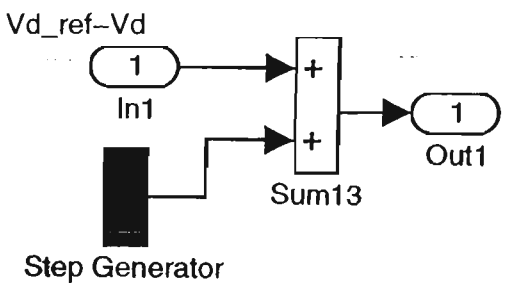

Fig. 4.9 The Configuration of the Step Signal Generator Subroutine

As can be seen in Fig. 4.9 there are simply a **Step Generator** block and a **Sum** block. The **Step Generator** block defines a step change at an instant t_o, the resultant output of the block is $V_{d\_ref} - V_d$. The signal is used to simulate the transient response of the system to a step change in V_{d_ref} at $t = t_o$.

4.4 STEP RESPONSE OF THE SYSTEM

The step response of the system is simulated with a utility supply voltage of 60 volts peak at 50Hz with a floating neutral point. The DC link voltage reference is set at 150 volts. A zero back EMF is set for a rectifying mode and a 290-volt back EMF is set for a regeneration mode in Fig. 4.2.

4.4.1 RECTIFYING OPERATION

When the converter is operated in its rectifying mode, the power flows from the AC side to the DC side. The step response of the DC link voltage V_d is given in Fig. 4.10. It takes less than 0.03 sec for the voltage to reach its steady state condition. Fig. 4.11 shows the DC output current of the converter, I_o, which flows from the AC side to the DC side in the rectifying mode. The line current and line-to-neutral voltage are given in Fig. 4.12. It can be seen that the line current is nearly sinusoidal with a unity power factor.

Fig. 4.13 and Fig. 4.14 show the sample and hold version of the modulating signal against the carrier waveform, their intersections determine the switching instants. The switching devices of the converter are turned on and off at a switching frequency of 1.25 kHz.

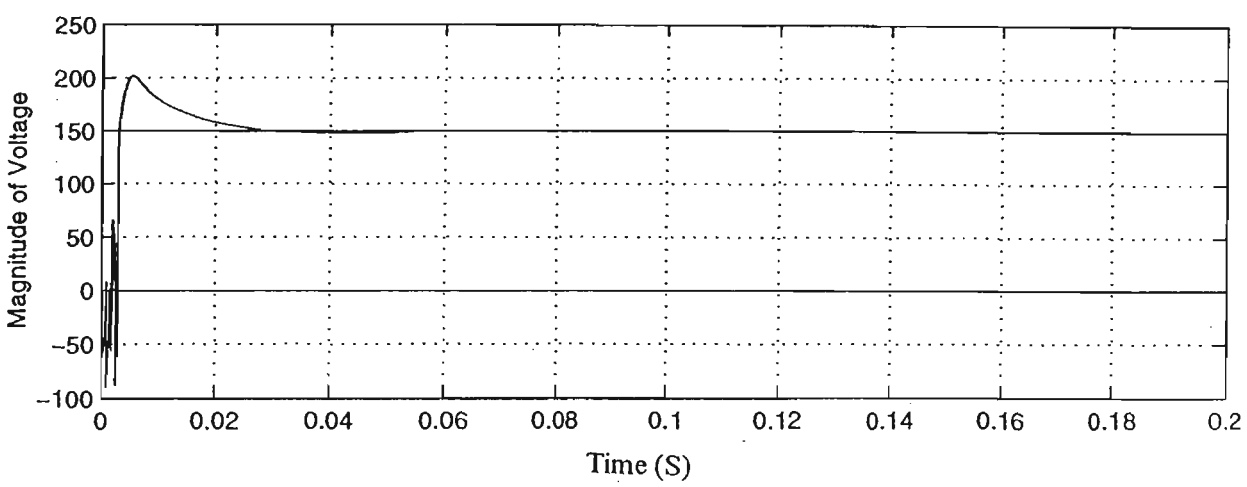

Fig. 4.10 Step Response of DC Output Voltage in the Rectifying mode

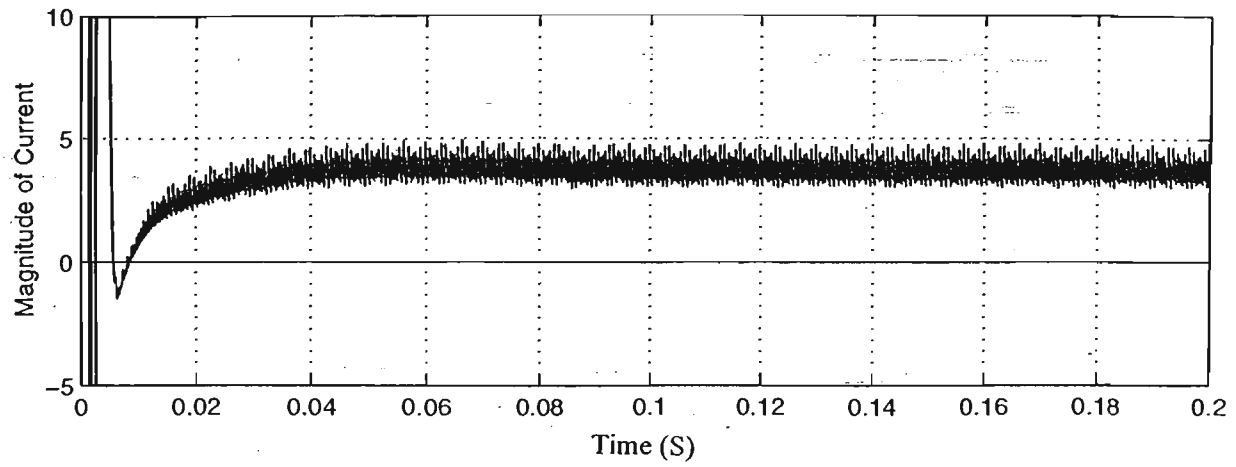

Fig. 4.11 Step Response of DC Output Current in the Rectifying Mode

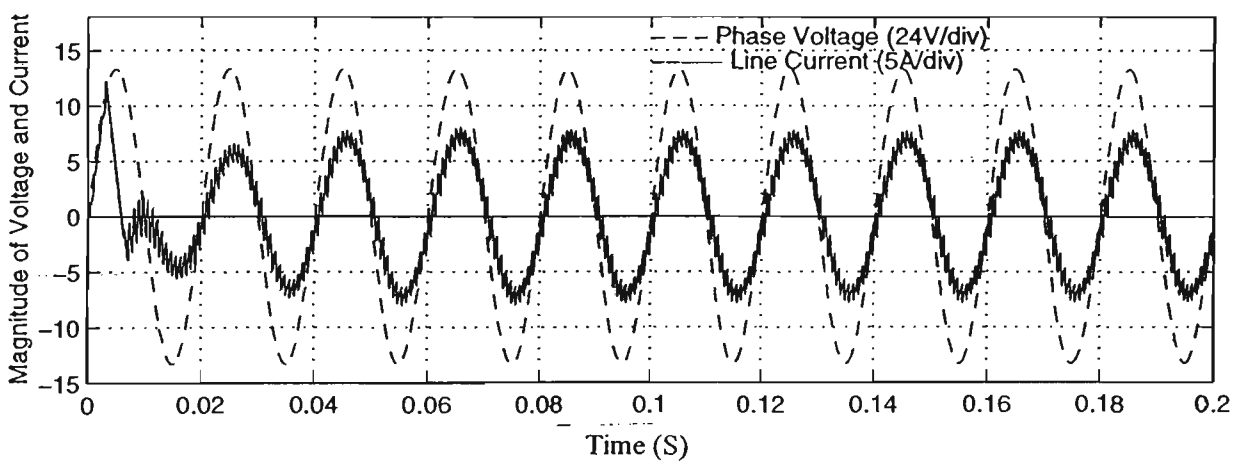

Fig. 4.12 Step Response of Line Current and Line-to-Neutral Voltage in the Rectifying Mode

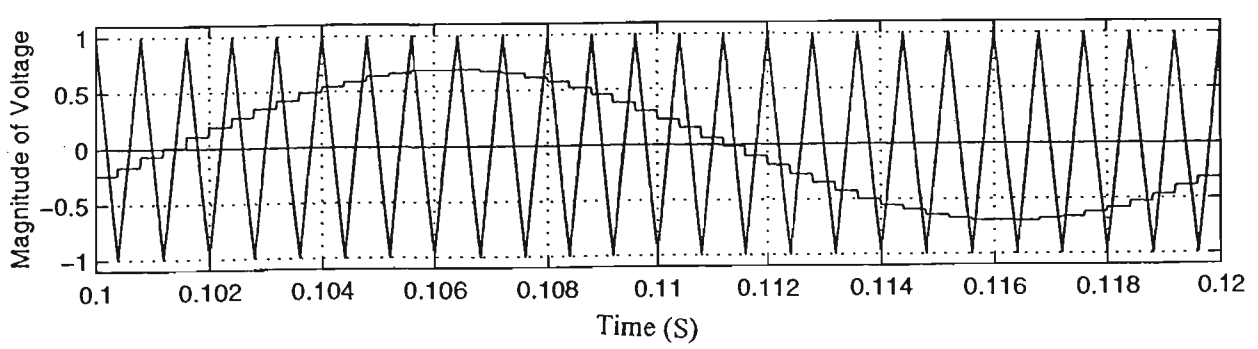

Fig. 4.13 Sample-Hold Modulating Waveform and Carrier Waveform in the Rectifying Mode

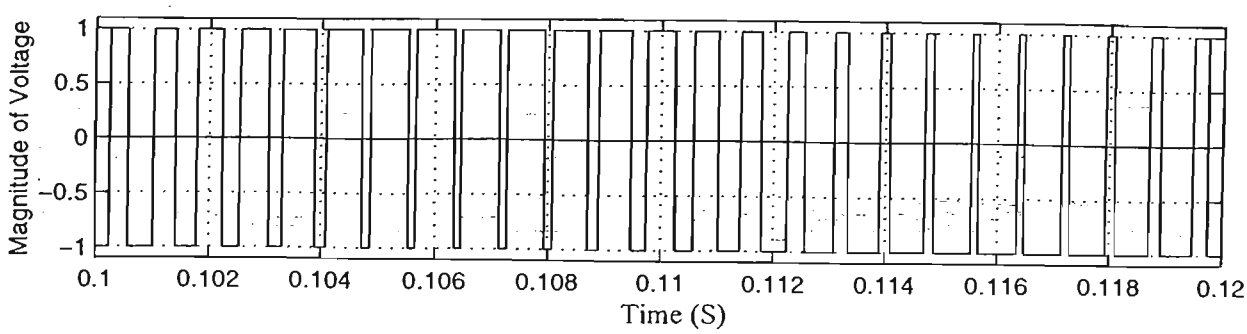

Fig. 4.14 Steady-State Pulse Width Modulated Waveform in the Rectifying Mode

In the steady-state, the system performance is satisfactory with the DC voltage maintained constant, line current is nearly sinusoidal and unity power is obtained. The line current contains harmonics of switching frequency and can be easy filtered.

4.4.2 REGENERATION OPERATION

When the converter is operated in its regenerating mode, it becomes a power inverter, in which the power flows from the DC side to the AC side. An equivalent DC voltage of 290 volts is connected in series with the load resistor as shown Fig. 4.1. The unity power factor under the regeneration condition becomes a phase shift of 180^0 between the line current and the phase voltage. This is verified by the simulation results show in Fig. 4.17.

Fig. 4.15 and Fig. 4.16 show waveforms of DC voltage and current of the converter respectively. It can be seen that the DC output voltage is constant when it reaches the steady state condition and the direction of DC output current is from the DC side to the AC side.

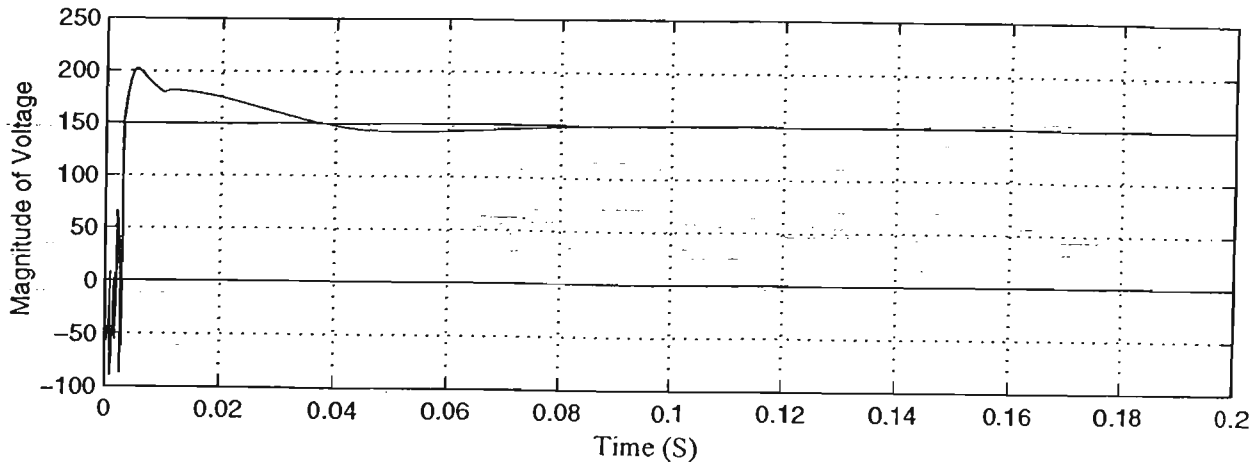

Fig. 4.15 Step Response of DC Output Voltage in the Regenerating Mode

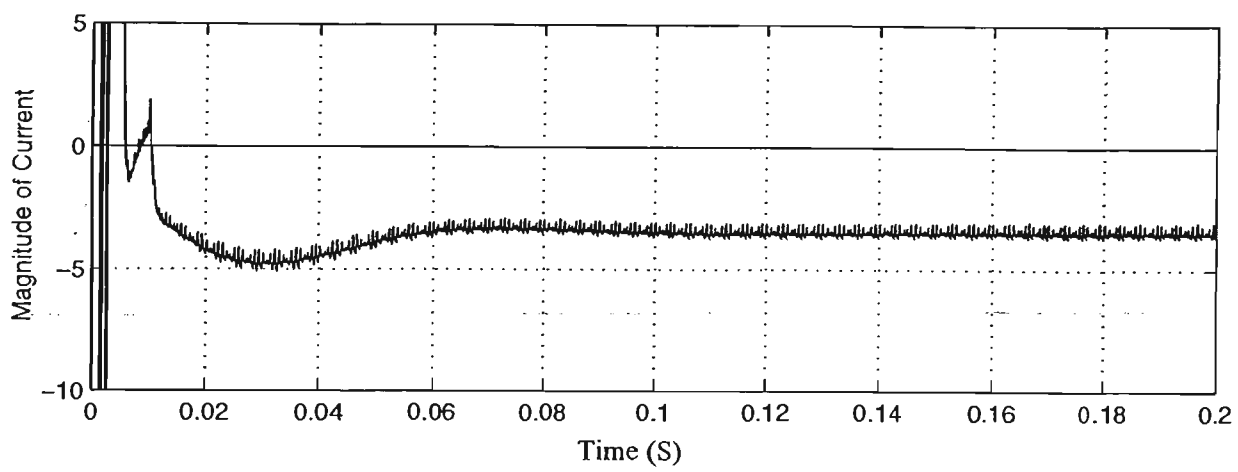

Fig. 4.16 Step Response of DC Output Current in the Regenerating Mode

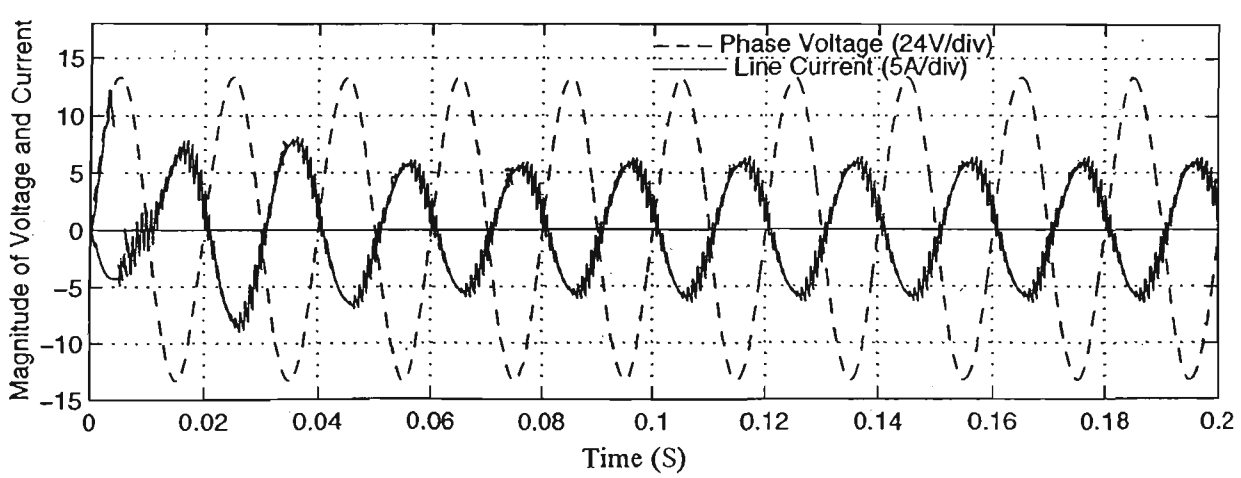

Fig. 4.17 Step Response of Line Current and Line-to-Neutral Voltage in the Regenerating Mode

4.5 DYNAMIC PERFORMANCE

The dynamic performance of the entire closed-loop system is simulated for two cases:

1. Step change to the DC voltage reference as described in Section 4.3.6,
2. Step change to the back EMF voltage from zero to 290 volts forcing the converter to go from rectifying to regenerating.

The two cases represent variations in converter's operating point and the large load disturbances. It is expected that under any type of disturbances, the DC output voltage V_d should be stable and be as close to its reference value as quickly as possible.

4.5.1 TRANSIENT RESPONSE DUE TO A STEP CHANGE IN THE DC VOLTAGE REFERENCE

The step response of the system is given in Fig. 4.18 through to 4.20 whereby the converter is in steady-state operation when a +30 volts step change (20%) is applied to the DC voltage reference $V_{d\text{-}ref}$ at t = 0.2 sec. Fig. 4.18 and Fig. 4.19 show responses of DC output voltage and current of the converter respectively. Response on the AC side of the converter is given in Fig.4.20 for the line current and phase voltage. It can be seen that under the proposed H_∞ voltage regulator, the DC link voltage increases to its new final value within 0.03 sec. The overshoot is less than 15%. The line current resumes unity power factor in one cycle of line frequency. This indicates that the closed-loop system is stability robustness and has performance robustness as specified at the design stage.

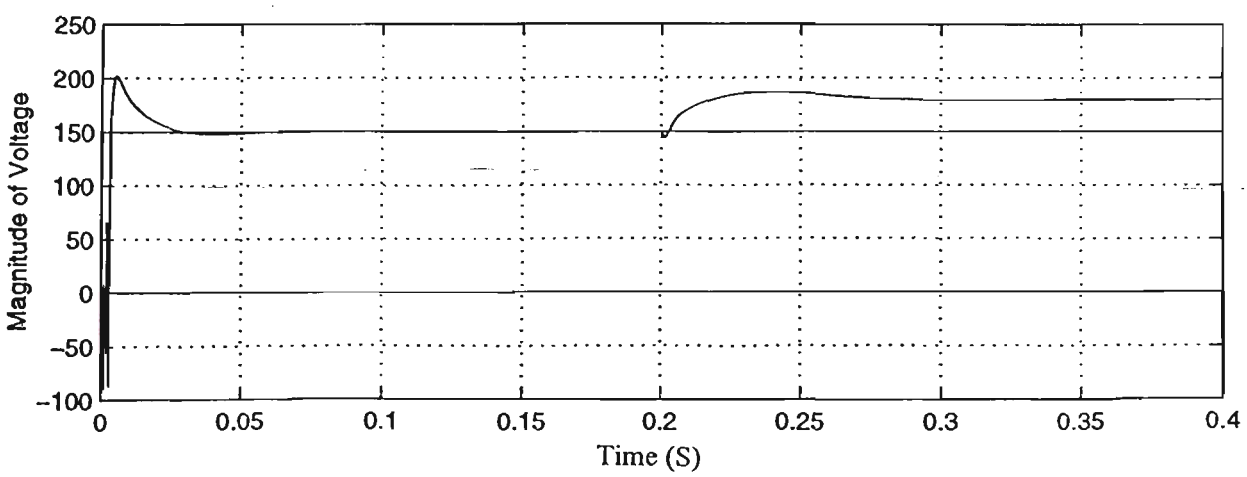

Fig. 4.18 Transient Performance of DC Output Voltage for an Input Change of 20% in $V_{d\text{-}ref}$

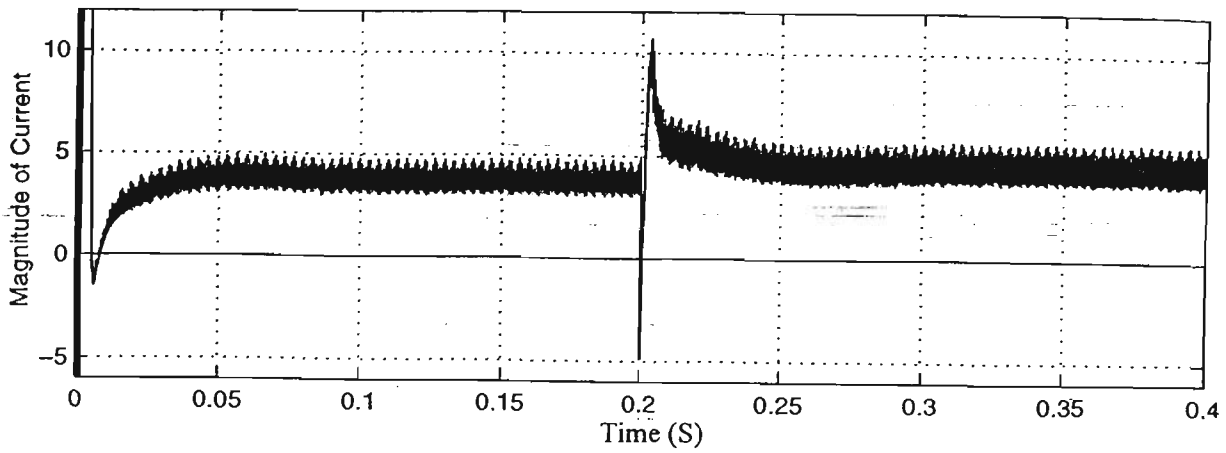

Fig. 4.19 Transient Performance of DC Output Current in the Input Change

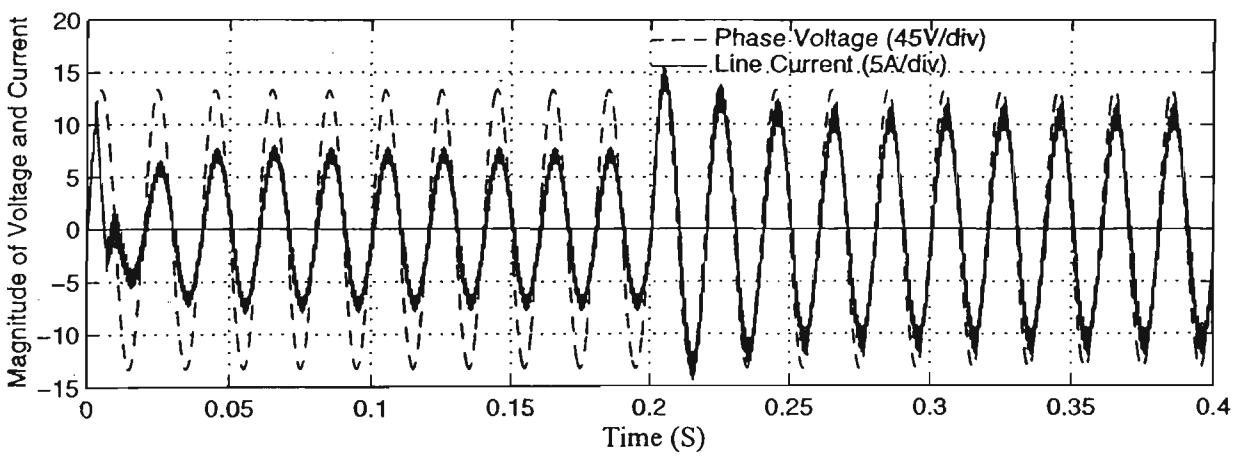

Fig. 4.20 Transient Performance of Line Current and Phase Voltage in Input Change

4.5.2 TRANSIENT FROM THE RECTIFYING TO THE REGENERATION

When the system is in its steady-state rectifying mode, its load back EMF is suddenly changed from zero volt to a 290 volts bus at $t = 0.2$ sec. Fig. 4.21 and 4.22 show the dynamic responses of the DC voltage and DC current respectively. A 15% overshoot of the DC output voltage V_d can be observed during the transient, and the DC current changes its direction instantaneously to the regeneration mode as shown in Fig. 4.22.

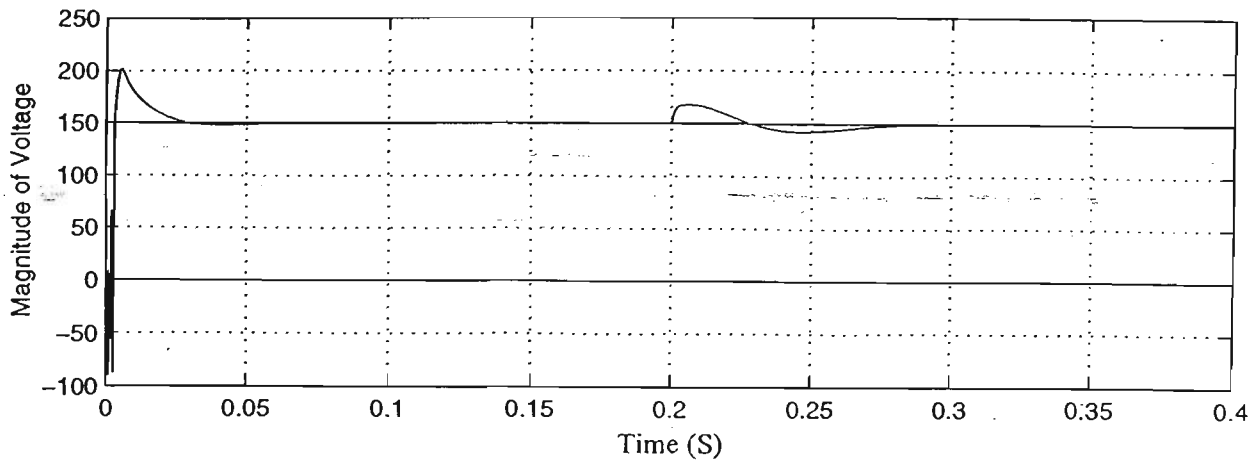

Fig. 4.21 Transient Performance of DC Output Voltage in the Load Change

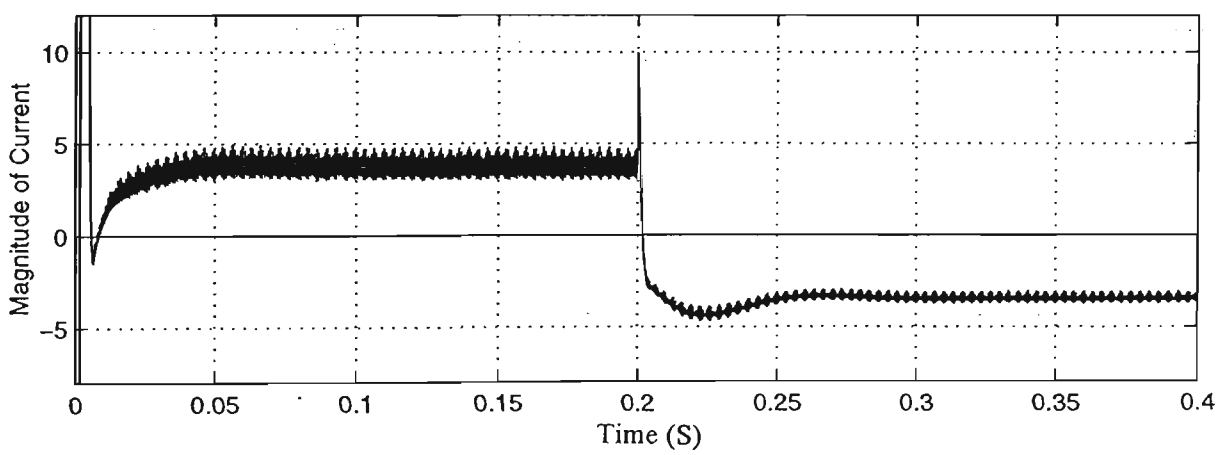

Fig. 4.22 Transient Performance of DC Output Current in the Load Change

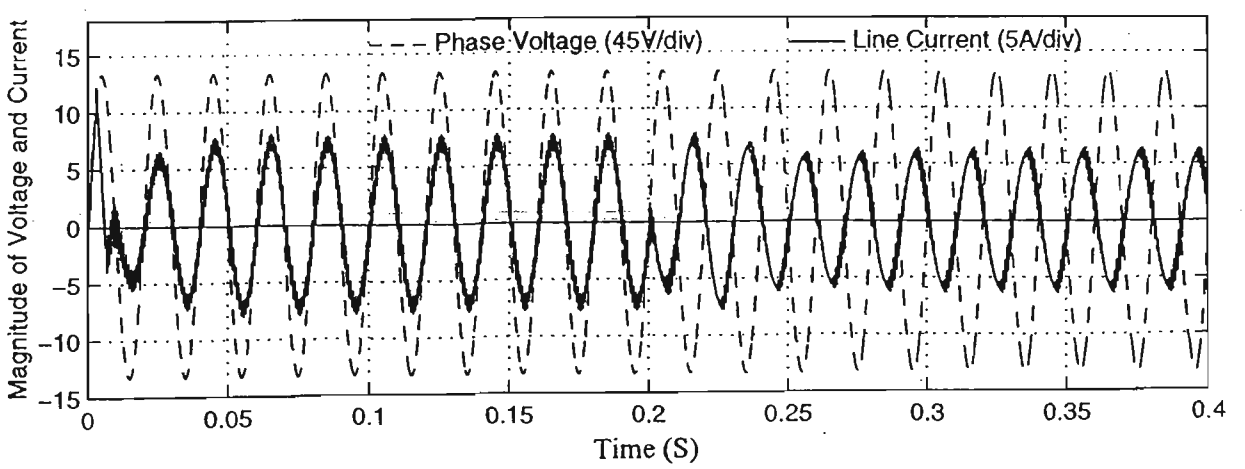

Fig. 4.23 Transient Performance of Line Current and Phase Voltage in the Load Change

Fig. 4.23 illustrates the transient response of the AC voltage and current to the disturbance. It can be seen that the line current is able to follow its reference to complete 180^{o} phase shift with respect to the phase voltage within half cycle of the line frequency (50 Hz).

In Fig. 4.21 it shows that during the transient the DC link voltage reaches its fianl value within 0.07 sec, which corresponds to a system bandwidth of approximately 90 rad/sec ($f = 90/2\pi$, $t=1/f$). Compare this with the design specification of 125 rad/sec, for the H_{∞} voltage regulator, both the performance robustness and stability robustness are achieved.

4.6 SUMMARY

The simulation of the three-phase predictive pulse width modulated AC/DC converter with an H_{∞} voltage regulator is performed to investigate the system responses to significant load disturbances. The simulation results presented in this Chapter are satisfactory, particularly the converter is able to transit from the rectifying to the regeneration mode in half a cycle of the line frequency. The overshoot of the DC link voltage is below 15%. The designed H_{∞} voltage regulator incorporated with the PCFF current control is able to stand up to significant disturbances, which result in significant parameter variation of the plant transfer function. Both stability robustness and performance robustness are obtained in the simulation.

Chapter 5

DEVELOPMENT OF EXPERIMENTAL SYSTEM

5.1 INTRODUCTION

The experimental system has been developed and commissioned at Victoria University to verify the performance of the computer controlled three-phase PWM 10 kVA voltage source IGBT power converter. The converter and the PWM generator board were manufactured at the Monash University, the software of the controller is developed by the author at Victoria University. In the development of the software, a lot of effort has been made to familiarize myself with the circuit details of the PWM board in order to interface the board with the PC. The experimental system consists of the following components:

1. A 10 kVA IGBT voltage source power converter as a plant to be controlled;
2. A PC-486 computer as a real time controller to calculate switching intervals for a given modulation index and frequency;
3. A pulse width modulation PCB board to output switching signals to the drive circuit of each IGBT device;
4. An RTI-815 Analogue to Digital Data conversion card;
5. Circuits to measure AC instantaneous and DC values of voltages and currents.

The PWM generator board generates PWM signals to the switching devices of the voltage source converter and is described in more detail in the following section. The visual display unit and the keyboard serve as the user interface, to change the set point for example.

The analog-to-digital converter is an RTI-815 multifunction card with 16 channels of analog signal-ended inputs, or 8 channels of differential inputs for measuring all system signals.

The design, development and testing of each component of the experimental system have been carried out in this study and are described in what follows.

5.2 VOLTAGE SOURCE CONVERTER

The converter is a three-phase voltage source bridge as shown in Fig. 5.1. It converts the utility AC power supplies to a DC voltage using a pulse width modulation (PWM) switching strategy. The power rating of the converter is 10 kVA. The insulated gate bipolar transistors (IGBT's) are used as the switching devices because they are recognised as the most efficient switching device. The IGBT has a simple gate drive requirement, relatively fast switching and good over-load capability [14, 38].

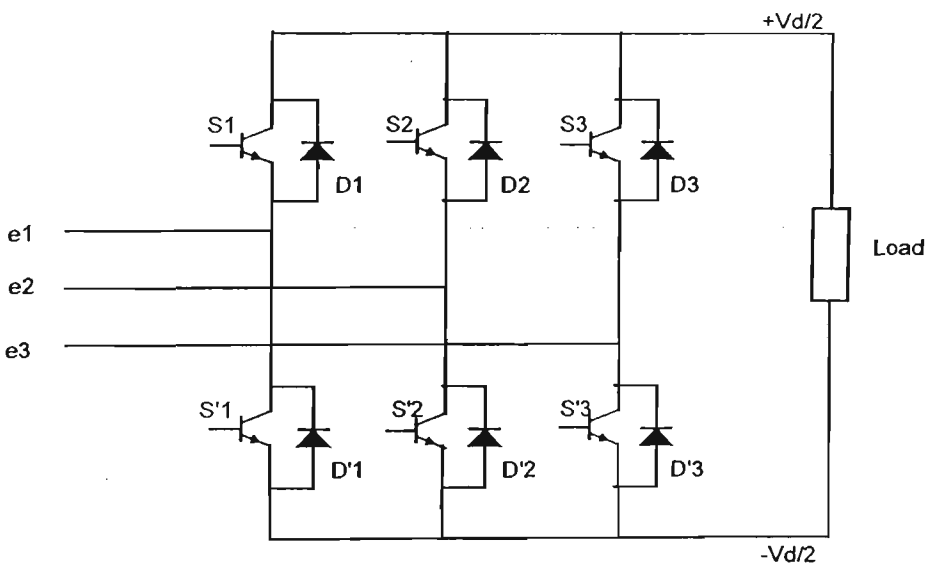

Fig. 5.1 Circuit Diagram of the Three Phase Voltage Source Converter

5.2.1 THE OPERATION OF AC TO DC CONVERTERS

In the voltage source power converter topology such as that of a full-bridge converter shown in Fig. 5.1 where diodes are connected in antiparallel with the IGBT switches, a distinction must be made between the on-state versus the conducting-state of a switch. Because of the diodes in antiparallel with the IGBT switches, when an IGBT switch is turned on, it may or may not conduct a current, depending on the direction of the current. If the IGBT switch conducts a current, then it is in a conducting state [1-3].

Since the three phase legs of a voltage source converter are symmetric, only one phase is considered here. Fig. 5.2 shows one phase leg of a converter, with the positive direction of line current assumed to be the direction in which line current flows into converter, as shown in Fig. 5.2(a). The negative direction of line current is the reverse case, as shown in Fig. 5.2(b).

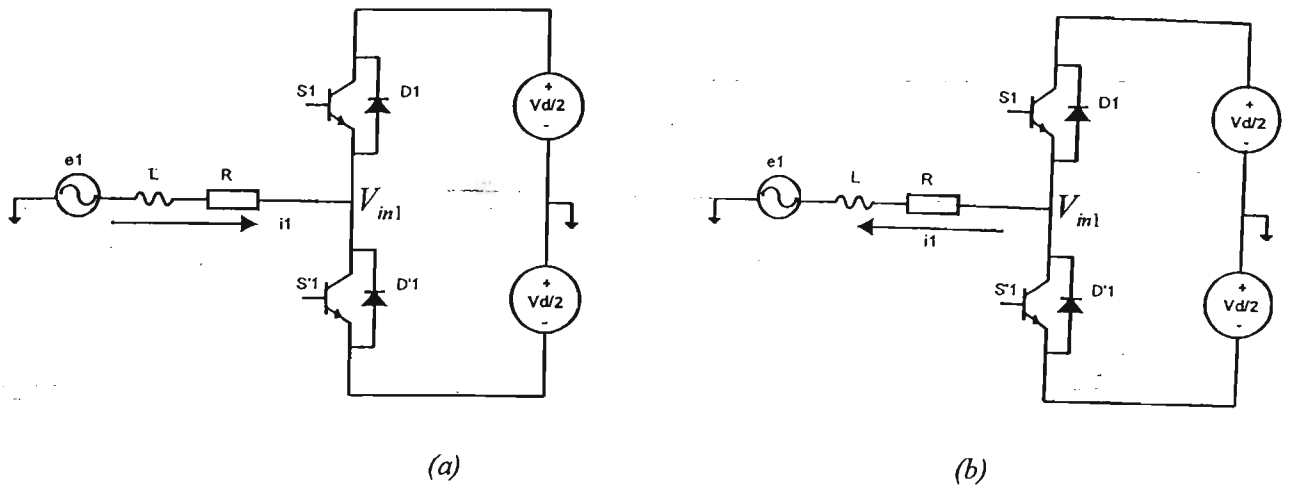

Fig. 5.2 Three Phase Leg Voltage Source Converter (with One Phase shown Only)
(a) Line Current Flows in Positive Direction (b) Line Current Flows in Negative Direction

In case (a), when the upper IGBT switch S_1 is switched off with diode D_1 conducting, the phase leg voltage V_{in1} will not switch to $-\frac{V_d}{2}$ until the lower IGBT switch S_1' is switched on, which will occur a delay period after S_1 is switched off. However, when the low IGBT switch S_1' is switched off, the phase leg voltage V_{in1} will switch to $\frac{V_d}{2}$ immediately irrespective of whether the upper IGBT switch S_1 is on or off. In this case, the line current i_1 flows through the freewheeling diode D_1, which is irrelevant to the switching status of IGBT switch S_1.

In case (b), when the lower IGBT switch S_1' is switched off with D_1' conducting, the phase leg voltage V_{in1} will not switch to $\frac{V_d}{2}$ until the upper IGBT switch S_1 is switched on, which will occur a delay period after S_1' is switched off. However, when the upper IGBT switch S_1 is switched off, the phase leg voltage V_{in1} will switch to $-\frac{V_d}{2}$ immediately irrespective of whether the lower IGBT switch S_1' is on or off. In this case, the line current i_1 flows through the freewheeling diode D_1', which is irrelevant to the switching status of IGBT switch S_1'.

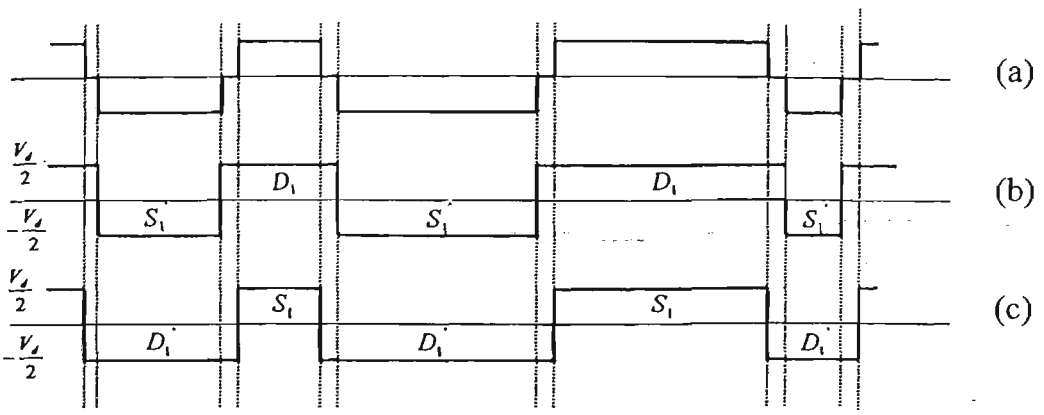

Fig. 5.3 The Waveforms of Driving Signal and Phase Leg Voltage

(a) Switching Pattern with Crossover Delay

(b) Phase Leg Voltage Waveform with Line Current in Positive Direction

(c) Phase Leg Voltage Waveform with Line Current in Negative Direction

The waveforms of the driving signals and phase leg voltage in these cases are shown in Fig. 5.3. As can be seen from Fig. 5.3, waveform (a) shows a ideal switching signal with crossover delay, and waveform (b) and (c) depict the waveform of the phase leg voltage in both cases where line current flows in either positive or negative direction.

5.2.2 GATE DRIVER CIRCUIT

The basic function of the gate driver is to interface, and provide electrical isolation between the IGBT devices and the microprocessor controller, and protect the devices from over-current. The selected driver has the merits of simple construction, fast response and large drive current. The design of the gate driver is based on the previous work [38]. There are six identical driving circuits in the system, one for each IGBT switch. The complete detailed circuit of the gate driver is shown in Appendix A. Fig. 5.4 shows that the gate driver has five main parts, which are input/output opto-couplers, memory logic, gate buffer, overload detector and power supply.

The opto-couplers provide electrical isolation between the controller and IGBT devices. The memory logic is a R-S flip-flop, which can be set to turn on the device and reset to turn off the device. The gate buffer provides high current charging and discharging of the device gate capacitance to give fast switching operation of the IGBT. The power supply provides two voltage levels to the driver circuit, a 5V level for the opto-couplers and the memory logic, and a 15V level for the gate buffer and overload detector.

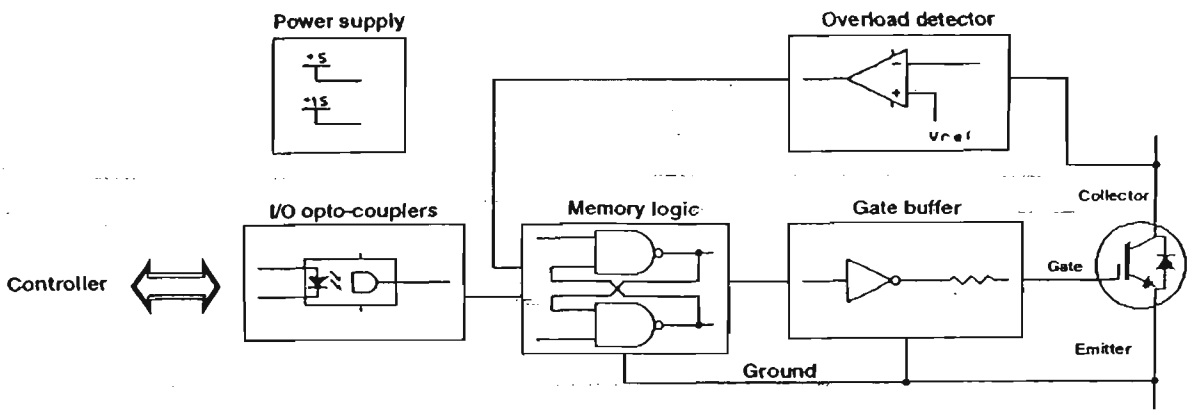

Fig. 5.4 Block Diagram of IGBT Gate Driver

The overload detector monitors for over-current and gives a fault signal in the event of an over-current. This fault signal blocks the gate signal by resetting the R-S flip-flop, meanwhile blocking the output of the microcontroller. The method for detecting over-current is by sensing the saturation voltage across the device which is the collector to emitter voltage as shown in Fig. 5.5. When the saturation voltage is greater than a certain threshold voltage, an overcurrent is detected. The low-pass filter is used to reduce the switching transient effect which may affect the operation of the detector. Therefore the IGBT devices are protected.

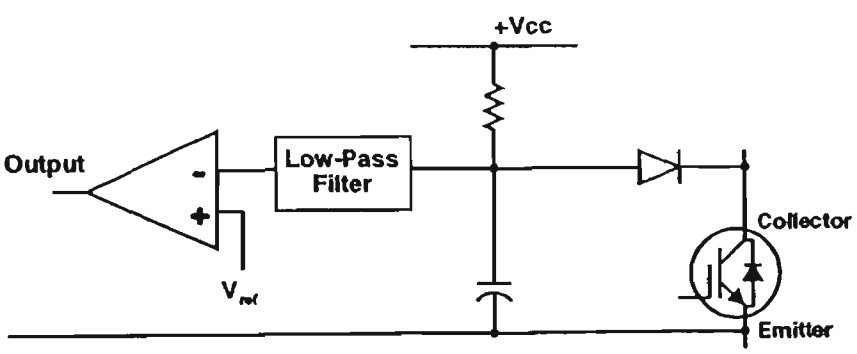

Fig. 5.5 Overload Detection for IGBT Devices

5.3 THE SINGLE CHIP PC-486 CONTROLLER

The function of the controller is to control the power converter via the PWM generator board. A single chip INTEL PC-486 computer is used as the controller with a monitor and key board as the user interface. The block diagram of the controlled system is shown in Fig. 5.6 [36].

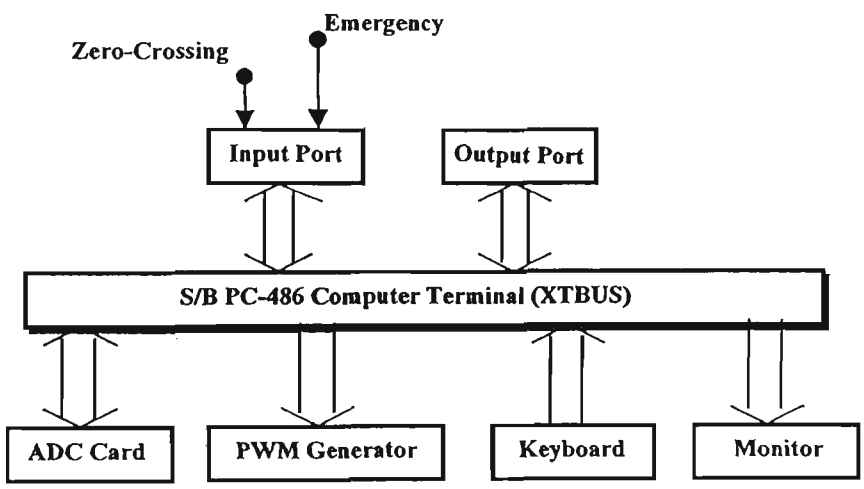

Fig. 5.6 PC-486 Controller

The INTEL PC-486 is a 32-bit processor running at a clock speed of 66MHz. The math co-processor is a 487 co-processor which computes all the floating point calculation for the main processor. The pin configuration of PC-486 terminal termed as XTBUS is shown in Fig. 5.7. The pins A_2 through A_9 are data bus D_0 through D_7 respectively which provide bi-directional communication between the CPU, memory, and I/O devices for instructions and data transfers. Pins A_{12} through A_{31} are address bus which provides the address to memory or denotes the I/O device number. IOR and IOW are read and write signals, which are used for memory and I/O read or write control. IRQ2-IRQ7 are interrupt pins. The interrupt request signals are generated from I/O devices and assigned priorities among the I/O devices. In this project, IRQ3 is used for synchronizing, IRQ4 is used for generating the sampling period and IRQ7 is for processing an emergency event. The interrupt requests are ordered in priority from IRQ3 through IRQ7 (IRQ3 highest). Each interrupt request input can be masked individually by the interrupt mask register. In the special mask mode, when a mask bit is set, it inhibits further interrupts at that level and enables interrupts from lower levels.

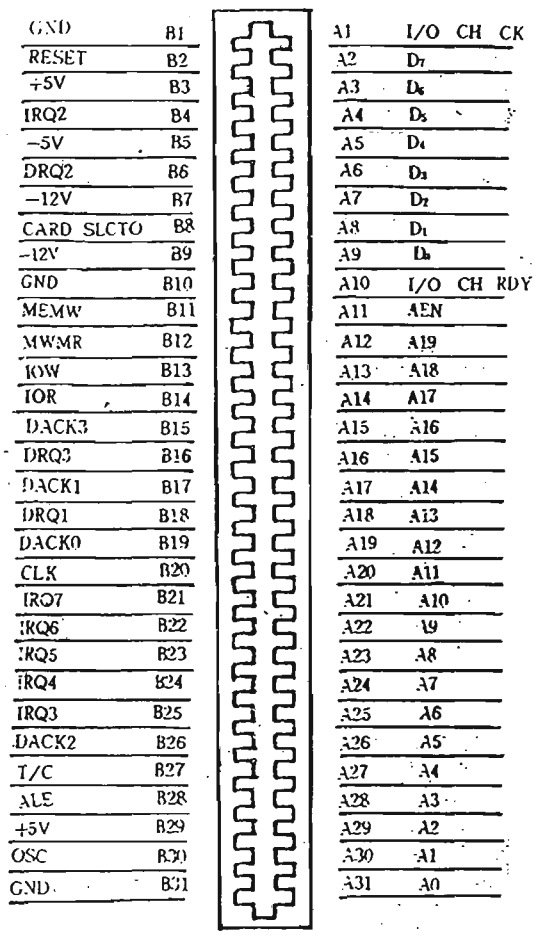

Fig. 5.7 Pin Configuration of PC-486 Terminal

In this design, the main function of the PC-486 controller is to calculate the switching intervals according to the modulation index, M and output frequency, ω_0 using space vector PWM algorithm, and synchronize the fundamental frequency of the PWM signal with the mains. In order to do these tasks, the zero-crossing interrupt signal (rising age triggered) produced from synchronizing unit requires the controller to enter the zero-crossing service routine. In the zero-crossing service routine, the controller compensates the delay that is caused by the low-pass filter in the synchronizing unit to synchronize the fundamental frequency of the PWM signal with the mains. Then, the controller returns from the zero-crossing interrupt routine and waits for the switching period interrupt request signal. When the switching period interrupt signal is received, the controller gets in the switching period service routine to calculate the turn-on and turn-off duration using space vector PWM algorithm, and the results are to download to the duration timers for the six switching devices. The frequency of switching period interrupt request signal is 2.5KHz.

The space vector modulation determines the duty cycle for each phase leg that is required to generate a sampled voltage reference vector by selecting at each sample time the nearest two of the six active space vector combinations for the three phase power converter [4]. For some of one carrier interval (ΔT) as shown in Fig.5.8, where m_1, m_3, and m_5 represent the fraction of each carrier interval ($\frac{\Delta T}{2}$) for which phase legs "1", "2" and "3" respectively are connected to the upper DC bus. The fractional period of each active space vector depends on the modulation index, and the remainder of the period is filled with zero space vectors. Referring again to Fig. 5.8, it can be seen how the modulation process produces two active voltage pulses for the line-to-line voltage within any one carrier interval. It is the placement of these active pulses within the carrier period which determines the current ripple component. If two active voltage pulses can be spaced equidistantly apart, the current ripple is reduced accordingly. V_n (n=1,2...6) is the active space vector.

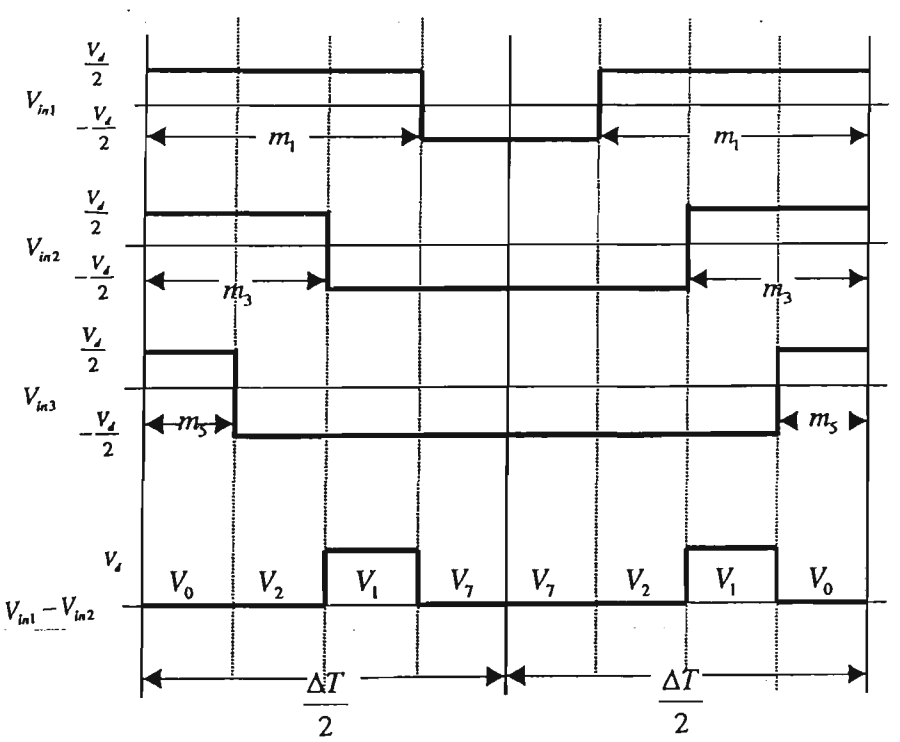

Fig. 5.8 Space Vector PWM Switching Patterns

For space vector PWM, the magnitude of the switching-on components are shown in Table 5.1.

Reference Vector	Active Space Vector	Switching-on Magnitude
$0^o -> 60^o$	$V_1 = \frac{\sqrt{3}M}{2}\cos(\omega_o t + \frac{\pi}{6})$ $V_2 = \frac{\sqrt{3}M}{2}\cos(\omega_o t + \frac{3\pi}{2})$	$m_1 = \frac{\Delta T}{4} + \frac{1}{2}(V_2 + V_1)$ $m_3 = \frac{\Delta T}{4} + \frac{1}{2}(V_2 - V_1)$ $m_5 = \frac{\Delta T}{4} - \frac{1}{2}(V_2 + V_1)$
$60^o -> 120^o$	$V_2 = \frac{\sqrt{3}M}{2}\cos(\omega_o t + \frac{11\pi}{6})$ $V_3 = \frac{\sqrt{3}M}{2}\cos(\omega_o t + \frac{7\pi}{2})$	$m_1 = \frac{\Delta T}{4} + \frac{1}{2}(V_2 - V_3)$ $m_3 = \frac{\Delta T}{4} + \frac{1}{2}(V_2 + V_3)$ $m_5 = \frac{\Delta T}{4} - \frac{1}{2}(V_2 + V_3)$
$120^o -> 180^o$	$V_3 = \frac{\sqrt{3}M}{2}\cos(\omega_o t + \frac{3\pi}{2})$ $V_4 = \frac{\sqrt{3}M}{2}\cos(\omega_o t + \frac{5\pi}{6})$	$m_1 = \frac{\Delta T}{4} - \frac{1}{2}(V_4 + V_3)$ $m_3 = \frac{\Delta T}{4} + \frac{1}{2}(V_4 + V_3)$ $m_5 = \frac{\Delta T}{4} + \frac{1}{2}(V_4 - V_3)$
$180^o -> 240^o$	$V_4 = \frac{\sqrt{3}M}{2}\cos(\omega_o t + \frac{7\pi}{6})$ $V_5 = \frac{\sqrt{3}M}{2}\cos(\omega_o t + \frac{\pi}{2})$	$m_1 = \frac{\Delta T}{4} - \frac{1}{2}(V_4 + V_5)$ $m_3 = \frac{\Delta T}{4} + \frac{1}{2}(V_4 - V_5)$ $m_5 = \frac{\Delta T}{4} + \frac{1}{2}(V_4 + V_5)$
$240^o -> 300^o$	$V_5 = \frac{\sqrt{3}M}{2}\cos(\omega_o t + \frac{5\pi}{6})$ $V_6 = \frac{\sqrt{3}M}{2}\cos(\omega_o t + \frac{\pi}{6})$	$m_1 = \frac{\Delta T}{4} + \frac{1}{2}(V_6 - V_5)$ $m_3 = \frac{\Delta T}{4} - \frac{1}{2}(V_5 + V_6)$ $m_5 = \frac{\Delta T}{4} + \frac{1}{2}(V_5 + V_6)$
$300^o -> 360^o$	$V_6 = \frac{\sqrt{3}M}{2}\cos(\omega_o t + \frac{\pi}{2})$ $V_1 = \frac{\sqrt{3}M}{2}\cos(\omega_o t + \frac{11\pi}{6})$	$m_1 = \frac{\Delta T}{4} + \frac{1}{2}(V_6 + V_1)$ $m_3 = \frac{\Delta T}{4} - \frac{1}{2}(V_6 + V_1)$ $m_5 = \frac{\Delta T}{4} + \frac{1}{2}(V_6 - V_1)$

Table 5.1 Space Vector PWM Algorithm

5.4 THE PWM GENERATOR BOARD

The board is designed to generate gating pulses to switching devices of the voltage source converter. The block diagram of the board is given in Fig. 5.9. It consists of four blocks which are control block, timer board, synchronising unit and crossover delay. The schematic diagram of the PWM generator is shown in Appendix A. The functions of each block are discussed in the following.

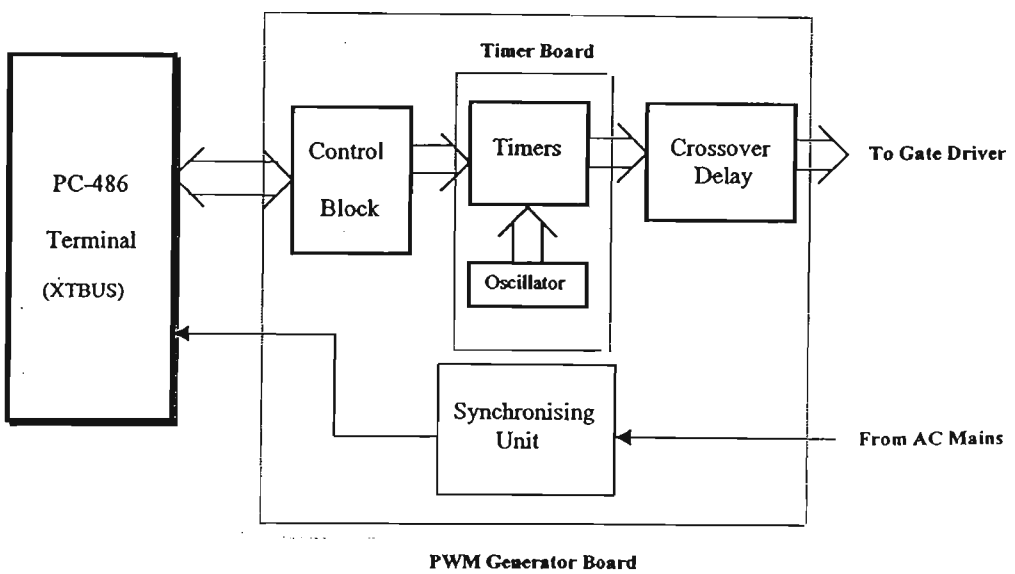

Fig. 5.9 Structure of PWM Generator Board

5.4.1 CONTROL BLOCK

The main function of the control block is to interface the PC 486 with the PWM board. That is when the PC is ready to download its calculated switching intervals to the PWM board, an 8-bit board address data is sent to the control block first. On receiving the address data, the control block compares it with a preset address (using 74LS682), if the address is confirmed, then a chip enable signal will be issued to the bi-directional bus transceiver, 74LS245, to allow for data flow between PC and the PWM board. The control block diagram is shown in Fig. 5.10

The 74LS245 device allows for two-way communications between data buses depending on the logic level at the direction control (DIR) input. When the direction control (DIR) connects the read line, if the read signal is logic low, the computer will read in data, otherwise, the computer is in writing operation. The enable-input (E) is used to either

enable or disable the device. If the device is disabled, the buses are effectively isolated and vice versa.

The 74LS244 is a buffer memory address register. The 4 address buses (A_0-A_3), read (RD) and write (WR) input signals from the PC are transmitted to timers. The 74LS682 is an 8-bit magnitude comparator. It is used to perform comparisons between two eight-bit binary or BCD words and provides P=Q output if the two inputs are equal. The Q input (Q_0-Q_6) is an address preset and is to be compared with the input address (A_4-A_9) via pins P_0-P_6. If Q equals P, the output P=Q sets a logic low signal, which is used to enable the chip 74LS245, i.e. allows for the communications between the PC and the PWM board.

The chip 74LS139 comprises two individual two-line-to-four-line decoders in a single package. Its active-low enable input is fed from the P=Q line of 74LS682. If P=Q is a low signal, the two-to-four line is decoded and timer 8254(0), timer 8254(1), input port or output port is selected. The outputs of 74LS139 are fed into the chip select (CS) of the timer 8254. At a low state of CS, the 8254 is to response to RD and WR signals. Otherwise RD and WR are ignored.

The P=Q signal also enables the chip 74LS245 to transmit or receive data. Referring to Fig. 5.10, there are three NAND gates for the selection of 74LS245's enable. The output of one NAND, B (=WR NAND RD), is always high. The output of the second NAND gate, A, depends on the P=Q signal. If the signal P=Q is low, then the output, A, must be high, resulting in a low state of the third NAND gate's output, C. This enables the 74LS245 to transmit or receive data.

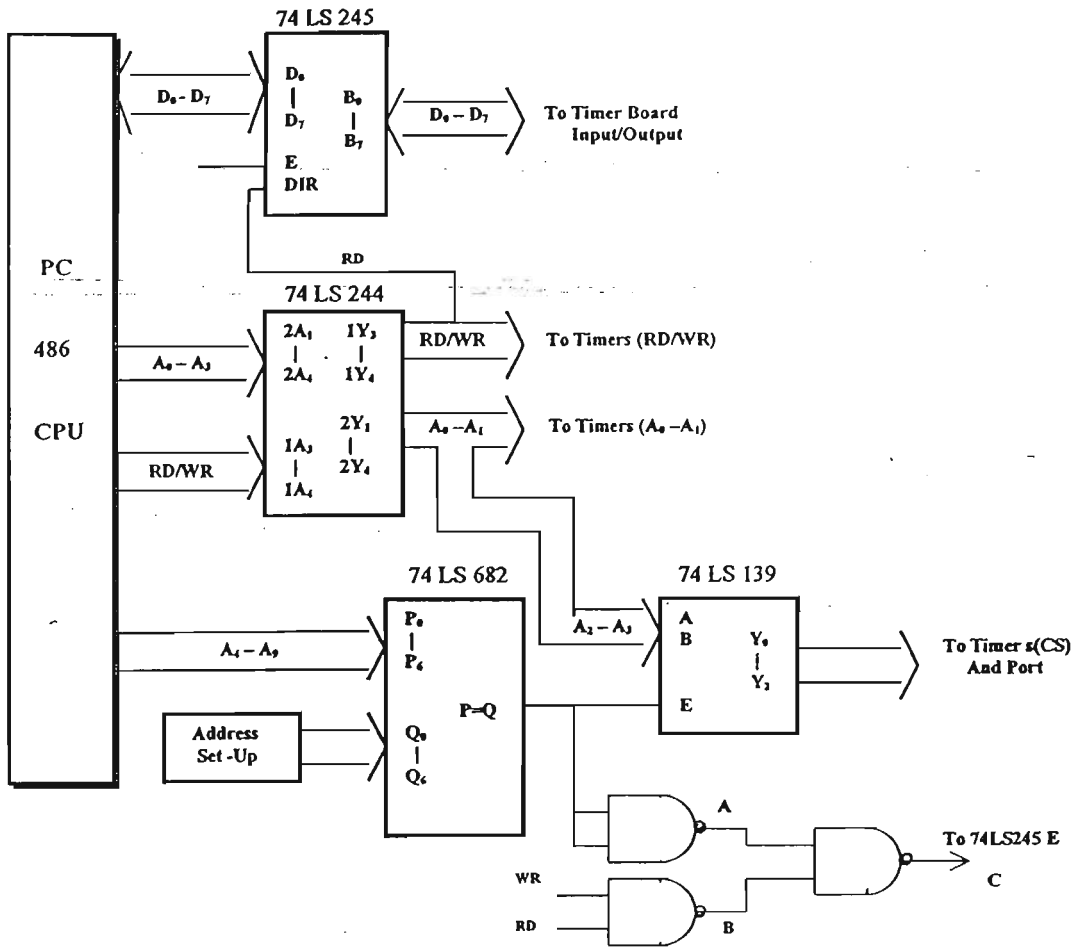

Fig. 5.10 Block Diagram of the Control Block

5.4.2 TIMER BOARD

Fig. 5.11 shows the block diagram of the timer board. There are four timers used to synthesize switching signals, three are pulse duration timers, one for each phase, and one is the sampling timer. The INTEL 8254 is a programmable timer that provides three independent 16-bit counters, each capable of handling clock input. The counter1 of 8254(1) is used as the sampling timer. The counter1, counter2 and counter3 of 8254(0) which are termed as duration timers, are responsible for the implementation of the switching intervals. The switching interval and status (ON or OFF) of each switching device are under software control. This allows greater flexibility in changing the PWM switching strategy.

In this study, the space vector PWM method with an asymmetrical switching is used. That is, the switching frequency is half of the sampling frequency, which is synchronized with the carrier frequency of the PWM method. At each half of the carrier interval, or the switching period, a sample is taken from the modulation waveform by the PC. To fulfill this task, an interrupt request signal is generated to the PC by the sampling timer at each half of the carrier interval, so that the software can perform an appropriate action by reloading the duration timers with new timing values. The sampling timer also initiates the timing of the other three duration timers.

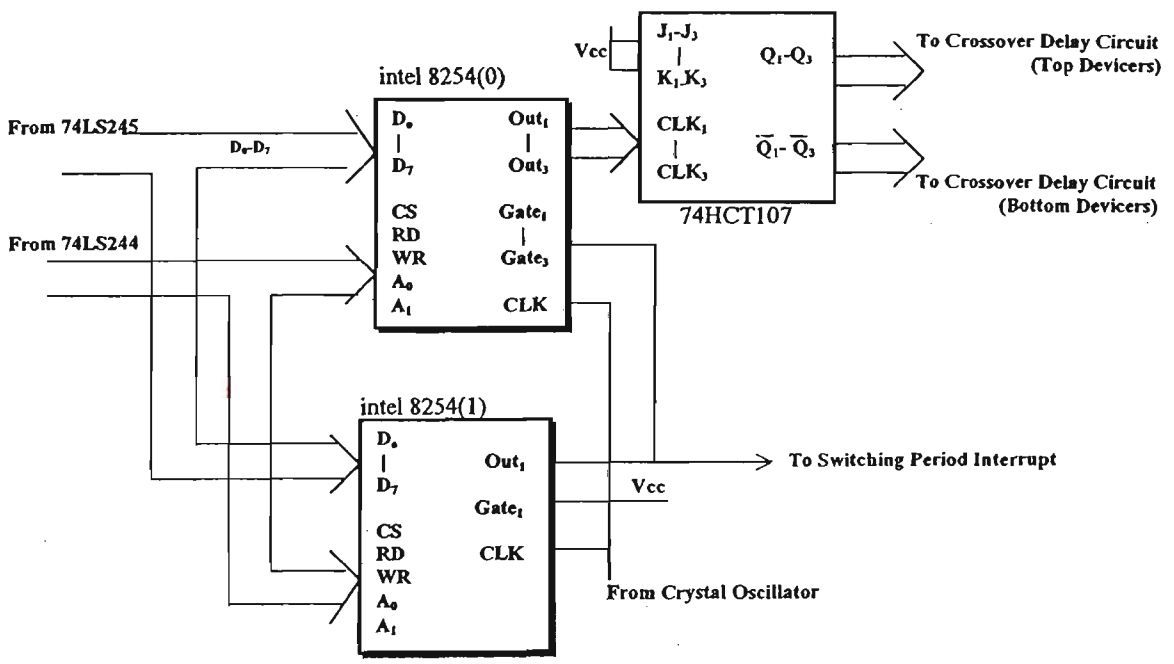

Fig. 5.11 Block Diagram of Timer board

The operation mode of the timers, the calculation of timing interval and chip select are all under software control. Each timer could be programmed with different operation modes independently. In this design, the sampling timer is programmed in mode 2 and the three duration timers are programmed in mode 5. The mode 2 functions as a divide-by-N counter and is typically used to generate a real time clock interrupt. The function of mode 5 is when the initial count has expired, the output on 8254 chip will go low for one clock pulse and then go high again.

The actual PWM firing signals are formed by three J-K flip-flops chip 74HCT107 of Fig. 5.11. The inputs of J and K are connected to a logic high, this means that the J-K flip-flop is in a toggle mode. When the duration timers time out, they toggle the J-K flip-flop, i.e. the switching status toggle accordingly. Three output Q are fed to the upper devices of the

the power converter, while the three outputs $\overline{Q}$ are fed to the lower devices. Fig.5.12 shows the duration timer output and two outputs of J-K flip-flop which are actual firing signals.

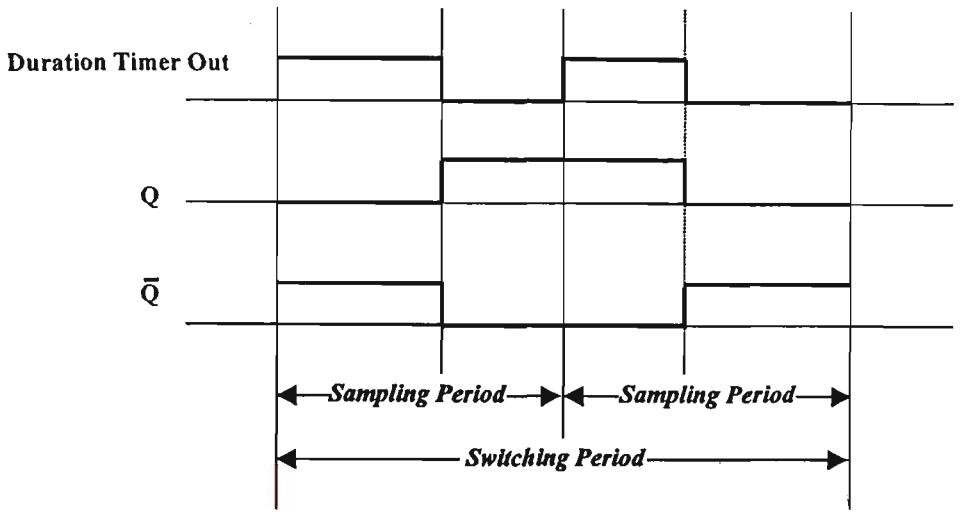

Fig.5.12 Waveforms of Timer Output and J-K Flip-Flop Outputs

In this design, the clock frequency of each timer is 2.5MHz (0.4μsec), which determines the timing precision of the timer. The clock frequency can be selected respectively according to the jump position of the crystal oscillator up to 10MHz. The sampling timer is programmed mode 2 in which the clock frequency 2.5MHz is divided by 1000 to generate a sampling frequency of 2.5KHz (400μsec) for the duration timers, 8254(0) and the switching period interrupt signal to PC. Fig.5.12 shows the duration timer output (out_1 of 8254(0)), and two outputs of the J-K flip-flop which are actual firing signals. In the software design, the PC loads on-duration to the duration timer in the sampling period, and then, off-duration to the duration timer in the next sampling period.

5.4.3 SYNCHRONIZING UNIT

The PWM switching of the converter needs to be synchronized with the mains in order for the power converter to operate properly. This is achieved using a synchronizing unit which detects the voltage zero-crossing (ZX) of the mains. Fig.5.13 shows the block diagram of the synchronising unit. An sampled phase voltage signal, say phase A from the mains is fed into the low pass filter, which removes most of the harmonics for the purpose of extracting only the fundamental 50Hz component. The phase shift caused by the filter is adjusted in software control. The comparator with hysteresis is then used to detect a ZX of the filtered waveform in each line cycle. The output of the comparator is thus a square

then used to generate an interrupt request for the PC to start its sampling process. In this way, the ZX signal provides an accurate start of the sampling timer.

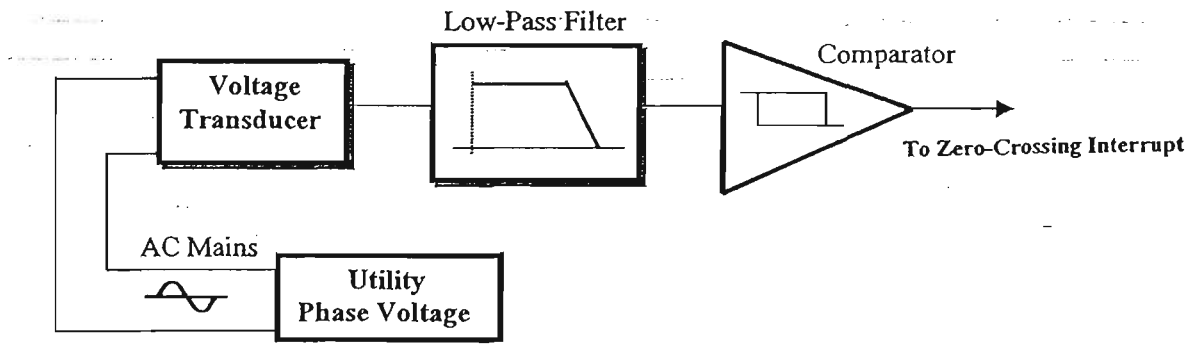

Fig. 5.13 Block Diagram of Synchronising Unit

5.4.4 CROSSOVER DELAY CIRCUIT

The hardware implementation of the crossover delay of 3.2 μsec is performed by this unit to ensure no shoot-through in any leg of the power converter. The block diagram and its operation principle is given in section 4.3.3.

5.5 SOFTWARE DEVELOPMENT OF CONTROL PWM BOARD

The implementation of the switching algorithm depends on the software development to control the PWM generator board. Details of this program development are given as follows:

1. To assign addresses to each unit, including three interrupt addresses (zero-crossing interrupt, switching period interrupt, emergent interrupt respectively); interrupt chip (8259) address; mask register address; addresses of the four timers and their control word registers; input/output address respectively.

2. The sine functions are stored as look-up tables and all other values are defined for the calculation of the pulse width duration.

3. Three interrupt vectors are defined. The old values of three interrupt vectors are read and stored, and new values of three interrupt vectors are set, which are pointers containing addresses of new interrupt functions.

4. The old content of mask register is stored, and the value that enables three interrupts is assigned to mask register. The input and output ports are turned on. The control word register of the sampling timer is written in mode 2, and control word registers of three duration timers are written in mode 5.

5. The zero-crossing interrupt request signal is waited. On receiving the zero-crossing interrupt, the program starts to compensate for the delay caused by the low-pass filter in a zero-crossing interrupt routine. Then, the program masks zero-crossing interrupt to wait for the low-level interrupt which is a switching period interrupt.

6. In the switching period interrupt routine, the turn-on and turn-off durations for the six switching devices are calculated according to the space vector PWM algorithm. The results are then downloaded to the three counters on the timer (8254). Before loading these duration timers, the values of switching intervals need to be bounded within the timing limits. If the timing duration is less than the lower limit, it is bounded to the lower limit. In this software design, the lower limit is set at $3.2\,\mu$sec to be consistent with the hardware design of the hardware crossover delay time of $3.2\,\mu$sec. If the

timing duration exceeds the upper limit, which is 396.8 μsec , it is bounded to the upper limit.

7. At the end of the sampling cycle, the old values of three interrupt vectors are restored. The old content of mask register is restored, and the input and output ports are turned off.

The flow chart of the computer software (in Borland C++ code) for the implementation of the switching scheme is shown in Fig. 5.14.

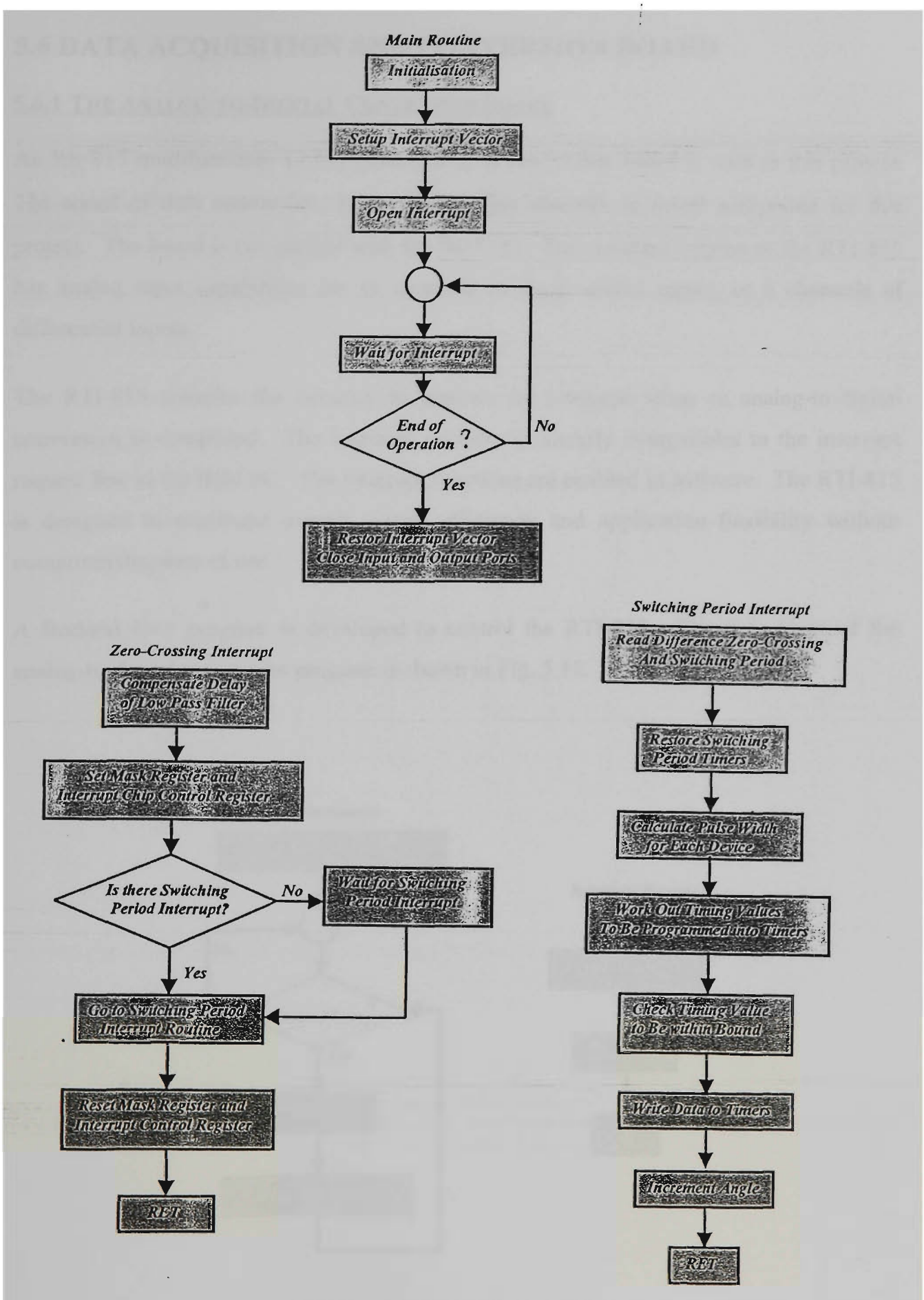

Fig.5.14 Flow Chart of the Controller Software

5.6 DATA ACQUISITION AND CONVERSION BOARD

5.6.1 THE ANALOG-TO-DIGITAL CONVERSION BOARD

An Rti-815 multifunction, 12 bit, Analog/Digital conversion board is used in this project. The speed of data conversion, being 25 μsec/per channel, is found acceptable for this project. The board is compatible with the IBM PC. The standard version of the RTI-815 has analog input capabilities for 16 channels of single-ended inputs, or 8 channels of differential inputs.

The RTI-815 contains the circuitry to generate an interrupt when an analog-to-digital conversion is completed. The interrupt circuitry is directly compatibles to the interrupt request line in the IBM PC. The interrupt functions are enabled in software. The RTI-815 is designed to maximize overall system efficiency and application flexibility without compromising ease of use.

A Borland C++ program is developed to control the RTI-815. The flow chart of the analog-to-digital conversion program is shown in Fig. 5.15.

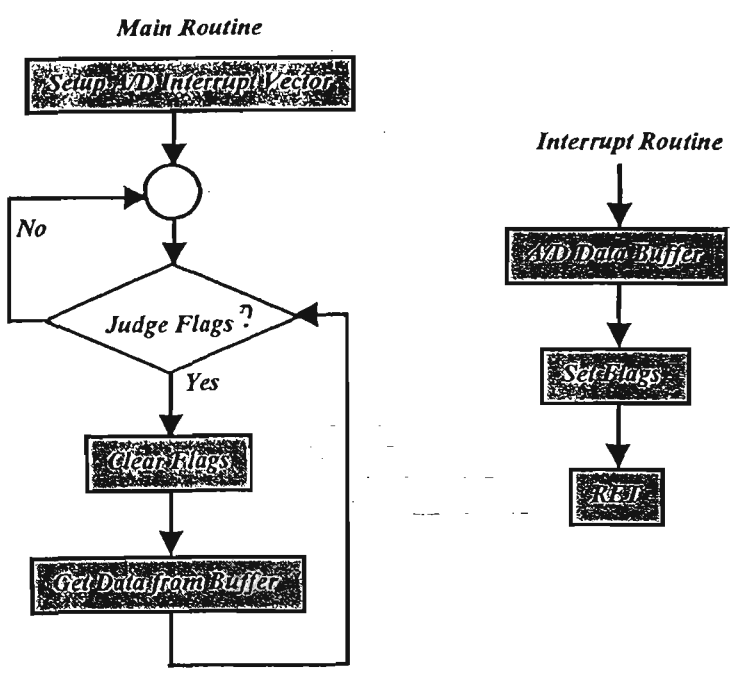

Fig. 5.15 Flow Chart of the A/D Conversion Software

The program for this implementation is listed in Appendix B.

5.6.2 CURRENT AND VOLTAGE TRANSDUCERS

The current and voltage transducers are developed in this project. The current transducer, FB50P and voltage transducer, LV25-P from Farnell are chosen to measure both AC and DC voltage and current. The current transducers are Hall effect type, which allows for accurate measurement of instantaneous values of AC and DC currents up to 50A. The transducers can provide either current or voltage output. The output is linearly related to the primary current flowing through the current core. The circuit connection of three current transducers and three voltage transducers is shown in Fig. 5.16.

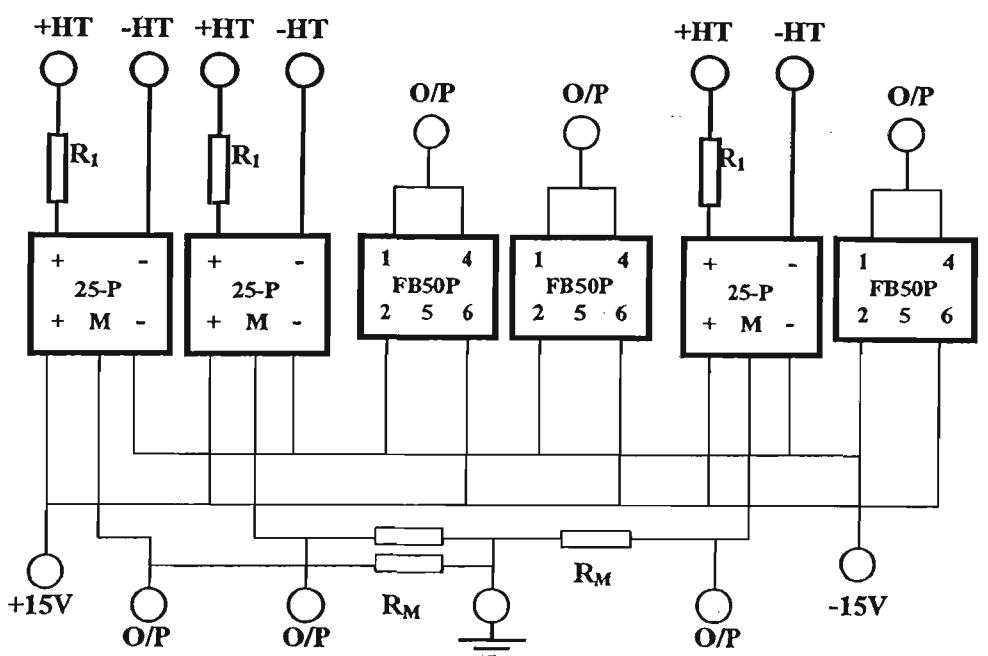

Fig. 5.16 Circuit Connection of Three Current Transducers and Three Voltage Transducers

The overview of the PC-486 computer controlled 10 kVA three-phase AC/DC power converter is shown in Fig. 5.17.

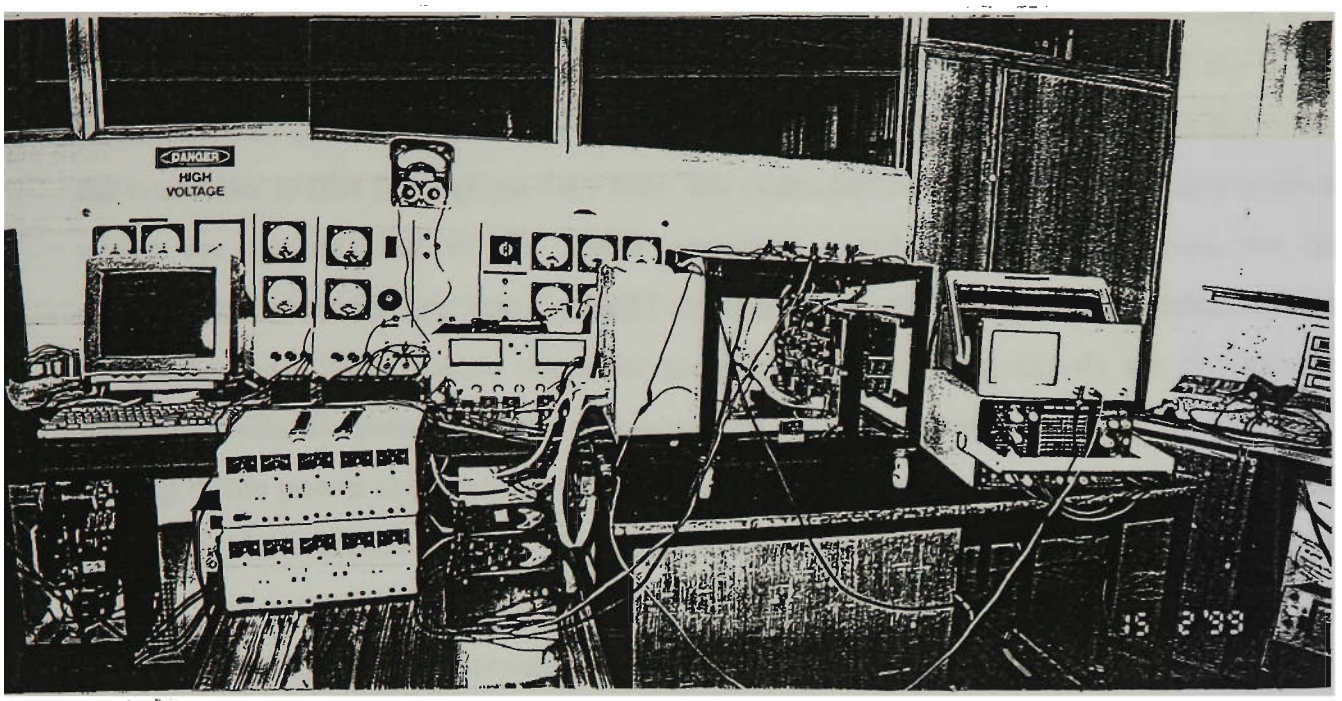

Fig. 5.17 View of the Computer Controlled Three Phase Voltage Source Converter

5.7 SUMMARY

The experimental system for the investigation of the PWM controlled three-phase AC/DC converter has been developed and tested. The operation principles of each unit of the entire system were described in this Chapter. The software which interfaces the PC-486 computer with the PWM generator board is designed and described. The main function of the controller is that for a given duty ratio, the controller calculates the switching intervals, which are downloaded to the PWM generator board. The gating signals are then synthesized before feeding into the IGBT devices of the voltage source converter. In order to operate the voltage source converter properly, the switching signals are synchronized with the utility frequency by the synchronizing unit. The crossover delay for preventing any leg of the power converter from shoot-through is hardware implemented and taken into account in the software design. The data acquisition and conversion card is also software tested. The controller software and A/D conversion software are all developed in Borland C++ code. Experimental results obtained using this system are described in the next chapter.

Chapter 6

EXPERIMENTAL RESULTS

6.1 INTRODUCTION

In Chapter 5, the experimental system was presented. In this Chapter, the performance of the system is experimentally verified. Four important components are investigated, namely synchronising unit, timer board, crossover delay and voltage source converter. All experimental results are analyzed and recorded using a BWD 880 power-scope and a Tektronix TDS 310 digital storage oscilloscope.

6.2 THE DESIGN OF POWER FILTER

Topology of the experimental circuit is shown in Fig. 6.1. It consists of six IGBT switches, three line inductances L, three line resistances R_L, output capacitor C and load resistance R_0. The line inductance and resistance provide low pass filter characteristics to minimize the line current harmonics. The output capacitor is to attenuate the high switching frequency.

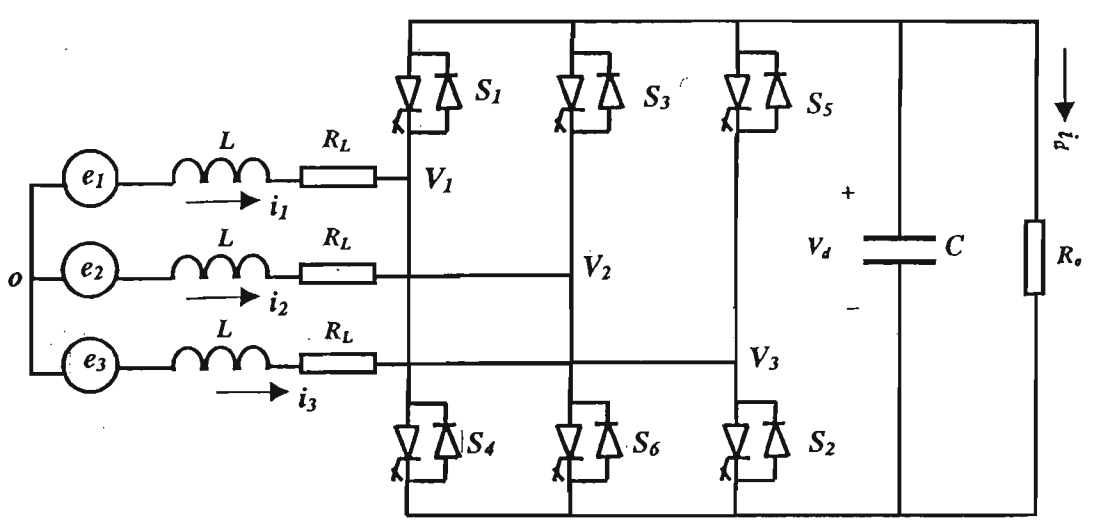

Fig. 6.1 The Circuit of Three Phase PWM AC/DC Power Converter

The tests were conducted with 15V (rms) phase voltage power supply, 40Ω load resistance, 1175 μF output capacitor and 2.5KHz sampling frequency.

The value of the line inductance is determined according to power balance and per unit expression. The conservation of power (in steady state) is given [1, 18].

$$V_d i_d \approx \frac{3}{2} E i_1 \cos\phi \qquad (6.2\text{-}1)$$

Where V_d and i_d are the DC output voltage of converter and load current. E and i_1 are the rms values of phase voltage power supply e_1, and line current . ϕ is an angle between E and i_1. If the unity power factor is obtained, $\cos\phi = 1$. In this study, the modulation index is assumed as 0.6. V_d, i_d and E are equal to 26V, 0.65A, 15V respectively. Per unit is chosen 0.25. From equation (6.2-1), the value of line current is derived, that is 0.6A. The per unit expression of i_1 is given as follows:

$$\frac{i_1}{\left(\frac{E}{\omega_o L}\right)} = 0.25 \text{ p.u.} \qquad (6.2\text{-}2)$$

From the equation (6.2-2), the value of line inductance is determined, that is 20mH. The PWM switching strategy produces little low-order harmonics, but a significant amount of high-order harmonics [28]. The high-order harmonics usually center around frequencies which are multiples of the switching frequency. Therefore, a power filter made by the line inductance and resistance is required to reduce these harmonics to the power system. The cut-off frequency of the filter is

$$f = \frac{R_L}{2\pi L} \qquad (6.2\text{-}3)$$

The line resistance is chosen such that the cut-off frequency of the filter is:

1. higher than the power frequency, 50Hz;
2. lower than the switching frequency;

In this design, a 6Ω line resistance is used which gives a cut-off frequency of 60HZ for the line inductance of 20mH.

6.3 EXPERIMENTAL RESULTS

6.3.1 EXPERIMENTAL RESULTS FOR SYNCHRONIZING UNIT

The synchronizing unit was described and its block diagram was presented in section 5.4.3 of chapter 5. Fig. 6.2 shows the utility phase voltage (top trace) and the output of the zero-crossing detector circuit. The zero-crossing signal repeats every 20 ms and is used as an interrupt to the PC to synchronize the switching period with the mains. In this design, the interrupt request, IRQ, in the PC-486 computer is set at edge triggered mode. The interrupt request is executed by raising an IRQ input (low to high). From Fig. 6.2, it can be seen there is a 3.3ms (60-degree) delay between the utility phase voltage and the zero-crossing signal caused by the low pass filter. This delay is compensated in the software.

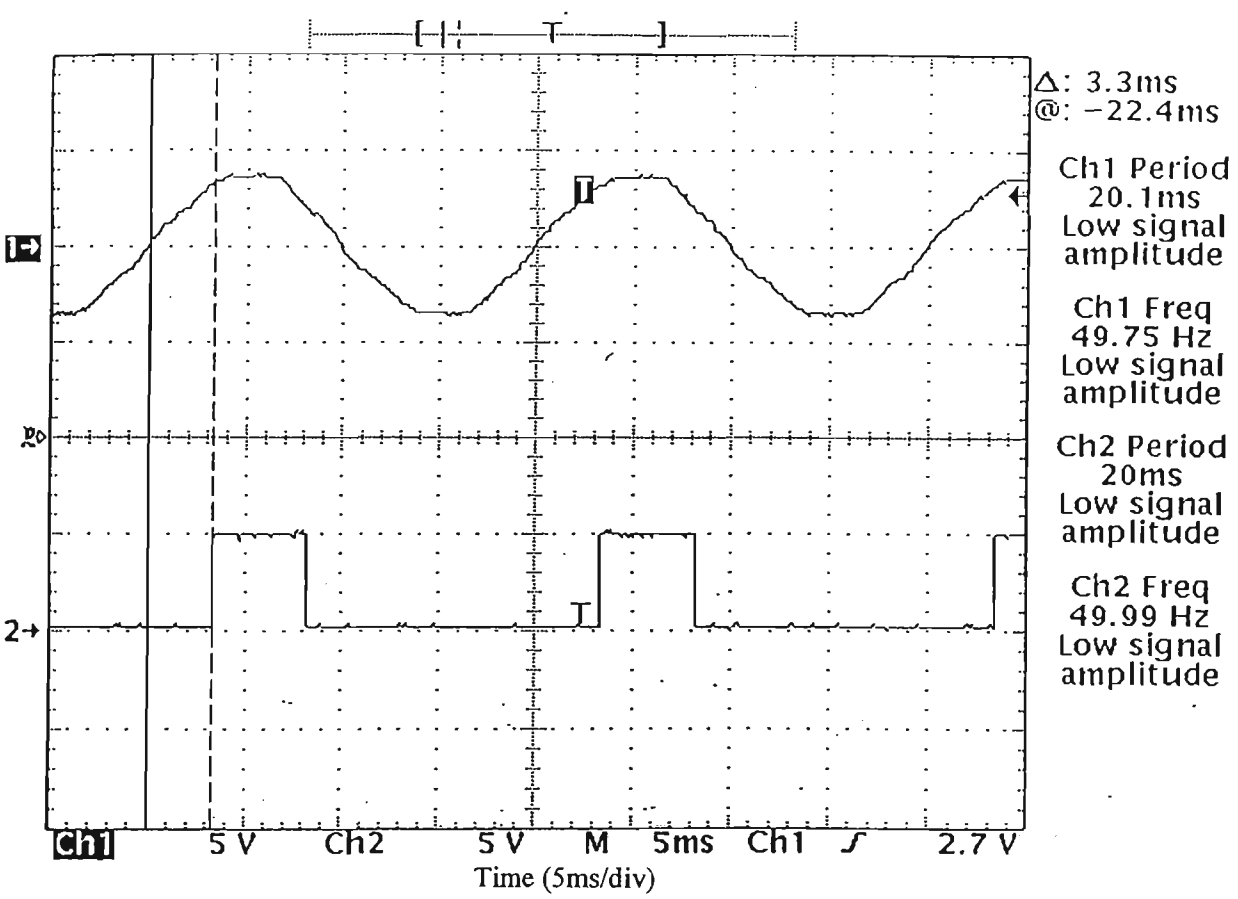

Fig. 6.2 Experimental Result of Synchronising Unit

6.3.2 EXPERIMENTAL RESULTS OF PWM GENERATOR BOARD

The block diagram and the function of PWM generator are detailed in section 5.4 of chapter 5. Fig. 6.3 gives the experimental results of the PWM generator board. The switching period interrupt signal output from the sampling timer is shown in the top trace,

and the actual PWM firing signal from the J-K flip-flop over one sampling period (400μs) is given in the lower trace. Please note that the switching period is 800μs (1.25KHz) being twice of the sampling period. This is referred to as a asymmetrical PWM strategy.

Fig. 6.4 shows the utility phase voltage (top trace) and the PWM firing signal (lower trace) over one line frequency period (20ms). The utility phase voltage is the one based on which the zero crossing signal is generated. Obviously, there is a phase shift between the utility phase voltage and the fundamental component of the switching function due to the presence of a large line inductance between them.

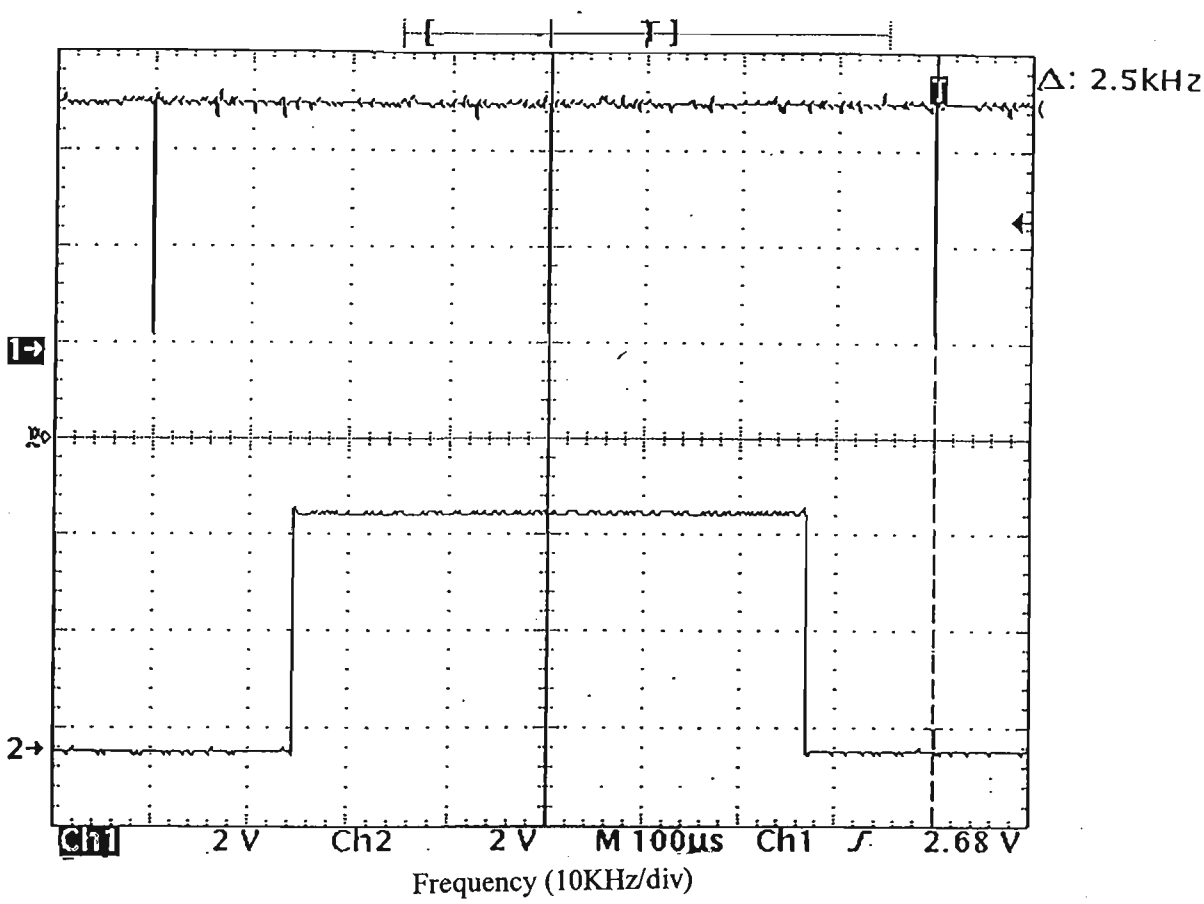

Fig. 6.3 Experimental Results of Sampling Signal and PWM Firing Signal

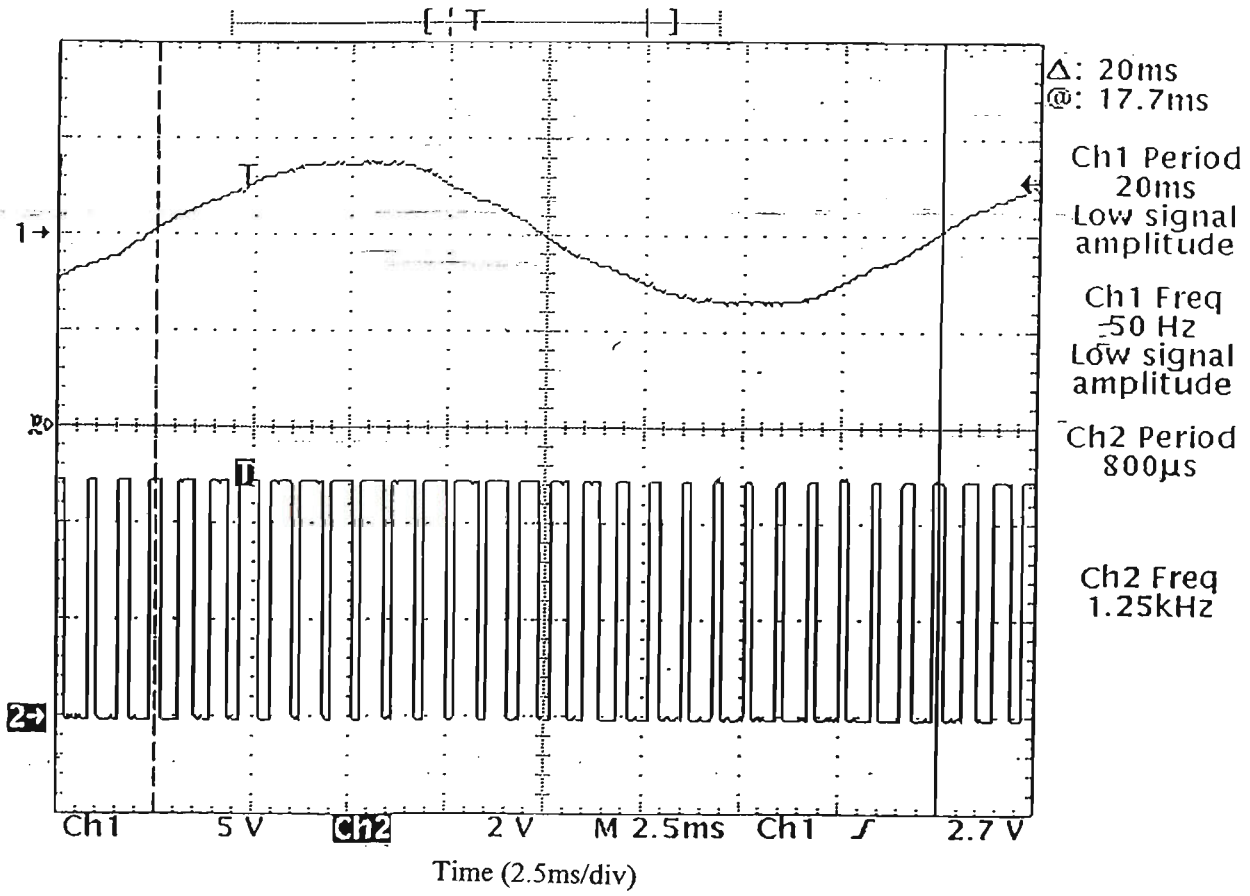

Fig. 6.4 Experimental Results of Utility Phase Voltage and PWM Firing Signal

6.3.3 EXPERIMENTAL RESULTS OF THE CROSSOVER DELAY CIRCUIT

The effect of crossover delay was described in section 4.3.3 of chapter 4. Fig. 6.5 gives the experimental results of the output of the crossover delay unit. The top and bottom traces indicate gating signals to the upper and lower devices of one phase leg respectively. It shows that there is $3.2\mu s$ crossover delay between two switching signals, this ensures from hardware side no shoot-through in any one leg of converter. The value $3.2\mu s$ is determined based on the rise and tailing times of the IGBT device in use.

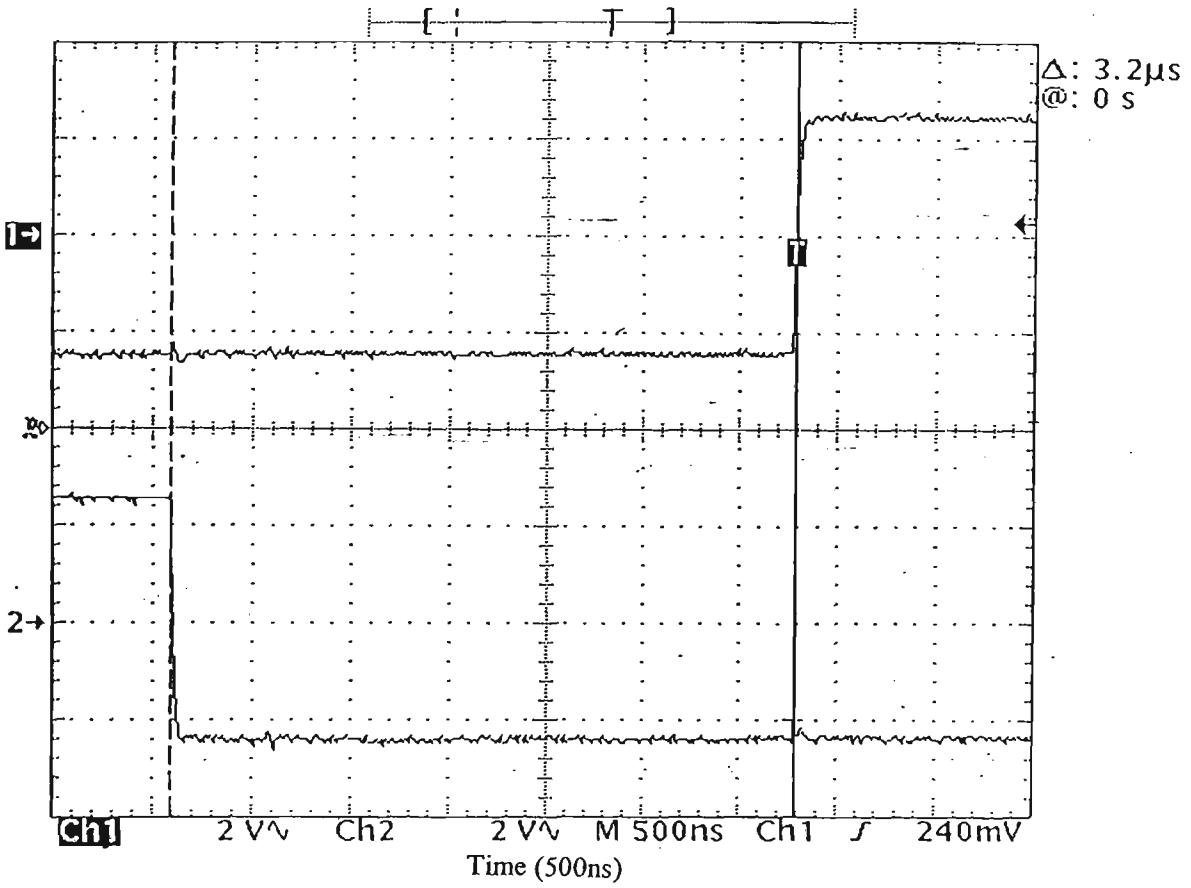

Fig. 6.5 Experimental Result of Crossover Delay

6.3.4 EXPERIMENTAL RESULTS OF THE VOLTAGE SOURCE CONVERTER

For the verification of the software and hardware of the PWM board, an open-loop low voltage test was performed at a supply voltage of 15 volt (rms). Modulation index is specified via the key board of PC, and the resulting voltages and currents on both AC and DC sides of the converter are measured. The experimental results are given in Table 6.1 for the modulation index range of 0.1 to 0.9. It can be seen that as the modulation index increases, the DC output voltage, V_d, is increased, the AC input current, i_1, decreases and the converter phase voltage, V_1, is also increased.

Modulation Index M	**DC-Output Voltage V_d(V)**	**AC Input Current i_1(A) (rms)**	**ConverterPhase Voltage V_1(V) (rms)**	**Load Current i_d(A)**
0.10	6.00	1.90	0.62	0.14
0.15	8.90	1.85	0.92	0.20
0.20	11.0	1.80	2.30	0.24
0.25	13.5	1.75	2.80	0.29
0.30	15.5	1.70	3.35	0.34
0.35	18.5	1.62	4.00	0.40
0.40	20.0	1.55	4.80	0.46
0.45	22.0	1.48	5.40	0.50
0.50	23.5	1.40	6.20	0.54
0.55	24.8	1.32	6.90	0.61
0.60	25.5	1.25	7.80	0.63
0.65	26.5	1.15	8.70	0.66
0.70	27.0	1.10	9.30	0.68
0.75	27.8	1.00	10.4	0.70
0.80	28.5	0.95	11.0	0.72
0.85	29.0	0.88	11.7	0.73
0.90	29.5	0.80	12.2	0.74

Table 6.1 The Experimental Results of the Converter

In order to justify these experimental results are correct, the equation (2.3-6) that is analyzed in Chapter 2 is rewritten here.

$$V_d = \frac{2V_k}{M} \qquad (k = 1,2,3;) \qquad (6.3\text{-}1)$$

Referring again to Table 7.1, it can be seen that V_d is DC output voltage of converter, M is the modulation index and V_k is the AC terminal phase voltage of converter pointed 1,2 and 3 respectively. The line current i_k is given:

$$i_k = \frac{e_k - v_k}{R_L + j\omega L} \qquad (k = 1,2,3;) \qquad (6.3\text{-}2)$$

From equation (6.3-1) and equation (6.3-2), the theoretical results are obtained in Table 7.2.

Modulation Index M	**DC-Output Voltage V_d(V)**	**AC Input Current i_1(A) (rms)**	**ConverterPhase Voltage V_1(V) (rms)**	**Load Current i_d(A)**
0.10	12.40	2.30	0.62	0.31
0.15	12.26	2.16	0.92	0.31
0.20	23.00	1.97	2.30	0.57
0.25	22.40	1.90	2.80	0.56
0.30	22.33	1.78	3.35	0.56
0.35	22.85	1.65	4.00	0.57
0.40	23.40	1.60	4.80	0.58
0.45	24.00	1.52	5.40	0.60
0.50	24.80	1.42	6.20	0.62
0.55	25.09	1.31	6.90	0.63
0.60	25.60	1.24	7.80	0.64
0.65	26.76	1.15	8.70	0.67
0.70	27.10	1.10	9.30	0.68
0.75	27.73	0.98	10.4	0.69
0.80	28.20	0.92	11.0	0.71
0.85	28.91	0.85	11.7	0.73
0.90	29.10	0.79	12.2	0.74

Table 6.2 The Theoretical Results of the Converter

The comparison of the experimental results, DC output voltage V_d and line current i_1 with those from theoretical results are shown in Fig. 6.6 and Fig. 6.7 respectively. In Fig. 6.6 and Fig. 6.7, it is clearly seen that the experimental results, DC output voltage and line current are approaching their theoretical values for the modulation index greater than 0.4.

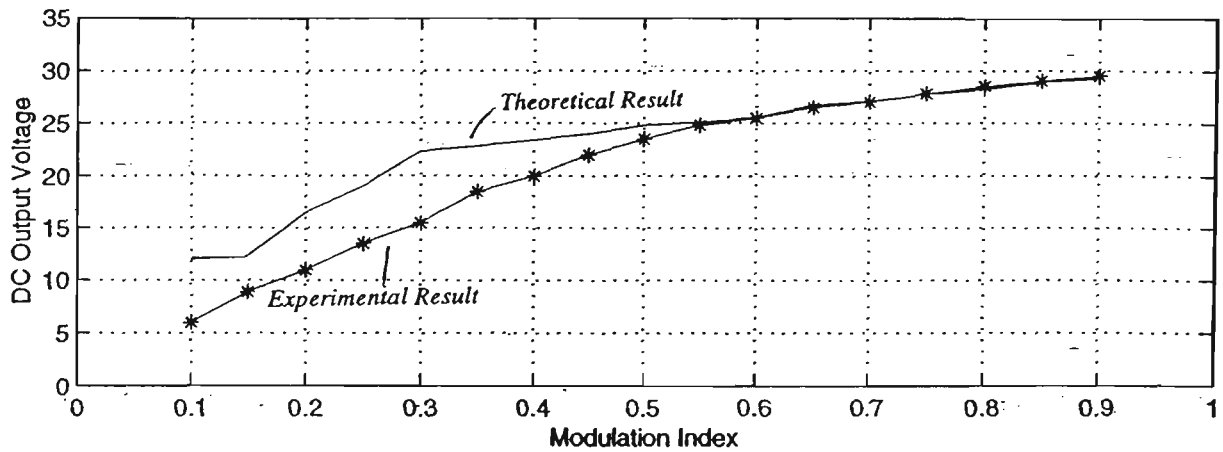

Fig.6.6 DC Output Voltage of Converter

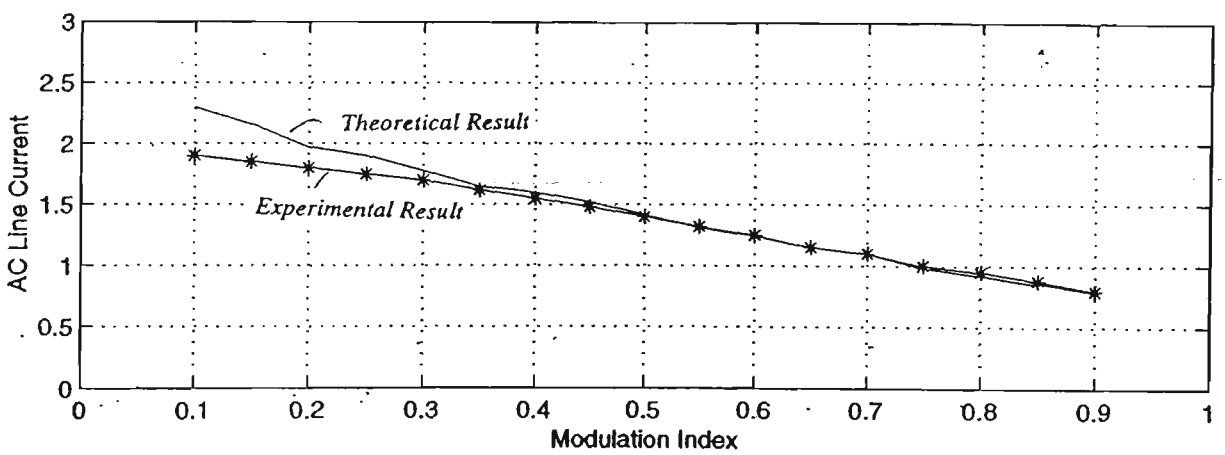

Fig6.7 Line Current

Waveforms of the experimental results at a modulation index of 0.6 are depicted in Fig.6.8. The converter's DC output voltage is shown as the top trace, and the low trace shows the AC input current of the converter. It can be seen that the DC output voltage is constant, while the line current of the converter is nearly sinusoidal.

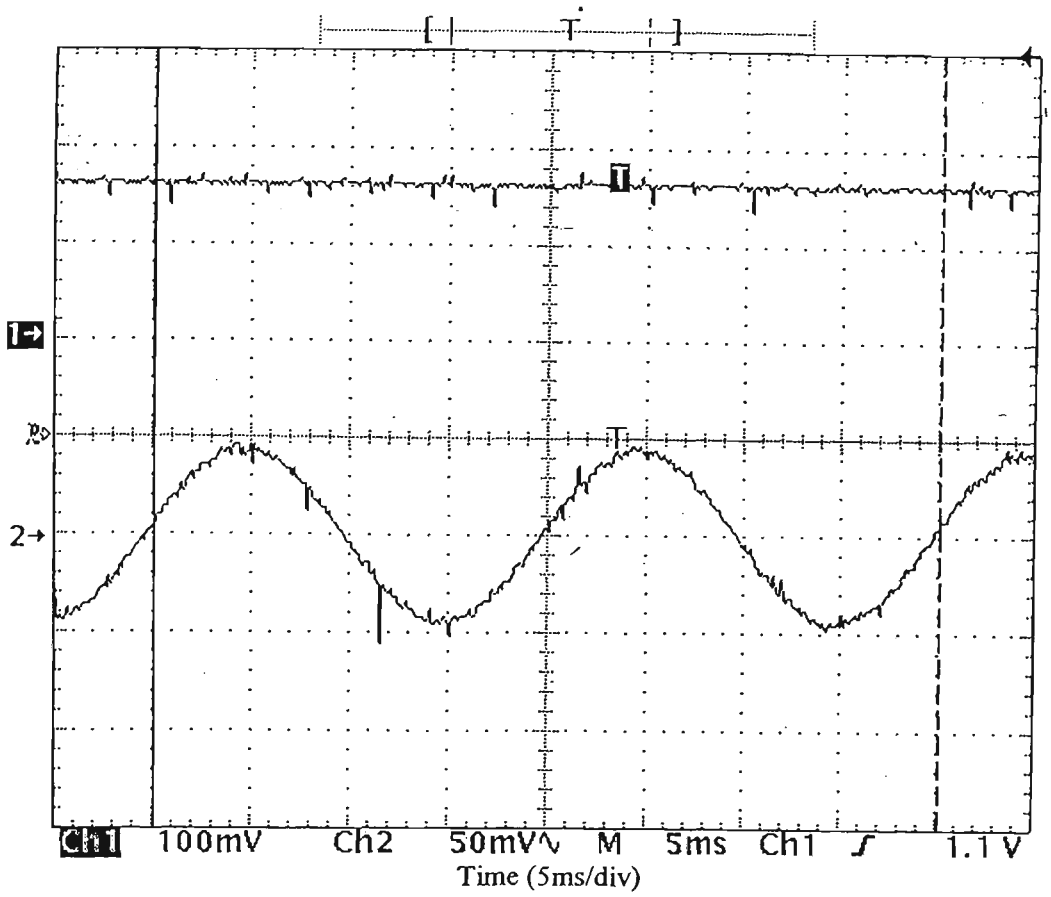

Fig. 6.8 Experimental Results of DC Link Voltage and Input Line Current

Comparisons of the experimental results with those from MatLab simulation are given in the following figures. Fig. 6.9 compares experimental waveforms of the line current and line-to-neutral voltage of the converter system with their simulation ones as shown in Fig. 6.10. The experimental result of chopped voltage waveform at the AC terminal of the converter shown in Fig.6.11 compares with their simulation ones depicted in Fig. 6.12. It is apparent that, the experimental waveforms identical with their simulation ones.

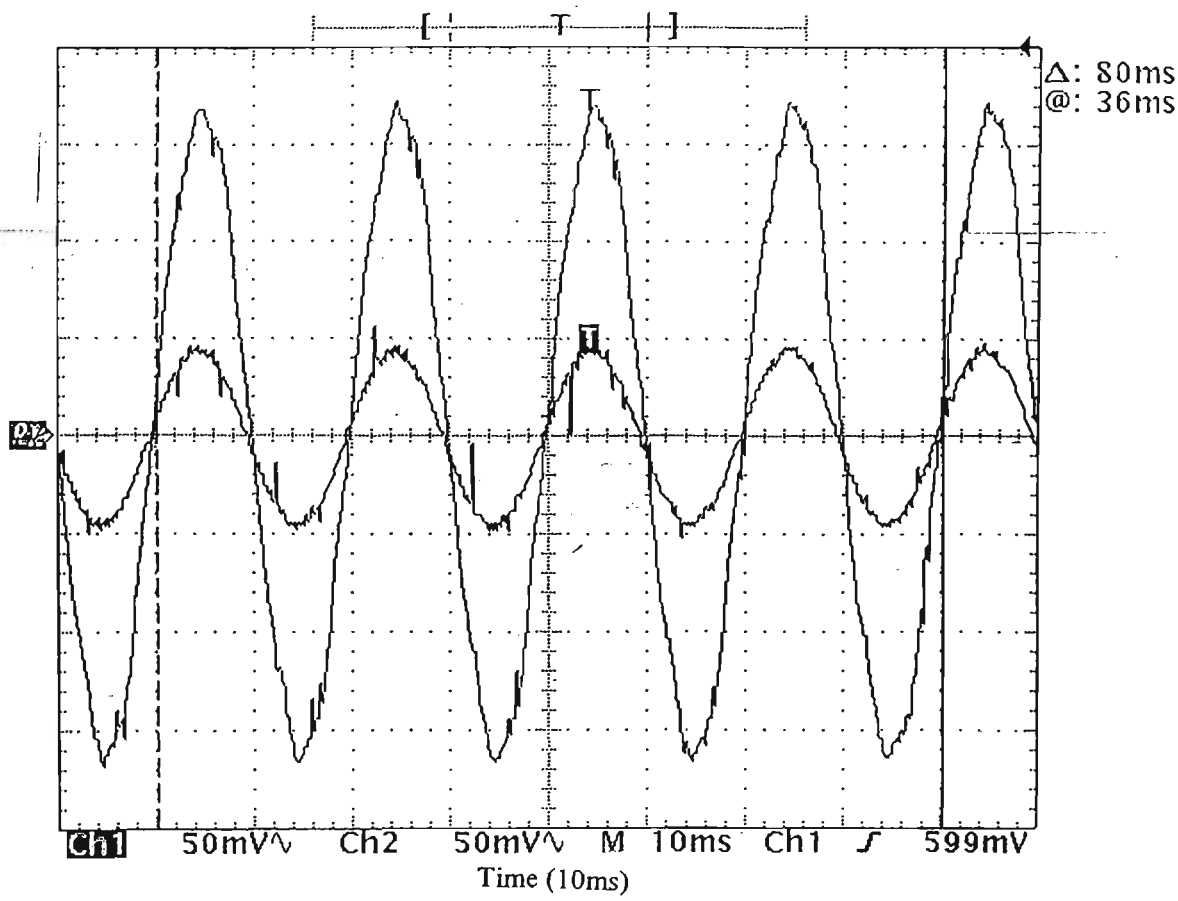

Fig. 6.9 Experimental Results of Line Current and Line-to-Neutral Voltage

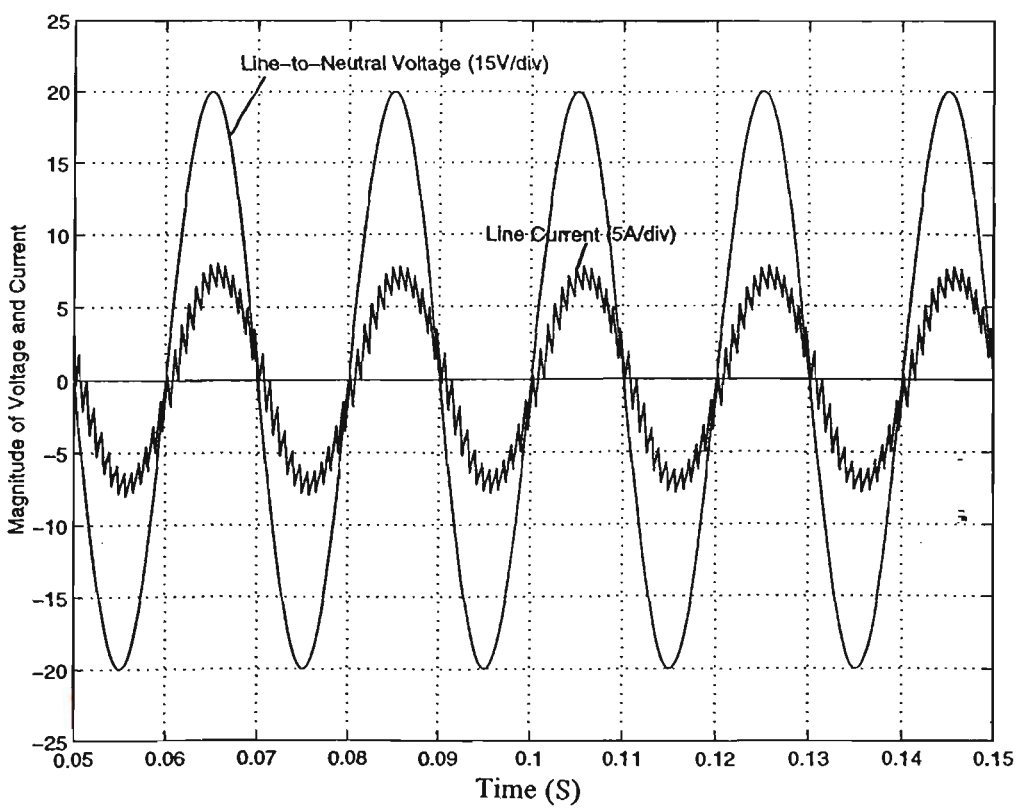

Fig. 6.10 Simulation Results of Line Current and Line-to-Neutral Voltage

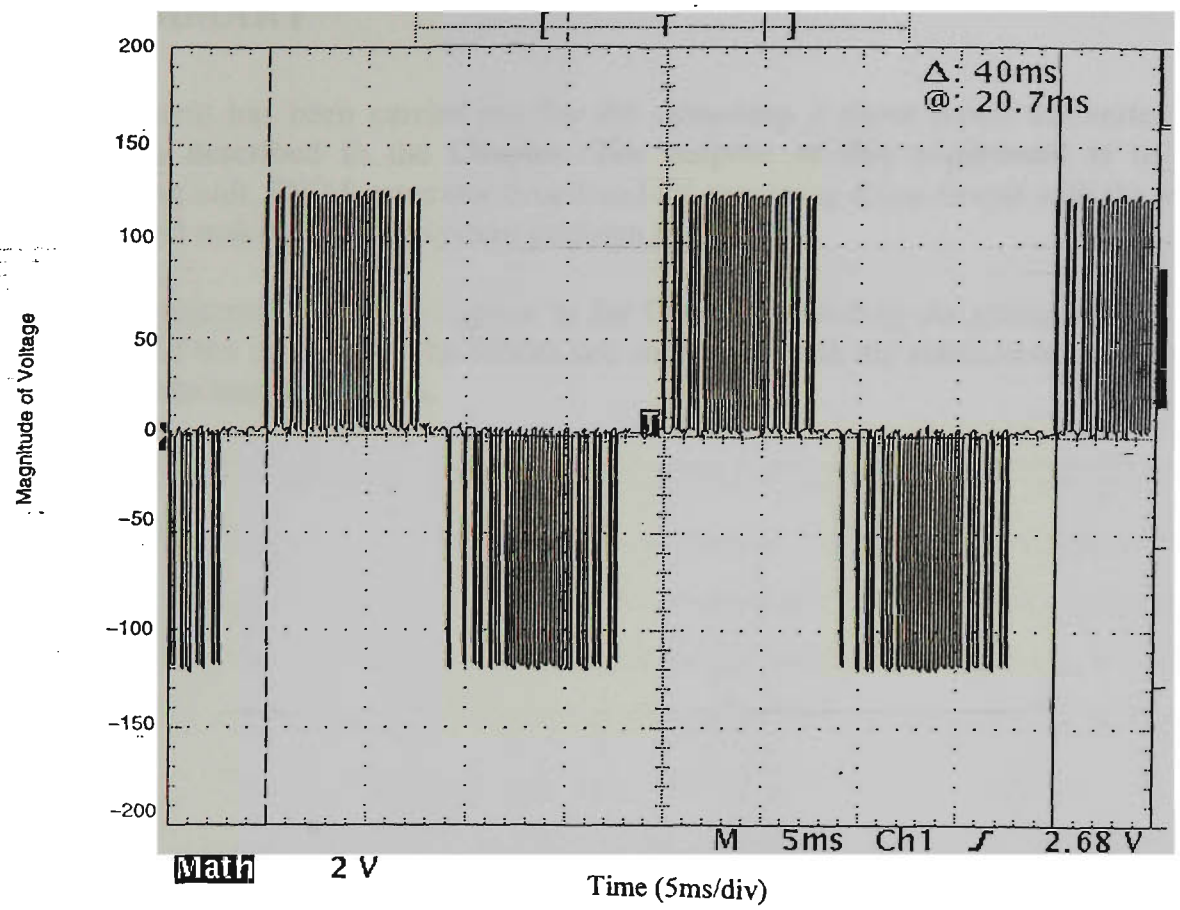

Fig. 6.11 Experimental Results of Line-to-Line Voltage of the Converter.

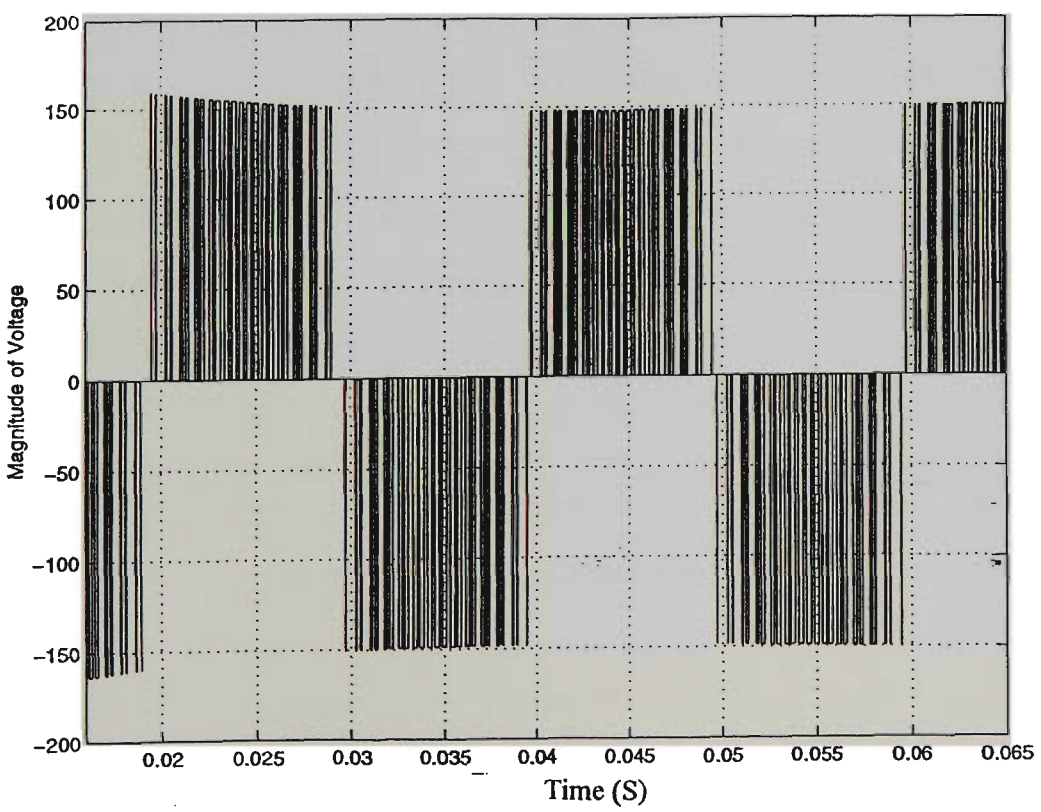

Fig. 6.12 Simulation Result of Line-to-Line Voltage at the AC Terminal of the Converter

6.4 SUMMARY

The experiment has been carried out for the open-loop 3-phase power converter with the test condition as described in the Chapter. The purpose of this experiment is to integrate the synchronizing unit, PWM generator board and the crossover delay circuit with the voltage source converter, and make the entire system perform as expected.

All the experimental results are given in the Chapter, including the gating signal, input voltage and current of the converter. The results are confirmed with the simulation results of the system as shown in the last two figures.

Chapter 7

CONCLUSIONS AND FURTHER WORK

7.1 CONCLUSIONS

Among various PWM AC/DC converter control schemes proposed in current publications, the PCFF control is favorable for some applications because of its well defined switching pattern and the stress on switching devices is predictable. In this technique, the modulating voltage required for controlling the line current is calculated based on the parameters of the power circuit and the switching frequency, this voltage is then compared to a carrier wave to generate a switching pattern to regulate the line current. The major shortcoming of the PCFF control is that its control principle is parameter dependent or sensitive. The power circuit parameters are required to implement the control logic. In practice, these design inputs vary. The accuracy of the control is degraded by these uncertainties.

In this thesis, an H_∞ controller is proposed as the DC voltage regulator, which is to work with the PCFF controller and compensate for its uncertainty problem. The new concept is derived from a predicted current control with fixed switching frequency (PCFF), with the H_∞ voltage regulator to replace a general proportional and integral (PI) voltage regulator to obtain stability robustness and performance robustness. The H_∞ theory has its unique approach to the uncertainty issue. A predictive (AC) current control strategy combined with an H_∞ (DC) voltage regulator is to control a pulse width modulated (PWM) voltage source converter (VSC), so as to achieve constant DC link voltage and nearly sinusoidal line current waveform with a unity power factor.

The H_∞ voltage regulator is designed in the frequency domain based on the worst case scenario, the sudden change of the operating condition from the rectifying to the regeneration. This load disturbance causes uncertainty problem as the transfer function of the PCFF controlled power converter experiences a significant change due to the shift of the operating point. From the simulation results, the system of the predicted current control with H_∞ voltage regulator is capable of achieving performance robustness and stability

robustness for the output DC link voltage of the AC/DC power converter, and nearly sinusoidal line currents with a unity power factor, while the power converter is transferred from the rectifying to the regeneration.

The thesis then moves on to describe the physical implementation. The operation of AC/DC IGBT power converter is analyzed and the input power filter is designed. The INTEL PC-486 single chip computer as real-time controller is designed to control the power converter (10 kVA) via a PWM generator board and synchronizing unit. The synchronizing unit synchronizes the fundamental frequency of the PWM signal with the mains. The PC-486 controller calculates the switching intervals according to the modulation index and output frequency using space vector PWM algorithm after the PWM signal has synchronized with the mains. The results of calculation are downloaded to the PWM generator board to generate gating pulses to six IGBT switches of the power converter.

Finally, the experimental results of PWM generator board are given, and the practical and simulation results of the power converter are shown to produce a comparable physical and simulation performance. The experimental results show that the computer controlled switching pattern of power converter can achieve the constant DC output voltage and nearly sinusoidal line currents with a unity factor.

7.2 FURTHER WORK

The work presented in this thesis confirms the basic concept of three-phase predictive pulse width modulated AC/DC power converter with an H_∞ controller, and verifies its effectiveness. There are still a number of areas of further investigation which would be desirable before the technique was included into a complete system. These areas can be separated into theoretical and practical issues.

7.2.1 FURTHER THEORETICAL WORK

In this thesis, the H_∞ controller is proposed and designed as DC voltage regulator for a three-phase AC/DC PWM voltage source converter, which is under the PCFF current control to compensate its uncertainty problem. Theoretically, the advanced H_∞ controller

has not much advantage for a single-input single-output system, compared with the conventional controller. If the H_∞ controller can be designed for a multiple-input multiple-output system, which means the H_∞ controller replaces the PCFF controller, there is a great deal of advantage. The robust multivariable feedback control system can maintain the system response and error signals to within prespecified tolerances despite the effects of uncertainty in the system.

7.2.2 FURTHER PRACTICAL WORK

The further practical work required by the project is the software development to integrate the H_∞ voltage regulator, the modulator, the data acquisition and the data conversion components, and the voltage source converter into a closed-loop system. Some fine tuning may be needed for the entire real-time system to perform as specified.

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Appendix A

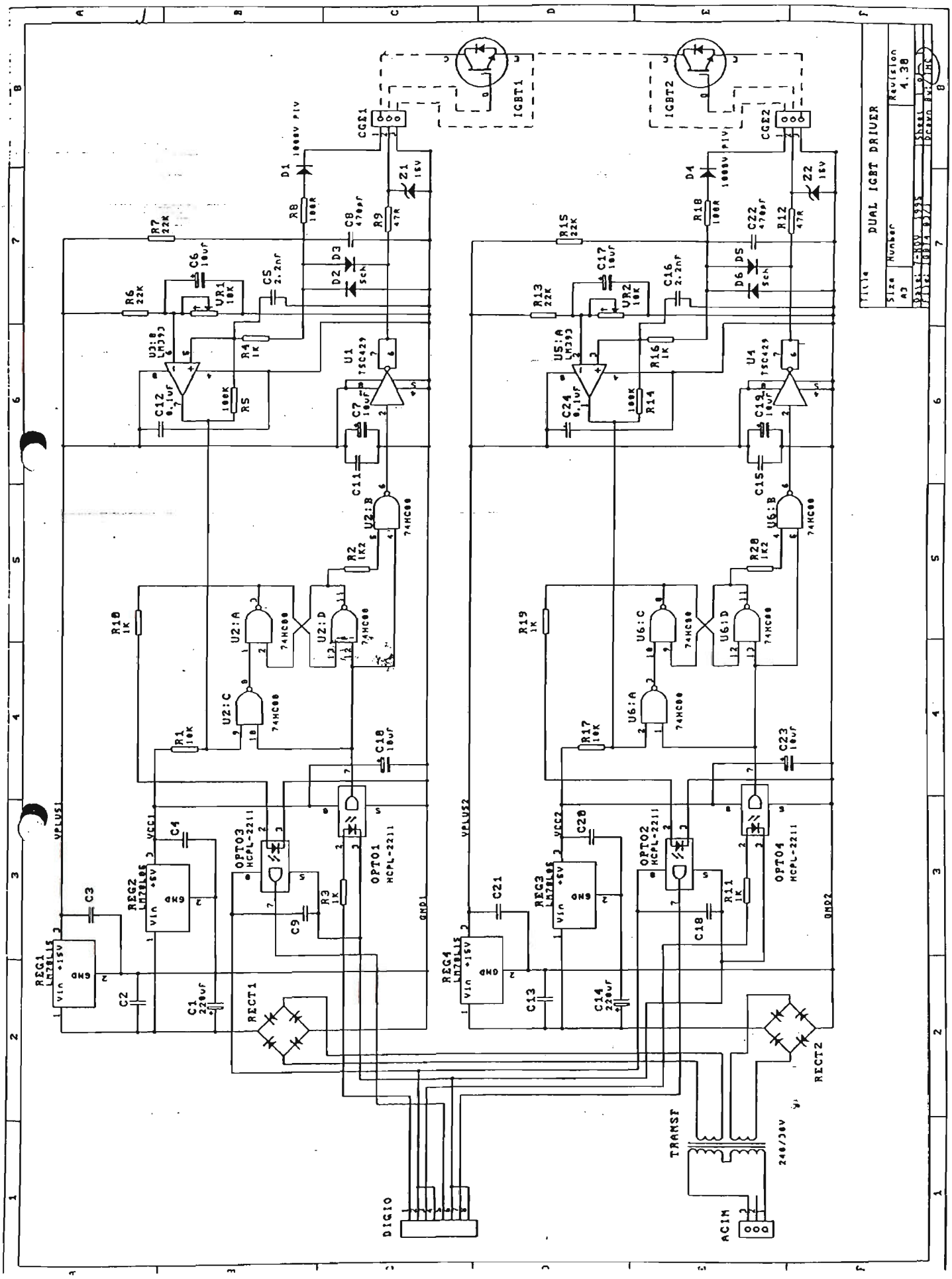
CIRCUIT SCHEMATICS

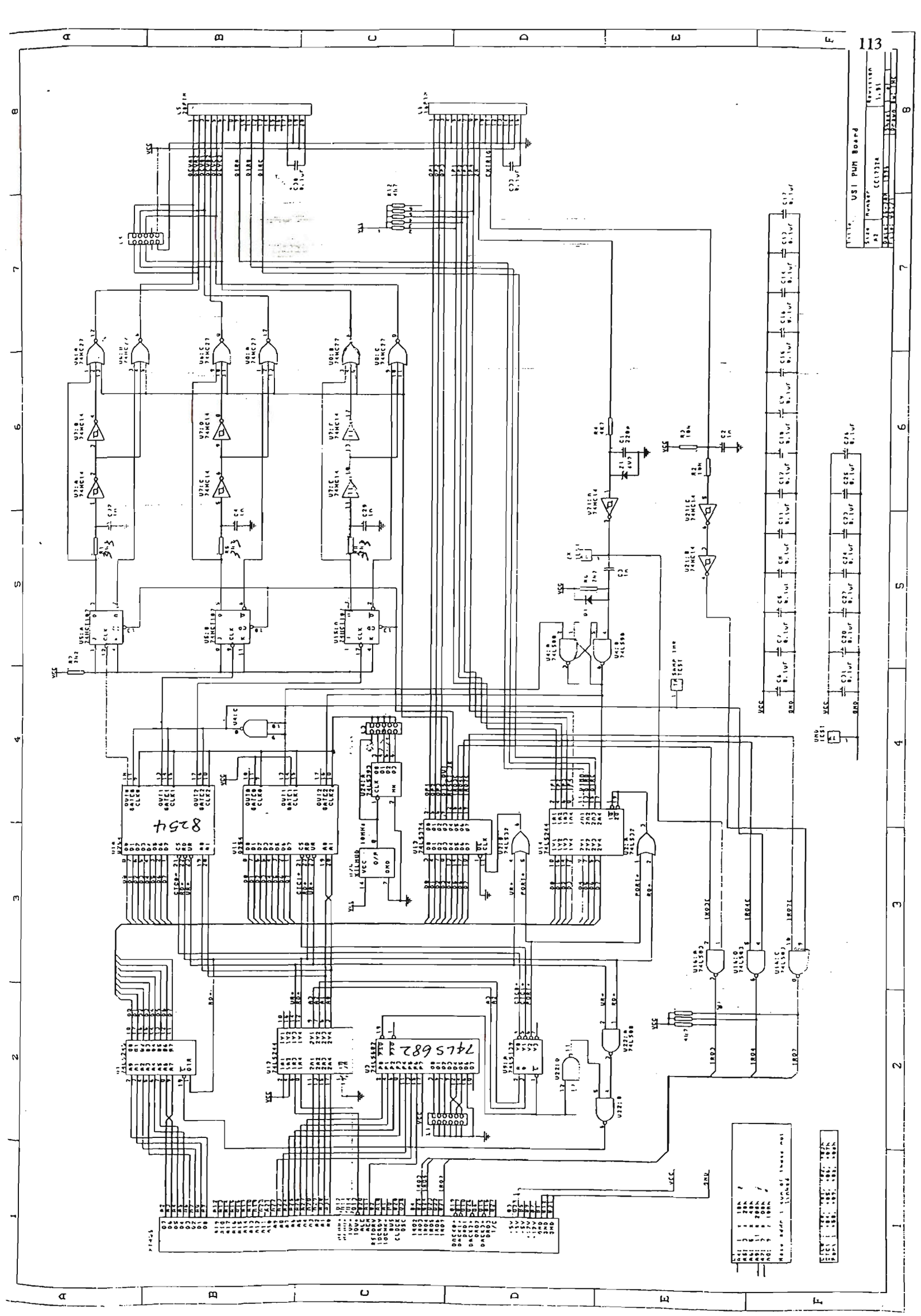
1. IGBT Driver (described in section 5.2.2)

   This circuit provides interfacing between the low-voltage computer controller and the high-voltage IGBT switching devices. The circuit also protects the switching devices from over-current.

2. PWM Generator Board (described in section 5.4)

   This circuit provides the hardware to generate PWM signals to the switching devices of the converter. The circuit consists of timer board, control block, synchronizing unit, zero-crossing board and crossover delay. The control block and timer board can be programmed to produce different PWM signals. The synchronizing circuit for synchronizing the computer controller to the synchronizing signal generated by the zero-crossing circuit. The crossover delay circuit can ensure no shoot-through in any leg of the converter and zero-crossing circuit detects zero-crossing of the mains for synchronizing the computer controller.


DUAL IGBT DRIVER
Revision
4.30
IGBT1
IGBT2
CGE1
CGE2
D1
D4
Z1
Z2
R7
R15
R8
R18
R9
R12
C8
C22
C6
C17
C5
C16
D2
D3
D5
D6
R6
R13
VR1
VR2
U3:B
U5:A
R4
R16
U1
U4
C12
C24
R5
R14
C7
C19
C11
C15
U2:B
U6:B
R2
R20
R10
R19
U2:A
U2:D
U6:C
U6:D
U2:C
U6:A
R1
R17
C18
C23
VPLUS1
VPLUS2
VCC1
VCC2
OPT03
OPT01
OPT02
OPT04
C4
C20
R3
C9
R11
C18
REG2
REG3
REG1
REG4
C3
C21
C2
C13
C1
C14
GND1
GND2
RECT1
RECT2
TRANSF
240/30V
DIGIO
ACIN


VSI PWM Board
8254
74LS682

Appendix B

SOFTWARE PROGRAMS

B1. SIMULATION FUNCTION

There are three simulation programs. The first one called 'set up parameters' used as SIMULINK function to set up system parameters and operating condition during the simulation. The second and third programs called 'frequency spectra subroutine' and 'total harmonic distortion subroutine' respectively, used to analyse the simulation results after simulation. The programs are given as follows.

1. Set-Up Parameters

```
%File Name:     setuppcff.m
%Title:         Voltage Source Converter Parameters Set up
%Date:          05/04/1996
%Programmer:    Ming Yu
%Discription:   This program will set up voltage source converter parameters and operating condition

R=1;                                %the value of line resistance, 1 Ω
L=0.01;                             %the value of line inductance, 10mH
Ro=40;                              %the value of load resistance, 40 Ω
C=0.0002;                           %the value of dc link voltage capacitor, 200 μF
Ts=1/1250;                          %the value of switching frequency, 1250Hz
K1=((L/Ts)-R);
K2=sqrt(2)*(60/sqrt(2));            %the amplitude of utility supply
K3=0.5;
K4=1/4.5;
K5=-(L/Ts);
K6=0.146;                           %the gain of H∞ controller
K7=1.05;                            %the gain of phase lead controller
zo1=-35.32;                         %the zeros of H∞ controller
zo2=-49.98;
zo3=-199.74;
po2=-2.0;                           % the poles of H∞ controller
po3=-321.2;
zo4=-23.31;                         %the zero and pole of phase lead controller
po4=-107.22;
```

2. Frequency Spectra Subroutine

```
%File Name:     spect.m
%Title:         Voltage Source Converter Frequency Spectra Analysis
%Date:          09/11/1996
%Description:   This program is to print usrfile frequency spectra waveform

%usrfile        which waveform stored in workspace is analysed in the frequency spectra (current i1)
%fo             fundamental frequency
%fs             switching frequency

function spect(usrfile,fo,fs)

fprintf('\n\nHave Entered Waveform, Fundamental Frequency and Switching Frequency\n\n');
fprintf('\nFundamental Frequency = %g\n',fo);
fprintf('\nSwitching Frequency = %g\n',fs);

input('\n*****Please Press Return Key To Continue*****\n');

subplot(2,1,1);
mn=length(usrfile);
y=fft(usrfile,mn);
f=(0: (mn/2-1))/(mn)*(fs/4);
plot(f,10*log10(abs(y(1: (mn/2))/abs(y((mn*fo/fs)+1))));
grid;
ylabel('Magnitude of Current (dB)');
xlabel('Frequency (Hz)');
```

The fft(x) is a MATLAB function which is the discrete Fourier transform of vector x, computed with a fast Fourier transform algorithm (FFT). The function fft(x) implements the transform given by:

$$X(k+1) = \sum_{n=0}^{N-1} x(n+1) W_N^{kn}$$

where $W_N = e^{-j(2\pi/N)}$ and N=length(x). The series is written in an unorthodox way, running over n+1 and k+1 instead of the usual n and k because MATLAB vectors run from 1 to N instead of from 0 to N-1.

Sometimes it is useful to normalize the output of fft so that a unit sinusoid in the time domain corresponds to unit amplitude in the frequency domain. To produce a normalized spectrum in this manner, MATLAB gives:

$$P_n = abs(fft(x)) * 2 / length(x)$$

which is used to analysis the simulation results after simulation.

3. Total Harmonic Distortion Subroutine

```
%File Name:     thdcb.m
%Title:         Voltage Source Converter Total Harmonic Distortion
%Date:          15/12/1996
%Description:   This function is to compute the total harmonic distortion of the periodic waveform of
%               usrfile, with fundamental frequency fo and simulation sampling frequency fs


%usrfile        which waveform stored in workspace is analysed in the frequency spectra (current i1)
%fo             fundamental frequency
%fs             simulation sampling frequency

function spect(usrfile,fo,fs)

fprintf('\n\nWelcome to Total Harmonic Distortion Program\n\n');
fprintf('\nFundamental & Simulation Sampling Frequency Have Entered\n');
fprintf('\nFundamental Frequency = %g\n',fo);
fprintf('\nSwitching Frequency = %g\n',fs);
fprintf('\n- - - - - - Please Wait for a While - - - - - -\n');

a=zeros(120);
b=zeros(120);


for n=1:120

        for m=3601: (3600+fs/fo)

            a(n)=a(n)+(usrfile(m)*cos(n*6.28*fo/fs*m)+usrfile(m-1)*cos(n*6.28*fo/fs*(m-1))
            b(n)=b(n)+(usrfile(m)*sin(n*6.28*fo/fs*m)+usrfile(m-1)*sin (n*6.28*fo/fs*(m-1))

        end

   a(n)=2*fo*a(n);
   b(n)=2*fo*b(n);

end

p=0.0;


for n=2:25

        p=p+a(n)*a(n)+b(n)*b(n);

end


Y=(sqrt(p)*100/sqrt(a(1)*a(1)+b(1)*b(1));

Fprintf('\n T.H.D. = %g(%)\n\n\n\n',Y);
```

B2. COMPUTER PROGRAM

There are two computer programs which uses Borland C++. One is the control algorithm program that generates switching signals. The other is used for analog-to-digital converter card.

1. VSC PWM Switching Control Routine

This program generates PWM signals for three-phase voltage source converter. The PWM used is a 'Predicted Current Control Duty Ratio Algorithm'.

The timing for the generation of PWM is achieved by four timers: one timer (Sampling Timer) is for switching period timing and the other three timers (Duration Timers) are for the timing of the switching duration of the six switching devices within a switching period. When the Duration Timers out, it toggles a J-K flip-flop which in turn generates switching signals for the devices.

```
/*      Title:          define.h
        Author:         Ming Yu
        Date:           10/01/1998      */

#ifdef_cplusplus                        // determine C or C++ application
        #define_CPPARGS...
#else
        #define_CPPARGS
#endif

#define IntNoIRQ3       0xb     // com 2, interrupt vector
#define IntNoIRQ4       0xc     // com 1, interupt vector
#define IntNoIRQ7       0xf     // printer, interrupt vector
#define IntCtrladdr     0x20    // interrupt chip 8259 address
#define MaskRegAddr     0x21    // Mask Register address
#define NonSpecEOI      0x20    // interrupt return
#define MaskReg         0x65    // enable IRQ 1,3,4,7

#define CTC0PWMD0       0x290   // CTC0 Timer 0 address
#define CTC0PWMD2       0x291   // CTC0 Timer 1 address
#define CTC0PWMD2       0x292   // CTC0 Timer 2 address
#define CTC0PWMCtrl     0x293   // CTC0 Control Word Register address
#define CTC1PWMD0       0x294   // CTC1 Timer 0 address
#define CTC1PWMD1       0x295   // CTC1 Timer 1 address
#define CTC1PWMD2       0x296   // CTC1 Timer 2 address
#define CTC1PWMCtrl     0x297   // CTC1 Control Word Register address
#define PortPWMIO       0x298   // input and output port address
#define PortOFF         0x08    // reset JK, disable IRQ inter and PWM output
#define PortON          0xf0    // JK toggle, enable IRQ inter and PWM output


#define sinsize         900     // deg 360
```

```
#define  Tz              1000     // equivalent to 400us (2.5KHz) for 2.5MHz
#define  zxdtofs         1500     // Tz*1.5
#define  maxdt           992      // Tz-cross_delay (3.3us)
#define  mindt           8        // cross-delay, minimum dt that can be implemented
#define  m2cnt           256      // equivalent to right shift 8 times
#define  one_half_t      500      // Tz/2
#define  delta_angle     18       // cossize/sampiv, point one switching period
#define  anglemax        900      // deg 360
#define  angle2cnt       55       // Tz/delta_angle, count number one point
#define  angletrim       0
#definezxdtofs           1500     // Tz*1.5

#define  rad120          2.094395102
#define  pi              3.141592654
#define  mcnt            1280              // m2cnt*Tz/maximum_modulation

         /* Assign index number to each switching device */
#define  Idev1           0        // device 1
#define  Idev2           1        // device 2
#define  Idev3           2        // device 3
#define  Idev4           3        // device 4
#define  Idev5           4        // device 5
#define  Idev6           5        // device 6

#define  deg360          900              // degree 360
#define  rad2cnt         143.23945        // radian to count
#define  deg2rad         17.453293e-3     // degree to radian
#define  rad2deg         57.2957795       // radian to degree
#define  deg2cnt         2.5              // degree to count
#define  mod2cnt         200.0            // modulation to count
#define  freq2cnt        0.36             // frequency to count
#define  cnt2deg         0.4              // count to degree
#define  cnt2m           0.005            // count to modulation
#define  cnt2freq        2.777778         // count to frequency

#define  maxm            200              // maximum modulation
#define  minm            1                // minimum modulation

#define  VDREF           150.0            // dc voltage reference
#define  k1              0.3279
#define  k2              0.01719
#define  k3              -0.06477
#define  k4              0.9992
#define  k5              -0.012
#define  k6              0.879
```

```
/*      Title:   Predicted Current Controller
        Author:  Ming Yu
        Date:    10/01/1998                */

#pragmainline
#include<stdio.h>
#include<float.h>
#include<math.h>
#include<dos.h>
#include<conio.h>
#include"define.h"

calc_width(flot reversvd,float ek,float ik,float ick,int ang);

extern void init_sin(void);
extern void init_var(void);
extern void init_scren(void);
extern void init_PWMB(viod);
extern void restore_PWMB(void);

float comparator(float vd);
float regulator(float erorn);

amplitude(float im,float id,float regulat,float *ik,float *ick);

int     oldmask, flag1, flag2, t1, t2, angle, theta[6],
        sin_11[sinsize], sin_21[sinsize], sin_31[sinsize];

void interrupt(*oldIRQ3)(__CPPARGS);          // interrupt vector setup
void interrupt(*oldIRQ4)(__CPPARGS);
void interrupt(*oldIRQ7)(__CPPARGS);

void init_sin(void)
{
        int x;
        float thetarad;

        /* setup sine tables */
        for (x=0;x<sinsize;x++)
          {
                thetarad=2.0*pi*x/sinsize;
                sin_11[x]=(int)((float)mcnt*sin(thetarad));
                sin_21[x]=(int)((float)mcnt*sin(thetarad-rad120));
                sin_31[x]=(int)((float)mcnt*sin(thetarad+rad120));
        }
}

void init_var(void)
{
        int x;

        flag1=0;
        flag2=0;
        t1=t2=0;

        /* initialise variables */
        for(x=Idev1;x<=Idev6;x++)
        {
                theta[x]=0;
        }
```

```
}

void init_PWMB(void)
{
        oldmask=inportb(MaskRegAddr);          // store content of Mask Register
        outportb(MaskRegAddr,MaskReg);         // setup Mask Register

        /* setup output port */
        outportb(PortPWMIO,PortOFF);
        outportb(PortPWMIO,PortON);

        /* setup switching period timer */
        outportb(CTC1PWMCtrl,0x74);            // CTC1 chn 1, mode 2, binary
        outportb(CTC1PWMD1,(_AX=Tz));          // load the timer with Tz
        outportb(CTC1PWMD1,_AH);

        /* setup timers control word for timing mode of the three legs */
        outportb(CTC0PWMCtrl,0x3a);            // CTC0 chn 0, mode 5, binary
        outportb(CTC0PWMCtrl,0x7a);            // CTC0 chn 1, mode 5, binary
        outportb(CTC0PWMCtrl,0xba);            // CTC0 chn 2, mode 5, binary

        /* setup timer for synchronizing */
        outportb(CTC1PWMCtrl,0xb0);            // CTC1 chn 2, mode 0, binary
        outportb(CTC1PWMD2,0);                 // load timer value
        outportb(CTC1PWMD2,0);
}


void restore_PWMB(void)
{
        outportb(MaskRegAddr,oldmask);         // restore Mask Register
        outportb(PortPWMIO,PortOFF);           // close outport port
}

calc_width(float reversvd,float ek,float ik,float ick,int ang)
{
        /* calculate switching on durations for each device */

if(((theta[Idev1]=(int)(reversvd*(((long)ek*sin_11[ang]+(long)ik*sin_11[ang]-
                                                (long)ick*sin_11[ang])>>8))+one_half_t)<0))
{       theta[Idev1]=0;         }

if(((theta[Idev3]=(int)(reversvd*(((long)ek*sin_21[ang]+(long)ik*sin_21[ang]-
                                                (long)ick*sin_21[ang])>>8))+one_half_t)<0))
{       theta[Idev3]=0;         }

if(((theta[Idev5]=(int)(zxdtofs-(theta[Idev1]+theta[Idev3])))<0))
{       theta[Idev5]=0;         }

if(((theta[Idev4]=Tz-theta[Idev1])<0))
{       theta[Idev4]=0;         }

if(((theta[Idev6]=Tz-theta[Idev3])<0))
{       theta[Idev6]=0;         }

if(((theta[Idev2]=Tz-theta[Idev5])<0))
{       theta[Idev2]=0;         }

return(0);
}
```

```
float comparator(float vd)
{
        float compart;

        compart=(VDREF-vd);

        Return(compart);
}

float regulator(float erorn)
{
        float regulat;
        static float rut1=0.0, rut2=0.0, rut3=0.0, rut4=0.0;

        rut1=K1*erorn;
        rut2=K2*erorn+rut2;
        rut3=K3*erorn+K4*rut3;
        rut4=K5*erorn+K6*rut4;
        regulat=rut1+rut2+rut3+rut4;

        return(regulat);
}

amplitude(float im,float id,float regulat,float *ik,float *ick)
{
        im=regulat+id;
        *ik=11.5*im*mod2cnt;
        *ick=12.5*im*mod2cnt;

        return(0);
}

void interrupt zero_crossing(_CPPARGS)
{
        static int count1=0;
        unsigned char b;

        count1++;

        b=inportb(0x03fd);

        disable();
        outportb(MaskRegAddr,0x6d);
        outportb(IntCtrlAddr,0x68);
        enable();

while(flag2==0)
{
        angle=144;
        flag1=1;
}

        disable();
        outportb(IntCtrlAddr,0x48);
        outportb(MaskRegAddr,MaskReg);          // setup Mask Register
        enable();

        outportb(IntCtrlAddr,NonSpecEOI);
}
```

```
void interrupt switch_period(__CPPARGS)
{
        outportb(CTC1PWMCtrl,0x30);
        outportb(CTC1PWMD0,0);
        outportb(CTC1PWMD0,0);

int             thetaa, thetab, thetac, ang, x;
static int      count2=0, u=0, revflag=0, angle=144;
unsigned        char b;
static float    vd=150.0, reversvd=1/(vd), ek=60.0*mod2cnt, ik=0.0, ick=0.0, id=7.1,
                im=0.0, regulat=0.0, erorn=0.0;

        count2++;

        b=inportb(0x03fd);

if(zedet)
{
        if(!(inportb(PortPWMIO)&0x80))
        {
        /* read difference between ZX and switching period */
        x=zxdtofs+(zxdt=inportb(CTC1PWMB2)+(inportb(_DX)<<8));

                if((angle=angletrim-(zxdt/angle2cnt))<0)
                {
                angle+=anglemax;

        /* adjust switching period timer */
        outportb(CTC1PWMD1,(_AX=x));
        outportb(_DX,_AX);                      // output MSB
        rsttmr=1;                               // set flag
        zxdet=0;                                // reset flag
        /* set the timer to zero */
        outportb(CTC1PWMD2,0);
        outportb(_DX,0);
        ofsang=angle;
        revflag=0;
                }
        }
        /* restore switching period timer */
        else if(rsttmr)
        {
        outportb(CTC1PWMD1,(_AX=Tz));
        outportb(_DX,_AH);                      // outport most significant byte
        rsttmr=0;
        }

        /* calculate the turning-ON durations for each device */

if((ang=angle-dt)<0)
{
        ang+=anglemax;
}

calc_width(reversvd,ek,ik,ick,ang);

erorn=comparator(vd);

regulat=regulator(erorn);
```

```
amplitude(im,id,regulat,&ik,&ick);

        /* work out timing values to be programmed into timers */
if(revflag)
{
        thetaa=theta[Idev4];
        thetab=theta[Idev6];
        thetac=theta[Idev2];
        revflag=0;
}
else
{
        thetaa=theta[Idev1];
        thetab=theta[Idev3];
        thetac=theta[Idev5];
        reflag=1;
}

        /* check timing values to be within bound */
if(thetaa<mindt)
{
        thetaa=mindt;                    // if timing too small, set it to the minimum
}
else if(thetaa>maxdt)
{
        thetaa=maxdt;
}
if(thetab<mindt)
{
        thetab=mindt;
}
else if(thetab>maxdt)
{
        thetab=maxdt
}
if(thetac<mindt)
{
        thetac=mindt;
}
else if(thetac>maxdt)
{
        thetac=maxdt;
}

        /* write delta to timers */
        outportb(CTC0PWMD0,(_AX=thetaa));
        outportb(_DX,_AH);
        optportb(CTC0PWMD1,(_AX=thetab));
        outportb(_DX,_AH);
        outportb(CTC0PWMD2,(_AX=thetac));
        outportb(_DX,_AH);

/* increment the angle */
if((angle+=delta_angle)>=anglemax)
{
        angle=-anglemax;
}

        if(u==0)
        {
```

```
        outportb(CTC1PWMCtrl,0x00);
        t1=inportb(CTC1PWMD0);
        t2=inportb(_DX);
        printf("%x %x",(t2),(t1));
        u=1;
        }

        outportb(IntCtrlAddr,NonSpecEOI);
}

void interrupt ext_trig(__CPPARGS)
{
        unsigned b;
        b=inportb(0x03fd);

        /* routine to handle external interrupt */

        ++exttrigF;

        outportb(IntCtrlAddr,NonSpecEOI);
}

void init_scren(void)
{
        clrscr();
        gotoxy(18,8);
printf("WELCOME TO LABORATORY OF MOTOR CONTROL");
        gotoxy(12,10);
printf("DARPARTMENT OF ELECTRICAL AND ELECTRONIC ENGINEERING");
        gotoxy(16,11);
printf("VICTORIA UNIVERSITY OF TECHNOLOGY (VUT)");
        gotoxy(18,16);
printf("Three Phase Voltage Converter");
        delay(8000);
        clrscr();
}

voidb main(void)
{
        char    ch;
        int     test;

        init_scren();
        init_sin();
        init_var();
do
{
        do
        {
        printf("\n\nDo you want operation to completed?(Y/N)\n\n");
        ch=getch();
        if(ch=='N'||ch=='n')
                {
                disable();
                oldIRQ3=getvect(IntNoIRQ3);
                setvect(IntNoIRQ3,zero_crossing);
                oldIRQ4=getvect(IntNoIRQ4);
                setvect(IntNoIRQ4,switch_period);
                oldIRQ7=getvect(IntNoIRQ7);
                setvect(IntNoIRQ7,ext_trig);
```

```
                init_PWMB();
                enable();

        while(flag1==0){}
                test=0;
        }
        else if(ch=='Y'||ch=='y')
        {
        test=1;
        }
        else
        {
        test=2;
        }
        }
        while(test==2);
}
while(test==0);

disable();
        setvect(IntNoIRQ3,oldIRQ3);
        setvect(IntNoIRQ4,oldIRQ4);
        setvect(IntNoIRQ7,oldIRQ&);
        restore_PWMB();
enable();

return;

}
```

2. Analog-to-Digital Converter Routine

This analog-to-digital data acquisition acquires six readings from six channels. In this program, six readings are acquires from six input channels (channel 0 – channel 5). For these readings the following parameters are selected: based address of 300H, signal-ended analog input operation, straight binary data coding and a gain of 1.

```
#include<stdio.h>
#include<dos.h>
#include<conio.h>

#define addctl   0x300
#define addmul  0x301
#define addcon  0x302
#define addvul   0x303
#define chanl0   0x00
#define chanl1   0x01
#define chanl2   0x02
#define chanl3   0x03
#define chanl4   0x04
#define chanl5   0x05

main()
{
        clrscr();

        int conbine0, conbine1, conbine2, conbine3, conbine4, conbine5,
            statu0, statu1, statu2, statu3, statu4, statu5, gain, d, I, j;
        int e0[200], e1[200], e2[200], e3[200], e4[200], e5[200];

                gain=0x00;              //select gain code of 1

                conbine0=gain|chanl0;   // conbine gain code and channel selection
                conbine1=gain|chanl1;
                conbine2=gain|chanl2;
                conbine3=gain|chanl3;
                conbine4=gain|chanl4;
                conbine5=gain|chanl5;

        for(j=0;j<200;j++)
        {
                outportb(addmul,conbine0);      //set gain and channel number
                outportb(addcon,conbine0);      //start analog conversion
                d=0;
                while(d==0)                     //wait for analog conversion to be finished
                {
                        statu0=inportb(addctl);
                        d=statu0&0x40;
                }                               //read status and loop if not done
                e0[j]=inportb(addvul);          //point at ADC data and read data


                outportb(addmul,conbine1);      //set gain and channel number
                outportb(addcon,conbine1);      //start analog conversion
                d=0;
                while(d==0)
```

```
        {
                statu1=inportb(addctl);
                d=statu1&0x40
        }                                   //read status and loop if not done
        e1[j]=inport(addvul);               //point at ADC data and read data

        outportb(addmul,conbine2);          //set gain and channel number
        outportb(addcon,conbine2);          //start analog conversion
        d=0;
        while(d==0)
        {
                statu2=inportb(addctl);
                d=statu2&0x40;
        }                                   //read status and loop if not done
        e2[j]=inport(addvul);               //point at ADC data and read data

        outportb(addmul,conbine3);          //set gain and channel number
        outportb(addcon,conbine3);          //start analog conversion
        d=0;
        while(d==0)
        {
                statu3=inportb(addctl);
                d=statu3&0x40;
        }                                   //read status and loop if not done
        e3[j]=inport(addvul);               //point at ADC data and read data

        outportb(addmul,conbine4);          //set gain and channel number
        outportb(addcon,conbine4);          //start analog conversion
        d=0;
        while(d==0)
        {
                statu4=inportb(addctl);
                d=statu4&0x40;
        }                                   //read status and loop if not done
        e4[j]=inport(addvul);               //point at ADC data and read data

        outportb(addmul,conbine5);          //set gain and channel number
        outportb(addcon,conbine5);          //start analog conversion
        d=0;
        while(d==0)
        {
                statu5=inportb(addctl);
                d=statu5&0x40;
        }                                   //read status and loop if not done
        e5[j]=inport(addvul);               //point at ADC data and read data

    }
}
```

Appendix C

PUBLICATIONS

1. Ming Yu & Qin Jiang, "A Three-Phase predictive PWM AC/DC Converter with a DC Load Current Observer", Australiasian Universities Power Engineering Conference (AUPEC'96), held at the University of Melbourne, Australia, on 2nd to 4th Oct. 1996, Vol.3, pp.543-546.

2. Ming Yu. Ying Tan & Qin Jiang, "Robust Control of AC/DC Power Converters Using an H_∞ Controller", IEEE 2nd International Conference on Power Electronics Drives and Energy System for Industrial Growth (PEDES'98), held at Rendezvous Observation City Hotel, Perth, Western Australia, on 30th Nov. to 3rd Dec. 1998, Vol.1, pp.336-341.

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VOLUME 3

A Three-Phase Predictive PWM AC/DC Converter with a DC Load Current Observer

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Abstract

This paper presents a method of estimating the dc load current for the control of voltage-regulated PWM rectifiers, where the dc load current is used as a feed forward to improve the dynamic response of the dc voltage. This method is based on load disturbance modelling using state space method. The load current is determined from the estimation of the load disturbance. A full-order state observer is designed for this estimation. The results of a study of incorporating this observer into the predictive current control scheme are presented.

1. INTRODUCTION

Most conventional AC/DC converters consist of uncontrolled diodes resulting in high harmonic content in the input ac line current and an input power factor that is dependent on operating conditions. Moreover, conventional uncontrolled converters do not permit bidirectional power flow. The use of a Pulse-Width Modulation (PWM) ac to dc voltage source converter allows the realization of unity power factor on the ac side, the reduction of harmonic content, and reversible power flow. The schematic of a stand alone ac/dc voltage-regulated PWM converter is given in Fig.1. The dc load of the converter is modelled by a Thevenized equivalent circuit with a load resistance r_o and a voltage source e_L. The output dc voltage across the capacitor, v_d , should be constant. This is achieved by controlling the duty cycle of the switches so as to provide a current on the dc side of the system to compensate for the power lost in the external load and thus keep v_d constant.

The topic of the three-phase Pulse-Width modulated AC/DC converter has recently drawn much attention [1,2] due to new demands concerning line disturbances. Several control strategies have been proposed to control the PWM converters. The predicted current control with a fixed switching frequency (PCFF) is superior to the other for its fast dynamic response, a good switching pattern, and less complexity [1,2]. Fig.2 gives the block diagram of the PCFF control including the load feedforward, i_L . The principle of the PCFF proposed in [2] is summarized in the next section as the background of this study.

In practice the installation of a dc current sensor, such as a current transformer, may be inconvenient.

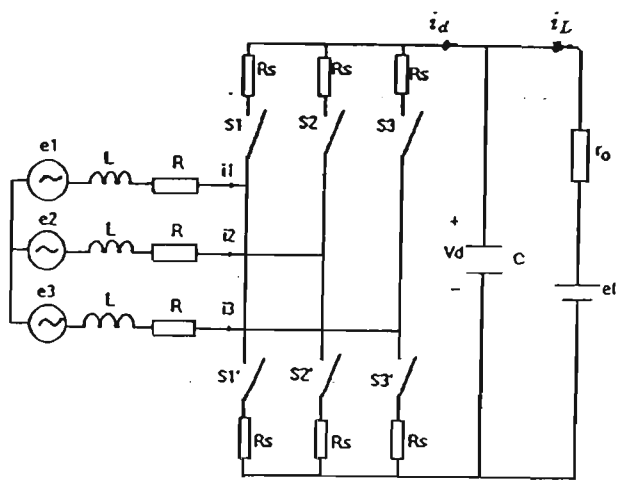

Figure 1: Schematic of an ac/dc PWM converter

The study of this paper intends to replace the dc current transformer with a load estimator using state space method. A full-order state observer is designed first to identify the load disturbance, which is then used to estimate the deviation of the dc load current. The method can be applied to any other ac/dc converter control where a dc current measurement is required.

The design method is described in section 3, and results are given in section 4.

2. THE PRINCIPLE OF PCFF CONTROL

2.1 The PCFF Control Law

The PCFF control proposed by Wu et al [2] is based on the circuit model of the converter. The 3-phase PWM converter as shown in Fig.1 can be represented by the equivalent circuit of Fig.3 [3]. Where the switch pairs act as a controlled current

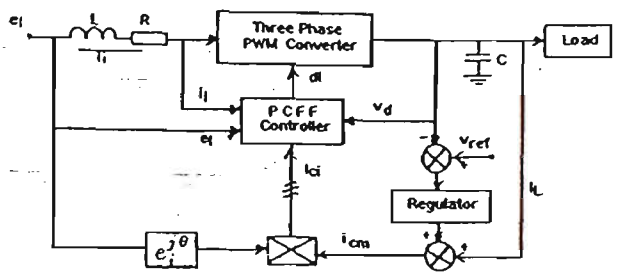

Figure 2: Block diagram of the PCFF control

source at the dc side. The ac terminals of the converter are equivalent to sinusoidal voltage sources v_{pi} , if the relatively small high-frequency harmonics of the switched waveform are neglected. e_i is the utility voltage, R is the line resistance, and L represents the transmission line inductance and the inductance of any input filter.

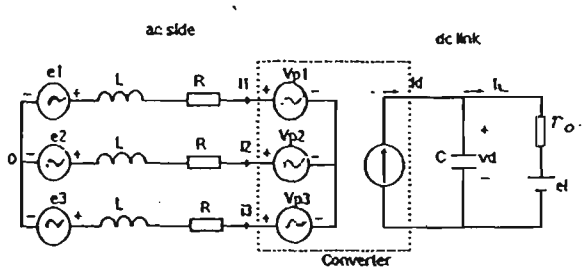

Figure 3: The equivalent circuit of the PWM converter

The single phase voltage equation on the ac side in Fig.3 is

$$e_i = L\frac{di_i}{dt} + Ri_i + v_{pi} \qquad i = 1, 2, \text{ or } 3 \quad (1)$$

If the duty ratio in one switching period is d_i , then v_{pi} can be expressed as [2]

$$v_{pi} = v_d\,(d_i - 1/2) \quad (2)$$

In the predicted current control scheme, the line current i_i is to change from its present value i_i to a command value i_{ci} within one switching period T_s , the required current change rate should be as follows:

$$\frac{di_i}{dt} = \frac{i_{ci} - i_i}{T_s} \quad (3)$$

The predicted current control law is therefore obtained by combining (1) - (3) together:

$$d_i = \frac{1}{v_d}[e_i - (R - \frac{L}{T_s})i_i - \frac{L}{T_s}i_{ci}] + \frac{1}{2} \quad (4)$$

If the duty ratio is produced by this equation, the line current would be forced to reach a "predicted" value at the end of a defined switching period.

2.2 Transfer Functions of PCFF

By applying circuit analysis to both the ac and dc side, and using the conservation of power, a set of nonlinear equations can be derived to describe the system in Fig.3 in a rotating frame of reference. In [2] the nonlinear equations are linearised about an operating point. By separating the dc component from the ac variation, both the steady-state dc model and small-signal ac model have been derived. Dynamics of the system can be described by the small signal ac model, whose state space representation is written as follows [2]:

$$\begin{aligned} Z\dot{x} &= Ax + Bu + Ed \\ y &= Cx \end{aligned} \quad (5)$$

where

$$\begin{aligned} x &= [\Delta i_f\ , \Delta i_b\ , \Delta v_d\ ]^T \\ y &= \Delta v_d \\ u &= \Delta i_{cm} \\ d &= [\Delta r_o\ , \Delta e_L\ , \Delta e_m\ , \Delta\omega\ ]^T \end{aligned}$$

Where Δi_f and Δi_b are the two-axis representation of line currents, Δr_o and Δe_L are load disturbances and Δe_m and $\Delta\omega$ are input disturbances. For the interest of this study as to estimate the load current i_L, the disturbance from the change of load resistance, Δr_o , alone is considered.

At the condition of the switching frequency, f_s , of the converter is much higher than the supply frequency (50 Hz), and that unity power factor is obtained, the PCFF control system can be reduced to a single-input and single-output system with transfer functions as follows:

$$\frac{\Delta v_{d1}(s)}{\Delta i_{cm}(s)} = K_{vi}\frac{(1 - s/\omega_o)}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})} \quad (6)$$

$$\frac{\Delta v_{d2}(s)}{\Delta r_o(s)} = \frac{K_{vr}}{1 + s/\omega_{p3}} \quad (7)$$

$$\Delta v_d = \Delta v_{d1} + \Delta v_{d2} \quad (8)$$

The system's output, v_d in this model is affected by the control Δi_{cm} as well as the load disturbance Δr_o . The expressions of K_{vi}, K_{vr}, ω_o, ω_{p1}, ω_{p2} and ω_{p3} can be found in [2], and depend on the parameters of the system.

By pole-zero cancellation, the 3rd-order system of equ.(5) is reduced to the 2nd-order transfer function of (6). This is considered as one of the advantages of the PCFF control strategy.

With parameters and operating point as given in [2], the numerical expression of (6-7) becomes

$$\frac{v_{d1}(s)}{i_{cm}(s)} = 11.2\frac{(1 - s/1400)}{(1 + s/3.46)(1 + s/3120)} \quad (9)$$

$$\frac{v_{d2}(s)}{r_o(s)} = \frac{8.175}{(s + 3.489)} \quad (10)$$

The discussion that follows will take the case study approach in which, the load current estimator is proposed and analysed based on the PCFF system model of (9) and (10).

3. ESTIMATION SCHEME FOR i_L

3.1 Mathematical Model of i_L

There are several methods of determining i_L . By applying Kirchhoff's Current Law to the left side of the capacitor of Fig.3, we have

$$i_L = i_d - C\frac{dv_d}{dt} \qquad (11)$$

where i_d is the terminal current of the converter at the dc side, and it can be determined by using the conservation of power

$$1.5 e_i\, i_i \approx i_d\, v_d \qquad (12)$$

e_i and i_i are directly measured in the PCFF control, so is v_d. However, in practice, the differentiation of a measured variable should be avoided due to the presence of high order harmonics.

Alternatively, i_L can also be determined from the right side of the capacitor of Fig.3 as

$$i_L = \frac{v_d - e_L}{R} \qquad (13)$$

Since

$$\begin{aligned} i_L &= I_L + \Delta i_L \\ v_d &= V_d + \Delta v_d \\ r_o &= R_o + \Delta r_o \end{aligned}$$

The first order Taylor series expansion of a function $f(x,y)$ around operating values $x = x_o, y = y_o$ is

$$f(x,y) \approx f(x_o,y_o) + \frac{\partial f}{\partial x}(x - x_o) + \frac{\partial f}{\partial y}(y - y_o)$$

Therefore, at the condition of zero deviation of e_L, (this assumption will not affect the generality of the following discussion) Δi_L becomes

$$\Delta i_L = \frac{1}{R_o}(\Delta v_d - I_L \Delta r_o / R_o) \qquad (14)$$

where Δv_d is directly measured. If the load disturbance Δr_o is known, then Δi_L can be determined from equ.(14).

3.2 Load Disturbance Modelling

In this study, an adaptive scheme to estimate Δr_o is proposed, where Δr_o is assumed step change in nature, then taking Δr_o as a state variable, x, which satisfies the state equation

$$dx/dt = 0 \qquad (15)$$

A newly defined disturbance model can be derived

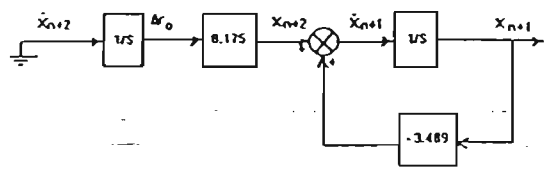

Figure 4: Modelling the load disturbance Δr_o

by incorporating (15) into the original disturbance model of (10). The block diagram of the new model is given in Fig.4, with its state space representation written as follows:

$$\begin{bmatrix} \dot{x}_{n+1} \\ \dot{x}_{n+2} \end{bmatrix} = \begin{bmatrix} -3.489 & 1 \\ 0 & 0 \end{bmatrix} \begin{bmatrix} x_{n+1} \\ x_{n+2} \end{bmatrix} \qquad (16)$$

$$y = [1 \quad 0]x \qquad (17)$$

where

$$\begin{aligned} x_{n+1} &= \Delta v_{d2} \\ x_{n+2} &= 8.175 \Delta r_o \end{aligned}$$

The state space representation of the transfer function (9) in the observable canonical form can be written as

$$\begin{bmatrix} \dot{x}_1 \\ \dot{x}_2 \end{bmatrix} = \begin{bmatrix} -3123.46 & 1 \\ -10795.2 & 0 \end{bmatrix} \begin{bmatrix} x_1 \\ x_2 \end{bmatrix} + \begin{bmatrix} -86.36 \\ 120904.0 \end{bmatrix} u \qquad (18)$$

$$y = [1 \quad 0]x \qquad (19)$$

where

$$\begin{aligned} y &= \Delta v_{d1} \\ u &= \Delta i_{cm} \end{aligned}$$

The state observer, which estimates Δr_o is therefore based on the system combining (16) and (18) as follows

$$\begin{aligned} \dot{\hat{x}} &= A\hat{x} + Bu + K_e\,(y - \hat{y}) \\ \text{or} \quad \dot{\hat{x}} &= (A - K_e\, C)\hat{x} + Bu + K_e\, y \end{aligned} \qquad (20)$$

where

$$A = \begin{bmatrix} -3.123.46 & 1 & 0 & 0 \\ -10795.2 & 0 & 0 & 0 \\ 0 & 0 & -3.489 & 1 \\ 0 & 0 & 0 & 0 \end{bmatrix} \quad B = \begin{bmatrix} -86.36 \\ 120904 \\ 0 \\ 0 \end{bmatrix} \qquad (21)$$

$$\begin{aligned} C &= [1 \quad 0 \; 1 \; 0] \\ \hat{x} &= [\Delta v_{d1}\,, x_2, \Delta v_{d2}\,, 8.175 \Delta r_o\,] \end{aligned}$$

Where $\hat{}$ indicates estimated values. K_e is the observer feedback gain matrix to be designed using the pole-placement method [4].

We propose the addition of this state observer to the original PCFF control in order to estimate the dc load current from load resistance disturbance. A block schematic of the complete control system is shown in Fig.5.

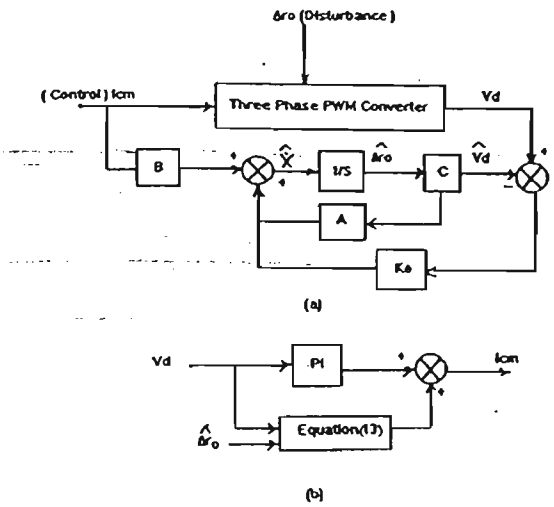

Figure 5: Block schematic of the state observer

From (20), the dynamic behavior of the estimation error, Δr_o - $\Delta \hat{r}_o$, is determined by the eigenvalue of (A-K_e C). As (A - K_e C) is a stable matrix, this difference will converge to zero for any initial error of Δr_o - $\Delta \hat{r}_o$. The speed of this convergence depends on the placement of desired poles, from which K_e can be determined using Ackermann's formula [4]. In principle, the placement of poles is arbitrary.

4. RESULTS

A small signal simulation for the control system of Fig.5 has been carried out under the MatLab computing environment. For desired poles placed at

$$-80 \pm j10, \quad -6 \pm j4$$

the feedback vector K_e is obtained using Ackermann's formula

$$K_e = [-3113.1, \quad -190753.9, \quad 58.2, \quad 4.8]^T$$

Simulation results for Δr_o , i_L and v_d are given in Fig. 6.

For the operating point at

$$V_d = 199 \text{ V}, \quad I_L = 4.74 \text{ A and } R_o = 42.1\Omega$$

a sudden change of the load resistance, $\Delta r_o = 5\Omega$ at $t = 0.1$ sec is applied.

Fig.6 (a) illustrates the load resistance step response with the estimated $\hat{r_o}$ against the real r_o . The estimated i_L compared with its real value is illustrated in Fig.6 (b). The transient response of v_d with the load current feedforward is given in Fig.6 (c).

It can be verified from these results that the proposed state observer follows the actual value of

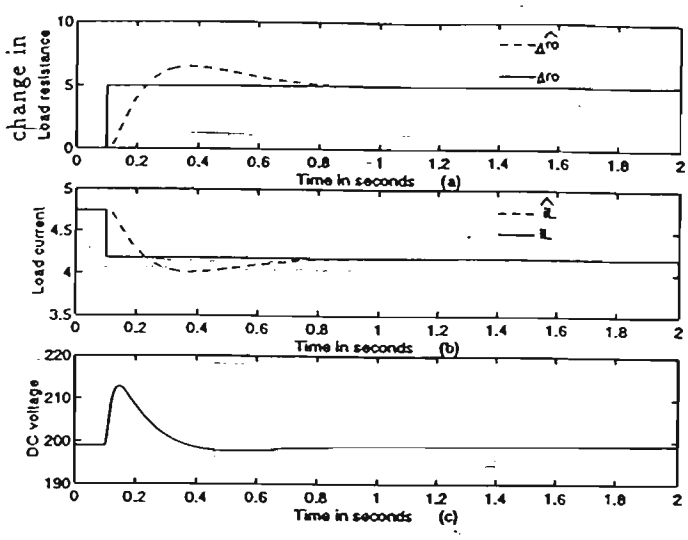

Figure 6: Simulation results

r_o in the transient states, and the PCFF control system works well without a dc current sensor.

5. CONCLUSION

This paper has presented a method for estimating the dc load current of a stand alone voltage-regulated PWM rectifier with PCFF control. The method is accomplished by modelling the load disturbance as a state variable, and then a state observer is designed using the pole-placement method. The deviation in the load current is therefore estimated accordingly. The proposed method can be applied to the PCFF scheme without a dc load current sensor. The validity of the load observer has been verified in simulation results.

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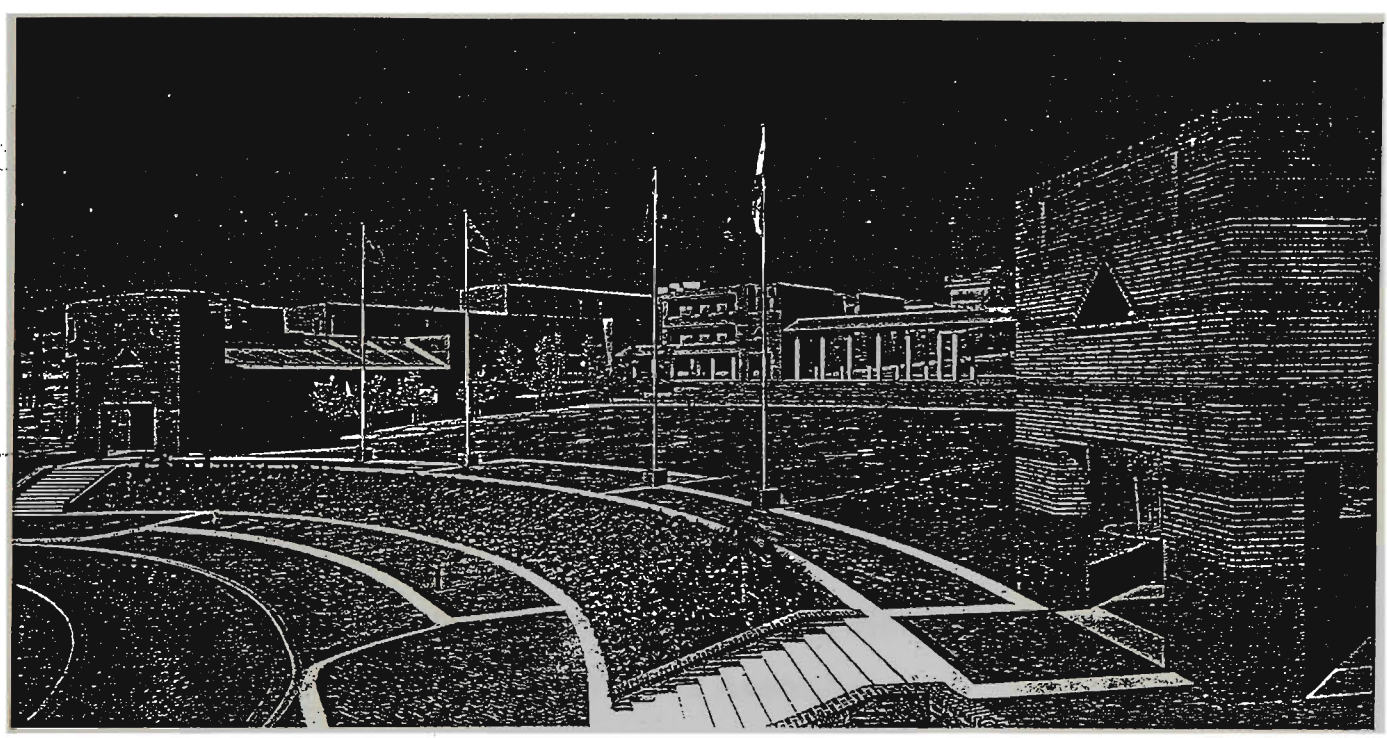

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Robust Control of ac/dc Power Converters Using an H∞ Controller

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Abstract

In this paper, an advanced H∞ controller is designed as a dc voltage regulator for a 3-phase ac/dc PWM voltage source converter, which is under a predictive current control with a fixed switching frequency (PCFF). The robust control offered by the H∞ controller is to deal with in particular system uncertainties, such as load change, sensor noise and variation of the system parameters, that directly degrades the performance of the PCFF scheme. The successful introduction of the H∞ control into the engineering application is demonstrated in this paper.

1. Introduction

The main control objective for a 3-phase PWM power converter as shown in Fig.1 is, in addition to a unit power factor and low harmonic distortion of line currents, to stabilize the system and to deliver an almost constant dc link voltage output when the system is subject to parameter variations and substantial load changes. Under the PCFF scheme, it offers combined advantages of other controllers including:

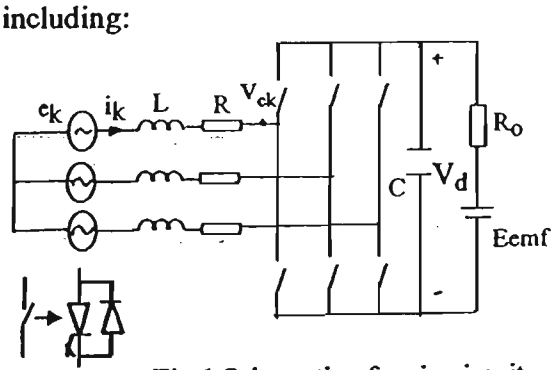

Fig.1 Schematic of main circuit

1. The calculation of the control law is simple as it directly deals with 3-phase quantities, no transformation of these quantities into a synchronous rotating frame is necessary;
2. Fast dynamic response (dead beat response);
3. The unity power factor can be obtained automatically;
4. A well defined switching pattern with a fixed switching frequency can be used in all load conditions.

However, such performance characteristics as stability and constant dc voltage output depend on the cooperation of a dc voltage regulator as shown in the system of Fig. 2. Where the output of the PCFF controller is the phase voltage commands, V_{ck}, to be synthesized by a PWM modulator. The PCFF control law is given in Eq.(1) below, in which the magnitude of the line current command, i_{ck}, denoted as i_{cm} in Fig.2, is determined by the sum of the voltage regulators' output, and the feedforward load current, I_{load}.

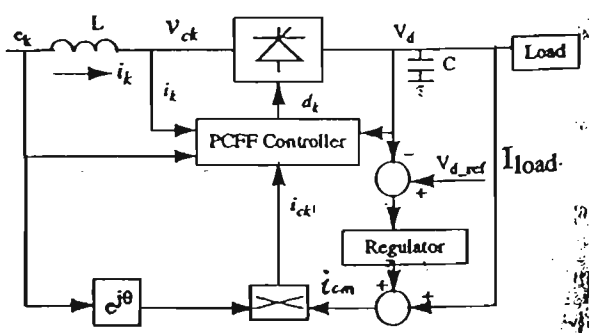

Fig.2 The block diagram of the PCFF controlled power converter

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$$v_{ck} = [e_k - (R - \frac{L}{T})i_k - \frac{L}{T} i_{ck}] \quad (1)$$

$$|i_{ck}| = (V_{ref} - V_d)K + I_{load} \quad (2)$$

$$k = 1,2,3$$

Referring to the system of Fig.1, R is line and device resistance; L is line inductance; e_k is utility power supply; i_k is line current; V_d and V_{ref} are dc link voltage and its reference; T is switching period and K is the voltage regulator.

It can be seen in Eq. (1) that PCFF control law directly depends on system parameters and feedback signals. While R and L have nominally fixed values in Eq.(1), they vary with load currents and surrounding temperature in a real system. Feedback signals are subject to sensor noise. The difference between a real system and its mathematical model is a source of uncertainty, which degrades the performance of the PCFF controlled system. The requirement of coping with uncertainty for the PCFF scheme is a robust control problem and can only be compensated by the dc voltage regulator, K.

In previous work, a conventional PI controller was used as the dc voltage regulator [1-3]. Although theoretically a conventional PI controller is comparable to any other controller for a single-input single-output system, it uses a trial and error design process and an optimal solution is not ready to be obtained. On the other hand, the H∞ theory has its unique approach to the uncertainty issue, its design method allows for both the robust stability and robust performance to be considered at the design stage. It optimizes the disturbance transfer matrix in such a way that the minimum gain is obtained. In this paper, the design procedure and outcome are presented. The simulation results using MatLab are also given.

2. Design of the H∞ controller

In order to design the dc voltage regulator, K, the PCFF controlled power converter is treated as one plant. Its transfer function from the current command, i_{ck}, to the dc link voltage output, V_d, is derived by linearizing the nonlinear and time variant system at a given operating point [1-2].

$$G_p(s) = k_{vi} \frac{(1 - s/\omega_o)}{(1 + s/\omega_{p1})(1 + s/\omega_{p2})} \quad (3)$$

Gp(s) represents a linear, time-invariant, single-input single-output system, where k_{vi}, ω_O, ω_{p1} and ω_{p2} are determined by the system parameters and the operating point. The assumption behind (3) is that the switching frequency, f_S, is much high than the supply frequency (50Hz), and a unity power factor is obtained. Now the system of Fig.2 can be re-organized as shown in Fig.3, where the controller, K, is to be designed, d represents disturbances, W is a weight function, the output z is the weighted error signal. Details of W will be given latter.

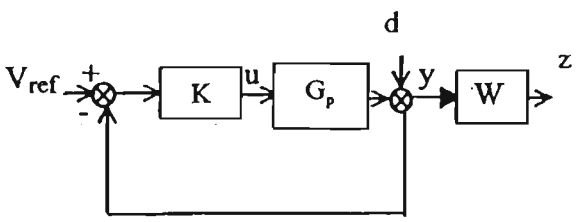

Fig.3 The re-organized control system

The tasks of the controller K are to stabilize the system and to minimize the effect of uncertainties such as parameter variations, sensor noises and change in load conditions. The problem of the design such a controller can be translated to the standard problem of H∞ control as illustrated in Fig.4 [8].

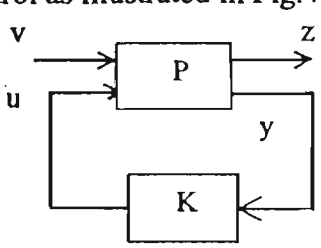

Fig.4 Standard configuration

Signals in Fig.4 are vectors, v is a generalized input vector which includes load disturbance, sensor noise and reference input. z is an output vector representing performance requirements. For example, it can be an error, a weighted control output and so on. Transfer matrices P and K represent plant and controller respectively. Here P is assumed to be real rational, and is defined as

$$P=\begin{bmatrix} p_{11} & p_{12} \\ p_{21} & p_{22} \end{bmatrix} \qquad (4)$$

So, the equations corresponding to the system of Fig.4 can be derived as follows:

$$\begin{aligned} z &= p_{11}v + p_{12}u \\ y &= p_{21}v + p_{22}u \qquad (5) \\ u &= Ky \end{aligned}$$

The transfer matrix from v to z, can be obtained from the last equation,

$$M(s) = p_{11} + p_{12}k(I - p_{22}k)^{-1}p_{21} \qquad (6)$$

where p_{22} is strictly proper and real rational.

The objective of H∞ design is to determine a proper and real rational controller K, which not only stabilize the plant but also minimize the H∞ norm of M(s). In other words, H∞ design is to solve the following optimal control problem:

$$\begin{aligned} &min \quad \| M \|_\infty \qquad (7) \\ &K \text{ stabilizing} \end{aligned}$$

This is called the standard problem in H∞ theory. In the design, weight functions are introduced to normalize M(s). The weight function expresses the relative importance of different frequencies (it is bigger for frequencies whose presence is more disturbing). By adjusting the weight function we can obtain better performance at frequencies concerned

$$M=\begin{bmatrix} W_1 S \\ W_2(I-S) \end{bmatrix} \qquad (8)$$

where, S and (I-S) are the sensitivity function and complementary sensitivity function respectively. W_1 and W_2 are weighted functions. S is defined as the transfer function from d to y in the system of Fig.3.

$$S= [I + G_p(s)K]^{-1} \qquad (9)$$

The system performance requirement is reflected from the transfer function, z/d, of Fig.3. In order to attenuate z as much as possible the performance specification is defined as

$$J=\|W_1 S\|_\infty \qquad (10)$$

The weighted sensitivity function in (10) represents the characteristic of disturbance attenuation for the system. W_1 attenuates the output due to the disturbance. When the weight function is adopted, the nominal value of the performance index can be taken as one. Based on this point, the norm performance specification is given as

$$\| W_1 S \|_\infty \leq 1 \qquad (11)$$

The robust stability is also included in the design of the controller. The robust stability means that the closed-loop system must remain stable for all possible perturbations, which result in discrepancy between real plant and its mathematical model. The robust stability condition obtained from the Nyquist criterion

$$\| W_2(I - S) \|_\infty \leq 1 \qquad (12)$$

It is noticed that conditions of the performance specification (11) and the robust stability (12) have a unified form under the H∞ norm. Thus the optimal design of the H∞ controller is

transformed to the H∞ optimal design by combining the two specifications in Eq. (13).

$$\min_{K \text{ stabilizing}} \left\| \begin{matrix} W_1 & S \\ W_2 & (I-S) \end{matrix} \right\|_\infty \quad (13)$$

The steps taken for the H∞ optimal design are summarized as follows [9-10]:

1. To define the weighted function W_2 according to the limitation elements;
2. To select an initial performance weighted function W_1;
3. To solve the following optimal problem for

$$\gamma := \min_{K \text{ stabilizing}} \left\| \begin{matrix} W_1 & S \\ W_2 & (I-S) \end{matrix} \right\|_\infty$$

$\gamma \approx 1$;

4. If $\gamma \geq 1+\varepsilon$, then to reshape the weighted function W_1 and go to step 3;
5. If $\gamma < 1$, then to increase the weighted function W_1 and go to step 3;
6. When γ approaches one, W_1 and W_2 can be used to calculated the H∞ controller, K.

3. Design of an H∞ controller for a Power Converter

As a design example, a prototype IGBT PWM power converter is used with parameters:

Supply phase voltage e_m = 44 volts;
Line inductance L = 2 mH;
Line resistance R = 1 Ω;
Load resistance R_O = 20 Ω;
dc link capacitor C = 100μF;
dc link voltage reference V_{ref} =100 volts;
Switching frequency f_{sw} = 1250 Hz;

The worst possible scenario taken into account in the design is the sudden change of the operation mode from rectifying to re-generation. That is, the system is first operated in a rectifying mode with a zero back EMF, E_{emf} (refer to the system of fig.1), the transfer function of the PCFF controlled power converter, $G_p(s)$, is obtained

$$G_p(s) = \frac{-375s + 4{,}500{,}000}{s^3 + 1350s^2 + 125{,}000} \quad (14)$$

Then an E_{emf} of 200 volts is suddenly applied, which forces the load current, I_{load}, to flow into the power converter, resulting in a re-generation mode. This disturbance also causes uncertainty problem as the transfer function, $G_p(s)$, experiences a significant change due to the shift of the operating point. Both robust stability and robust performance are required for the H∞ controller. By following preceding design steps, the performance weighted functions $W_1(s)$ and $W_2(s)$ are determined according to system uncertainties and bandwidth respectively.

$$W_2 = \frac{5(T_1 s + 1)}{(T_2 s + 1)} \quad (15)$$

$$W_1 = \frac{\rho(T_3 s + 1)(T_4 s + 1)}{(T_5 s + 1)(T_6 s + 1)} \quad (16)$$

where T_1= 1/300, T_2=1/20, T_3=100, T_4=1/30 T_5=1/800 and T_6= 1/2000. The Bode plot for W_1^{-1} and W_2^{-1} are show in Fig.5.

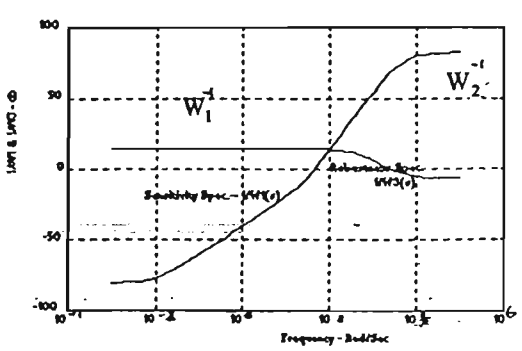

Fig.5 Bode plot of W_1^{-1} and W_2^{-1}

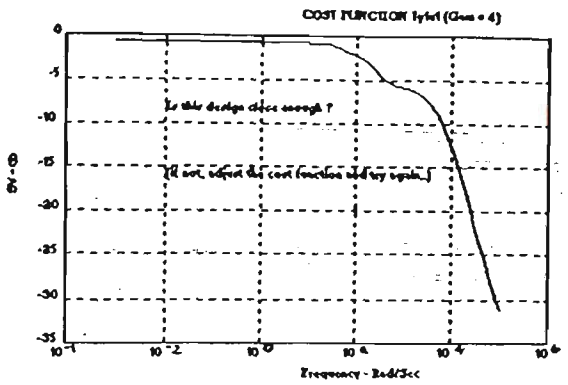

Fig.6 The cost function plot

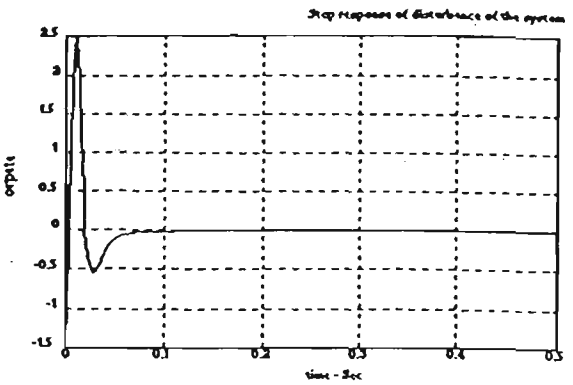

Fig.7 The disturbance response

In H∞ optimal design, ρ of Eq.(16) should be as large as possible to obtain the maximum attenuation of disturbance. H∞ optimal design is obtained at ρ=75, and K has its poles and zeros at:

Poles: -252.09, -10.00, -0.01, –1.80
Zeros: -538.86, -86.99, -215.06, –22.56

This raw controller is of 4th order, and can be approximate to a 3rd order one by simply ignoring the insignificant zero and pole at -252.09 and -538.86 respectively. Thus we have

$$K = \frac{(s+215)(s+87)(s+22.56)}{(s+10)(s+1.80)(s+0.01)} \quad (17)$$

4. Simulation Results

The cost function plot and step disturbance response of the dc link voltage, V_d, are shown in Fig.5 and Fig.6 respectively. The negative overshoot exhibits in Fig.6 is due to a non-minimum phase zero of $G_p(s)$, ie. a zero in the right half s plane (see Eq.(14)).

Fig.7 shows the transient responses of dc link voltage, V_d and current I_d, while Fig.8 gives the transient response of the line current, i_l compared with the utility voltage, e_l, when the power converter goes from rectifying to regenerating. It can be seen in Fig.8 that the 180^o phase change in the ac line current is completed within one cycle of power frequency, while the overshoot of V_d is less than 15%. This implies that the system has a very good dynamic response to large perturbations.

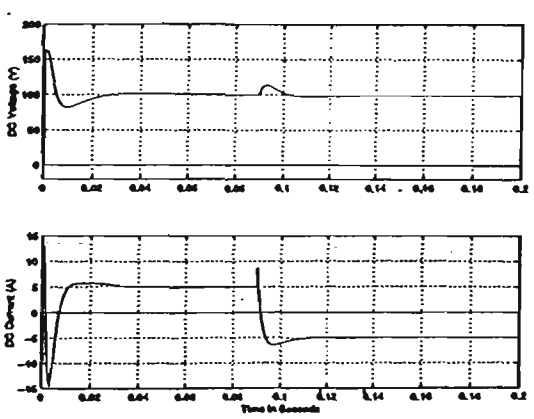

Fig.8 Waveforms of V_d and I_d

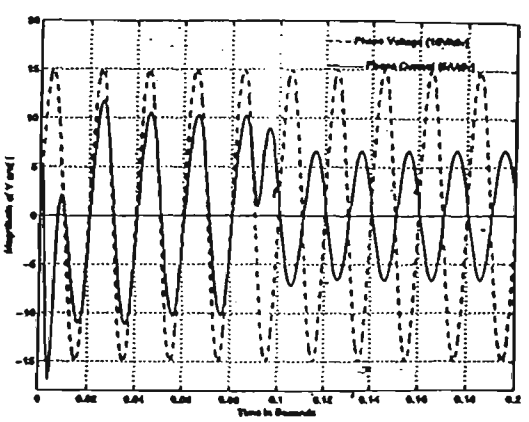

Fig.9 Waveforms of e_l and i_l

5. Conclusion

An H∞ optimal controller is proposed and validated by simulation results. The analytical design approach is given for the H∞ controller, where both the robust stability and robust performance is considered at the design stage. It has demonstrated that the H∞ optimal design has a great potential for engineering application. More advantages can be obtained if a plant to be controlled is a multi-input and multi-output system.

The order of the designed H∞ controller is three. When the order of the plant is high, we can use order reduction technique to get a low-order H∞ controller [11].

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