Implementation of the IEC61850 International Protocol for Accurate Fault Location in Overhead Transmission Lines

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*My work is dedicated to my father **Rade Stojcevski**, mother **Vera Stojcevska** and siblings **Aleksandar** and **Filip Stojcevski**. Their constant encouragement, guidance and support has shaped the type of person I have become, both academically and socially.*

*A heartfelt appreciation also goes out to my godparents **Slobodan Anastasovski** and **Nikolina Anastasovska**, along with their children **Vele** and **Steven Anastasovski**. Their relentless enthusiasm and faith throughout my lifetime has allowed me to see the world in a different light, for all its beauty and essence.*

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Declaration of Originality

I declare, that to the best of my knowledge, the research described herein is the result of my own work, except where otherwise stated in the text. It is submitted in fulfilment of the candidature for the degree of Doctor of Philosophy in Engineering at Victoria University, Melbourne, Australia. No part of this work has been submitted for any other degree.

I too, hereby give consent, for a copy of this thesis to be deposited in the Victoria University library, being made available for loan and photocopying, subject to the provisions of the Copyright Act 1968. This thesis is no longer than 100,000 words exclusive of appendices, bibliography, figures and tables.

Blagojce Stojcevski
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List of Abbreviations

AC	Alternating Current
ACSI	Abstract Communication Service Interface
ATL	Artificial Transmission Line
BOOTP	Bootstrap Protocol
BPDU	Bridge Protocol Data Unit
CB	Circuit Breaker
CDC	Common Data Class
CID	Configured IED Description
COMTRADE	Common Format for Transient Data Exchange
CT	Current Transformer
CTR	Current Transformer Ratio
CVT	Capacitor Voltage Transformer
DC	Direct Current
DDB	Digital Data Bus
DFT	Discrete Fourier Transformation
DHCP	Dynamic Host Configuration Protocol
DMS	Distribution Management Systems
DNP	Distributed Network Protocol
EMI	Electromagnetic Induction
EMS	Energy Management Systems
EPRI	Electric Power Research Institute
FACTS	Flexible AC Transmission System

FLA	Fault Locator Algorithm
FTP	File Transfer Protocol
GOOSE	Generic Object Oriented Substation Event
GPS	Global Positioning System
GSSE	Generic Substation State Event
GVRP	Generic VLAN Registration Protocol
HMI	Human Machine Interface
I&C	Instrumentation and Control
ICD	IED Capability Description
IEC	International Engineering Consortium
IEC TC	International Electrotechnical Commission Technical Committee
IEC61850	Substation Communication Protocol for Interoperability of IEDs
IED	Intelligent Electronic Device
IEEE	Institute of Electrical and Electronic Engineers
IP	Internet Protocol
ISO	International Standards Organisation
IUG	International Users Group
LAN	Local Area Network
LCD	Liquid-Crystal Display
LED	Light-Emitting Diode
LFI	Link Fault Indicator
LN	Logical Node
MMS	Manufacturing Message Specification
NCC	National Control Centre
OHS	Occupational, Health and Safety
OSI	Open Systems Interconnection
PLC	Programmable Logic Controller
PSL	Programmable Scheme Logic
PSM	Plug Setting Multiplier
PTR	Potential Transformer Ratio
PVID	Port VLAN Identifier
RCC	Regional Control Centre

RCC	Reinforced Concrete Cement
RMS	Root Mean Square
RTD	Resistance Thermal Detector
RTU	Remote Terminal Unit
SAS	Substation Automation System
SCADA	Supervisory Control and Data Acquisition
SCC	Substation Control Centre
SCD	Substation Configuration Description
SCL	Substation Configuration Language
SCSM	Specific Communication Service Mapping
SFP	Small Factor Pluggable
SM	Single Mode
SMS	Short Message Service
SMV	Sampled Measured Value
SSL	Secure Socket Layer
TCP	Transmission Control Protocol
TMS	Time Multiplier Setting
TNC	Threaded Neill-Concelman connector
UCA	Utility Communications Architecture
UDP	User Datagram Protocol
URL	Uniform Resource Locator
VAR	Voltage Ampere Reactive Controller
VLAN	Virtual LAN
VT	Voltage Transformer
WAN	Wide Area Network
XML	Extensible Markup Language

List of Publications

Journal Publications

[1] B. Stojcevski, A. Kalam, "Fault Location in Overhead Power Lines using the IEC61850 International Protocol", Accepted for publication in the International Review on Modelling and Simulations, IREMOS Journal, Vol. 3, No. 5, pp. 888-899, 2010.

[2] B. Stojcevski, N. Asyik Hidayatullah, A. Kalam, "Analysis of Distributed Generation Systems, Smart Grid Technologies and Future Motivators Influencing Change in the Electricity Sector", Accepted for publication in the Smart Grid and Renewable Energy, SGRE Journal, Vol. 2, No. 3, pp. 216-229, 2011.

Conference Publications

[1] B. Stojcevski, A. Kalam, "Laboratory Upgrades for the Next Generation Power Utility", Proceeding of the Central Board of Irrigation and Power, 5th International Conference on Power Systems Protection and Automation, PSPA'10, New Delhi, India, pp. 216-226, 2010.

[2] B. Stojcevski, A. Kalam, "IEC61850 Portable Testing Unit Capable of Multi-Vendor Interoperability", Proceeding of the Australian National Committee of CIGRE and the B5 Protection and Automation Panel, South East Asia Protection and Automation Conference, SEAPAC'11, Sydney, Australia, pp. 1-13, 2011.

[3] B. Stojcevski, A. Kalam, "Acceptance Testing, Conformance & Quality Assurance of IEC61850 Devices", Proceeding of the Australian Protection Symposium, APS'11, Sydney, Australia, pp. 59-64, 2011.

Abstract

The rapid growth of electric power systems has resulted in many utility companies increasing the investment of Substation Automation Systems (SAS). Free marketing, deregulation and competition has brought about greater restrictive requirements to produce reliable, continuous and good-quality power supply, without a significant increase in the cost of delivery. For this reason, engineers ever since the development of the earliest microprocessor based Intelligent Electronic Devices (IEDs), have depended on digital superiority to assist personnel in the precise location of faults. The ability of these IEDs to generate an abundance of valuable network data through information exchange of relays, permits power authorities to capitalise in areas such as control, protection, monitoring, fault recording and communication. These Instrumentation and Control (I&C) devices facilitate on-site personnel to accurately establish the fault distance of a transmission line and repair any damage at reduced outage times using Supervisory Control and Data Acquisition (SCADA).

However, the system inherent problem endured by the earlier IED models was the fact that the serial bus communication caused a dilemma in the overall response times of the data. This was greatly attributable to the profusion of copper wiring and the lack of compatibility between vendor specific IEDs. To contend with these concerns, a variety of standardised communication paradigms and international protocols were introduced. These incremental additions to the existing substation framework lead to the reduction of copper wiring through the use of fibre optic technologies and interoperability between different vendor specific IEDs via the use of Generic Object Oriented Substation Event (GOOSE) messaging. The majority of

in-service substation protocols are still based on MODBUS and DNP3 standards. These standards however are slowly becoming replaced by Ethernet and fibre optic technologies in the form of the IEC61850 protocol.

This thesis contributes to knowledge in two parts. Part I attempts to construct a portable IEC61850 testing unit capable of achieving interoperability between three different vendors including ABB, Areva and SEL. The IEC61850 testing unit is built to serve as a replica of a real-life in-service substation. The rig is equipped with copper, fibre and Ethernet capabilities in order to set and capture GOOSE messages in the form of ICD, CID, SCL and SCD files using logical nodes. Part II of the research develops an innovative fault locator algorithm to determine the distance to fault error in overhead transmission lines. The algorithm is derived using Discrete Fourier Transformation (DFT) and uses a square wave arc model to determine the fault distance, arc resistance, total fault resistance and tower footing resistance. The algorithm is simulated and tested using the portable IEC61850 testing unit and a 300km Artificial Transmission Line (ATL).

Chapter 1 – Thesis Overview

1.1 Introduction

The International Electrotechnical Commission (IEC) Technical Committee (TC) 57 was established in 1964 because of an urgent need to produce international standards in the field of communications for electrical utilities. The IEC considered not only equipment aspects, but to a greater extent system parameters. This scope was modified to prepare standards for Supervisory Control and Data Acquisition (SCADA), Energy Management Systems (EMS), Distribution Management Systems (DMS), distributed automation, teleprotection and associated communications [1].

Following a similar pathway, the Electric Power Research Institute (EPRI) founded in 1973 was working towards drafting proposals for the implementation of protocols, interfaces and data models. EPRI recognised the potential benefit of a unified scheme of data communication for all operating purposes across the entire utility enterprise. In 1980, EPRI commissioned the Utility Communications Architecture (UCA) project which identified the overall structures, requirements, technologies and layers to implement such a scheme. It focused on the ease of combining a broad range of devices and systems; and the sharing of management and control information [1,2].

By 1994, EPRI had combined substation control equipment and power apparatuses into the UCA scheme. EPRI launched Research Project 3599 to define, demonstrate and endorse an industry wide UCA compatible communications approach for the

integration of substation IEDs [1,2]. The objective was to avoid expensive marketplace shakeout of incompatible systems.

Many utilities and IED manufacturers took an immediate interest in the UCA work and joined in the efforts to produce a communications network stack. The forward-looking approach was intended to define the technical requirements for a system to control and monitor substations large and small [2]. The specifications include requirements for fast messaging among peer IEDs to achieve fault-related control over data communication systems. The objective was to use the substation Local Area Network (LAN) messaging to replace the mass of dedicated copper wiring between IEDs.

Another feature of the approach was to identify communication system layers which may have already existed in widespread use. This allowed EPRI researchers to buy commonly used hardware and software components for substation control. For lower layers of the system, the researchers looked at a variety of industrial field bus solutions, as well as office-LAN technologies like Ethernet and Internet Protocol (IP) [2]. These were not suited for fast substation control, but had the advantage of global usage to support a rich array of affordable system components that could be implemented within substations.

After detailed study by EPRI, a group of prominent utilities lead by the American Electric Power (AEP) company forged ahead in a proposal to decide on specific layers. These users were developing projects to equip substations with the most modern LAN-based and standardised control schemes and pushed ahead to demonstrate a working result [2]. The objective was to define a standard which could achieve interoperability and use fibre optic cable.

The call for an international standard intensified as different vendors introduced proprietary solutions into the market. Many manufacturers had already developed versions of integrated LAN-based systems. At the request of the users, several European suppliers worked together with the International Electrotechnical Commission (IEC) to create the communications standard IEC60870-5 . Subsections of IEC61870-5 provided for basic information transfer and control between one vendor relay and the overall system of another vendor [2]. The markets where these manufactures

sold their products tended to support more expensive, futuristic systems as part of a major project.

In 1995, the IEC commissioned a new project identified as IEC61850, to define the next generation of standardised high-speed substation control, protection and monitoring communications. The main objective was to have utilities and vendors collaborating with each other to develop the framework of the standard. The EPRI UCA 2.0 and IEC61850 joint task forces worked on the interoperability between station, bay and process levels [2].

In October 1997, the Edinburgh TC57 Working Groups 10-12 meeting concluded that a single communications standard for Substation Automation Systems (SAS) will be bound for the world market [2,10]. The IEC61850 was officially launched after careful planning and development in the year 2004. Major UCA models, data types and services were incorporated into the final standard.

During this struggle for standardisation, MODBUS and DNP3 became the de facto standards across all substations worldwide. While MODBUS and DNP3 are successful in providing standard-based intercommunications between station computers, Remote Terminal Units (RTUs) and Intelligent Electronic Devices (IEDs); modern technology has surpassed the networking capabilities these standards were originally designed for. MODBUS and DNP3 are classed as tag-based protocols, where users access data by specifying a tag number [3]. IEC61850 presents a common naming convention which removes the mapping processes of unknown tags and allocates them into specific power system functions. From a SCADA perspective, the IEC61850 is a true, high-speed, robust and interoperable protocol [3].

However, electrical utilities are conservative by nature and driven by budgets. This has lead to the slow migration of the standard into substations. Due to these limitations, the mainstream of engineers have either never or only vaguely been exposed to the intricacies of the IEC61850 standard. Those who have had some experience, usually are forced to learn 'on the job'. This restricts utilities to administer their networks using traditional copper-wired approaches, even though alternative, and far more cost-effective Ethernet and fibre optic technologies in the form of the IEC61850 protocol are available. Regardless, it is inevitable that when a new standard is adopted as part of

a utilities business practice, it takes time to implement. Migration can take years and forecasts in Australia anticipate a mass transformation within the next 10-25 years [4]. Alongside this transformation, is the importance of IEC61850 IEDs to be capable of detecting faults on the network. IEDs assist in prioritising restoration efforts based on the number of customers affected and the severity of the outage. When a fault is apparent, the utility dispatches a crew to find the site of the problem. If the utility has SCADA capability, it may have an approximate estimation of the fault location, but not the type of component that has been damaged.

In Australia, 70% of outages are believed to be attributed by overhead transmission lines, while 30% are by underground networks. The average duration for an overhead fault to be restored is 50-55 minutes, while an underground fault is approximately 65-70 minutes [4]. If faults are dealt with in good time, the Commonwealth, State and Territory Governments in accordance with the Australian Energy Market Agreement (AEMA) 2004 are obliged to pay cash incentives to electrical utilities, and vice versa if restoration is belated during periods of peak load [5].

Having acknowledged these difficulties the spotlight is seemingly in the path of developing new algorithms that can accurately establish the fault location of countless real-life fault scenarios. Although several algorithms have previously been derived, none take advantage of the new IEC61850 international protocol or emphasise on the phenomenon of arcing when related to stochastic factors such as the arc resistance, fault resistance and tower footing resistance in overhead transmission lines.

1.2 Objectives

The objectives of this research are summarised as follows:

- Review the specifications of the IEC61850 protocol;
- Implement devices that are test conformant, interoperable and match performance requirements;
- Design, assemble and wire a portable IEC61850 testing unit comprising of four IEDs, two Ethernet switches and a GPS clock. All wiring connections must comply with the AS/NZS 3000 Wiring Regulations;
- Prepare a virtual wiring map to indicate which GOOSE messages will publish and subscribe to the IEDs;

- Individually configure all IEDs using relay specific software packages to obtain SCL files, either in ICD or CID format;
- Export the CID files using OMICRON's CMC356 test set to obtain overall system configurations and interoperability between the relays;
- Review different types of fault locator algorithms based on arcing;
- Develop an unsymmetrical single phase-to-ground fault locator algorithm for overhead transmission lines capable of estimating the fault distance, arc resistance, total fault resistance and tower footing resistance;
- Simulate the positive, negative and zero sequence components;
- Practically test the validity of the algorithm using both the portable IEC61850 testing unit and the 300km Artificial Transmission Line.

1.3 Methodologies and Techniques

The design, communication, derivation and testing aspects of certain project deliverables was executed through both hardware and software implementation. The use of high level automation tools such as AcSELerator Quickset, MiCOM S1 Studio, PCM600 Engineering Pro and IEDScout was employed on account of their ability to support the IEC61850 protocol and cater for all protection IEDs and bay control units. On the other hand, OMICRON's Test Universe software was specifically used towards the simulation and testing of the proposed algorithm and verification of fault properties.

The details of the proposed methodology and techniques to achieve the requirements of the PhD research are as follows:

- *Hardware Assembly:* Unlike conventional hard-wired approaches, the newly developed IEC61850 protocol replaces a large number of parallel copper wires with merely a few serial links by employing the use of Ethernet and fibre optic technologies. This mode of peer-to-peer communication aims to reduce the overall maintenance costs associated with projects via utilisation of asset management capabilities.

  The task of practically wiring different vendor specific IEDs to achieve information exchange between substation automation equipment was carried out. The IEDs

and peripherals used include the SEL-311L Line Current Differential Protection and Automation Relay, SEL-487E Transformer Differential Relay, P145 Feeder Management Relay, REF615 Feeder Protection and Control Relay, SEL-2407 Satellite-Synchronised Clock, SEL-2725 Unmanaged Ethernet Switch and a Ruggedcom RSG2200 9-Port Managed Gigabit Ethernet Backbone Switch.

In addition to this task, the manufacture and mounting of a secure portable IEC61850 testing unit to house all substation automation devices and loose wiring was engineered abiding modern Occupational, Health & Safety (OHS) guidelines.

- *GOOSE Interoperability:* Having satisfactorily completed the practical wiring of the vendor specific IEDs, the project focuses on accomplishing interoperability between relays using the IEC61850 entity of Generic Object Oriented Substation Event (GOOSE) messaging. The main concern with this particular task is that IEDs from different manufacturers are difficult to configure due to the fact that each manufacturer uses their own proprietary tools.

  The objective was to modify the existing ICD files of the various IEDs using a XML-based language or independent IEC61850 System Configurator. The ICD files were imported into relay specific IED configuration tools and the GOOSE messages were programmed by specifying the sender and receiver of the messages. At the end of the entire description process the GOOSE messages are stored in a SCD file. Each of the proprietary tools were then able to import the SCD files and extract the information needed for the necessary IEDs. OMICRON's CMC356 test set was used to create test templates for the IEDs and inject current and voltage signals.

- *Algorithm Derivation:* The major benefit of being able to detect the fault location within a high degree of precision comes as operating personnel can narrow their search for possible damages on the transmission line and restore power to customers at lower outage times. For this reason, the project concentrates on developing an innovative algorithm for accurate fault location in overhead transmission lines. More specifically the proposed algorithm draws attention to the application of unsymmetrical single phase-to-ground faults by deriving the fault

distance, arc resistance, total fault resistance and tower footing resistance on overhead transmission lines. The algorithm is derived for line lengths between 0-100km (short lines) and 100-300km (medium and long lines). Shunt capacitances are neglected for short lines and added for long lines.

- *Testing & Results:* Immediately following the derivation of the algorithm, a series of physical and computer simulated tests was performed in order to check the validity of the proposed algorithm. The exercise involves connecting a 300km Artificial Transmission Line (ATL) to the portable IEC61850 testing unit and simulating a range of fault waveforms. The CMC356 test set was used alongside the IED to register a variety of signals that can be visualised on a computer. The registered data was compared to the algorithm derivations of the fault distance. If the estimations are identical the algorithm is justifiable.

1.4 Originality of the Thesis

The research contributes to knowledge by implementing the IEC61850 protocol to meet the requirements of interoperability between vendor specific IEDs. Prior to the standardisation of the IEC61850, different vendor IEDs were virtually impossible to communicate with one another. This came as manufacturers deliberately designed their products using their own proprietary tools, meaning customers had to favour one vendor more than another. For this reason, manufacturers built their products in such a way that if one piece of equipment failed, then all or some accompanying devices required replacement. This is a major downfall for all substations seeing as a great deal of auxiliary equipment needs to be stockpiled.

Moreover, the study contributes to the development of an innovative fault locator algorithm aimed at improving the accuracy, economics and reliability of overhead transmission lines. The size and sophistication of power systems has increased the failure to locate faults, therefore heightened the importance of fault location. When a fault occurs on a line, it is crucial for the fault location to be identified as accurately as possible, allowing the damage caused by the disturbance to be repaired quickly before the line is put back into service. If the fault is not identified, it may cause prolonged outages during periods of peak load. An outline of the major contributions to knowledge is discussed as follows:

(1) Adopt and promote the IEC61850 protocol as opposed to other substation protocols like DNP and MODBUS by developing and wiring a multi-vendor portable IEC61850 testing unit. The original design of the rig employs a combination of copper and fibre optic technologies that assist in the reduction of operational costs and complexity when compared to conventional stationary protection panels. The rig has immense future potential for the education and training of industrial personnel given that it is compact in size and manoeuvrable.

(2) Programming GOOSE messages to accomplish interoperability between four IEDs each of which come from three different vendors (ABB, Areva and SEL) by implementing object modelling technologies such as logical nodes and common data classes. This is of great importance for substation environments for the reason that most in service communication protocols are outdated.

(3) Establishing a new fault locator algorithm used for unsymmetrical single phase-to-ground faults in overhead transmission lines. The algorithm differs from conventional methods that only establish the fault distance, by determining the arc resistance, fault resistance and tower footing resistance. This is confirmed by a number of automated and practical tests using the 300km Artificial Transmission Line.

1.5 Organisation

The thesis comprises of seven chapters and is organised as follows:

- *Chapter 1:* covers a brief introduction of the key objectives, motivations and methodologies of the research, while providing insight into the original contributions of knowledge the study has in the discipline of electrical engineering.
- *Chapter 2:* presents a comprehensive literature review exploring core aspects of Substation Automation Systems (SAS) and conventional Fault Locator Algorithms (FLA). Part I highlights network architectures, functions, protocols and middlewares with particular significance given to the IEC61850 protocol. Part II addresses several types of fault locator algorithms used for the analysis of distance to fault calculations. The algorithms are derived from frequency, time and high impedance domains.

- *Chapter 3:* provides all AC and D C wiring schematics developed for the practical assembly of the portable IEC61850 testing unit. A detailed description of all IEDs, Ethernet switches and a GPS clock is discussed.
- *Chapter 4:* demonstrates the individual and overall system configurations of GOOSE messages using relay specific configuration tools. A virtual wiring map, flow chart and mapping matrix outlining the configuration processes of the publisher and subscriber to create, test and set IEDs is stressed through CID, ICD, SCD and SCL files. Technical issues are also examined during commissioning and interoperability of the rig.
- *Chapter 5:* investigates common types of unsymmetrical faults transpiring on overhead transmission lines including phase-to-ground, phase-to-phase and three-phase faults. A range of design and construction aspects with and without ground are considered including conductor materials, line supports, insulators, string efficiency, corona, sag calculations and arcing. An innovative fault locator algorithm is derived using arcing to determine the fault distance, arc resistance, total fault resistance and tower footing resistance.
- *Chapter 6:* validates the accuracy of the algorithm by means of simulated and practical tests incorporating the portable IEC61850 testing unit and 300km Artificial Transmission Line. The CMC356 test set is configured together with the CT and VT settings of the SEL-311L in order to generate fault recordings. Magnetic couplers are attached across the A-B-C-N phases of the line at a distance of 75km apart. These segments operate as the zones of protection required to plot the R-X planes of the IEDs. The trip time, reach, distance to fault accuracy and harmonics are all analysed.
- *Chapter 7:* summaries the conclusions and future recommendations of the research.

Chapter 2 – Literature Review

2.1 Introduction

The purpose of this chapter is to provide a background knowledge of the IEC61850 protocol by exploring core aspects of Substation Automation Systems fundamental to the interoperability efforts of IEDs. The chapter makes a distinction between several types of fault locator algorithms derived from frequency, time and high impedance domains in order to establish a distance to fault error in overhead transmission lines.

PART I

2.2 Substation Automation Systems

Modern power networks rely on the mainstream of electricity to be produced via strongly built centralised power stations that are connected to an abundance of unified transmission networks [6]. The electricity generated from these power stations is transmitted and distributed solitarily in one direction across far-reaching zones until reaching the consumer end of the supply. The electricity produced employs the use of traditional paradigms such as combustion turbines, diesel, fossil fuels and rotating machinery [6].

However, with current developments arising from matters relating to climate change, escalating energy prices and energy security, the power systems network is gradually being transformed into a decentralised power systems architecture. This allows multi-directional flow of electricity by way of small distributed energy generation units. The generation units are located either near the utility system or at an isolated site

disconnected from the power grid [6]. They incorporate the use of renewable energy technologies such as biomass, solar and wind, but also Combined Heat and Power (CHP) technologies.

Irrespective of the type of power systems architecture or energy source being utilised, it is the obligation of Substation Automation Systems to control, monitor and protect the numerous primary and secondary switchgear equipment located within these power stations. The way in which this is achieved is through the use of Supervisory Control and Data Acquisition (SCADA), which monitors the status of all connections across the entire network and gathers functional data from installed equipment [3,6]. The data gathered can be anything in the context of basic voltage or current readings, right the way through to the most difficult fault recording or phase displacement characteristics. The data is processed through scores of inter-linked station computers, all of which administer the latest asset management capabilities.

2.2.1 Hierarchy

The supervisory tasks of SCADA flow through a hierarchy of control levels before data can effectively be communicated between station level computers. These control levels, in order of highest to lowest priority, consist of the National Control Centre (NCC), Regional Control Centre (RCC) and Substation Control Centre (SCC) [7]. The Substation Control Centre is divided into a further three core levels comprising of a station, bay and process [7]. The local and remote operators situated amongst these control centres have authority to mutually accept or decline any requests from personnel at lower control levels. Figure 2.1, illustrates the Substation Automation hierarchy.

2.2.1.1 Station level

The station level is used for the archiving, automation, data storage and management of countless bay level devices through the use of dedicated software tools. The hardware necessary to carry out such tasks is sheltered in a separate room away from all switchgear equipment [7]. The room comprises of countless HMI computers, printers, modems, GPS receivers and Ethernet switches. The large storage capacity provided by these peripherals allows significant amounts of data files to be stored in real-time databases. These databases are continuously updated through station

level modems, which act as a communications gateway to the Network Control Centre (NCC). The modems require physical coupling of Wide Area Networks (WAN), but also demand the presence of protocol converters capable of decoding incoming software commands [7]. Such protocol converters are integrated within modern HMI computers.

2.2.1.2 Bay level

The bay level connects a wide range of control and protection IEDs using station level Ethernet switches. The serial connection of these devices isolates various substation objects such as lines and transformers from the rest of the substation. These digitally manufactured IEDs have inbuilt LCD screens, push buttons and LEDs for the indication of measured voltage and current values [7]. Their popularity in recent times has seen them replace a wide range of electromechanical components as a result of their price, flexibility and functionality. Depending on the communication commands received from the station level, these IEDs are capable of performing functions such as bay control, bay protection, bay monitoring and fault recording [7]. All bay level automation systems are housed in stand-alone kiosks, away from primary and secondary switchgear equipment [7].

2.2.1.3 Process level

The process level similarly interlinks all primary and s econdary switchgear equipment, together with the substation automation systems located in the bay level kiosks. A large quantity of serial communication links are essential to carry out such manipulation, especially when connecting countless number of actuators, sensors, Current Transformers (CTs), Voltage Transformers (VTs) and Resistance Thermal Detectors (RTDs) [7]. The use of equipment that utilises both input and output (I/O) terminals is a clever way to reduce hardwiring in the process level.

2.2.1.4 Enterprise level

The enterprise level is a generic stage for all clients or third-party users that require data from the station level or bay level devices either interior or exterior to the substation [7]. The third-party users must obtain company authorisation before being allowed access to confidential records, for fear that a cyber-attack could immobilise systems. Consequently, strict guidelines and security checks must be obeyed at all times.

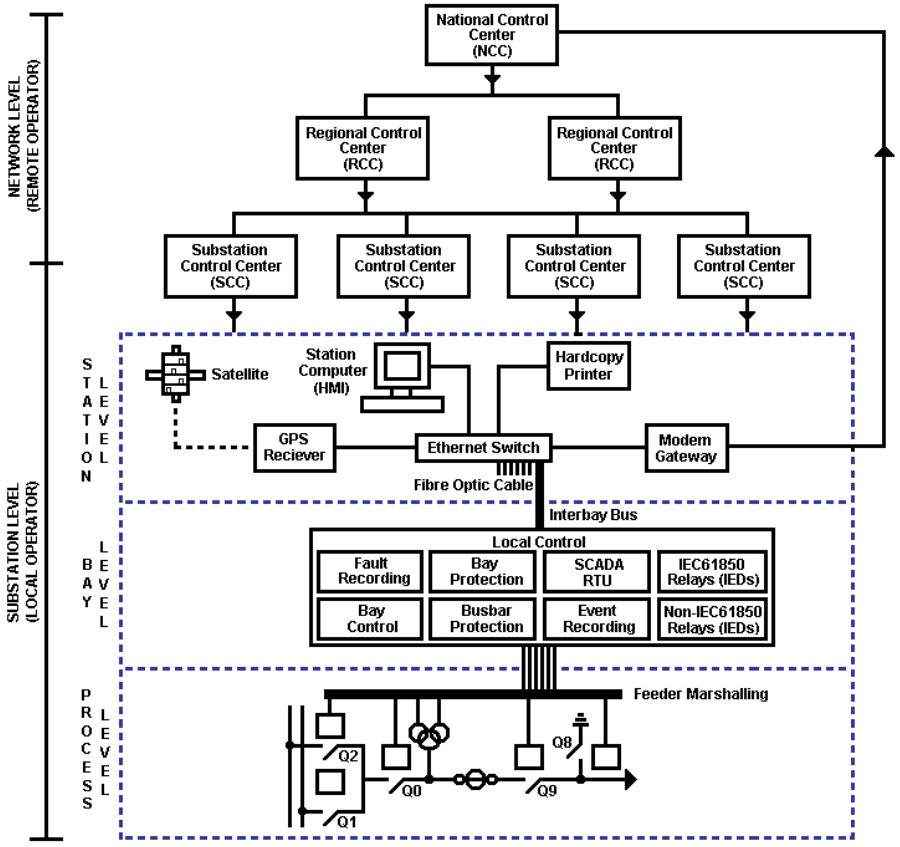


Figure 2.1: Substation automation hierarchy

2.2.2 Architectures

Substation automation systems have numerous network architectures which offer a wide range of performance trade-offs. The majority of these architectures employ the use of Ethernet technologies as opposed to copper wiring. The most popular of these include the bus, star, ring, tree and mesh topologies.

2.2.2.1 Bus topology

The bus topology is a passive architecture that requires the use of a terminator circuit to avert noisy signals through the master Ethernet switch. By way of this circuit, packets of data commonly referred to as 'virtual tokens' are broadcast from the HMI computers across fixed bandwidth channels in order to ping certain IP addresses [7,8,10]. If the tokens are identical to the IEDs, communication can be achieved between the relays. However, if the tokens are distinct, data is polled back into the network. Evidently so, this leads to certain downfalls in the system including slower communication times, added maintenance costs and limited cable length [7,8,10]. Figure 2.2, shows the bus substation architecture.

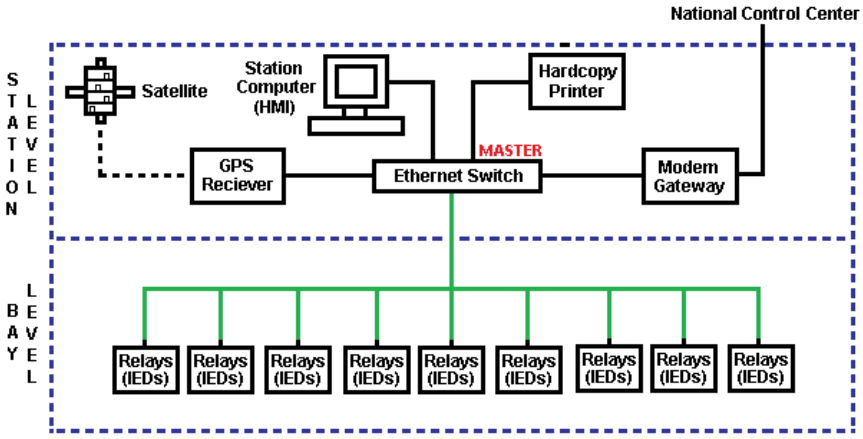


Figure 2.2: Bus substation architecture

2.2.2.2 Star topology

The star topology incorporates the use of a single station level master Ethernet switch that communicates to multiple bay level Ethernet switches via direct connection. These bay level Ethernet switches are connected to various IEDs supported by the IEC61850 protocol. The central hub of the master Ethernet switch consolidates all data signals to a common node before broadcasting virtual tokens to the IEDs [7,8]. This allows for the reduction of IED delay times, while simultaneously improving network performance [7,8]. The disadvantage however is that if the Ethernet switch situated in the station level is to stop working, all IEDs will become non-operational. Figure 2.3, illustrates the star substation architecture.

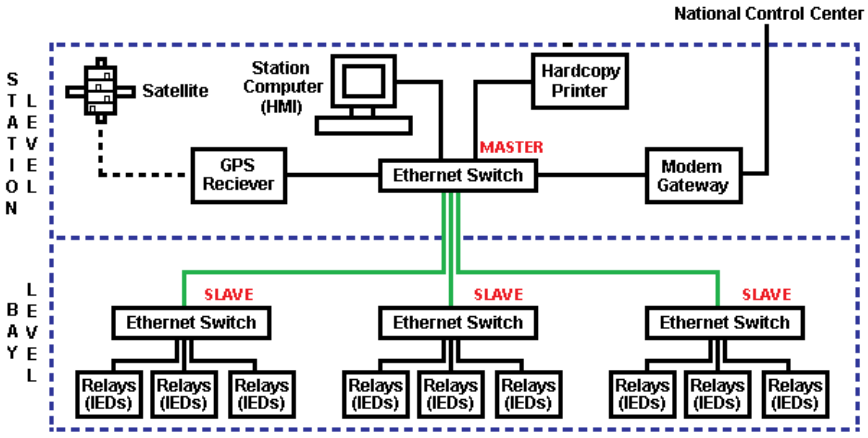


Figure 2.3: Star substation architecture

2.2.2.3 Ring topology

The ring topology connects all station level and bay level Ethernet switches through two separate fibre optic wires [8]. These fibre optic wires are connected in a clockwise and anticlockwise direction. The station level, unlike that shown in the star topology

can have more than one Ethernet switch to share communication responsibilities. The advantage of the ring topology is that once a fault takes place across a single fibre optic wire, it can be recovered in a matter of milliseconds without any IEDs shutting down [8]. However, the disadvantage is that large latencies can be conjured if data is passed through the critical path of the topology. Figure 2.4, illustrates the ring substation architecture.

Alternatively, depending on the application or the size of the network it is possible to use a multi-ring topology. A good measure for designing this topology is separating the network into different rings based on substation voltage levels or the division of bays. For example, devices at certain voltage levels may pertain to a different communications ring or have a separate Ethernet fibre optic channel. The advantage of this topology is the logical separation of the network that follows the physical topology of the substation and the natural division of IEDs into different groups. The logical separation of traffic can be achieved by more sophisticated mechanisms such as VLANs or multicast filtering.

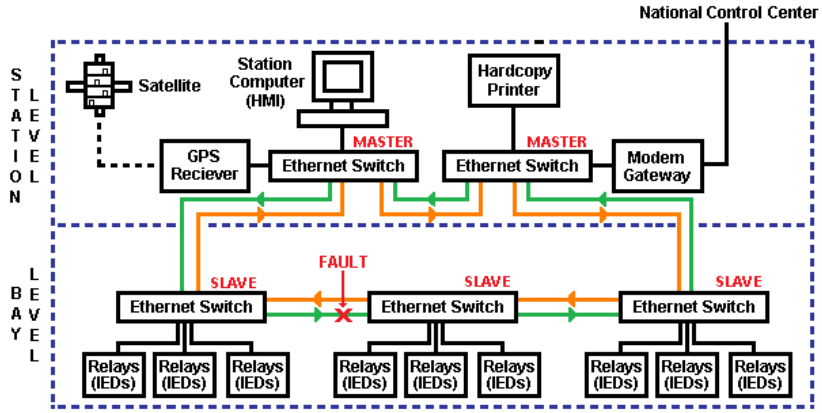


Figure 2.4: Ring substation architecture

2.2.2.4 Tree topology

The tree topology is a hierarchical network which uses the master Ethernet switch of the station level as its central node [8]. The master Ethernet switch is considered to be at the top of the hierarchy, allowing it to connect to one or more Ethernet switches located in the branches below. For example, if the master Ethernet switch were to transmit a signal to the slave 1 Ethernet switches, then both these switches will further transmit a signal to the slave 2 Ethernet switches (Figure 2.5). In practical applications, this is referred to as the ‘branching factor’ [8]. It broadcasts purely on a symmetrical basis.

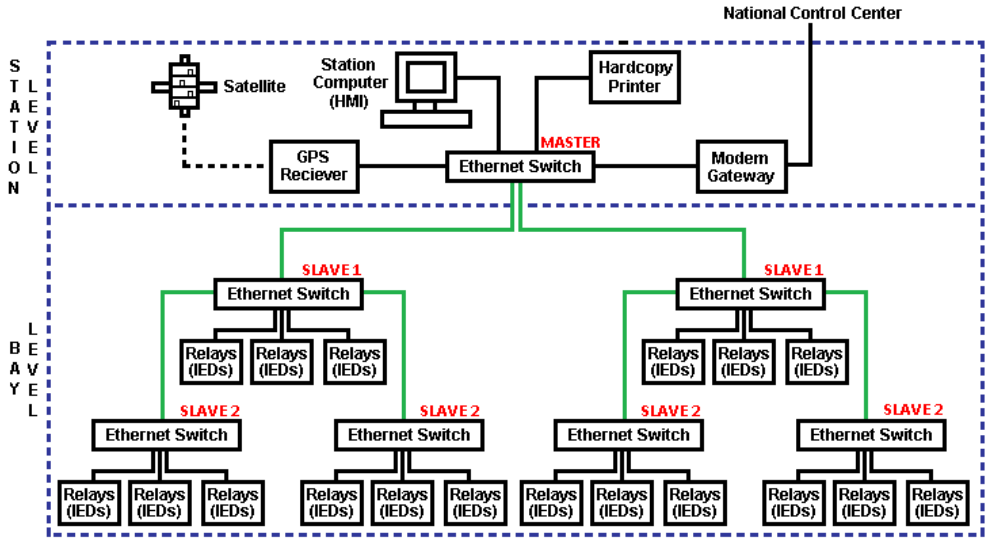


Figure 2.5: Tree substation architecture

2.2.2.5 Mesh topology

The mesh topology is a self-healing network that allows each Ethernet switch to act as a separate router. The ad-hoc nature of this topology permits each device to connect homogeneously to one another, forming either an entirely or partially connected network [8]. If a fault across any one of the connected cables becomes apparent, there will have at least one additional path available for the HMI computers to communicate with the IEDs. This means that high speed communication can continuously be achieved along the critical path of the network. However, the mesh architecture is quite complex and expensive to maintain. Figure 2.6, illustrates the mesh substation architecture.

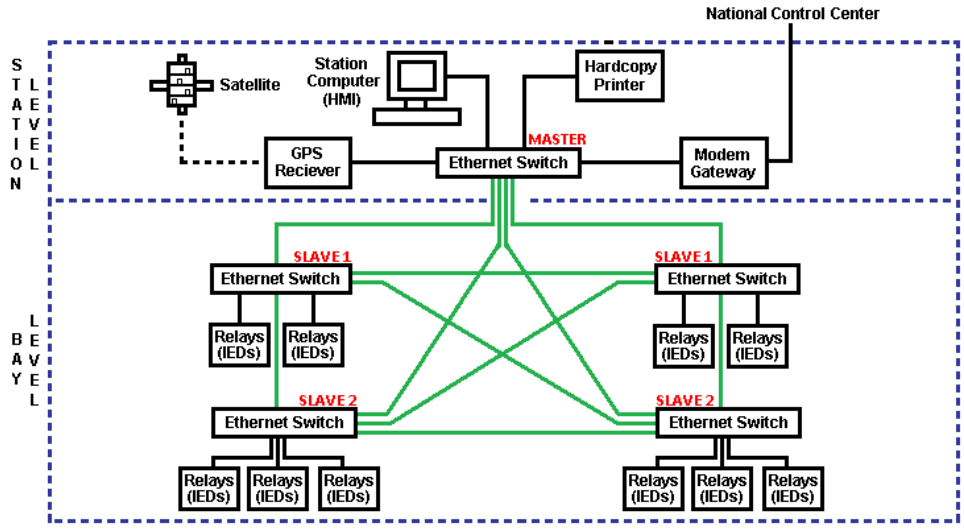


Figure 2.6: Mesh substation architecture

2.2.3 Functions

The primary functions of substation automation systems are those related to the control, monitoring, protection and fault recording of the network through the use of station level HMI computers [9]. All functions apart from fault recording are typical SCADA tasks.

2.2.3.1 Monitoring

Function monitoring is achieved through archiving, alarm management, log management and event management [9]. Archiving deals with the storage of important system data that can later be infiltrated for performance analysis and planning purposes. The archived data is stored within a fixed duration (i.e. a day, month or year) and can be used to inspect graphical visualisations and summary reports. Alarm management deals with the acknowledgement of warning messages communicated to the operator. The operator must then analyse the importance of these messages and take appropriate action to prevent a disaster from taking place in the power network. If the station level is unmanned these warning messages can be sent via SMS. Event management supervises all state changes and limit violations to substation equipment, while log management concentrates on the blocking of functions for particular maintenance tasks. Further functions that can be monitored include electrical quantities such as voltages, currents, active and reactive powers, but also switchgear statuses such as transformer taps [7,9].

2.2.3.2 Control

Control functions are either used to direct the power flow under normal operating conditions or for maintenance of certain primary and secondary switchgear equipment [9]. These functions take advantage of control dialogues that perform tasks like toggling of circuit break switches and fine-tunning of transformer taps. A ‘Select’ and ‘Execute’ option embedded in the HMI computers is used to control such functions. The ‘Select’ option ensures that the station level operator has chosen the correct device and action to be controlled. On the other hand, the ‘Execute’ option is used as a buffer for fear that the operator has made an incorrect decision. Before any control functions can be executed it is important that other control behaviours such as block state, interlock validity and synchronism checks are performed [9]. Block state is a

function capable of disconnecting power at particular zones in the substation during maintenance. Interlock validity control is a function capable of overriding manual specifications of equipment. Synchronism checks are control functions that verify the harmonisation of voltages (i.e. before a circuit breaker is closed).

2.2.3.3 Protection

Protection functions are concerned with the safety and reliability of switchgear equipment ranging from busbars, feeders, generators, shunt capacitors, transformers and lines [9]. The main objective of these functions is to prevent the occurrence of faults, either by the use of automation tools or the installation of auxiliary equipment. For this purpose, HMI computers must be authorised to override conventional monitoring and control functions without constraint. These protection functions are expected to expose both internal faults (i.e. coil defects or transformer oil leaks) and external faults (i.e. frequency drops and voltage rises).

2.2.3.4 Fault Recording

Fault recording functions utilise dedicated software tools to determine a sequence of sampled data values during the instant of a fault or short-circuit. Approximately 50% of these faults occur in overhead transmission lines, 15% in circuit breakers, 12% in transformers, 10% in cables, 3% in control equipment, 2% in current and voltage transformers and 8% in other facets [9,10]. Nevertheless, the advantage of these fault recording functions is their ability to archive a wide range of data values so that engineers can re-evaluate at a later date. Such data consists of numerous analog and binary values that can be converted into graphical fault visualisations and summary reports.

2.2.4 Protocols

Protocols are a set of rules that must be obeyed in order to meet the communication requirements of different vendor products. The International Standards Organisation (ISO), also referred to as the Open Systems Interconnection (OSI), developed a 7-layer model describing the way in which communication can flow from one end of the network to the other. The model provides the groundwork necessary for users to categorise data into profiles such as error control, line control, sequence control and time-out control [11]. The principle protocols that abide by the OSI model are the

MODBUS, DNP3 and IEC61850. Other protocols such as Ethernet may also be used alongside Instrumentation and Control (I&C) devices, but are not confined to the OSI model. Figure 2.7, shows the seven layers of the OSI model.

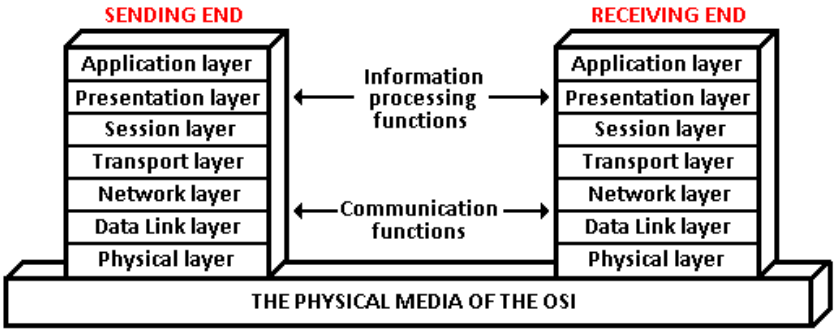


Figure 2.7: OSI model

The Application Layer is used for the data acquisition and sharing of sensitive substation information [10,11]. The Protocol Stack, which comprises of the middle five layers, assists in the manipulation of the OSI model in order to produce independent communication protocols such as the Internet Protocol (IP), User Datagram Protocol (UDP) and Transmission Control Protocol (TCP) [10,11]. The Physical Layer on the other hand, describes the tangible connections necessary across all communication channels. Figure 2.8, illustrates these protocol stacks in parallel layout.

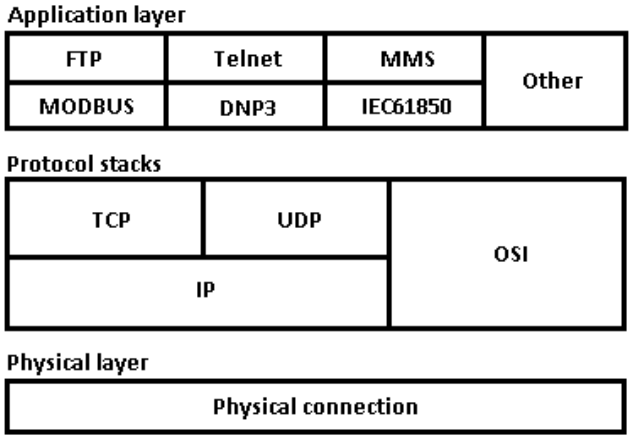


Figure 2.8: Parallel protocol stacks

2.2.4.1 MODBUS

MODBUS is a master-slave protocol which was originally designed to communicate with Programmable Logic Controllers (PLCs). It incorporates the use of basic READ/WRITE commands that employ checksum operands that aid in the safe transfer of data. These checksums are predominantly located in the physical layer of

the protocol and are used in conjunction with five different MODBUS versions including the Modus RTU, Modbus ACSI, Modbus TCP/IP, Modbus over TCP/IP and Modbus Plus [11].

The Modbus RTU is purely used for serial communication and draws on binary data produced from recurring checksums. The Modbus ACSI employs the use of ACSI characters which incorporate a longitudinal checksum. The Modbus TCP/IP does not use a checksum, unlike its Modbus over TCP/IP counterpart. The Modus Plus requires a dedicated HMI computer to cope with high-level data signals.

Additional drawbacks of the MODBUS protocol include [11]:

- boundaries in remote communications given that transmissions must be nearby;
- capacity to operate no more than 247 commands on a single communications link;
- limits on the number of data types available due to restrictions in binary objects.

2.2.4.2 DNP3

The Distributed Network Protocol (DNP3) is an intelligent and robust standard designed to facilitate in the communications between data acquisition and control devices [11]. It regularly appears across electrical and water companies on account of its ability to perform multiplexing, data fragmentation, error checking and prioritising services. The DNP3 is a layer 2 protocol meaning it avoids harsh environments arising from Electromagnetic Induction (EMI) and legacy components [11]. It too is capable of simulating large scale Neural Networks (NN) through the use of parallel structures employing arithmetic and control units [11].

2.2.4.3 IEC61850

The IEC61850 is based on the use of sophisticated object model abstracts to achieve interoperability between different vendor IEDs [12]. The protocol was established by the International Electrotechnical Commission (IEC) Technical Committee 57 (TC57), in direct response to a lack of communication standards in substation automation systems [12]. It incorporates the use of logical nodes to resolve problems related to interchange ability, but also physical character mappings to overcome IED proprietary restrictions.

The IEC61850 does not however describe any individual implementations, product functionalities or communication architectures [12]. It instead focuses only on the visible specifications of both primary and secondary equipment. The protocol is encapsulated over a series of fourteen documents spanning over ten parts as shown in Table 2.1.

Further benefits of the IEC61850 protocol include [12]:

- use of software tools to analyse Abstract Communication Service Interfaces (ACSI), Logical Nodes (LN) and Common Data Classes (CDCs);
- capability to download data from client applications communicating with IEC61850 devices without manual configuration of data names or objects;
- elimination of unnecessary ambiguity on the suppliers behalf by precisely defining user requirements through SCL files configured in XML format;
- reduction of wiring, maintenance and calibration costs by using high-level services such as GOOSE, GSSE and SMV that employ the use of Local Area Networks (LAN) to separate links between IEDs;
- reduction of incompatibility through the use of regular naming conventions in which engineers can easily identify data names without having to characterise mappings that enclose indexed number of voltages, currents and other quantities.

Table 2.1: IEC61850 arrangement

Part	Content
1	**Introduction and overview:** Summary of the IEC61850 protocol using texts and figures from other parts of the standard.
2	**Glossary:** Collection of specific terminologies and definitions from other standards and terms defined in different parts of the IEC61850 protocol.
3	**General requirements:** Basics of the IEC61850 protocol such as system availability, reliability, security, maintainability and more.
4	**System and project management:** Challenges in substation automation systems such as parameter classification, tools, documentation, factory tests, quality assurance responsibilities, and system tests.
5	**Communication requirements for function and device models:** Communication requirements related to function and device models such as interoperability, logical nodes (LN), and piece of information for communication (PICOM).
6	**Substation automation system configuration language:** Substation configuration language (SCL) based on XML file format.
7	**Basic communication structure for substation and feeder equipment:** This part is divided into four subsections that define the details of the abstract model used in the IEC61850 to meet the requirements of all functions and applications in the substation and automation domain.
7-1	**Principles and models:** Concepts of communication modelling.
7-2	**Abstract communication service interface:** Abstract communication models and services required by substation automation and protection systems.
7-3	**Common data classes:** Common data classes (CDC) necessary to implement the concepts of the hierarchical object model.

7-4	**Compatible logical mode classes and data classes:** 92 logical node classes associated with basic substation functions such as control, monitoring, protection, and fault recording.
8	**Specific Communication Service Mapping (SCSM):** Mapping of abstract models to selected MMS and ISO/IEC 8802-3 protocols.
9	**Process bus mapping:** This part is divided into two subsections that define the implementations of the IEC61850 Process Bus.
9-1	**Sampled values over serial unidirectional multi-drop point-to-point links:** Mapping of core elements from the model for transmission of sampled measured values in a point-to-point link.
9-2	**Sampled values over ISO/IEC 8002-3:** Mapping of the complete model for transmission of sampled measured values and the model for Generic Object Oriented System Events (GOOSE).
10	**Conformance testing:** Procedures for conformance testing of IEC61850 compliant devices such as documentation, device related conformance testing, validation of test equipment, and quality assurance.

2.2.5 Middlewares

Middlewares are a group of softwares explicitly designed to contend with the rising challenges of interoperability in substation automation systems. They present a trouble free platform wherein raw data can be isolated from the application layer using architectures such as point-point, client-server and publish-subscribe.

2.2.5.1 Point-Point

The point-point architecture is the simplest form of middleware which incorporates the use of a dialog box to achieve two-way communication [12,13]. When used in conjunction with large scale substation environments, the point-point architecture lacks the performance capability required to ensure a single IED can simultaneously communicate with multiple IEDs. It is therefore designed only to support one-to-one communication channels.

2.2.5.2 Client-Server

The client-server architecture has a many-to-one methodology in which a server node connects simultaneously to numerous client nodes. The architecture is most constructive when all nodes of the network require access to centralised data that is sent to the server before being accessed by IEDs [12,13]. The architecture may lead to unknown delay times being foreseen, given that the receiving IEDs do not know when new data will be queued up at the subscriber end of operation.

2.2.5.3 Publish-Subscribe

The publish-subscribe architecture is an asynchronous communications process which relies on the preferences expressed by the subscriber to deliver messages too-

and-from the publisher, as opposed to the publisher relying on the specifications of a predefined address [13]. The publisher makes use of different types of subscription mechanisms known as channel-base, subject-base and context-base.

The channel-base mechanism allows the subscriber to examine specific communication channels by sending numerous event messages across all broadcast channels. The subject-base mechanism further extends on this notion by incorporating a more flexible addressing action by way of additional notification paths. These notification paths get weighed-up against the subject attributes of the event message, so that only matching subscriptions will be forwarded to their relative events [13]. The context-base mechanism on the other hand, is capable of minimising irrelevant messages being delivered to the subscriber, due to the fact that the consumer expresses a higher level of interest [12,13]. Figure 2.9, illustrates the publish-subscribe communications model.

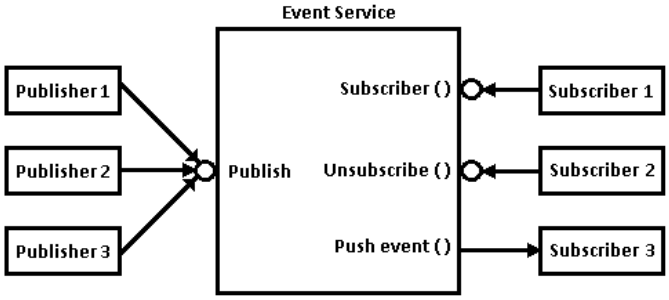


Figure 2.9: Publish-subscribe communication model

The model takes advantage of three messaging schemes referred to as unicast, multicast and broadcast. The schemes are simply used to overcome the problem of routing and accomplish low coupling signals. The unicast method is least suitable when trying to achieve real-time objectives since it consumes bandwidth resources when attempting to reach a number of point-point links [13]. It requires the publisher to consecutively send individual messages to each subscriber, as shown in Figure 2.10.

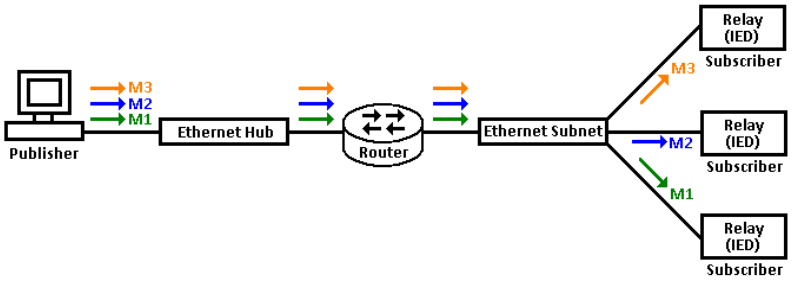


Figure 2.10: Unicast transmission

The multicast method conversely allows the publisher to send only a single stream of data across the network, which is replicated and forwarded to the subscriber instead of sending countless number of messages throughout the routers. The subscriber draws upon a multicast session group in order to filter any unnecessary messages and indicate the path in which the messages are being sent [13]. The multicast session group aids in the reduction of congested traffic, but also increases overall network efficiency as shown in Figure 2.11.

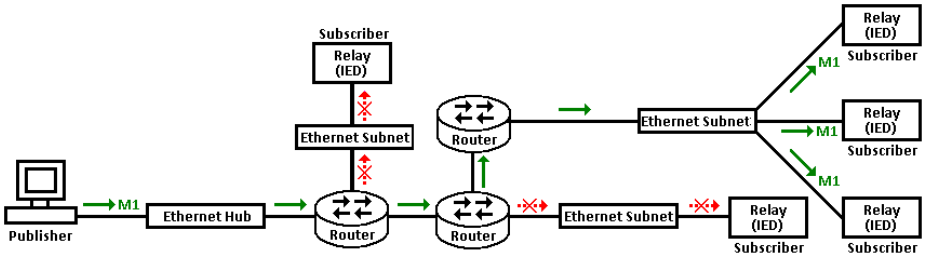


Figure 2.11: Multicast transmission

The broadcast method on the other hand, uses the concept of transmitting an identical message to all nodes in the network. The message is sent to the subscribers regardless of whether or not they request the content. The broadcast method does not make use of either filtering or binding processes, meaning it cannot determine the relative addresses necessary to forward a message [13]. This leads to increased CPU usage and reduced network efficiency. Figure 2.12, illustrates the broadcast messaging scheme.

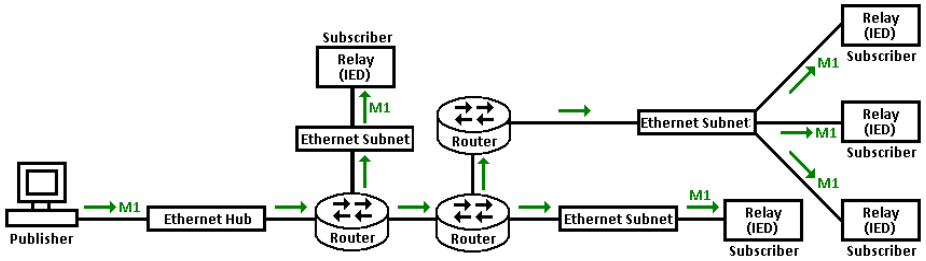


Figure 2.12: Broadcast transmission

PART II

2.3 Conventional Fault Locator Algorithms

Fault locator algorithms are classified into two groups including one-terminal and two-terminal methods. The one-terminal method is deemed to be more cost effective as it does not dictate data transfer over long distances [14]. The two-terminal method on the other hand, is more accurate in fault location but requires the support of a

data transfer system [14]. All fault locator algorithms are classified either by frequency, time or high impedance domains. They incorporate fault detection and phase selection principles based on the methods of Least Square Fitting, Parameter Estimation, Newton Raphson, Fast Fourier Transformation, Travelling Wave and Differential Equation theories.

Fault detection principles monitor the amplitude of the phase impedance, phase current, phase voltage and zero-sequence current using methods known as 'sample-by-sample' and 'cycle-by-cycle' [15]. The sample-by-sample method computes the first derivative of a signal. If the derivative overruns a pre-set value, the absolute value of the derivative can be calculated. When it reaches another pre-set threshold, a fault is confirmed. The cycle-by-cycle method on the other hand compares an existing sample with the first sample in the cycle. The threshold for such a difference may be set much lower than in the sample-by-sample method. A fault is detected when the successive difference in overreach overruns the absolute value of the second threshold. Figure 2.13 (a) and (b), illustrate the sample-by-sample and cycle-by-cycle methods.

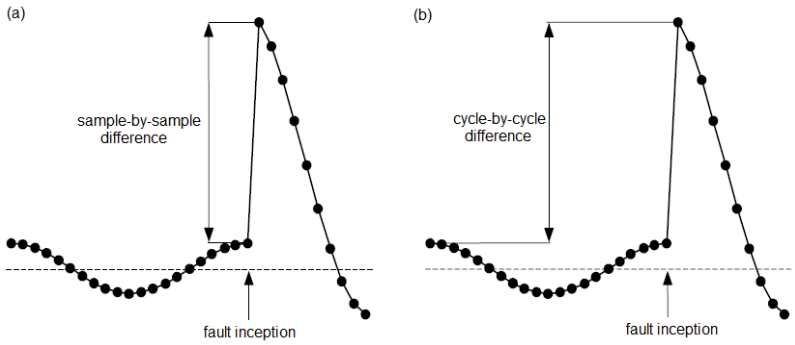


Figure 2.13: (a) Sample-by-sample and (b) Cycle-by-cycle

In contrast, phase selection principles assume the zero-sequence quantities are used as indicators of faults with respect to ground. They make use of a superimposed approach to sampling of the voltage and current. The criteria is based on checking the relations between adequate post-fault angles, which change significantly quicker than the magnitude. This symmetrical approach introduces three decisive factors including the negative-sequence verse the positive-sequence relation; the negative-sequence verse the zero-sequence relation; and the difference between the positive-sequence quantity with absence of the negative and zero-sequence components [16].

2.3.1 Frequency Domain Algorithms

Frequency domain algorithms use a combination of voltage and current signals to establish the amplitude and displacement angle of a phasor diagram. They are classified as either being based on impedance methods or current diversion ratio methods. Impedance methods assume a zero fault resistance and voltage drop per unit length in order to capture the fault location [17]. Current diversion ratio methods assume the fault current is equally divided between the faulted line and the rest of the system [18].

The majority of main stream frequency domain algorithms address one of the concerns related to the fault resistance, back-feed factor, pre-fault compensation, mutual inductance and non-linearity of arcs when attempting to locate a fault. Takagi et al. [19] presented one of the earliest papers addressing the inaccuracies of fault locator algorithms where a fault on a single-phase network was solved using two equivalent circuits. The first circuit employed a load current component, whereas the second circuit used a fault current component. The algorithm proved to be accurate for distances less than 100km. However, for transmission lines greater, an approximation factor was subtracted from the estimated distance to increase the accuracy error. A field test on a 7.2km transmission line recorded a maximum distance to fault error of 2.6%.

Takagi et al. [19] published a second paper, introducing a back-feed factor with sources at both ends of the transmission line. The back-feed factor or current distribution factor is defined as the ratio of the fault current component flowing from the local and remote sources as shown in Figure 2.14. The purpose of the back-feed factor is to eliminate the effect of remote source back-feed. This is achieved by estimating the remote current flowing into the fault as a product of the back-feed factor and fault current at the local point. The algorithm demonstrates the back-feed factor as a real value. A field test on the same 7.2km transmission line recorded a maximum distance to fault error of 2.4% [19].

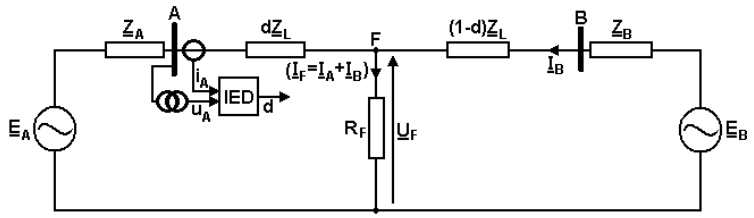


Figure 2.14: Fault location on a transmission line (lumped parameter model)

The distance to fault error is determined by formulating Kirchhoff's Voltage Law for the fault loop seen at terminal A. This leads to the complex scalar equation of:

$$\underline{U}_A - d\,\underline{Z}_L\,\underline{I}_A - \underline{I}_F\,R_F = 0 \tag{2.1}$$

The equation can be simplified into real and imaginary parts in order to determine the fault resistance (R_F), where $\underline{U}_A$ is the voltage and $\underline{I}_F$ is the fault current:

$$\frac{\underline{U}_A}{\underline{I}_F} = \frac{d\,\underline{Z}_L\,\underline{I}_A}{\underline{I}_F} + R_F \Rightarrow R_F = \frac{\underline{U}_A}{\underline{I}_F} - \frac{d\,\underline{Z}_L\,\underline{I}_A}{\underline{I}_F} \tag{2.2}$$

The total fault current is obtained by subtracting the pre-fault current from the actual fault current. This produces an incremental current component of:

$$\Delta\underline{I}_A = \frac{(1-d)\underline{Z}_L + \underline{Z}_B}{\underline{Z}_A + \underline{Z}_L + \underline{Z}_B}\underline{I}_F \Rightarrow \underline{I}_F = \frac{\Delta\underline{I}_A}{\underline{k}_F} \tag{2.3}$$

The back-feed factor (k_F) is determined by:

$$\underline{k}_F = \left|\underline{k}_F\right| e^{j\gamma} = \frac{-d\underline{Z}_L + \underline{Z}_L + \underline{Z}_B}{\underline{Z}_A + \underline{Z}_L + \underline{Z}_B} \tag{2.4}$$

Substituting equations (2.3) and (2.4) into equation (2.1) results in:

$$\underline{U}_A - d\underline{Z}_L\,\underline{I}_A - \frac{R_F}{\left|\underline{k}_F\right| e^{j\gamma}}\Delta\underline{I}_A = 0 \tag{2.5}$$

Multiplying equation (2.5) by the element ($e^{j\gamma}\Delta\underline{I}_A^{\,*}$) and taking the imaginary part yields the distance to fault formula:

$$d = \frac{\mathrm{Im}\left(\underline{U}_A\,\Delta\underline{I}_A^{\,*}\,e^{j\gamma}\right)}{\mathrm{Im}\left(\underline{Z}_L\,\underline{I}_A\,\Delta\underline{I}_A^{\,*}\,e^{j\gamma}\right)} \tag{2.6}$$

where x^* denotes the conjugate of x.

Wiszniewski [20] developed an algorithm that determines the fault location using a combination of fault resistances and remote sources feeding into the fault. The distance to fault error is identified by applying the impedance method as a phase shift between the current measured at one end of the line and through the fault resistance. The algorithm is derived with the assumption that the fault resistance is

linear. This gives rise to several findings including the back-feed factor is independent of the source voltages; the back-feed factor is a function of the network impedances; and the back-feed is a real value unless the fault transpires at the remote end of the line. The pre-fault current and voltage measurements are subtracted from the actual values during the fault condition to account for pre-load conditions. This reduces any resistance on the line impedances, seeing as the phase angle of the calculated impedance is the same as the line impedance. A simulated test on a 150km transmission line recorded a maximum distance to fault error of 2.1% [20].

The distance to fault error is determined using Figure 2.14 in which the fault loop is expressed as:

$$\underline{Z}_A - d\underline{Z}_L - \frac{R_F}{|\underline{k}_F|} \cdot \frac{\left(\underline{a}_{F1}\Delta\underline{I}_A + \underline{a}_{F2}\Delta\underline{I}_A\right)}{\underline{I}_A e^{j\gamma}} = 0 \tag{2.7}$$

The fault impedance yields:

$$\underline{Z}_A = \frac{\underline{U}_A}{\underline{I}_A} = R_A + jX_A \tag{2.8}$$

provided that the weighted coefficients ($\underline{a}_{F1}$ and $\underline{a}_{F2}$) of the symmetrical components abide by positive sequence quantities.

Solving equation (2.7) into the real and imaginary parts results in:

$$R_A - dR_L - \frac{R_F}{|k_F|}a = 0 \tag{2.9}$$

$$X_A - dX_L - \frac{R_F}{|k_F|}b = 0 \tag{2.10}$$

where $a = R_e\left(\frac{a_{F1}\Delta\underline{I}_A + a_{F2}\underline{I}_A}{\underline{I}_A e^{j\gamma}}\right)$ and $b = I_m\left(\frac{a_{F1}\Delta\underline{I}_A + a_{F2}\underline{I}_A}{\underline{I}_A e^{j\gamma}}\right)$.

The distance to fault formula is:

$$d = \frac{X_A}{X_L} - \frac{\frac{R_A}{X_L}tg(\varphi_L) - \frac{X_A}{X_L}}{\frac{a}{b}tg(\varphi_L) - 1} \tag{2.11}$$

where the angle of the positive sequence line impedance is $\varphi_L = \angle(R_L + jX_L)$.

Sachdev et al. [21] proposed an algorithm featuring a impedance relay at the local measuring point. Voltage and current signals from both the local and remote feeders were used to calculate the fault impedance. The voltage and current signals do not require synchronisation. Instead, the algorithm subtracts the charging currents to increase the accuracy in the transmission line. This procedure in theory should result in exact results. However, simulations proved that the error is as high as 8% for faults in the centre of a 500km line with a fault resistance of 25Ω [21]. This comes as the source impedance is not readily available and any slight alteration in the network configuration can modify the effective source impedance leading to a change in the back-feed factor. To reduce the error the source impedance of the remote supply needs to be increased, thereby reducing the in-feed current.

An additional algorithm using measurements at both ends of the transmission line was proposed in reference [22]. The algorithm is executed twice in order to improve the accuracy. After first execution, the approximate total shunt capacitance at both ends of the fault is calculated. The symmetrical components of the charging currents are determined using estimated capacitance values as well as the measured voltages at the line ends. A field test on a 500km transmission line recorded a maximum distance to fault error of 1% [22].

The distance to fault error is determined by expanding the back-feed factor of the positive sequence quantities:

$$\underline{k}_F = \left|\underline{k}_F\right| e^{j\gamma} = \frac{\underline{K}d + \underline{L}}{\underline{M}} \tag{2.12}$$

where $\underline{K}$, $\underline{L}$ and $\underline{M}$ are coefficients determined by the impedances.

Substituting equation (2.12) into equation (2.7) yields:

$$\begin{aligned} &\underline{Z}_A - d\underline{Z}_L - R_F \cdot \frac{\underline{M}\left(\underline{a}_{F1}\Delta\underline{I}_A + \underline{a}_{F2}\underline{I}_A\right)}{\left(\underline{K}d + \underline{L}\right)\underline{I}_A} = 0 \\ &\Rightarrow \underline{K}\underline{Z}_L d^2 + \left(\underline{L}\underline{Z}_L - \underline{K}\underline{Z}_A\right)d - \underline{L}\underline{Z}_A + R_F \frac{\left(\underline{a}_{F1}\Delta\underline{I}_A + \underline{a}_{F2}\underline{I}_A\right)\underline{M}}{\underline{I}_A} = 0 \end{aligned} \tag{2.13}$$

where $\underline{Z}_A$ is the fault loop impedance.

Equation (2.13) can be rewritten using complex numbers in order to determine the two unknowns of the distance to fault (d) and fault resistance (R_F):

$$\underline{A}_2 d^2 + \underline{A}_1 d + \underline{A}_0 + \underline{A}_{00} R_F = 0 \tag{2.14}$$

where $\underline{A}_2 = \underline{K}\underline{Z}_L$, $\underline{A}_1 = \underline{L}\underline{Z}_L - \underline{K}\underline{Z}_A$, $\underline{A}_0 = -L\underline{Z}_A$, $\underline{A}_{00} = \dfrac{(\underline{a}_{F1}\Delta\underline{I}_A + \underline{a}_{F2}\underline{I}_A)\underline{M}}{\underline{I}_A}$.

Equation (2.14) is independently derived for the real and imaginary parts. Combining them in such a way that the fault resistance is eliminated yields the quadratic formula for the distance to fault:

$$B_2 d^2 + B_1 d + B_0 = 0 \tag{2.15}$$

where $B_2 = \mathrm{Re}(\underline{A}_2)\mathrm{Im}(\underline{A}_{00}) - \mathrm{Im}(\underline{A}_2)\mathrm{Re}(\underline{A}_{00})$, $B_1 = \mathrm{Re}(\underline{A}_1)\mathrm{Im}(\underline{A}_{00}) - \mathrm{Im}(\underline{A}_1)\mathrm{Re}(\underline{A}_{00})$, $B_0 = \mathrm{Re}(\underline{A}_0)\mathrm{Im}(\underline{A}_{00}) - \mathrm{Im}(\underline{A}_0)\mathrm{Re}(\underline{A}_{00})$.

There are two solutions for equation (2.15) of which only one is the real distance to fault (d), while the other solution lies outside the line range:

$$d_1 = \frac{-B_1 - \sqrt{B_1^{\,2} - 4B_2B_0}}{2B_2} \tag{2.16}$$

$$d_2 = \frac{-B_1 + \sqrt{B_1^{\,2} - 4B_2B_0}}{2B_2} \tag{2.17}$$

The fault resistance is calculated by taking the real part of equation (2.14):

$$R_{F1} = \frac{-\mathrm{Re}(\underline{A}_2)d_1^{\,2} - \mathrm{Re}(\underline{A}_1)d_1 - \mathrm{Re}(\underline{A}_0)}{\mathrm{Re}(\underline{A}_{00})} \tag{2.18}$$

$$R_{F2} = \frac{-\mathrm{Re}(\underline{A}_2)d_2^{\,2} - \mathrm{Re}(\underline{A}_1)d_2 - \mathrm{Re}(\underline{A}_0)}{\mathrm{Re}(\underline{A}_{00})} \tag{2.19}$$

Liao et al. [23] developed a set of 12 equations in which the fault resistance is constant. This two-terminal method takes into consideration pre-fault settings by subtracting the pre-fault conditions from the current during the fault condition. The error due to the arc resistance is only an estimate seeing as the exact fault is a function of the fault resistance and load. Both these quantities are unknown during the fault and have three constants (a^0, a^1, $a^2 = 1\angle 120°$) [23]. A simulated test on a 100km transmission line recorded a maximum distance to fault error of 1.9% [23].

Ibe et al. [24] put forward an algorithm using a distributed parameter line model for fault location as shown in Figure 2.15. The algorithm draws upon modal analysis to solve the iterative calculations of differential equations. The algorithm produces results independent of the fault resistance, pre-load conditions and back-feed current. However, some difficulties were experienced during testing including no minima was present for the voltage function if the point-of-wave of the fault was below 30º. This comes as the rate-of-rise falls below the point-of-wave when the fault approaches a zero crossing. A second iterative with respect to the measuring point is applied. A simulated test on a 1 25km transmission line recorded a maximum distance to fault error of 1.4% [24].

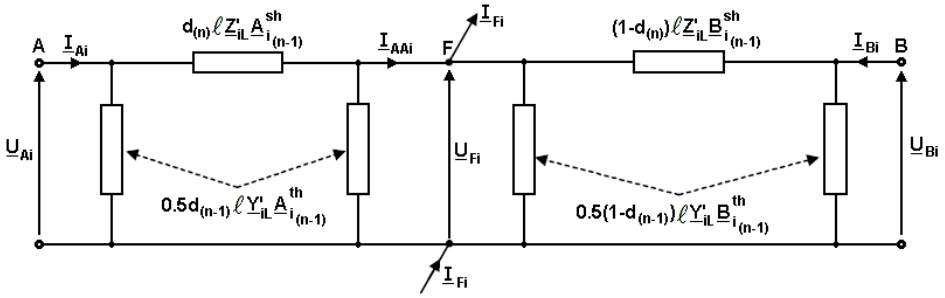


Figure 2.15: Fault location on a transmission line (distributed parameter model)

The distance to fault error is determined by introducing the fault loop equation:

$$\underline{U}_A - d\underline{Z}_{1L}\left(\underline{a}_1\underline{I}_{A1} + \underline{a}_2\underline{I}_{A2} + \underline{a}_0\frac{\underline{Z}_{0L}}{\underline{Z}_{1L}}\underline{I}_{A0}\right) - R_F\left(\underline{a}_{F1}\underline{I}_{F1} + \underline{a}_{F2}\underline{I}_{F2} + \underline{a}_{F0}\underline{I}_{F0}\right) = 0 \qquad (2.20)$$

The shunt capacitances for the faulted line section is determined by the value obtained by the last iteration (n-1). The unknowns $d_{(n)}$ and $R_{F(n)}$ are solved iteratively while checking the convergence of the iterative calculations or applying a pre-defined number of iterations. Rearranging equation (2.20) yields:

$$\begin{aligned}&\underline{U}_A - d_{(n)}\underline{Z}_{1L}\left(\underline{a}_1\underline{A}^{sh}_{1_{(n-1)}}\underline{I}^{comp}_{A1} + \underline{a}_2\underline{A}^{sh}_{2_{(n-1)}}\underline{I}^{comp}_{A2} + \underline{a}_0\underline{A}^{sh}_{0_{(n-1)}}\frac{\underline{Z}_{0L}}{\underline{Z}_{1L}}\underline{I}^{comp}_{A0}\right)\\ &- R_{F_{(n)}}\left(\underline{a}_{F1}\underline{I}^{comp}_{F1} + \underline{a}_{F2}\underline{I}^{comp}_{F2} + \underline{a}_{F0}\underline{I}^{comp}_{F0}\right) = 0\end{aligned} \qquad (2.21)$$

where

$d_{(n)}$, $d_{(n-1)}$ - distance to fault from current and previous iterations

$R_{F(n)}$ - fault resistance from current iterations

$\underline{A}^{sh}_{1_{(n-1)}} = \underline{A}^{sh}_{2_{(n-1)}} = \dfrac{\sinh\left(\gamma_1 d_{(n-1)}\ell\right)}{\gamma_1 d_{(n-1)}\ell}$ - correction factor (positive sequence impedance)

$\underline{A}^{sh}_{0_{(n-1)}} = \frac{\sinh(\gamma_0 d_{(n-1)}\ell)}{\gamma_0 d_{(n-1)}\ell}$ - correction factor (zero sequence impedance)

$\underline{I}^{comp}_{A1} = \underline{I}_{A1} - 0.5 d_{(n-1)}\ell \underline{Y}_{1L} \underline{A}^{th}_{1_{(n-1)}} \underline{U}_{A1}$ - positive sequence current

$\underline{I}^{comp}_{A2} = \underline{I}_{A2} - 0.5 d_{(n-1)}\ell \underline{Y}_{2L} \underline{A}^{th}_{2_{(n-1)}} \underline{U}_{A2}$ - negative sequence current

$\underline{I}^{comp}_{A0} = \underline{I}_{A0} - 0.5 d_{(n-1)}\ell \underline{Y}_{0L} \underline{A}^{th}_{0_{(n-1)}} \underline{U}_{A0}$ - zero sequence current

$\underline{I}^{comp}_{F1}$, $\underline{I}^{comp}_{F2}$, $\underline{I}^{comp}_{F0}$ - symmetrical components of the total fault current

Johns et al. [25] presented a more accurate one-terminal fault locator algorithm. The algorithm is based on the assumption that the impedance is real at the point of fault. By using the phase difference between the voltages and currents, it is possible to calculate the position where the phases converge. The algorithm presents two assumptions including the remote source impedance is known; and the fault current is equal to the difference between the line current and pre-fault current. The algorithm proves for small fault resistances (R_f < 5Ω) the influence of ±30% change in the source impedance produces an distance to fault error of 0.8% [25].

2.3.2 Time Domain Algorithms

Time domain algorithms make use of differential equation concepts that employ RL circuits when applicable to overhead transmission lines. They assume the resistance and inductance is calculated between two successive sampling points in which the fault resistance is purely resistive [26]. The majority of time domain algorithms are influenced by many of the same factors present in frequency domain algorithms, however much less literature is available. The most common of these is the back-feed factor caused by non-zero fault impedances. A constant back-feed coefficient for the estimation of back-feed current is essential in standard differential equations. This improves the speed of the algorithm by assuming the network impedances are fixed and equal to those obtained by the pre-fault estimations. Figure 2.16, illustrates a lumped parameter model for a short-to-medium lengthed overhead transmission line. Such a model is adequate for distances less than 100km [26].

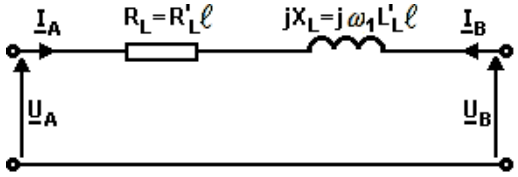


Figure 2.16: Short-to-medium transmission line

For long transmission lines, a distributed parameter model is applied as shown in Figure 2.17. The voltage and current is represented as a function of the distance (d) from the sending end (A) at a time (t). The voltage u(d,t) and c urrent i(d,t) are associated with the parameters of the line (R_L, L_L, C_L - resistance, inductance, capacitance per unit length) by the so-called telegrapher equations [27]:

$$\frac{\partial u(d,t)}{\partial d} + L_L \frac{\partial i(d,t)}{\partial t} = -R_L i(d,t) \tag{2.22}$$

$$C_L \frac{\partial u(d,t)}{\partial t} + \frac{\partial i(d,t)}{\partial d} = 0 \tag{2.23}$$

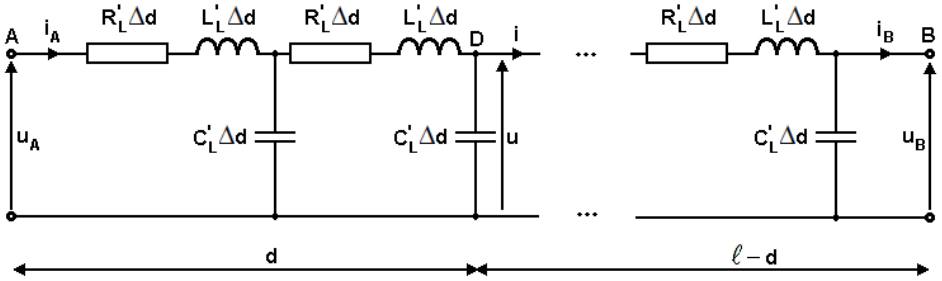


Figure 2.17: Long transmission line

The partial differential equations of expression (2.22) and (2.23) are solved using the method of characteristics [27], which gives rise to the modified telegrapher equations:

$$\frac{\partial v(d,t)}{\partial d} - \chi^2 \frac{\partial i(d,t)}{\partial t} = -\eta i(d,t) \tag{2.24}$$

$$\frac{\partial v(d,t)}{\partial t} - \frac{\partial i(d,t)}{\partial d} = 0 \tag{2.25}$$

where $v(d,t) = -C'_L u(d,t)$, $\chi = \sqrt{L'_L C'_L}$, $\eta = R'_L C'_L$.

The method of characteristics introduces characteristic lines in which partial differential equations are transformed into ordinary differential equations. The partial differential equations of the voltage and current components of equations (2.24) and (2.25) can be written as ordinary differential equations [27]:

$$\frac{dv}{ds} - \chi \frac{di}{ds} = \frac{\eta i}{\sqrt{1+\chi^2}} \tag{2.26}$$

$$\frac{dv}{d\rho} - \chi \frac{di}{d\rho} = \frac{-\eta i}{\sqrt{1+\chi^2}} \tag{2.27}$$

where s and ρ is the length along the characteristic $t \pm \chi d$ = const.

The solution of (2.26) and (2.27) requires the discretisation of the continuous time system. Discretisation is the process of transforming continuous equations into discrete equivalents. Firki [28] proposed a fault location algorithm estimating the distance to fault error by assuming the distance (d) is discretised by the index j, while the time (t) is discretised by the index k. The expression for the voltage and current yields:

$$v_{j,k} = \frac{1}{2}\left(v_{j-1,k-1} + v_{j-1,k+1}\right) + \frac{Z_c}{2}\left(i_{j-1,k-1} - i_{j-1,k+1}\right) + \frac{R_L^{'}\Delta d}{4}\left(i_{j-1,k-1} + i_{j-1,k+1}\right) - \frac{R_L^{'}\Delta d}{2} i_{j,k} \quad (2.28)$$

$$i_{j,k} = \frac{1}{2Z_c}\left(v_{j-1,k-1} - v_{j-1,k+1}\right) + \frac{1}{2}\left(i_{j-1,k-1} + i_{j-1,k+1}\right) + \frac{R_L^{'}\Delta d}{4Z_c}\left(i_{j-1,k-1} - i_{j-1,k-1}\right) \quad (2.29)$$

where $Z_c = \sqrt{L_L^{'} / C_L^{'}}$ is the arc impedance of the transmission line. A simulated test on a 100km transmission line recorded a maximum distance to fault error of 0.9% [28].

Akke et al. [29] developed an algorithm that neglects the series resistance R'_L from equations (2.28) and (2.29), resulting in the use of Bergeron equations for a transmission line. The algorithm computes the profile of the voltage and current at any point of the transmission line through a discrete sample. For each discrete sample, the voltage at the sending end is determined. The Bergeron equations for the voltage and current at point d_j and time t_k are expressed as in equations (2.30) and (2.31). A simulated test on a 200km transmission line recorded a maximum distance to fault error of 0.8% [29].

$$v_{j,k} = \frac{1}{2}\left(v_{0,k-j} + v_{0,k+j}\right) + \frac{Z_c}{2}\left(i_{0,k-j} - i_{0,k+j}\right) \quad (2.30)$$

$$i_{j,k} = \frac{1}{2Z_c}\left(v_{0,k-j} - v_{0,k+j}\right) + \frac{1}{2}\left(i_{0,k-j} + i_{0,k+j}\right) \quad (2.31)$$

Jamali et al. [30], proposed a fault location algorithm using travelling waves as an alternative to solving partial differential equations. Information extracted from the secondary voltages and currents is used to determine the distance to fault error. The algorithm correlates the initial transients at the relaying terminal from the fault point by the use of forward and backward transients. The algorithm is distinctive of the fault type, fault resistance, inception angle and system source parameters. The algorithm propagates heavy surges due to the pre-fault charge rapidly discharging. A simulated test on a 150km transmission line recorded a maximum distance to fault error of 0.7% [30].

Figure 2.18, illustrates a Bewley Lattice diagram of the travelling waves. Two sources at busbar A and B connect to the transmission line, at which the voltage and current signals are measured at busbar R. If a phase-to-ground fault in the forward direction occurs at point F, the fault wavefronts will travel along both directions of the line. The wavefronts that travel from point F towards busbar R under a forward fault are known as 'backward travelling' waves. These waves travel past busbar R and reflect at busbar A. The wavefronts which travel towards the forward direction from busbar R are known as 'forward travelling' waves. If these waves reach point F, most of them will reflect from the fault point while the remaining part propagates towards busbar B. These two components are known as 'reflected' and 'transmitted' waves [30].

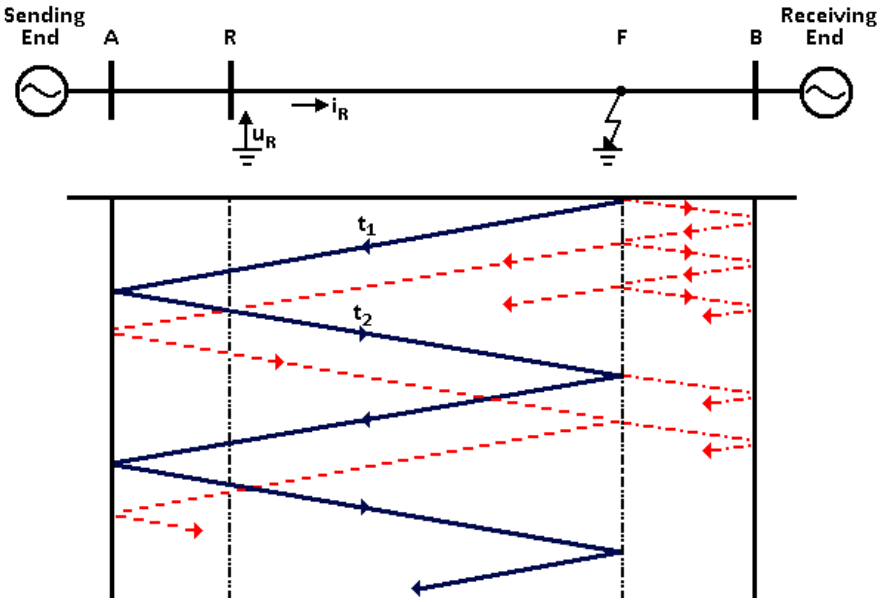


Figure 2.18: Bewley lattice diagram of a fault on a transmission line

The voltage and current signals are considered to be the summation of backward travelling waves (F_1) and forward travelling waves (F_2). These waves propagate with a constant amplitude at a velocity slightly less than the speed of light [30]. Equations (2.32) and (2.33) can be used to represent the general solution for the travelling wave method in order to derive the distance to fault error:

$$u(d,t) = F_1(d - at) - F_2(d + at) \tag{2.32}$$

$$i(d,t) = \frac{1}{Z_c}\left[F_1(d - at) + F_2(d + at)\right] \tag{2.33}$$

where Z_c is the arc impedance of the transmission line and 'a' is the propagation velocity of the wave.

Radojevic et al. [31] introduced a two-terminal time domain algorithm assuming a constant arc resistance. The algorithm draws on the method of least square fitting to calculate the distance to fault error. A sampling window of 20ms is used to determine three unknowns. A test on a 500km transmission line recorded a maximum distance to fault error of 1.8%, resulting in a highly unstable distance to fault estimation with singularities [31]. These singularities are due to rapid increases in the arc resistance during low fault currents. The ideal response would be to modify the sampling window to 3ms, creating two equations while the arc voltage is assumed at zero as expressed in equation (2.34).

$$u_k = \left\{ ri_{k+} \frac{x}{2T\omega_o} \left[i_{k+1} - i_{k-1} + K_L\left(i_{o(k+1)}\right) \right] l + sgn(i_{0k}) U_a + i_{0k} R_e + \varepsilon_k \right\} \quad (2.34)$$

where

$K_L = \frac{(x_0 - x)}{x} =$ function of the line impedance

$x_0 =$ line per unit length of the zero sequence inductance

$x =$ line per unit length of the positive sequence inductance

$R_e = (r_0 - r)l + k_a R_f =$ equivalent resistance

$r_0 =$ line per unit length of the zero sequence resistance

$\varepsilon_k =$ modelling errors and random variances of the arc

Aggarwal et al. [32] presented a fault locator algorithm used on teed feeders. The method is independent of the fault resistance and insensitive to variations of source impedance, teed and line configurations such as line untransposition. The method is based on utilising voltage and current waveforms at all three ends of an EHV teed feeder, which is filtered using Discrete Fourier Transformation (DFT) techniques to produce a measure of steady-state power frequency. The algorithm described makes use of superimposed modal components of voltage and current values rather than the total phase values. The fault point and tee point phasors produce an distance to fault error of:

$$x = \text{Arctan} \frac{\left(\frac{D_k}{C_k}\right)}{\gamma_k} \quad (2.35)$$

where

$D_k = -V_{Pk} + A_k Cosh(\gamma_k L_{Pk}) + Z_{Ok} B_k Sinh(\gamma_k L_{Pk})$

$C_k = -Z_{Ok} I_{Pk} + A_k Sinh(\gamma_k L_{Pk}) - Z_{Ok} B_k Cosh(\gamma_k L_{Pk})$

$B_k = -Cosh\left(\gamma_k L_{Qk}\right) I_{Qk} + Y_{Ok} Sinh(\gamma_k L_{Rk}) V_{Rk} - Cosh(\gamma_k L_{Rk}) I_{Rk} + Y_{Ok} Sinh\left(\gamma_k L_{Qk}\right) V_{Qk}$

$A_k = Cosh\left(\gamma_k L_{Qk}\right) V_{Qk} - Z_{Ok} Sinh\left(\gamma_k L_{Qk}\right) I_{Qk}$

2.3.3 High Impedance Domain Algorithms

High impedance domain algorithms are generally not suitable for the estimation of distance to fault errors on transmission lines seeing as most distance and overcurrent relays have difficulty detecting insignificant amounts of fault current. These algorithms are derived from voltage unbalance, energy randomness and digital signal processing concepts. Voltage unbalance methods detect the loss of voltage at each end of a transmission line and send a signal back to the feeder or circuit breaker. Sensors connected to these lines aid in the detection of phase losses [33]. Energy randomness methods monitor the levels of power stored within certain frequency ranges before summing the total power generated across the fundamental frequency. The non-harmonic component of the network is then used for arc identification [33]. Digital signal processing methods identify the waveforms associated with high impedance faults using techniques such as Crest Factor [34], Wavelet [34] and Current Flickering [34].

2.4 Conclusion

This chapter provided the necessary framework to identify the benefits of using the IEC61850 protocol in substation automation systems. The background covered aspects related to architectures, functions, protocols and middlewares in order to control, monitor and protect primary and secondary switchgear equipment situated within substations. The chapter also highlighted different types of fault locator algorithms derived from frequency, time and high impedance domains. The review focused on the inaccuracies of overhead transmission lines with special attention given to the distance to fault error.

Chapter 3 – Hardware Assembly

3.1 Introduction

The purpose of this chapter is to provide a detailed insight into the practical wiring and design of a portable IEC61850 testing unit using a selection of IEDs, Ethernet switches and a GPS clock. The chapter begins with a pragmatic explanation of the steps necessary to build an interoperable network. Hardware descriptions and dimensions of each device are illustrated for AC and DC schematics by using fibre optic cable instead of traditional copper wire. The overall cost of the rig is $340,000 AUD.

3.2 Steps To Building An Interoperable Network

Interoperability is much more than simple data transfer between two or more devices of similar intelligence. It provides information exchange between multiple vendors in order to realise the performance functionalities intended for correct co-operation. Data transfer for utility networks has historically been a one-way practice with data flowing from a simple sender to a highly sophisticated receiver which interprets the data [35]. This is very often the role of a human being who can read and understand the data. The receiver must be familiar with not only the syntax of the data, but also its meaning (i.e. the semantics in the context of the process).

For this reason, selecting which devices are suitable when building the portable IEC61850 testing unit is no simple task. It is important to consider a number of aspects when planning the construction of the rig including:

- *Understanding the environmental conditions of the substation and yard* - substation environments are extremely harsh, upon which installed IEDs located within apparatus cabinets or on pole-tops endure even harsher environments. The industry has learnt many lessons about reliability and av ailability that cannot be discarded in the interest of adopting a new communications standard. The biggest physical change is moving to Ethernet substation LANs, which increase the number of fibre optic connections between the server and client. An example of this is the integration of protection relays to provide basic status readings using the SCADA network. Traditional methods utilise a direct copper connection linking the relay and processor. Nowadays, Ethernet LANs replace this approach with a combination of copper and fibre optic cables, one at the Ethernet switch and the remaining between the relay, processor and switchgear equipment [35]. Therefore, in order for the network to be dependable, it needs to match performance and reliability functions at both ends of devices. Taking this into consideration, it is decisive to recognise that many Ethernet technologies are developed for commercial applications meaning when deciding to select devices make sure they are utility graded and can reliably operate in harsh conditions for the life span of the installation [35].

- *Choosing devices that are conformant to the IEC61850 protocol* - the standard addresses a l arge number of communication data models and s ervices, of which only a subset are implemented within physical devices. Vendors tend to publish those elements to which their products have been tested for conformance. The Utility Communications Architecture (UCA) International Users Group (IUG) specifies that test centres must be recognised or accredited for IEC61850 device testing. The minimum requirement to be accredited is the presence of a certified ISO 9000-based quality system that allows autonomy from commercial and financial pressures that could influence test results [35]. The test result assures each IED meets the communication requirements and functionalities of the system by processing an IEC61850 conformance, interoperability and pe rformance certificate. This certificate has a number of benefits including guaranteed interoperability, bragging rights, enhanced reliability and reduced risk [35].

- *Electing to use devices that are interoperable* - even though devices are expected to be interoperable if they conform to the same standard, industry experience with protocols proves that different development teams may create conformant but non-interoperable devices. One obvious way to improve the likelihood of interoperability is to choose devices that are created by the same manufacturer. This however is not recommended seeing as most substations incorporate devices from multiple vendors [35]. Instead the best method to assure interoperability is to test and observe it. Although one cannot physically test every interoperability permutation, specific information should be available for the end user prior to product purchase.

- *Making sure devices match performance requirements* - local and distributed functions must perform accurately and at high-speeds, regardless of the vendor or protocol used. Local performance such as push button functionality on IED front panels, must meet intended operation but not affect network performance. Time stamping, synchronisation and message acceptance, such as GOOSE, have a direct bearing on distributed network functionality [35]. Even though the standard does not dictate required accuracy and speed of IEDs, the practising engineer will need to know these parameters to understand the interaction of networked devices and appreciate how they will execute a distributed function.

3.3 Hardware Inventory and Design

Compared to conventional stationary protection panels, the portable IEC61850 testing unit is designed with the intent of being compact in size and manoeuvrable. The portable IEC61850 testing unit weighs 101.5kg and has a length of 19 inches, width of 21 inches and height of 33 inches. The inner frame is interconnected by corner connectors and gussets made from galvanised steel profiles. The front and rear panels use a transparent polycarbonate material with a thickness of 3mm and 10mm, respectively. The front panel employs an earthing strap and has a foldable door handle. The side, roof and base panels use a zinc powdered material complying with protection class IP54 to DIN40050/IEC144. Additional accessories include four transportable brackets bolted with M12 screws, four 50lbs heavy duty caster wheels and two roof mounted fans.

The core of the portable IEC61850 testing unit comprises of several protection IEDs, Ethernet switches and a GPS clock. Table 3.1 illustrates the dimensions of each device when rack mount to the unit. There are four IEDs in total, all from different vendors (ABB, Areva and SEL). The SEL-487E draws upon three-phase differential protection in transformer applications. It is capable of supplying up to five different current signals and can perform circuit breaker failure with open pole status detection [36]. The SEL-311L is a line current differential protection and automation relay suitable for protection of any transmission line or underground cable [37]. It eliminates traditional control switches by means of sixteen local switches in order to trip or close circuit breakers. A Mho phase distance characteristic is further employed using both Mho and Quad phase-ground distance elements. The REF615 is a feeder protection and control relay offering directional and non-directional earth-fault protection [38]. Directional earth-fault protection is mainly used in isolated or compensated networks, whereas non-directional earth-fault protection is intended for low impedance earthed networks. The P145 is a feeder management relay designed for a wide-range of overhead distribution and transmission voltage levels [39]. It has ten function keys offering operator control for applications such as auto-reclose, breaker failure and remote communications. The P145 incorporates a series of non-protection features in order to aid with power system diagnosis and fault analysis.

Table 3.1: Hardware dimensions

Dimensions	Height (mm)	Length (mm)	Width (mm)
SEL-2407	43.7	266.4	231.6
SEL-2725	38.8	136.3	142.6
SEL-487E	310.4	482.6	241.8
SEL-311L	132.6	482.6	232.4
P145	177.0	309.6	168.0
REF615	161.5	165.5	194.0
RSG2200	44.3	479.4	313.0
Testing Unit	838.2	482.6	533.4

The Ruggedcom RSG2200 nine-port managed gigabit Ethernet backbone switch is an industrial switch providing advanced cyber security and networking features [40]. Virtual Local Area Networks (VLAN) allow segregation of physical networks into separate logical clusters with independent broadcasting domains. GVRP support is provided to simplify switch configuration of the VLAN. The SEL-2725 unmanaged Ethernet switch is used as a copper-to-fibre optic converter and has five-ports [41]. It is rated at 125V/48W. The SEL-2407 satellite synchronised clock provides

demodulated IRIG-B timecode at six outputs for driving numerous applications [42]. A bullet antenna rated at 5V/40dB gain and TNC connectors are mandatory. A 240/115V isolated stepdown transformer is connected to a 35W bridge rectifier to provide DC input.

Figures 3.1 (a and b) demonstrate the front and rear panels of the portable IEC61850 testing unit. OMICRON's CMC356 test set sits comfortably on top of the rig and is used to inject current and voltage signals for protection and metering purposes. The CMC356 test set consists of ten analog inputs making it possible to achieve accurate measurements during IED testing. Appendix A provides more information on device descriptions, conformance statements, mounting methods and physical properties.

Figure 3.1(a): Front view

Figure 3.1(b): Rear view

3.4 Wiring Layout

The wiring layout of the portable IEC61850 testing unit is simulated using the simSCADA software. Figures 3.2 to 3.7, illustrate the wiring connections of the rig. The SEL-487E has three current input groups (S, T and U) designated across terminals 9-20. Reciprocally, the SEL-311L, REF615 and P145 have voltage and current inputs across terminals 44-51, 74-80 and 98-105. The main circuit breakers (MCB) are rated at 125V and vary between 17-48W. Optoisolated input signals such as IN101 and OPTO6 are used for circuit breaker status.

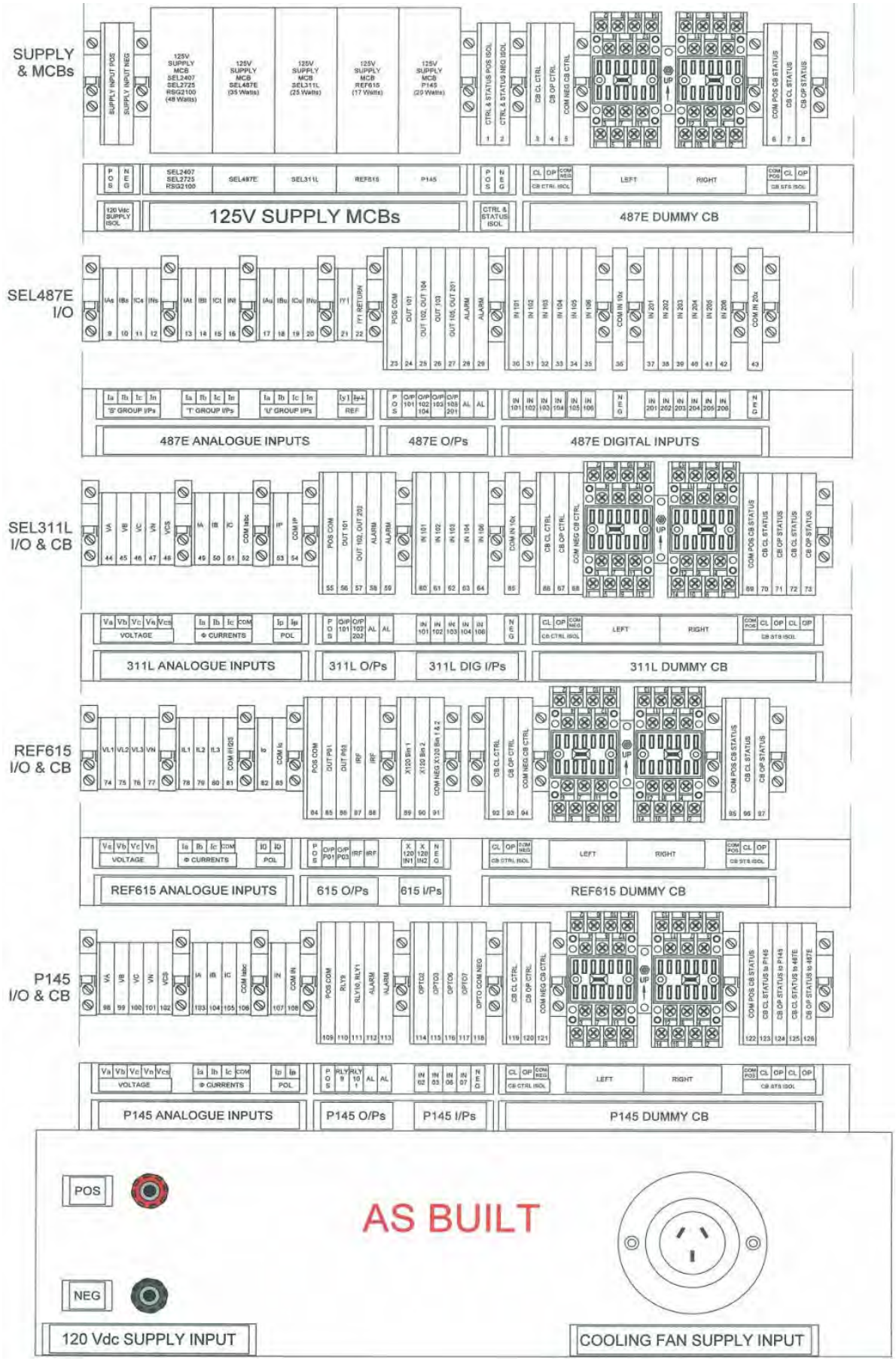


Figure 3.2: Portable IEC61850 testing unit (Complete Structure)

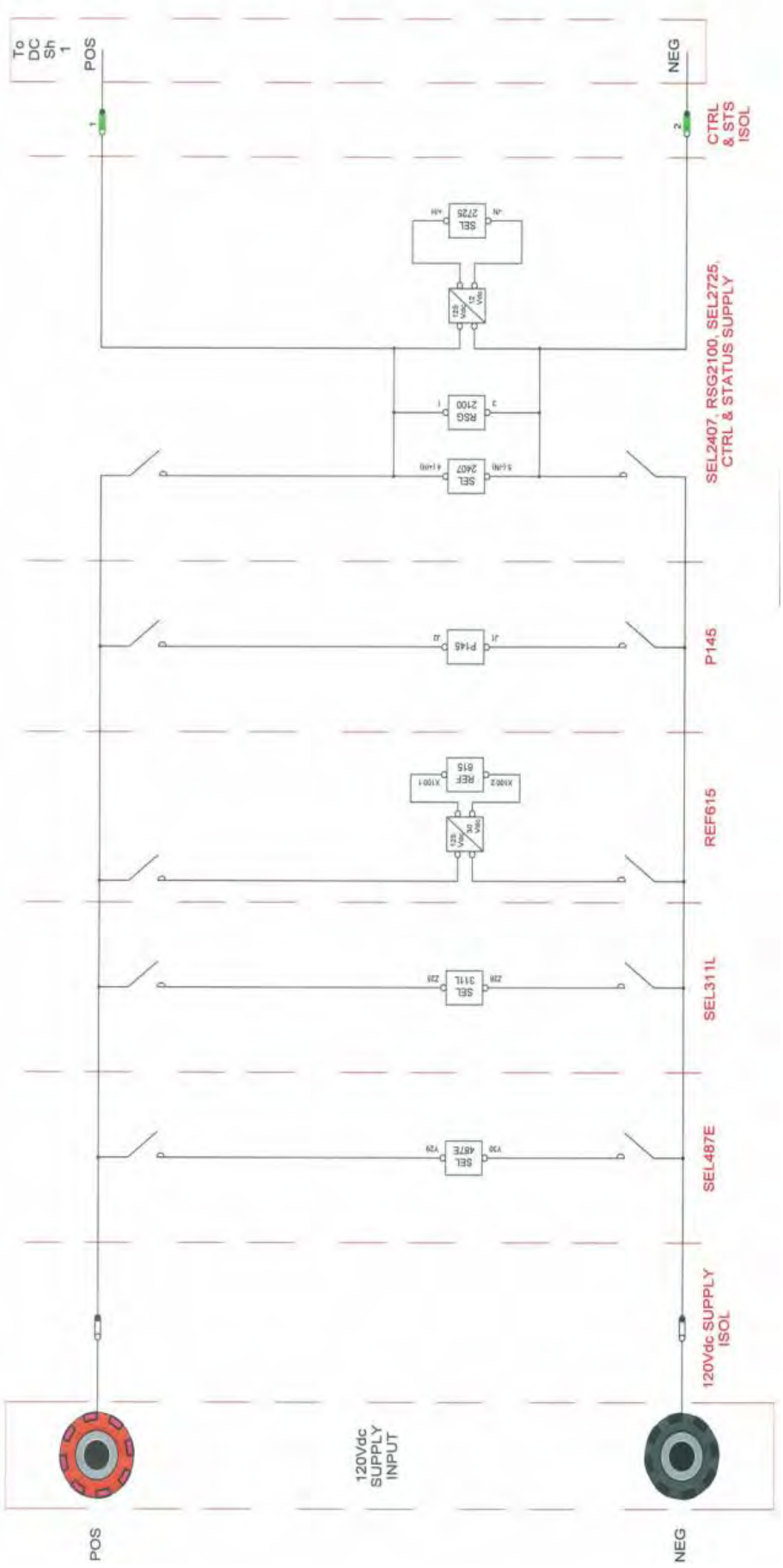


Figure 3.3: Input supply (DC wiring)

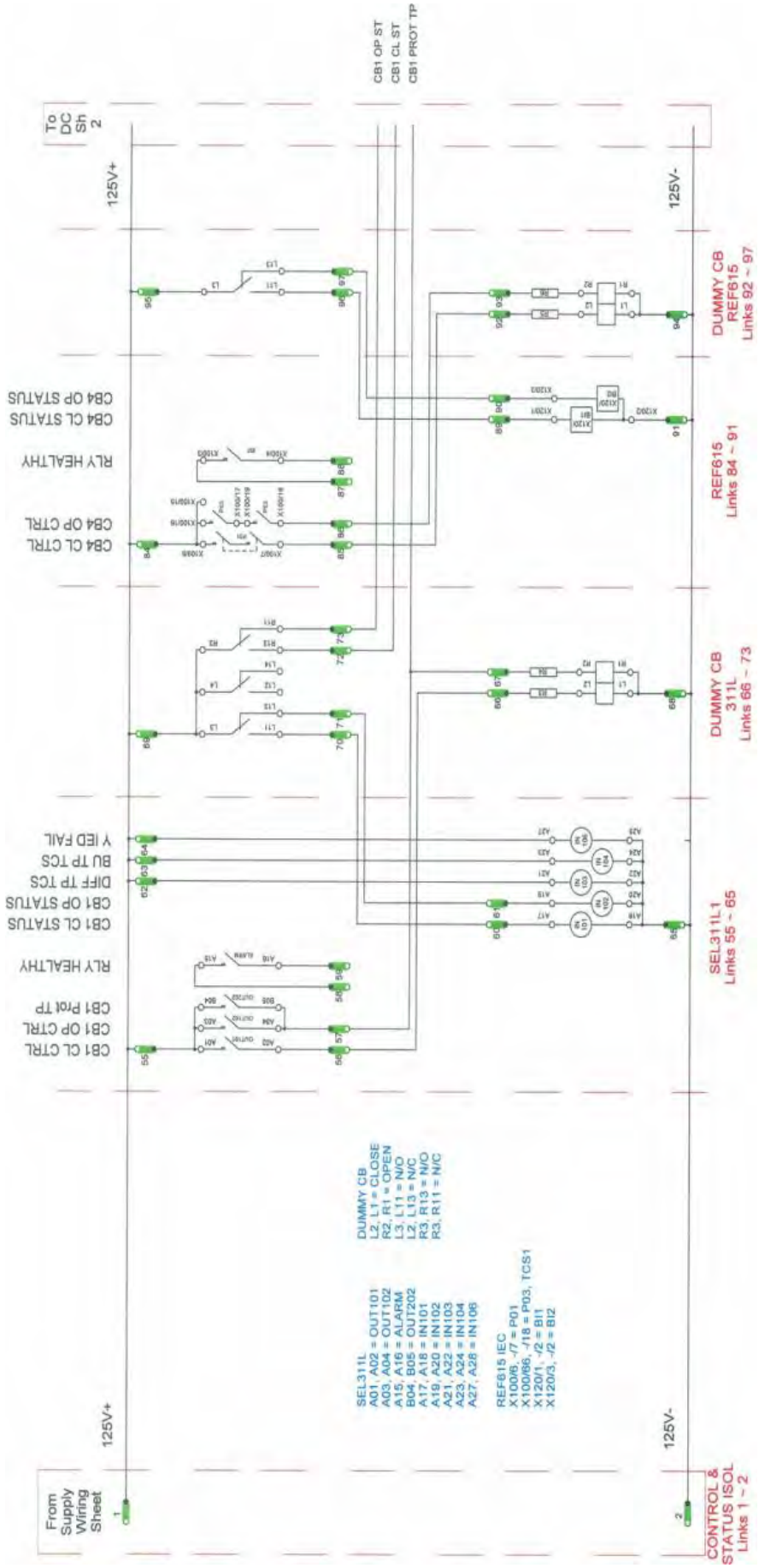


Figure 3.4: SEL-311L and REF615 (DC wiring)

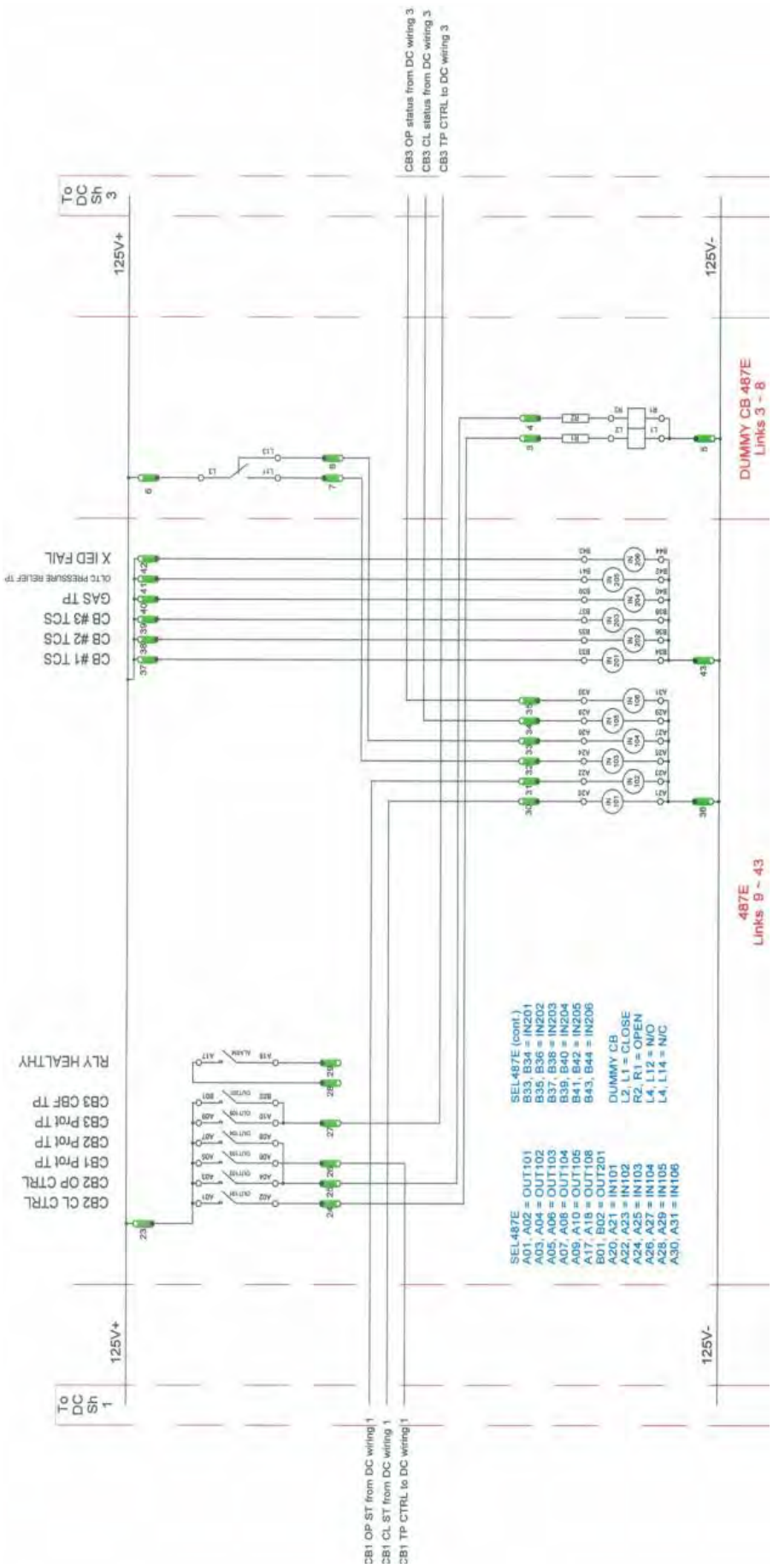


Figure 3.5: SEL-487E (DC wiring)

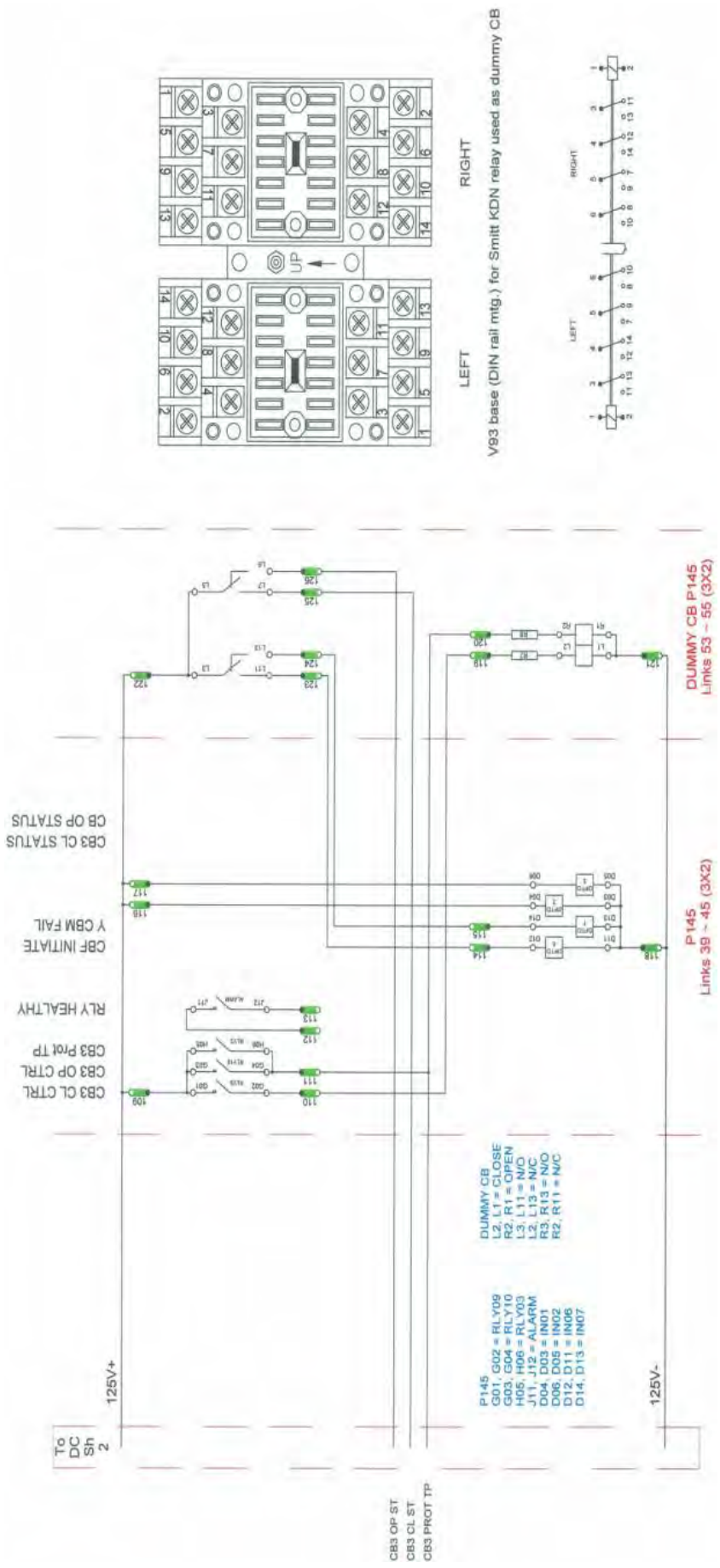


Figure 3.6: P145 (DC wiring)

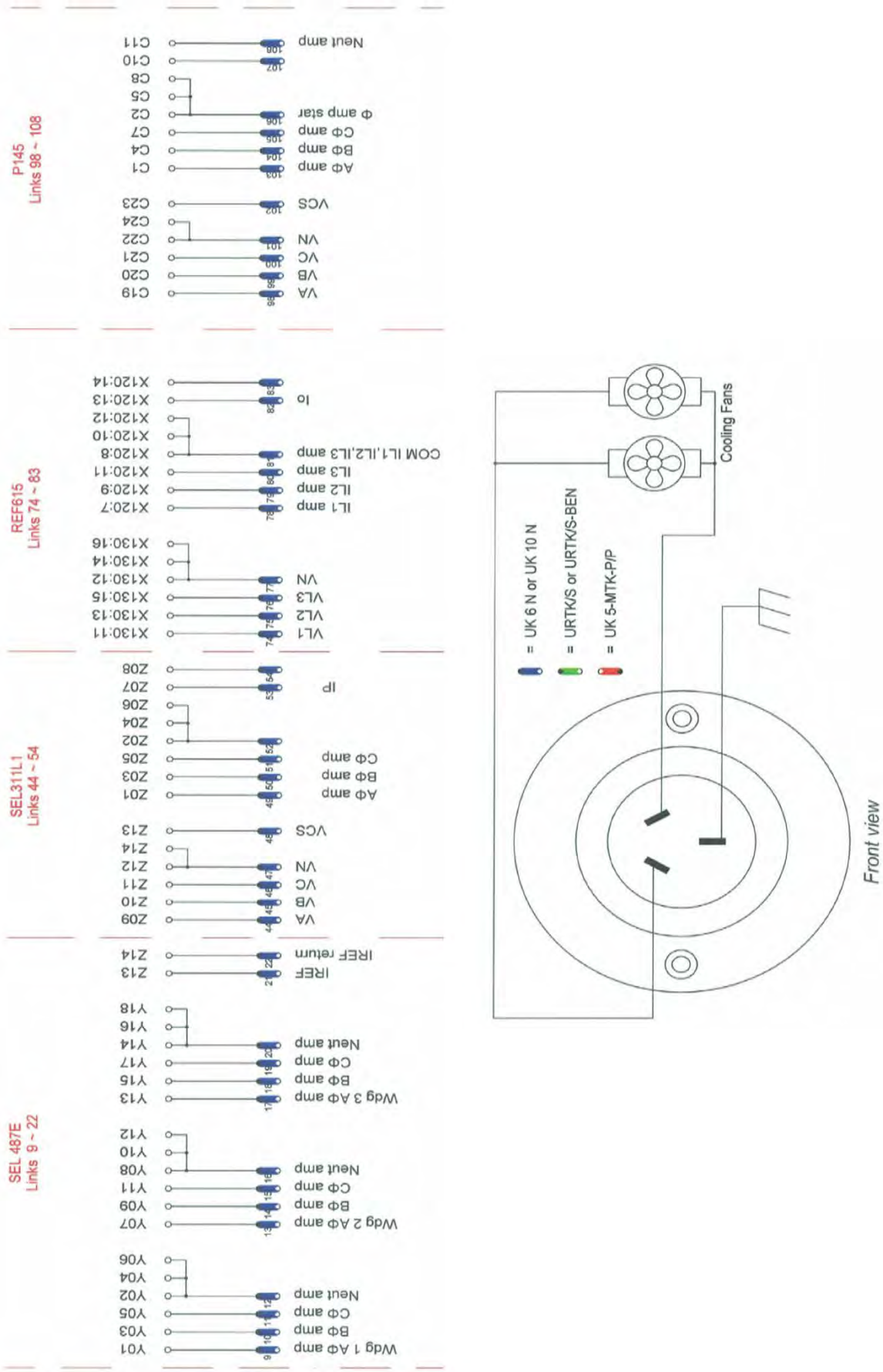


Figure 3.7: Cooling fans (AC wiring)

3.5 Conclusion

This chapter discussed the types of hardware inventory used throughout the construction of the portable IEC61850 testing unit by presenting AC and DC wiring schematics. The rig is assembled using Ethernet and fibre optic technologies as opposed to conventional hardwired copper. The cost over life cycle of the installation allows for the utilisation of GOOSE messages by creating virtual links between IEDs.

Chapter 4 – GOOSE Interoperability

4.1 Introduction

The purpose of this chapter is to provide a synopsis of the individual and overall system configurations necessary to configure, map and simulate GOOSE messages using relay specific softwares. The chapter presents concepts related to logical nodes, operating characteristics and grading margins to assist in interoperability. A virtual wiring map, flow chart and mapping matrix representing the publisher and subscriber commands at each IED is considered in the form of an CID, ICD, SCD or SCL file. Technical issues and troubleshooting is further assessed during commissioning of the portable IEC61580 testing unit.

4.2 Logical Nodes

Logical nodes are named groupings of data services that are logically related to some power systems function. They are categorised into 13 groups including automatic control (A), supervisory control (C), generic functions (G), interfacing (I), system nodes (L), metering and measurement (M), protection (P), protection related (R), sensors (S), instrument transformers (T), switchgear (X), power transformers (Y) and other equipment (Z) [43]. Logical nodes are identified by four mnemonic characters (i.e. XCBR for a circuit breaker) as depicted in Table 4.1. The XCBR logical node has several data attributes such as 'Loc' for determining remote and local operation, 'OpCnt' for count operation, 'Pos' for switch positioning, 'BlkOpn' for blocking breaker open commands, 'BlkCls' for blocking breaker close commands and 'CBOpCap' for circuit breaker operating capability.

Table 4.1: Anatomy of the XCBR logical node

XCBR class			
Attribute Name	**Attr. Type**	**Explanation**	**M/O**
LN Name		Shall be inherited from Logical-Node Class (see IEC 61850-7-2)	
Data			
Common Logical Node Information			
		LN shall inherit all Mandatory Data from Common Logical Node Class	M
Loc	SPS	Local operation (local means without substation automation communication, hardwired direct control)	M
EE Health	INS	External equipment health	O
EE Name	DPL	External equipment name plate	O
OpCnt	INS	Operation counter	M
Controls			
Pos	DPC	Switch position	M
BlkOpn	SPC	Block opening	M
BlkCls	SPC	Block closing	M
ChaMotEna	SPC	Charger motor enabled	O
Metered Values			
SumSwARs	BCR	Sum of Switched Amperes, resetable	O
Status Information			
CBOpCap	INS	Circuit breaker operating capability	M
POWCap	INS	Point On Wave switching capability	O
MaxOpCap	INS	Circuit breaker operating capability when fully charged	O

Data Name — Common Data Class — Mandatory/ Optional

Each element of data within a logical node conforms to the specification of a Common Data Class (CDC) by describing the type of data structure. There are CDCs for status information, measured information, controllable status information, controllable analog set point information, status settings and analog settings [43]. These data objects are mandatory, optional or conditional. In the process of mapping an object, the IEC61850 specifies the method of transforming the logical information into a Generic Object Oriented Substation Event (GOOSE) message or Manufacturing Message Specification (MMS) variable that results in a unique object name. For example, if a logical device referred to as 'Relay 1' consists of a single circuit breaker logical node 'XCBR1' that performs local communication, the object name will be assigned as in Figure 4.1.

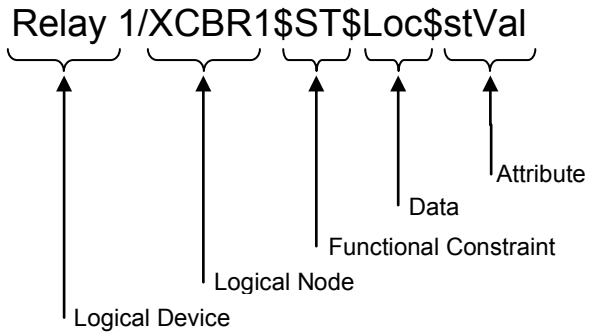


Figure 4.1: Structure of an object name

4.3 Configuration Flow

Although some proprietary tools are free to download, others demand expensive license files which are accessible from the manufacturer. A total of five software tools were used to configure the IEDs of the portable IEC61850 testing unit including AcSELerator Quickset, AcSELerator Architect, MiCOM S1 Studio, PCM600 and CCT. These softwares are used to create and edit settings, view graphical logic and access templates. OMICRON's QuickCMC and IEDScout are used to inject current and voltage signals, along with detecting GOOSE messages on the network. The GPS clock on the other hand is set using the SEL-5860 Time Service application which synchronises each device through time stamping of events. Figure 4.2 illustrates the substation layout of the portable IEC61850 testing unit based on a breaker failure scheme.

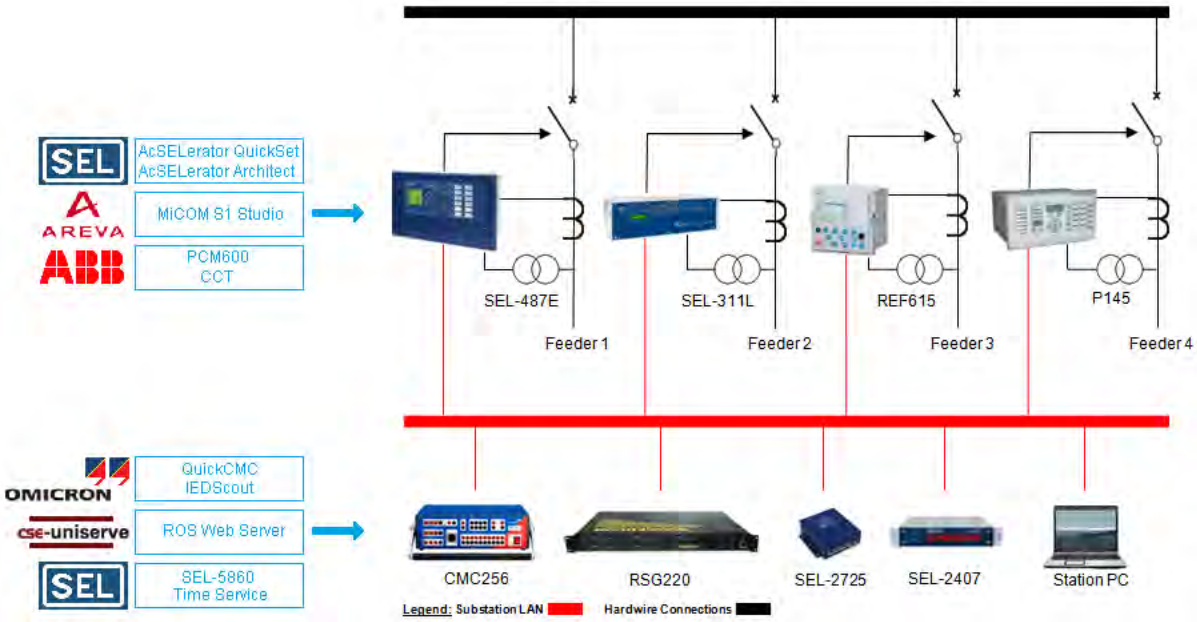


Figure 4.2: Substation layout

Part 6 of the IEC61850 standard introduces four common file types including Configured IED Description (CID), IED Capability Description (ICD), Substation Configuration Description (SCD) and System Specification Description (SSD) [44]. Each of these file types are shown in the configuration flow of Figure 4.3. The ICD files are imported into the IEC61850 system configurator, which allows the configuration of GOOSE messages by specifying the publisher and subscriber of the messages. The system configurator creates a SCD file, which consists of a single line diagram of the station and descriptions of GOOSE messages. The proprietary tools must import the SCD file and extract the information needed for the IEDs to achieve interoperability. However,

some misconceptions exist in terms of the type of SCL file to be generated. Most IEDs export only ICD files, while others export CID files. This leads to problems when downloading the final configuration files into the IEDs, resulting in manufacturers transmitting their files through IEC61850 file services or proprietary protocols designed for file transfer [44].

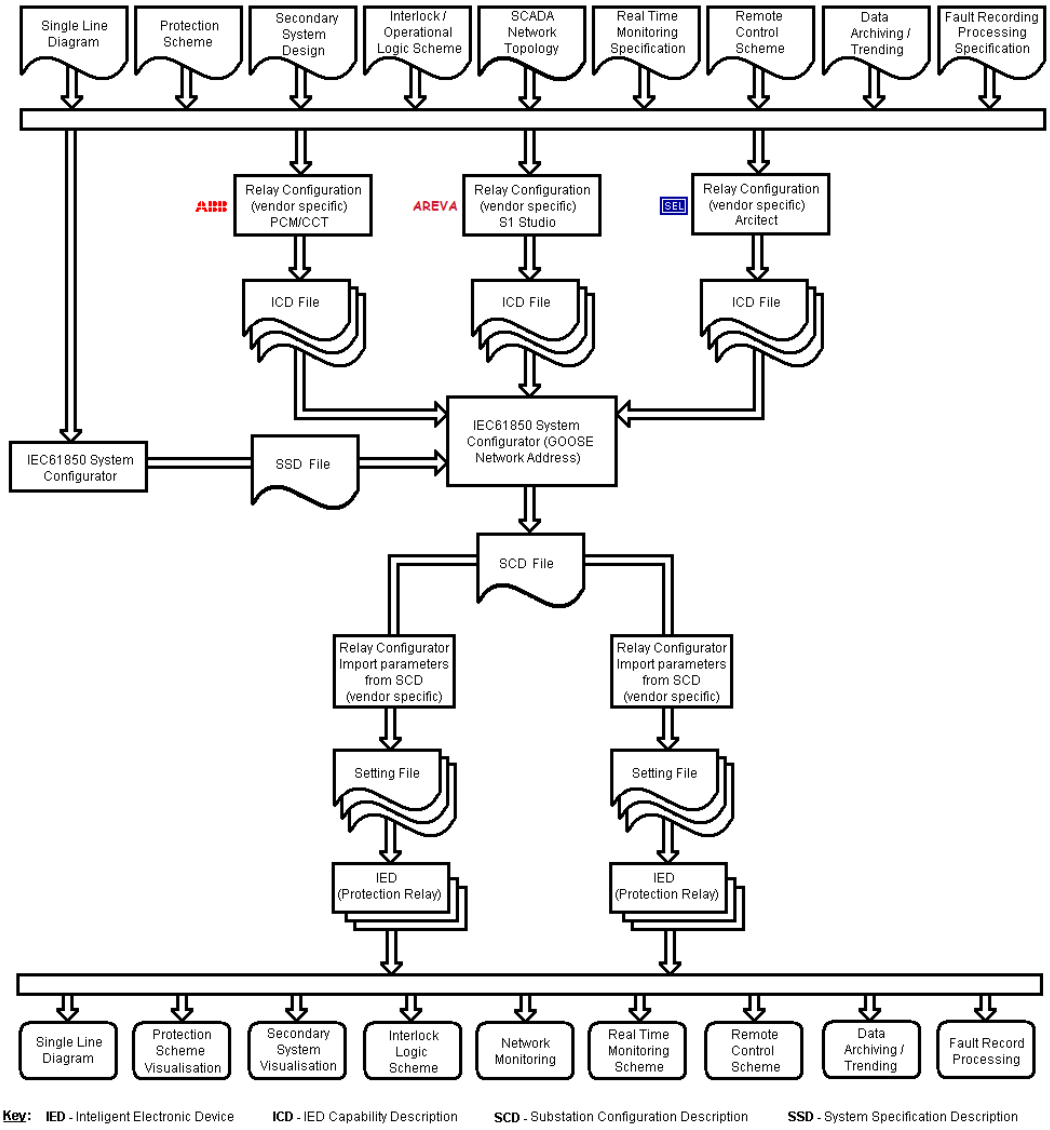


Figure 4.3: Configuration flow

4.4 Virtual Wiring Map

A virtual wiring map incorporates Boolean logic in the form of OR gates to direct IED message flow. All IEDs are assigned to certain GOOSE bits in order to execute control and protection functions. For example, in the virtual wiring map of Figure 4.4, GOOSE bit (SEL487EGOOSE.Bit6) is activated once the circuit breaker of the SEL-487E is closed. This gives the reverse effect to trip contact OUT101, which triggers an open

status across the circuit breaker. The 'red' indicator on the dummy CB will signal an open command, while a 'green' indicator will signal a close command. Function keys and push buttons are also set to light up LEDs and transmit texts. For example, using bit (REF615GOOSE.Bit3) the SEL-311L displays 'GOOSE from REF615'.

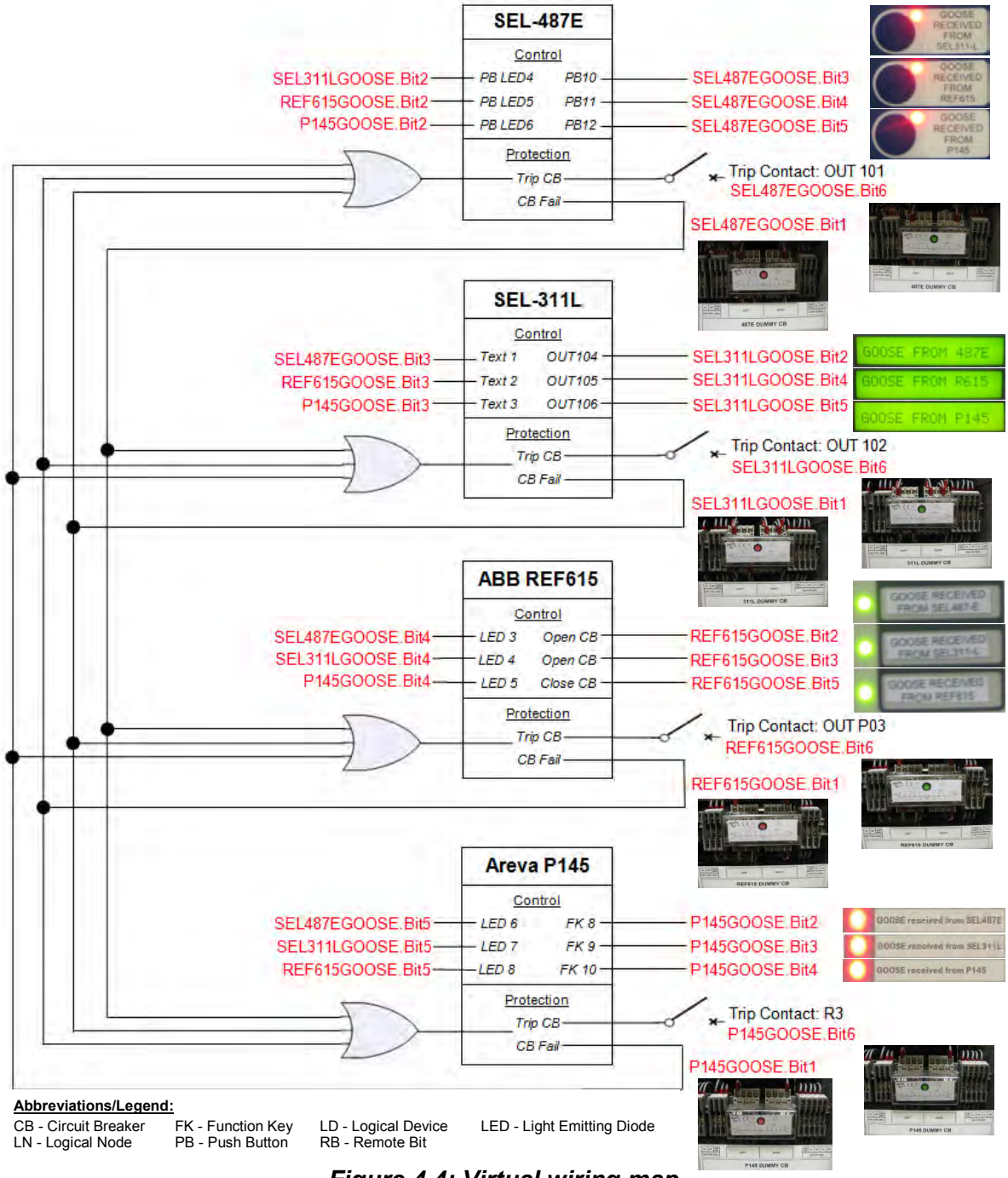


Figure 4.4: Virtual wiring map

4.5 GOOSE Configuration

There are two types of methods available in order to configure the portable IEC61850 testing unit including using a independent IEC61850 system configurator or vendor

specific software packages. The latter approach is adopted in this research, seeing as it allows manual configuration of datasets and logical nodes, along with the import and export of GOOSE messages. A complete rundown of the steps necessary to configure the relays, Ethernet switches and GPS clock is examined.

4.5.1 RSG2200

The RSG2200 9-Port Managed Gigabit Ethernet Backbone Switch makes use of the Rugged Operating System (ROS) Web Server interface to configure the switch. The ROS Web Server interface uses a secure communications method called Secure Socket Layer (SSL) to encrypt and maintain confidential traffic exchange [40]. To login to the ROS Web Server a browser session must commence in order to enter a URL which specifies the host name and IP address of the switch. The IP address used for the RSG2200 is set to 192.168.2.50. For administrator rights of the switch a valid user name and password must be entered. The user name and password by default is 'admin'. Figure 4.5, illustrates the main menu login screen of the ROS Web Server with extended sub-menus for the Administration, Ethernet Ports and Virtual LANs.

Figure 4.5: Main menu screen of ROS web server

The *Administration* menu provides administrative parameters for both device and network (i.e. local service availability, security methods, system identification and IP

network functionality). The *Ethernet Port* menu covers physical settings of port allocations (i.e. configuring port alarms, rates and statuses). The *Virtual LAN* menu manages traffic identification in the form of logical frames (i.e. tagged or untagged operation and GVRP support).

A RSG232 over RJ45 cable is required for temporary serial connection between the PC and switch. The cable features a DB9-female and RJ45-male pin-out specification as depicted in Table 4.2. The cable requires settings of 57600 baud, no parity bits, 8 data bits and 1 stop bit.

Table 4.2: RS232 over RJ45 cable pin-out

RuggedCom RS232 over RJ45 pin-out specification		
Signal Name (PC is DTE)	**DB9-Female**	**RJ45-Male**
DCD - Carrier detect	1	2
RxD - Receive data (to DTE)	2	5
TxD - Transmit data (from DTE)	3	6
DTR - Data terminal ready	4	3
GND - Signal GND	5	4
DSR - Data set ready	6	1*
RTS - Ready to send	7	8
CTS - Clear to send	8	7
RI - Ring indicator	9	1*

The *System Identification* form of Figure 4.6 consists of three parameters including the System Name, Location and Contact. The 'System Name' parameter is used to identify the switch provided that other switches in the network have unique names. The 'Location' parameter is used to indicate the physical position of the device (i.e. zone, substation, state or country). The 'Contact' parameter is used to single out the persons responsible for configuring the switch in case of an emergency.

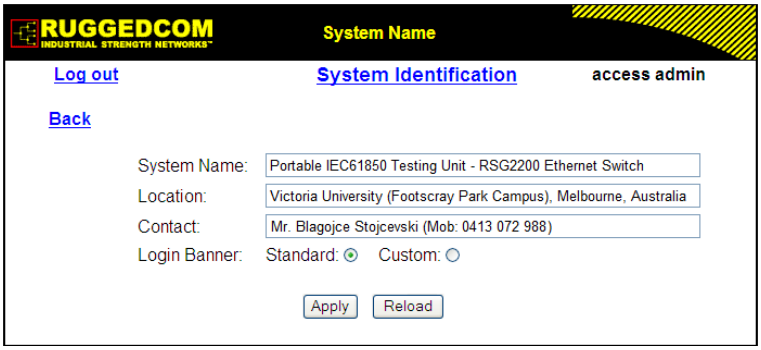


Figure 4.6: System identification form

The *System Time Manager* form enables the viewing and setting of the local time and date (Figure 4.7). The 'Time' parameter is set in format HH:MM:SS, whereas the 'Date' parameter is characterised by MMM DD, YYYY. A range of time zones are present

using Universal Coordinated Time (UCT) banners such as UTC+10:00 (Melbourne and Sydney). These banners allocate the transition between standard and Daylight Saving Time (DST).

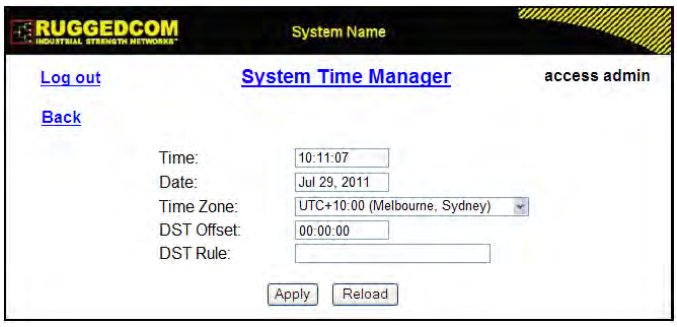


Figure 4.7: System time manager form

The *IP Interface* form allows the configuration of IP addresses, types and subnets. A single VLAN type must be allocated as the management (Mgmt) device interface, which permits an IP address type in the form of static, DHCP, BOOTP or dynamic. The static IP address type refers to the manual assignment of an IP address while the others suggest automatic assignment. DHCP is used in LAN environments to dynamically assign IP addresses from a centralised server, which reduces the overhead of administrating IP addresses. BOOTP is a subset of the DHCP protocol which supports the transfer of a BOOTFILE. The BOOTFILE corresponds to any valid ROS file such as config.csv. The name of the BOOTFILE on the BOOTP server must match the corresponding ROS file. The dynamic IP address type refers to a combination of BOOTP and DHCP protocols where the system tries to register data in a round-robin approach until it receives a response from the corresponding server. Figure 4.8 illustrates several VLAN interfaces assigned to distinct IP addresses, ID's and subnets. The RSG2200 is configured as the management device interface and has a VLAN ID of 1. All other relays are assigned with a VLAN ID of 5 given that they act as a slave and must report back to the switch.

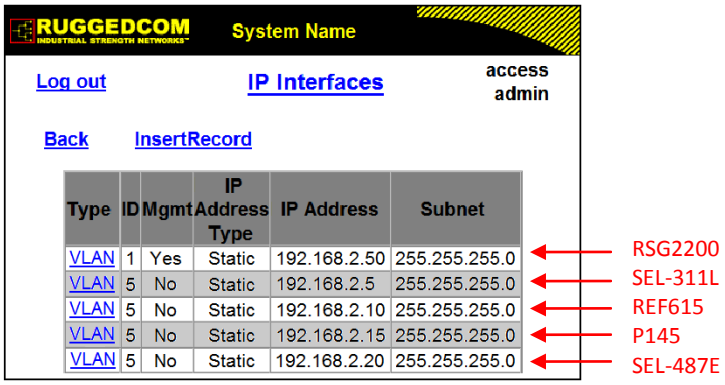
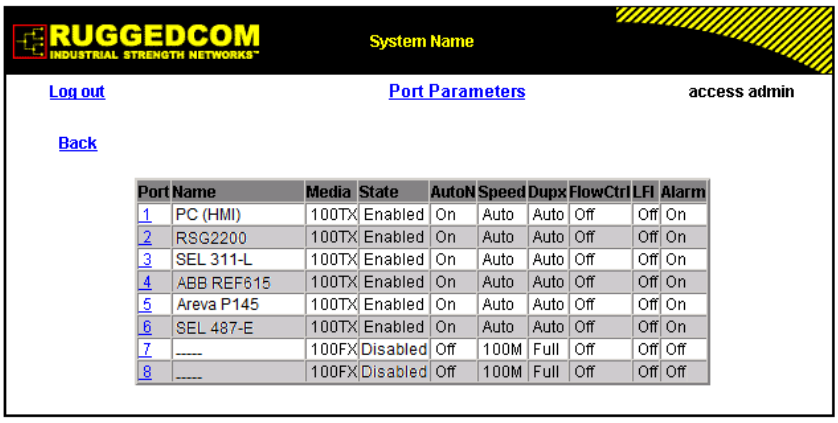


Figure 4.8: IP interfaces form

Figure 4.9 illustrates the physical properties of the *Port Parameters*. A descriptive maximum 15 character name is used to identify devices connected to a port. The type of port media is set to either 100TX, 10FL, 100FX, 1000X, 1000T. The 'State' parameter may be disabled or enabled to prevent frames from being sent and received during link detection. Auto-Negotiation (AutoN) is forced 'ON' when the port speed is set to 1Gbps and forced 'OFF' when the port speed is set to 100Mbps. The 'Duplex' parameter is configured to half or full operation given that it does not support Auto-Negotiation. Full duplex operation requires both ends of the port to be configured due to server frame losses occurring during heavy network traffic. The 'Link-Fault-Indication' (LFI) parameter directs transmission flow when an existing link has failed. This enables the device at the far end of operation to detect any link failure under all circumstances.



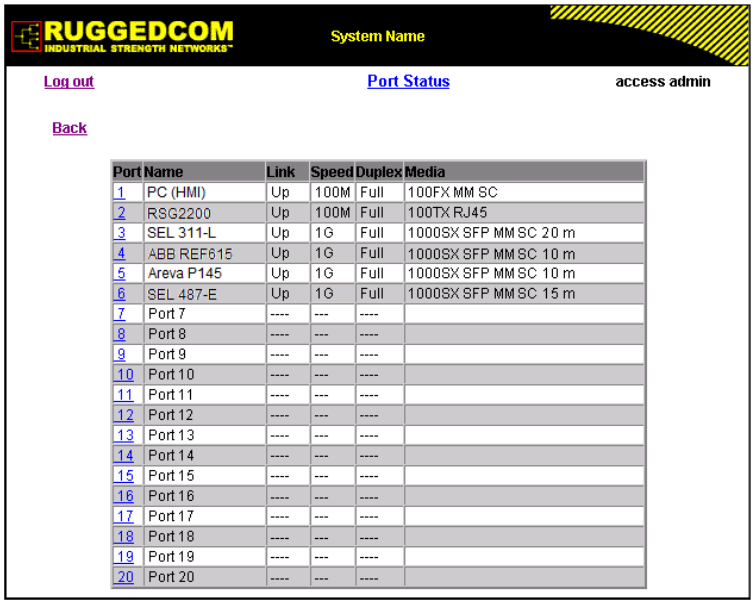
Port	Name	Media	State	AutoN	Speed	Dupx	FlowCtrl	LFI	Alarm
1	PC (HMI)	100TX	Enabled	On	Auto	Auto	Off	Off	On
2	RSG2200	100TX	Enabled	On	Auto	Auto	Off	Off	On
3	SEL 311-L	100TX	Enabled	On	Auto	Auto	Off	Off	On
4	ABB REF615	100TX	Enabled	On	Auto	Auto	Off	Off	On
5	Areva P145	100TX	Enabled	On	Auto	Auto	Off	Off	On
6	SEL 487-E	100TX	Enabled	On	Auto	Auto	Off	Off	On
7	-----	100FX	Disabled	Off	100M	Full	Off	Off	Off
8	-----	100FX	Disabled	Off	100M	Full	Off	Off	Off

Figure 4.9: Port parameters form

The *Fast Link Detection* form provides system protection against faulty devices generating irregular signals. When a faulty device or fibre optic port is connected to the switch, a large number of continuous state changes are reported in a short period of time. These state changes can result in the system being unresponsive. Consequently, three parameters are available to detect such state changes including ON, OFF and ON_withPortGuard. The 'ON' parameter is used only in special cases where prolonged state changes constitute legitimate link operation. The 'OFF' parameter permanently disables Fast Link Detection. The 'ON_withPortGuard' parameter uses the Port Guard feature to generate an alarm to warn users of bouncing if excessive link state changes persist for more than two minutes. By disabling Fast Link Detection on the port, excessive link state changes fail to consume a substantial amount of system resources. Figure 4.10 illustrates the Fast Link Detection form.

Figure 4.10: Fast link detection form

The *Port Status* form evaluates if the link is up or down during operation. The 'Media' parameter provides users with the description of installed fibre optic modes in the form of Single Mode (SM), Multi Mode (MM), Short Distance (SD), Long Distance (LD) and Very Long Distance (VLD). Figure 4.11 represents Port 1 as being assigned to the PC at a rate of 100Mbps. Port 2 is assigned to the RSG2200 Ethernet switch, which embraces an RJ45 connection. Ports 3-6 are rated at 1Gbps and are all considered Small Factor Pluggable (SFP) devices capable of multi-mode operation and offer fibre optic connections between 10-20 meters.



Port	Name	Link	Speed	Duplex	Media
1	PC (HMI)	Up	100M	Full	100FX MM SC
2	RSG2200	Up	100M	Full	100TX RJ45
3	SEL 311-L	Up	1G	Full	1000SX SFP MM SC 20 m
4	ABB REF615	Up	1G	Full	1000SX SFP MM SC 10 m
5	Areva P145	Up	1G	Full	1000SX SFP MM SC 10 m
6	SEL 487-E	Up	1G	Full	1000SX SFP MM SC 15 m
7	Port 7	----	---	----	
8	Port 8	----	---	----	
9	Port 9	----	---	----	
10	Port 10	----	---	----	
11	Port 11	----	---	----	
12	Port 12	----	---	----	
13	Port 13	----	---	----	
14	Port 14	----	---	----	
15	Port 15	----	---	----	
16	Port 16	----	---	----	
17	Port 17	----	---	----	
18	Port 18	----	---	----	
19	Port 19	----	---	----	
20	Port 20	----	---	----	

Figure 4.11: Port status form

The *Port VLAN Parameter* form introduces four types of VLAN memberships including Edge, Trunk, PVLANEdge and QinQ. The 'Edge' parameter consists of a single native VLAN port which is set using the PVID attribute. The 'Trunk' parameter is automatically configured to support all VLAN ports. Frames transmitted out of this port are tagged with the exception of the native VLAN. The 'PVLANEdge' parameter is only a member of one VLAN and does not forward traffic to other PVLANEdge ports within the same VLAN. It conforms to a feature of the switch whereby multiple VLAN Edge ports on a single device are effectively isolated from one another. All VLAN Edge ports

are 'protected' in this way and are prohibited from sending frames to each other. However, these frames are still allowed to send frames to other 'non-protected' ports within the same VLAN. This protection extends to all traffic on the VLAN (i.e. unicast, multicast or broadcast). The 'QinQ' parameter is a t runk port using double-VLAN tagging or nested VLANs. An extra VLAN tag is added to all frames allocated to this port given that a single VLAN tag is stripped from frames entering the port.

The 'Port VLAN Identifier' (PVID) parameter specifies the VLAN ID associated with untagged and tagged frames. By default, the switch is programmed to use VLAN 1 for management. The 'Generic VLAN Registration Protocol' (GVRP) parameter automatically distributes VLAN configuration information. Each switch in a network needs only to be configured with VLANs it requires locally. GVRP-aware is configured for a particular VLAN ID which can be connected to a trunk via GVRP BPDUs. When a switch sends GVRP BPDUs out of all GVRP-aware ports, GVRP BPDUs advertise all the VLANs known to that switch (configured manually or learned dynamically through GVRP) to the rest of the network. Three modes of GVRP operation are available including Disable, Advertise Only and Advertise & Learn (Figure 4.12). The Disable operation signifies the port is not capable of any GVRP processing. Advertise Only permits VLANs to be declared, but not learned. Advertise & Learn allows all VLANs to be dynamically declared and learned. Only trunk ports are GVRP capable.

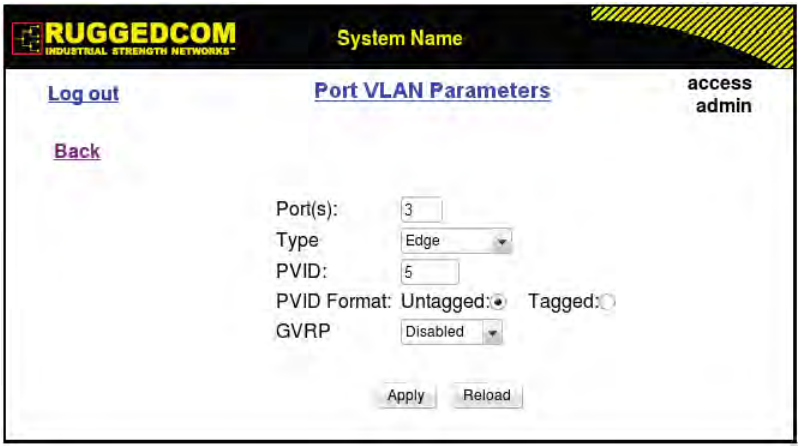


Figure 4.12: Port VLAN parameters form

4.5.2 SEL-311L

The SEL-311L Line Current Differential Protection and Automation Relay makes use of the AcSELerator Quickset and AcSELerator Architect softwares. Subsequent to launching the start-up menu of the AcSELerator Quickset program (Figure 4.13), the

user is provided the option of creating, reading or opening new, existing or saved settings. For new projects, it is recommended to click the 'New' parameter button which activates the Settings Editor Selection form as shown in Figure 4.14.

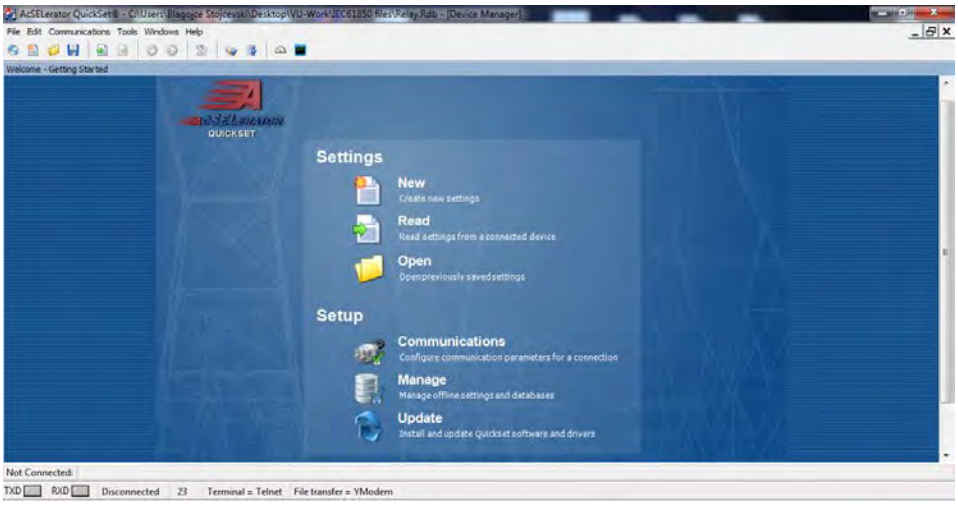


Figure 4.13: AcSELerator Quickset start-up menu

The *Settings Editor Selection* form prompts the user to choose the device family, model and version of the relay. If the relay is not listed in the device family grouping, it is necessary to associate the relay via the 'Install Devices' parameter. This leads to the setup of the Device Part Number as shown in Figure 4.15.

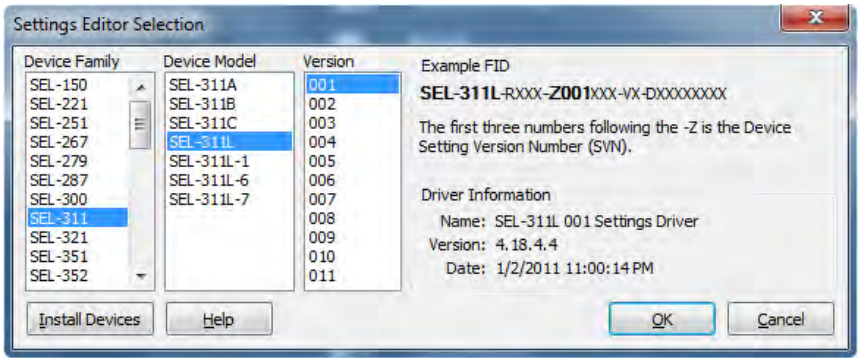


Figure 4.14: Settings editor selection form

The *Device Part Number* is used to determine the intrinsic characteristics and physical properties of the relay and is noticed on the back of the device in the form of a barcode. The part number of the SEL-311L has a standard firmware version with enhanced features for functions. The line current differential channels X and Y are set to fibre optic and have a secondary input current of 5A. A total of 8 inputs and 12 outputs are built-in to the board and allow both Ethernet and IEC61850 communication. Failure to enter the correct part number will result in non-recognition of the relay.

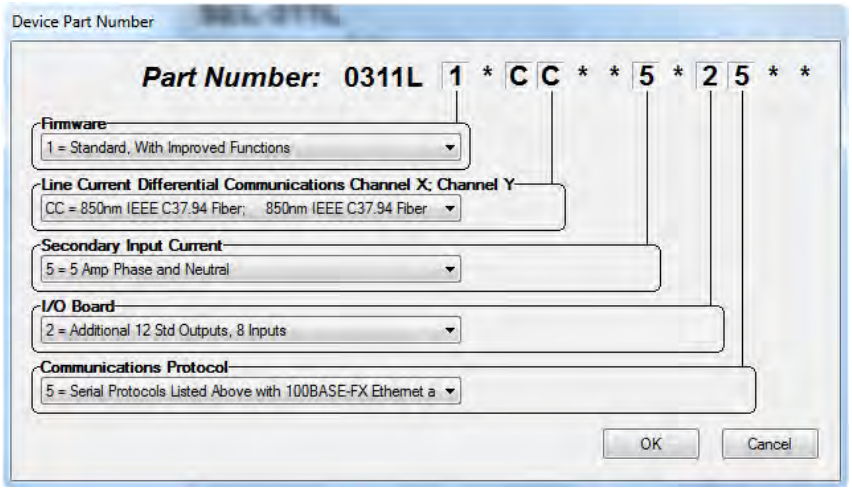


Figure 4.15: Device part number

The navigation panel on the left-hand side of the main screen is used to set the Group 1 settings by expanding the '+' symbol. *General Settings* have two identifier labels including the Relay Identifier (RID) and Terminal Identifier (TID). The RID is typically used to identify the relay or type of protection scheme. The TID label is used to declare the substation name or line terminal. These tags appear in all reports for easy analysis and reporting. The CT ratio can be set independently through equation (4.1) to determine the Current Transformer Ratio (CTR) and Potential Transformer Ratio (PTR). Considering the range is between 1 to 6000 for CTR, the local CT ratio of 1/7 is multiplied by a factor of 7 to provide a ratio of 7/49.

$$CT_{ratio} = \frac{CTR}{PTR} = \frac{1/7}{1/1} = \frac{1}{7} \cong \frac{7}{49} \tag{4.1}$$

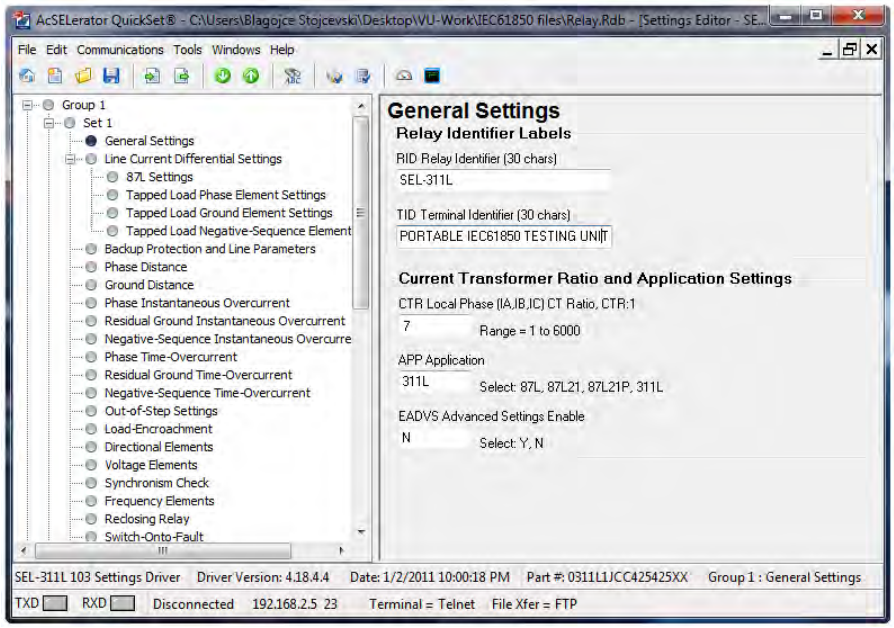


Figure 4.16: General settings

The line impedance parameters Z1MAG, Z1ANG, Z0MAG and Z0ANG are set by converting the primary impedances into secondary quantities. There are four primary impedances including $Z_{1(0-75\text{km})} = 28.873\angle 69.64^\circ$, $Z_{2(75-150\text{km})} = 45.812\angle 65.54^\circ$, $Z_{3(150-225\text{km})} = 74.047\angle 65.10^\circ$ & $Z_{4(225-300\text{km})} = 97.344\angle 65.09^\circ$. The secondary quantities are calculated using equation (4.2). The EFLOC Fault Locator option must be enabled (Figure 4.17).

$$Z_{\text{Secondary}} = Z_{\text{Pr imary}} \times \frac{\text{CTR}}{\text{PTR}} \qquad (4.2)$$
$$= 28.873 \times \frac{7}{49} = 4.12471\Omega$$

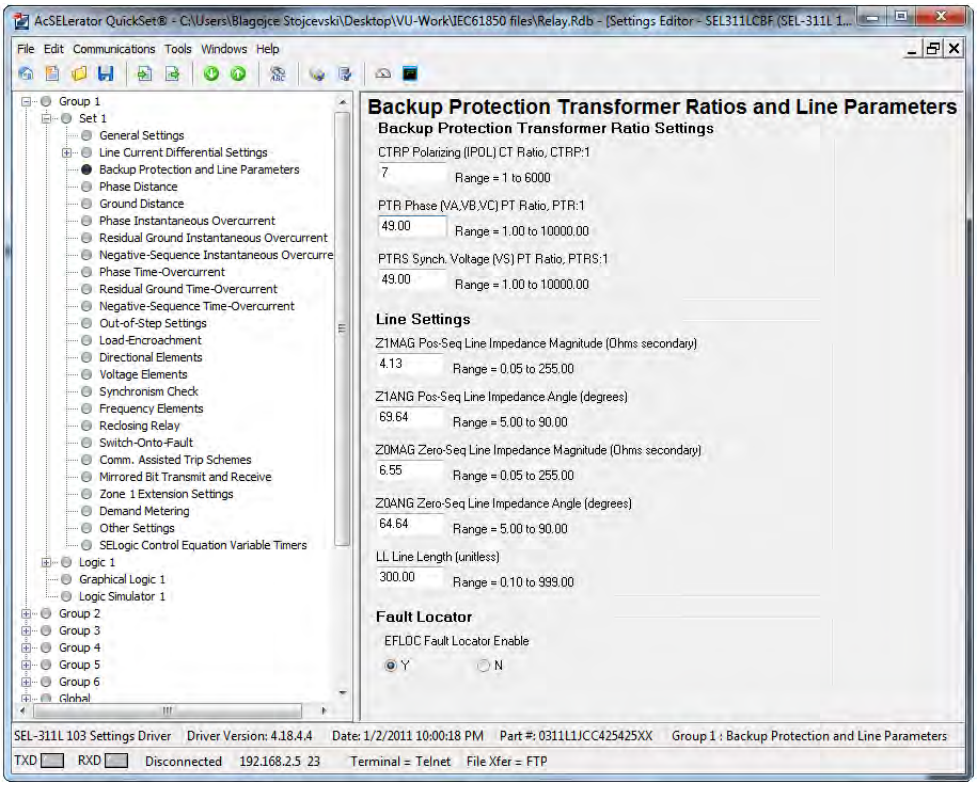


Figure 4.17: Backup protection transformer ratios and line parameters

The reach settings are set using the *Phase Distance Elements* form (i.e. at 30%, 50%, 70% and 90% of the protected line impedance). The ECCVT Transient Detection parameter is disabled given that CCVT is only required if the Source Impedance Ratio (SIR) is greater than 5. To set the zones, the secondary impedance is multiplied by the reach as expressed in equation (4.3).

$$Z_{1\,\text{Pr imary}} = \text{Re ach} \times Z_{1\text{Secondary}} \qquad (4.3)$$
$$= 0.30 \times 4.13 = 1.239\Omega$$
$$= 0.50 \times 6.55 = 3.275\Omega$$
$$= 0.70 \times 10.5781 = 7.405\Omega$$
$$= 0.90 \times 13.9063 = 12.516\Omega$$

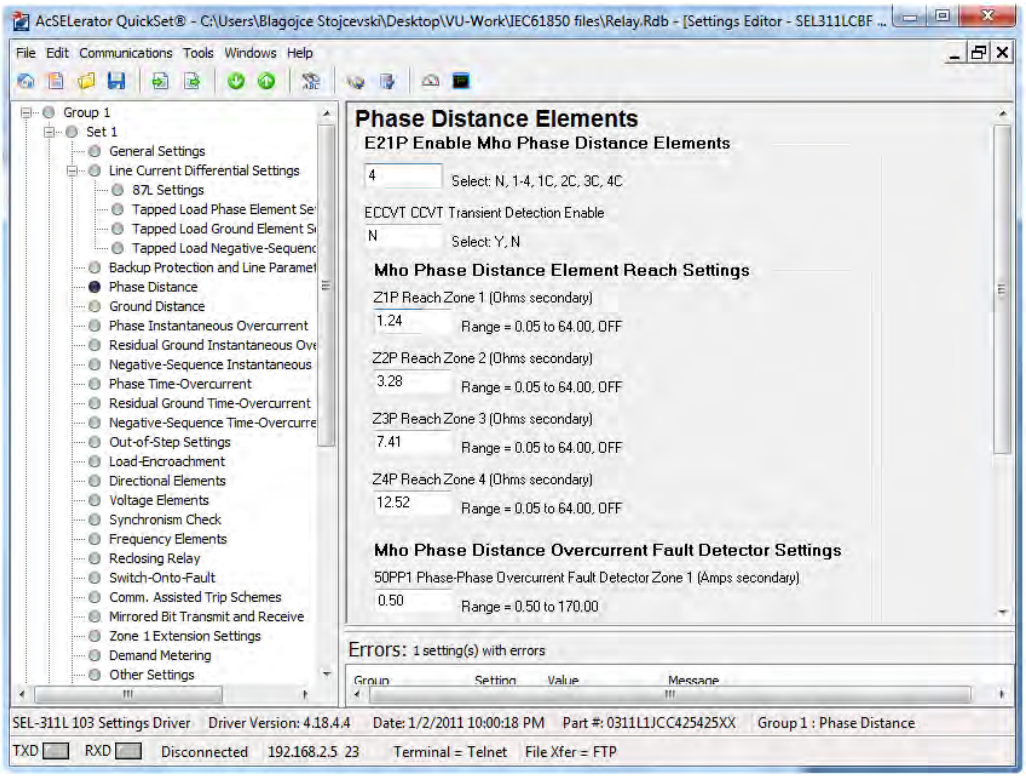


Figure 4.18: Phase distance elements

The reach settings remain unchanged during the setting of the *Ground Distance Elements*. The SEL-311L uses equation (4.4) to determine the magnitude and angle of the compensation factor. Zone 1 is set with a time delay of zero cycles given that a fault is intended to trip instantaneously. Zones 2, 3 and 4 are set with a time delay of 10, 20 and 30 cycles in order to time grade the backup protection. Time grading is achieved by proper discrimination of the relay. The best convention is to ensure that the IEDs furthest from the source have current settings equal to or less than adjacent IEDs [7]. Discrimination can be carried out by either time, current or a combination of time and current principles. Discrimination by time alone result in the fault being cleared at the longest possible operating time, whereas discrimination by current produces considerable impedances between the circuit breakers. Due to these limitations, a combination of time and current coordination is used to achieve fast fault tripping and clearance times. If the grading margin is insufficient, all four IEDs in the portable IEC61850 testing unit will operate at the same time. This will cause problems when detecting the fault location. The grading margin must therefore take into consideration factors such as the circuit breaker interrupting time, overshoot and safety margin [10].

$$k_{01} = \frac{Z_0 mag \angle Z_0 ang - Z_1 mag \angle Z_1 ang}{3 \times Z_1 mag \angle Z_1 ang} \qquad (4.4)$$

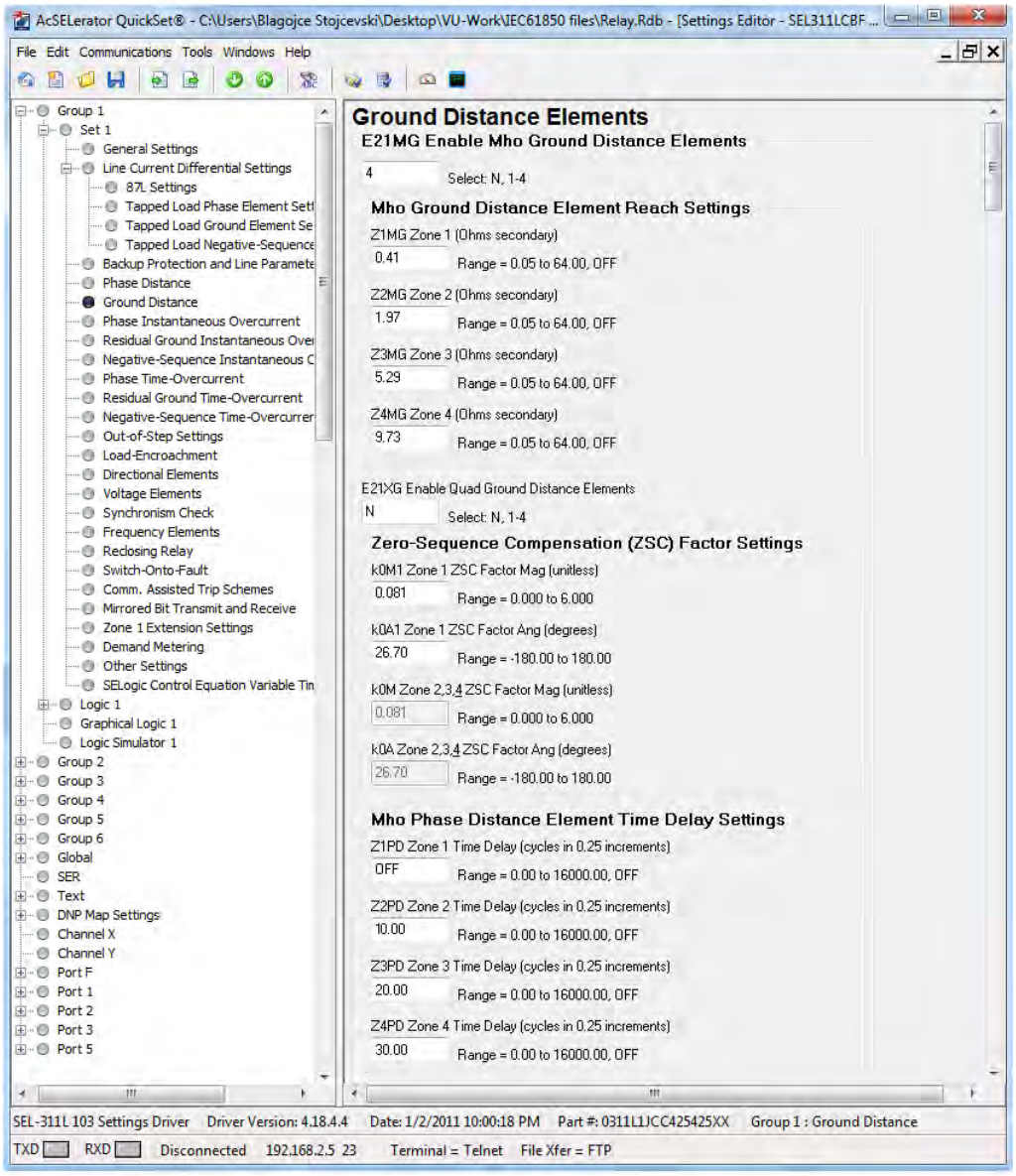


Figure 4.19: Ground distance elements

The IEDs are graded using operating time characteristics such as Definite Time, Standard Inverse, Very Inverse, Extremely Inverse and Long Time Standby Earth Faults [37]. All IEDs are provided with a number of tap or plug settings, each of which represent the minimum current the relay will start to operate. This is referred to as the minimum pickup value [10]. The Time Dial setting may be extremely long and unpredictable resulting in small deviations and significant time changes. Vendors generally do not show their curves below 1.5 to 2.0 times the minimum pickup [37]. Two factors must therefore be considered during grading of IEDs including the Time Multiplier Setting (TMS) and Plug Setting Multiplier (PSM). The TMS controls the relay movement, while the PSM determines the current at which the relay will start to operate. Figure 4.20 illustrates several IEC operating characteristics.

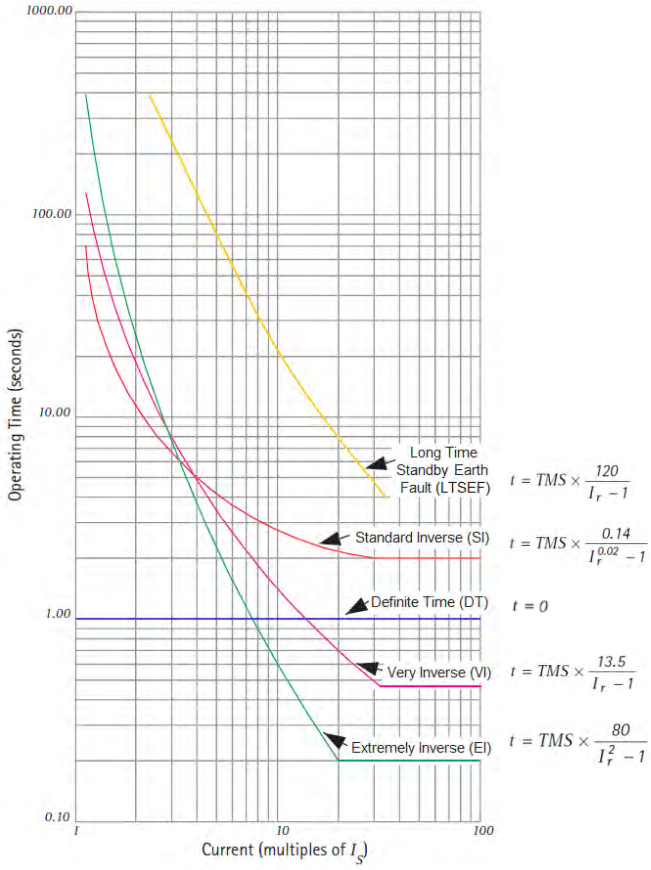


Figure 4.20: IEC operating characteristics

The TMS and PSM are expressed by equations (4.5) and (4.6).

$$TMS = \frac{T}{T_m} = \frac{T \times \left[(PSM)^{\alpha} - 1.0\right]}{K} \tag{4.5}$$

$$PSM = \frac{I}{I_S} \tag{4.6}$$

where: $T = K \times \dfrac{TMS}{\left(\dfrac{I}{I_S}\right)^{\alpha} - 1.0}$

K = constant { 0.14 Standard Inverse; 13.5 Very Inverse; 80.0 Extremely Inverse; 120 Long Standby Earth Current

α = constant { 0.02 Standard Inverse; 1.0 Very Inverse; 2.00 Extremely Inverse; 1.0 Long Standby Earth Current

I = Fault current (Amperes)

I_S = Relay current threshold setting – tap/plug setting (Amperes)

T_m = Time obtained from the operating characteristic curve at TMS=1.0, while using the PSM equivalent of the maximum fault current.

The *Phase Time-Overcurrent Element* form is used to configure the SEL-311L as shown in Figure 4.21. As a rule of thumb, the pickup value must be set lower than the minimum fault current, but 1.25 times greater than the maximum load current [37]. The SEL-311L is configured with a Class A Standard Inverse (C1) operating curve.

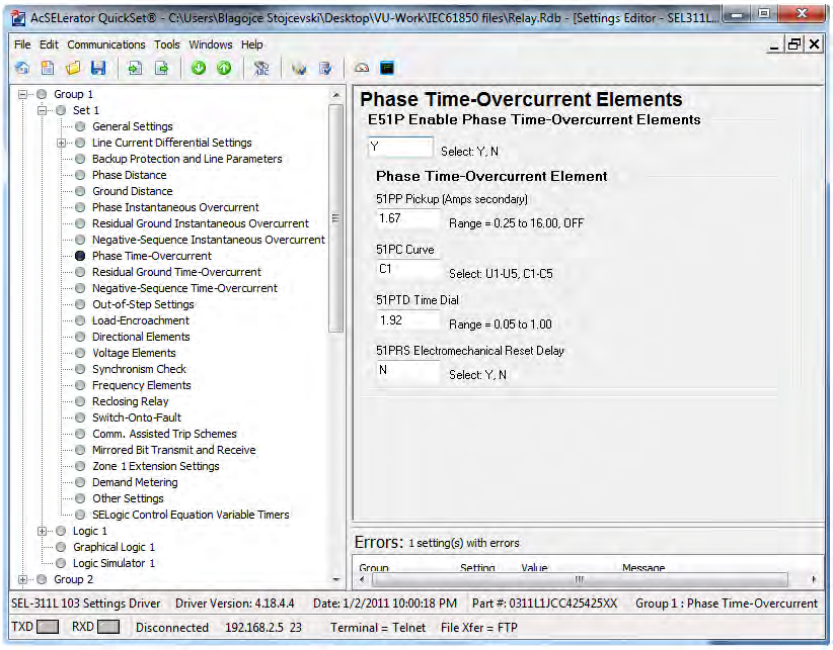


Figure 4.21: Phase time-overcurrent elements

The *Directional Elements* are set by activating the E32 Directional Control parameter to AUTO and setting the Ground Directional Element Priority to QVI. This repeatedly monitors the negative-sequence voltage, zero-sequence voltage and zero-sequence current polarised directional elements illustrated in Figure 4.22.

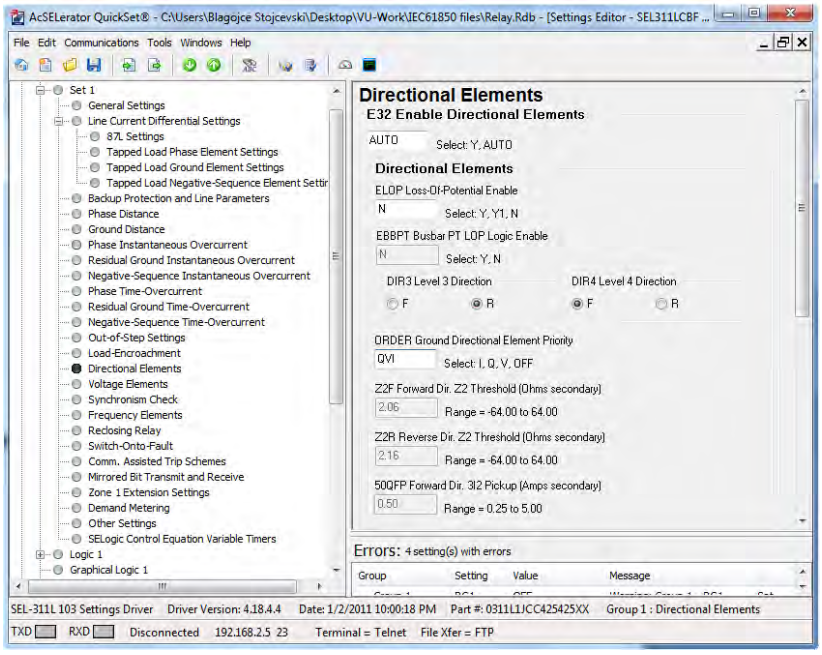


Figure 4.22: Directional elements

The *Close Logic Equations* form incorporates high-speed SELogic to bypass the normal trip logic and directly control breaker status trip contacts. Auxiliary contact 52A is wired to optoisolated input signal IN101, which is opened during a fault. The close condition is set to CL=CC in order to enable unlatched conditions. ULCL prevents the circuit breaker from closing inadvertently by setting TRIP+TRIP87. Figure 4.23 illustrates the Close Logic settings.

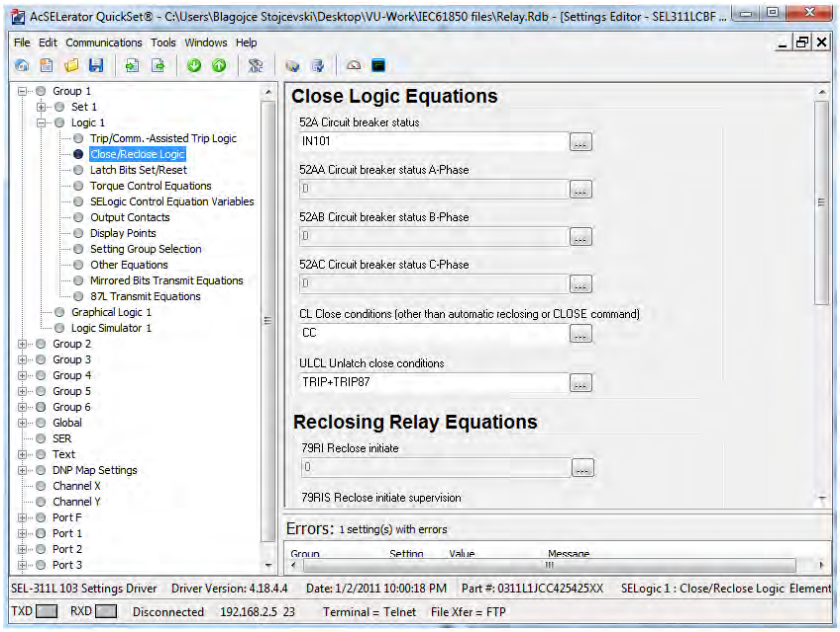


Figure 4.23: Close logic equations

The *Output Contacts* are set to trip, close and control hardware contacts OUT101-OUT107. Remote bits RB1, RB2 and RB3 are used to perform circuit breaker failure, while SV1T manages the output timer as shown in Figure 4.24.

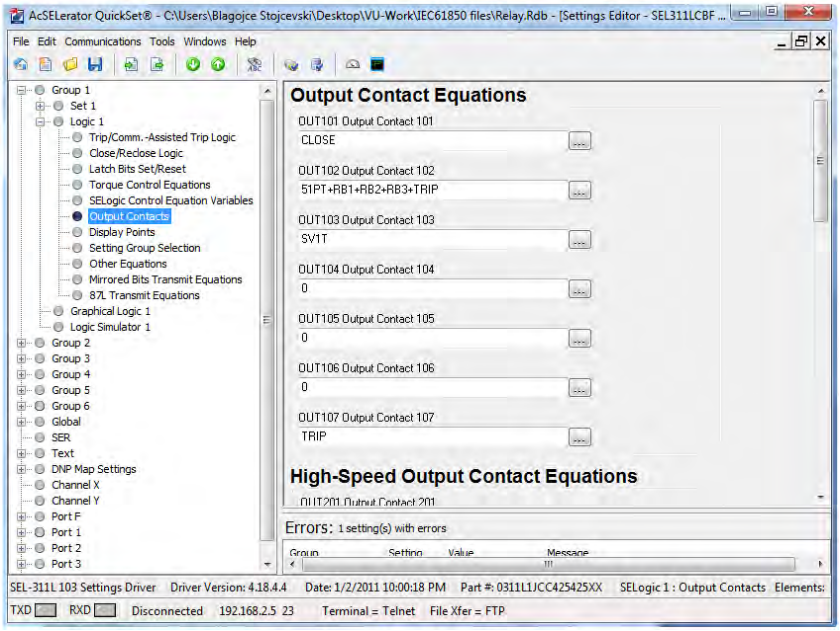


Figure 4.24: Output contact equations

The *Display Point Labels* are used to identify the GOOSE messages received from the relays. These messages are displayed on the front panel LED interface of the SEL-311L. DP1, DP2 and DP3 represent the circuit breaker failure captions. DP4, DP5 and DP6 detect the origins of the message. Figure 4.25 illustrates the labels.

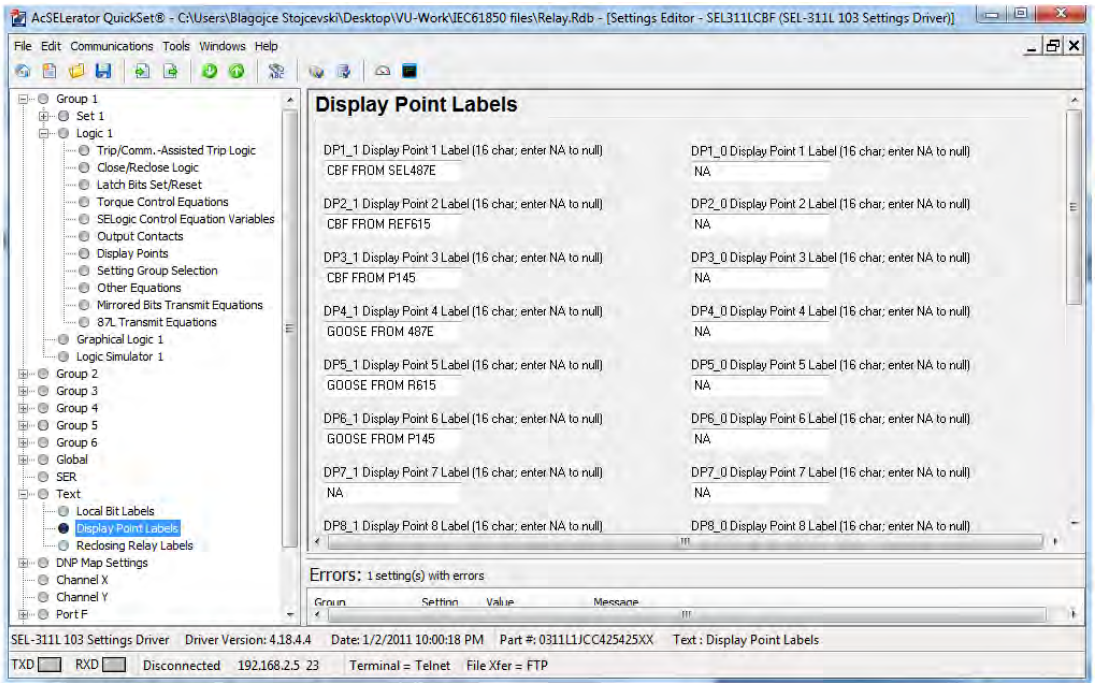
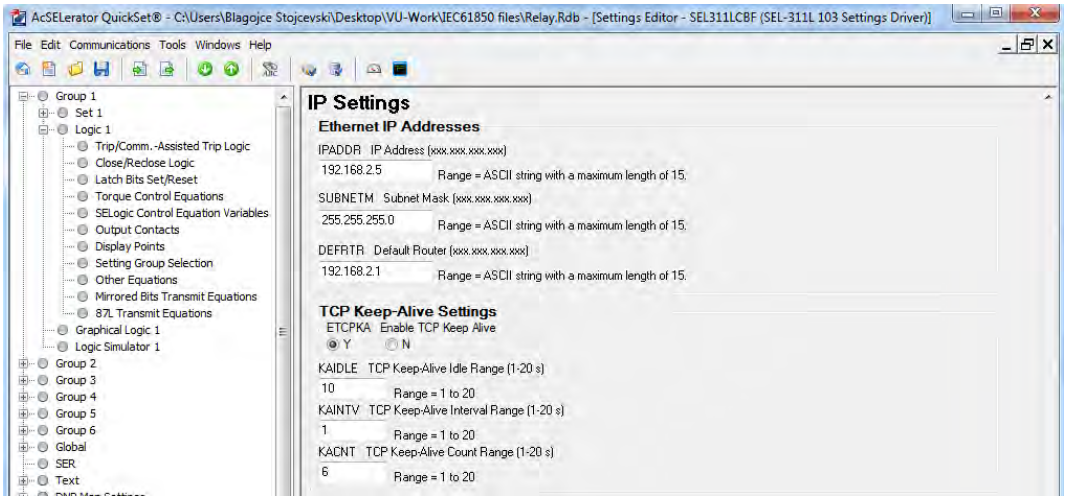


Figure 4.25: Display point labels

The *IP Settings* form is set to provide Ethernet, TCP, Telnet, FTP and IEC61850 communication. The SEL-311L is configured with an IP address of 192.168.2.5, subnet mask of 255.255.255.0 and default router of 192.168.2.1. The Telnet settings are set across the TCP/IP network which operates similar to a serial port. The File Transfer Protocol (FTP) is used for file exchange. The IEC61850 protocol and GOOSE messaging is enabled through the E61850 and EGSE parameters (Figure 4.26).



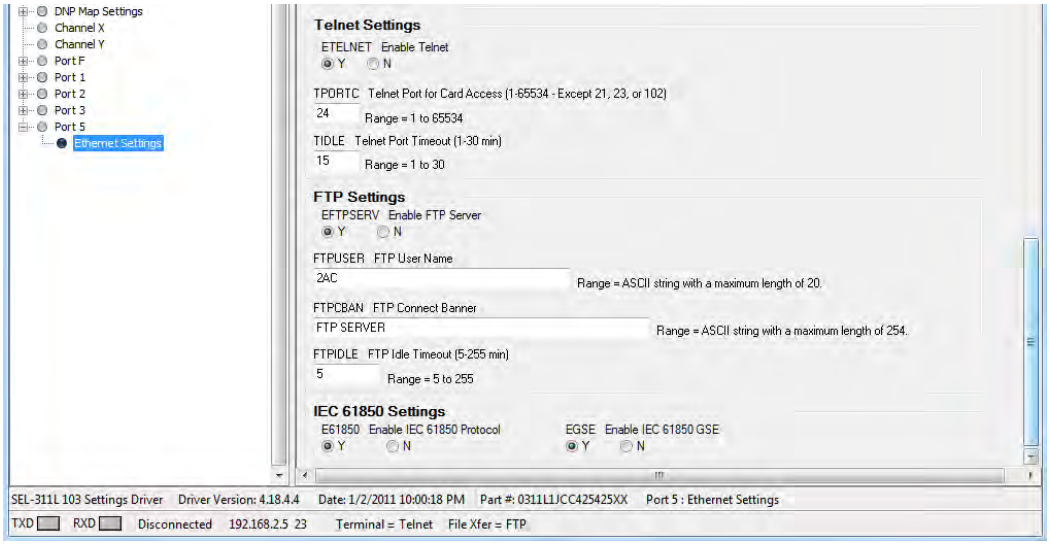


Figure 4.26: IP settings

Once all relay settings have been programmed, the *Communication Port Parameters* must be set including the Host IP Address, Port Number, User ID and Password. By default the port number is 23. The file transfer type is FTP. The User ID is set to 2AC in order to shift from Access Level 1 to 2. The Password is 'TAIL'. Figure 4.27 illustrates the Communication Port Parameters form.

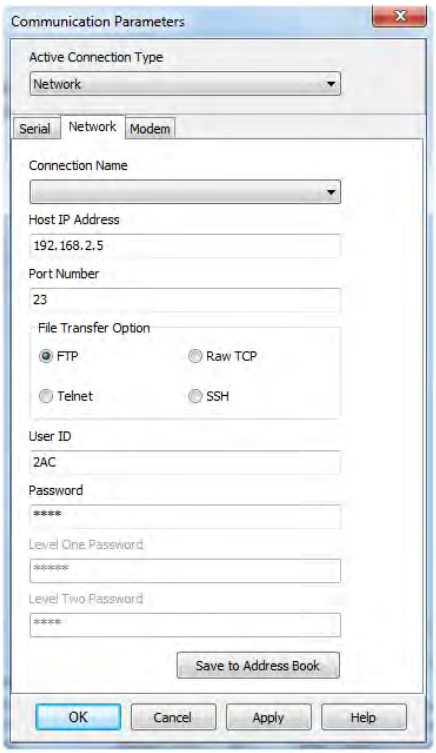


Figure 4.27: Communication port parameters

The active settings are sent to the relay by marking the groups configured (i.e. Group 1, Port F, Port 5 etc.). If no errors occur, the relay will function as programmed.

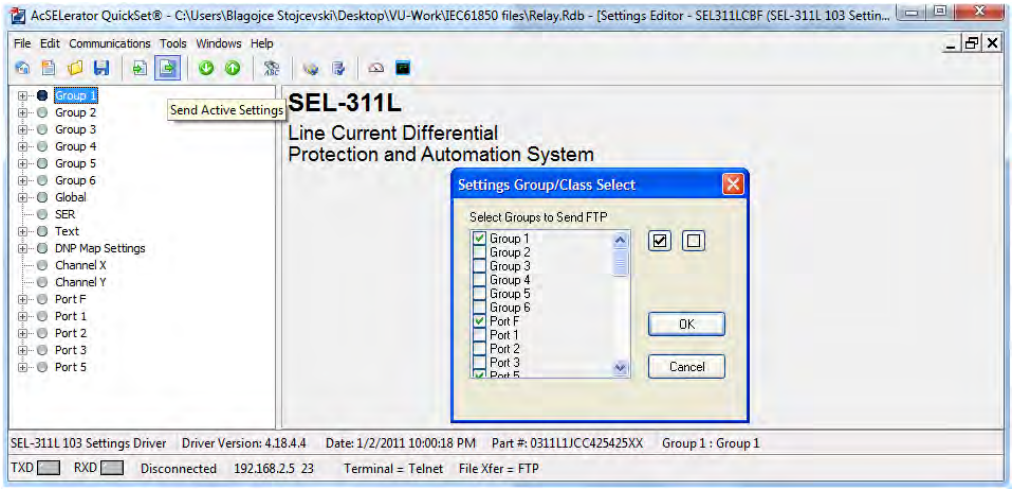


Figure 4.28: Send active settings

The AcSELerator Architect program is launched in order to subscribe and transmit GOOSE messages, but also to achieve overall system configuration of the SEL-311L. On start-up of the program, a 'New Project' is created in the Project Editor window which allows the user to add the device from a list of relays. The IED properties are set to their corresponding IP Address, Subnet Mask and Gateway (Figure 4.29).

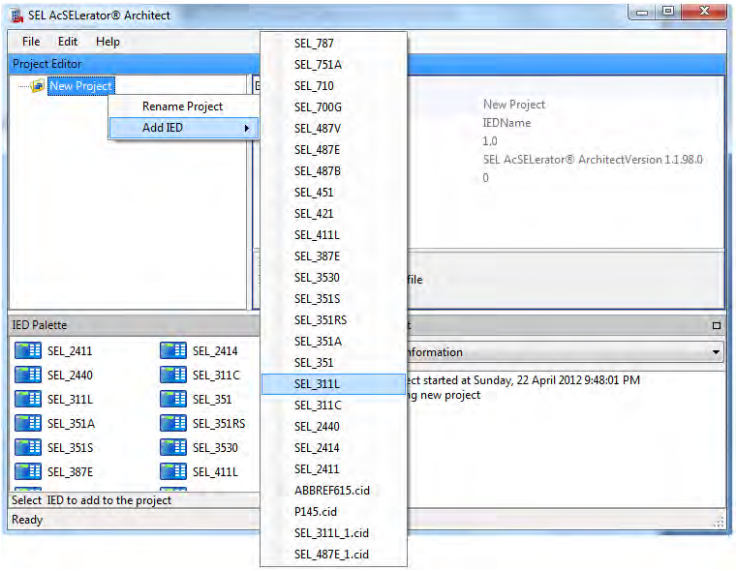


Figure 4.29: AcSELerator Architect start-up menu

To subscribe GOOSE receive messages, it is necessary to navigate through the data tree and drag the logical nodes to the control input. For example, to configure an REF615 Close Circuit Breaker Switch 1 (CBCSWI1) logical node to Remote Bit 5 (RB5) of the SEL-311L, the status value (stVal) must be set to the open position (PosOpn) as shown in Figure 4.30. All six control inputs (RB1-RB6) must be set to the functions allocated in the virtual wiring map.

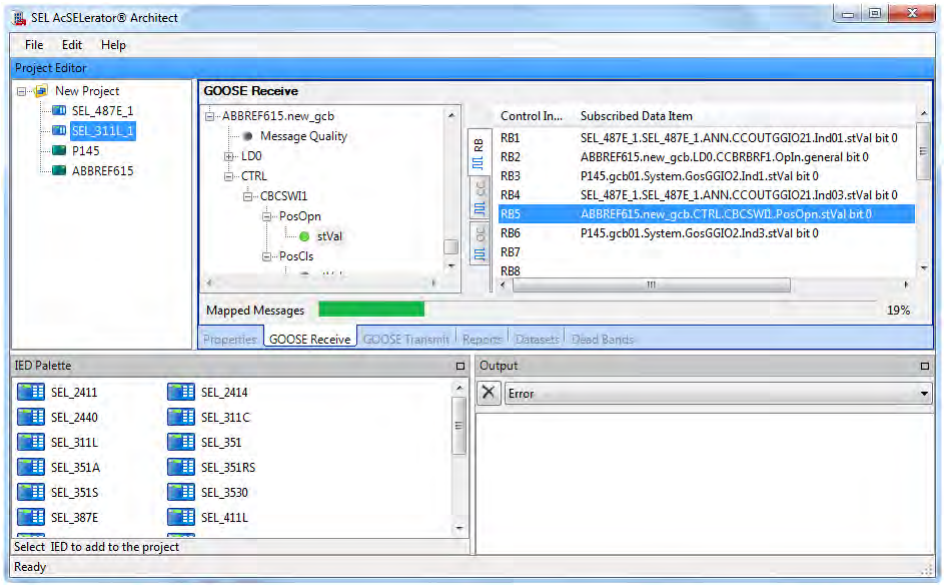


Figure 4.30: GOOSE receive

To transmit the configured GOOSE messages to the relay, the MAC Address, Application ID, VLAN ID and VLAN priority need to be edited as shown in Figure 4.31. The APP ID is set to 0x0003 seeing as it is located on Port 3 of the RSG2200. The VLAN ID and VLAN priority are set to 5. The GOOSE ID is labelled SEL_311L_1.

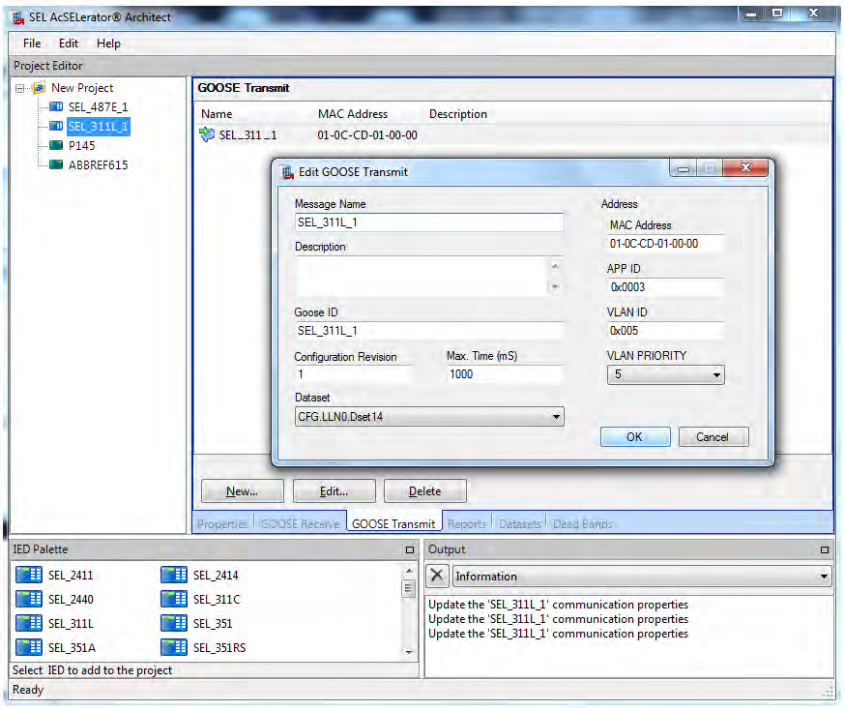


Figure 4.31: GOOSE transmit

The *Project Editor* window is clicked anywhere on the screen to generate the ICD or CID file. The instant the FTP Address, User Name and Password are entered; the AcSELerator Architect software sends the IEC61850 settings to the SEL-311L as shown in Figure 4.32.

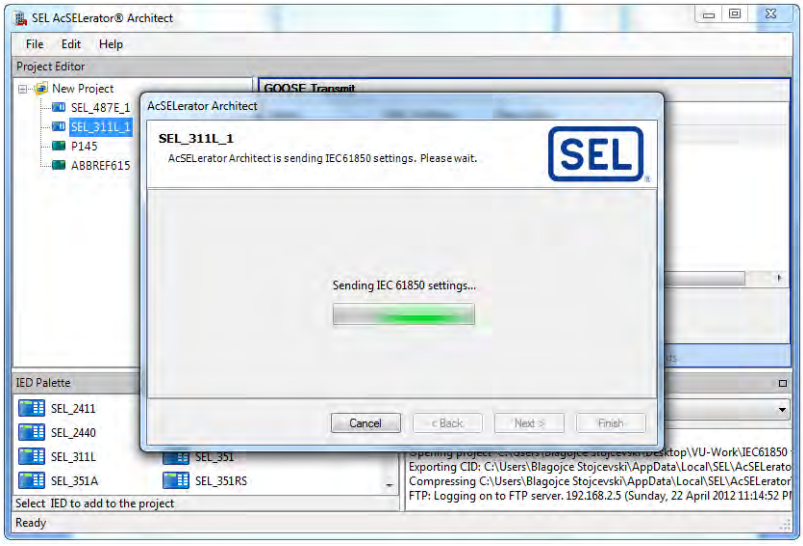


Figure 4.32: Sending ICD or CID files to the SEL-311L

4.5.3 SEL-487E

The SEL-487E Transformer Differential Relay, similar to the SEL-311L, takes advantage of the AcSELerator Quickset and AcSELerator Architect softwares. After creating a new project, the *Settings Editor Selection* form is set with the device family, model and version. The *Device Part Number* has six current channels (S, T, U, W, X and Y) rated at 5A. An dual 100BASE-FX Ethernet card with 8 optoisolated independent level-sensitive inputs, 13 standard form A inputs and 2 standard form C outputs are used to provide IEC61850 communication. Figure 4.33 illustrates the Device Part Number of the SEL-487E.

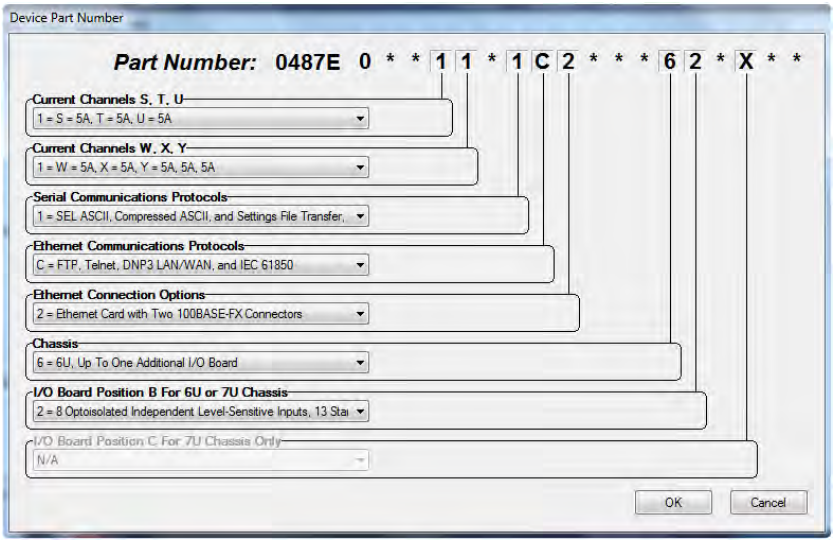


Figure 4.33: Device part number

The *Global Settings* are used to control synchronised phasor measurements which provide real-time description of electrical quantities across the system. The Nominal

System Frequency (NFREQ) and System Phase Rotation (PHROT) influence directional and differential elements. The frequency is 50Hz, while the phase rotation is set to ABC. The Primary Source Voltage Terminal (FRQST) is configured to either OFF, V or Z. The SEL-487E makes use of the primary terminal (V) for functions that employ NFREQ. The Time and Date Management (DATE_F) is set to Month-Day-Year (MDY) or Year-Month-Day (YMD) formats. The Control Input setting is available only when all inputs have the same debounce setting (i.e. EICIS=N). There are three individual groups including main board (IN1XXD), interface board one (IN2XXD) and interface board two (IN3XXD). By default all three are set to 2.0 in order to facilitate the pickup and drop-off times.

The *Monitor Enable Settings* represent which circuit breakers will be activated for monitoring. The Station DC Battery Monitor (EDCMON) is set to N. The Breaker Selection (BK_SEL) channels S, T and U are enabled through breaker monitoring parameter EBMON. The Through Fault Monitor Enable (ETHFLTM) is set to Y. Figure 4.34 illustrates the Monitor Enable Settings form.

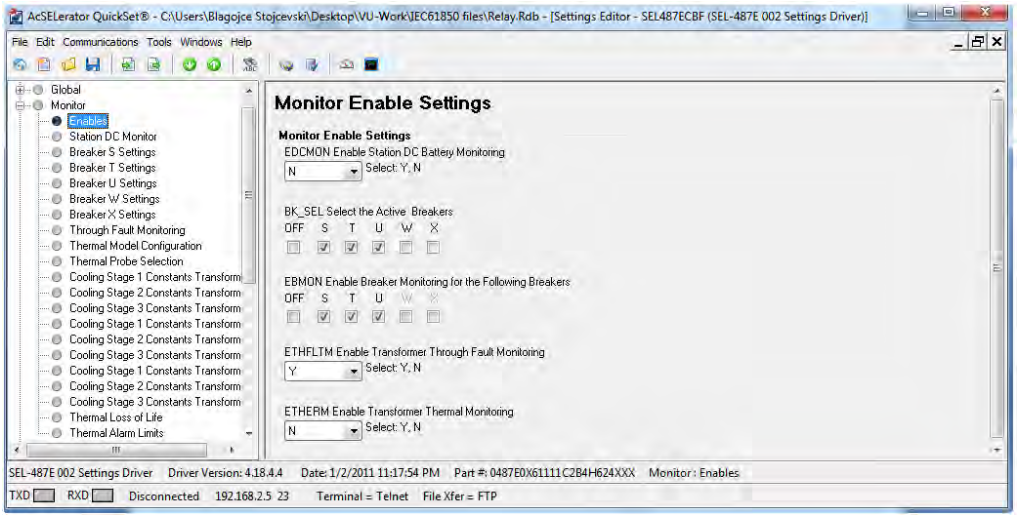


Figure 4.34: Monitor enable settings

After selecting the circuit breakers through the BK_SEL parameter, the CBs are configured to monitor on a three-pole basis, except for interrupted current which is determined on a per-phase basis. The breaker ID is set to the Bk_ID settings (k = S, T, U, W, X) and the Breaker Normally Open (NO) Contact Input is configured using 52_k. The SEL-487E assigns inputs IN101 through to IN103 as illustrated in Figure 4.35. The Breaker Contact Wear Monitor (BSCOSP1) function is used to sum the number of open/close operations and compare data using predefined circuit breaker

curves. This assists in the calculation of the fault current arc times, given that each trip has an matching quantity.

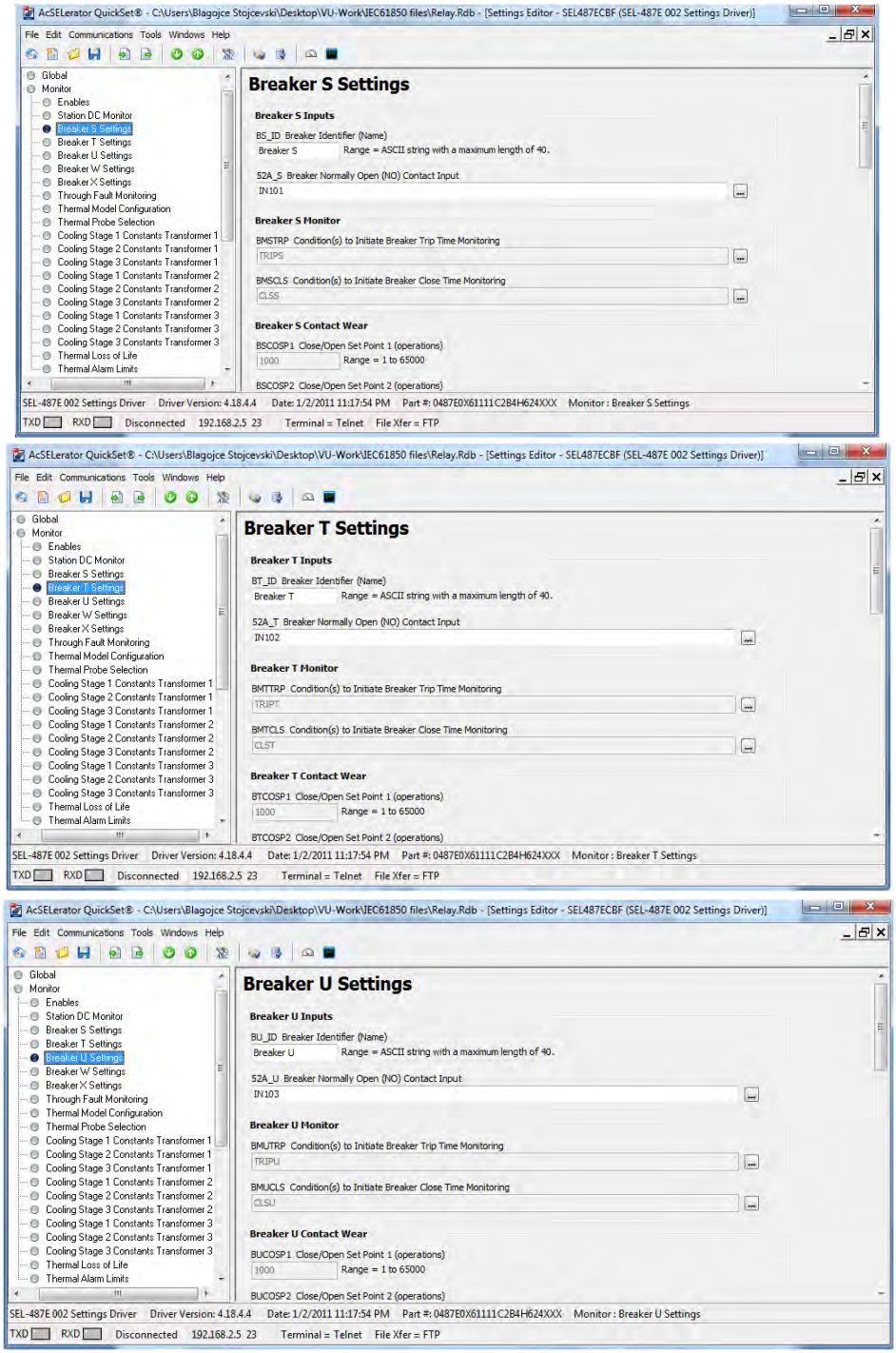


Figure 4.35: Breaker S, T and U settings

The *Terminal Enable Settings* are arranged in a multitier structure to allow enabling and control of input currents. First-tier settings identify which of the 21 analog inputs are processed. The Enable Current Terminal (ECTTERM) is set to access REF channels IY1, IY2 and IY3. The Enable Voltage Terminal (EPTTERM) setting by default is set to OFF. Second-tier settings enable protection functions such as Differential Element

Protection (E87), Restricted Earth Fault (EREF), Definite Time Overcurrent Elements (E50), Inverse Time Overcurrent Elements (E51), Current Unbalance Elements (E46), Overvoltage Elements (E59), Undervoltage Elements (E27), Over/Under Frequency Elements (E81), Volts per Hertz Protection (E24), Breaker Failure Protection (EBFL) and Demand Metering Elements (EDEM). The third-tier provides torque control (TC), for example, if Terminal S is enabled (ECTTERM = S, T, U, ...) and specified to differential elements (E87 = S, T, U, ...), E87T will provide a method to dynamically enable/disable current S in the differential function. Figure 4.36 depicts the terminal enable settings.

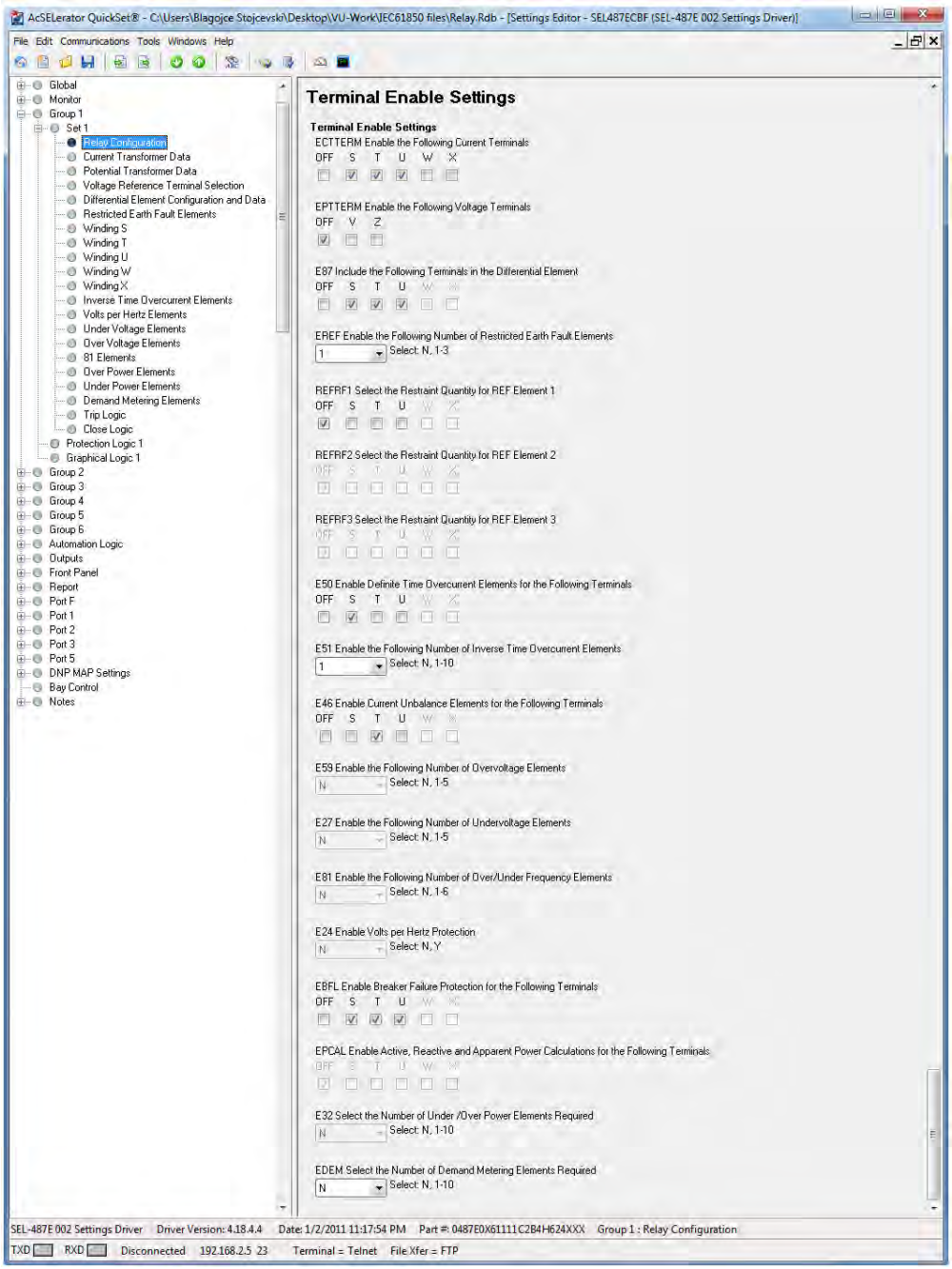


Figure 4.36: Terminal enable settings

The E50S parameter is used to specify the type of phase (P), negative-sequence (Q) and zero-sequence (G) directional element required for *Winding S*. Selecting E50S = G, P, Q makes the definite-time overcurrent element hide any gray-outs. External Breaker Failure Initiate Pickup (EBFPUS) is set to 10 cycles before asserting the re-trip timer. This suggests that when a phase current exceeds the Fault Current Pickup (50FPUS) or the Neutral Current Pickup (INFPUS), the relay will trip. Figure 4.38 illustrates the breaker failure logic associated to Terminal S.

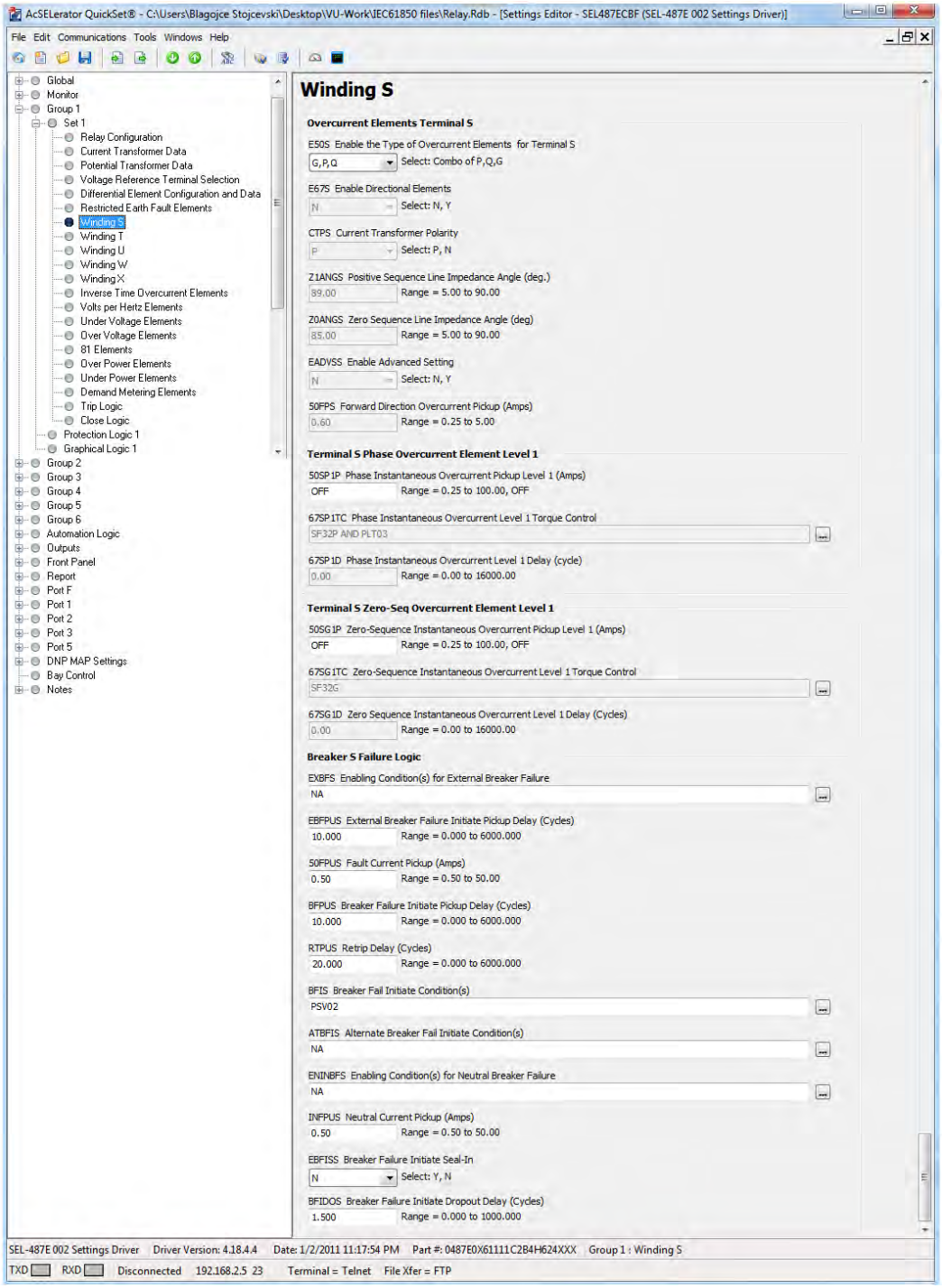


Figure 4.37: Winding S

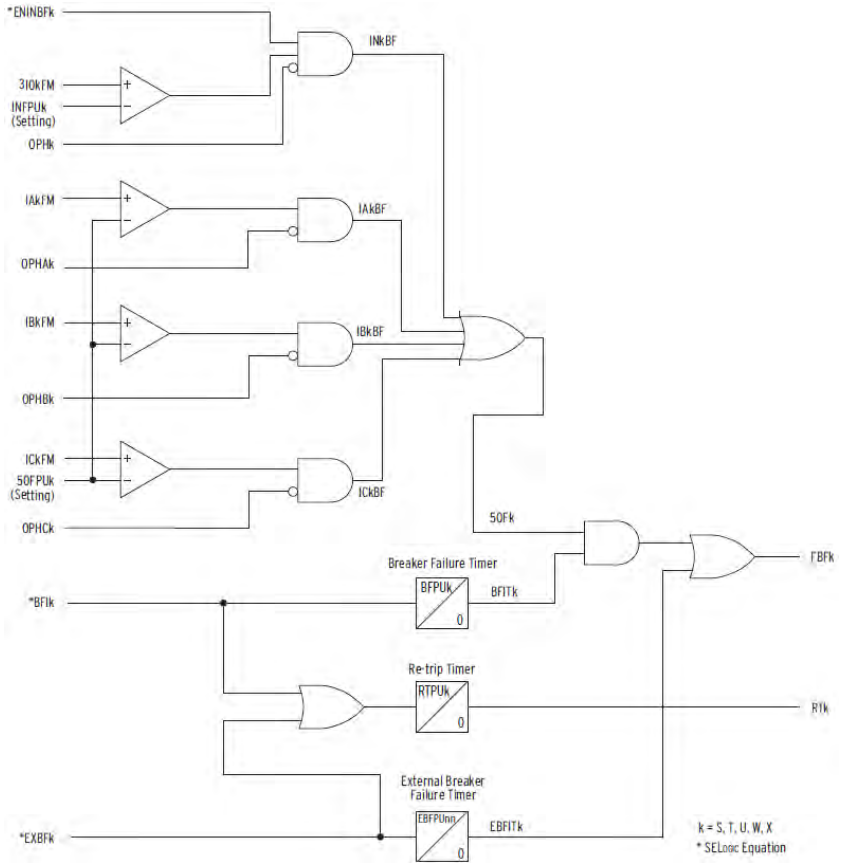


Figure 4.38: Breaker failure logic

The *Inverse Time-Overcurrent* form is used to configure the directional 51 elements as shown in Figure 4.39. The operating quantity is set to calculate the Instantaneous Filtered Maximum Phase Current Magnitude (51O01 = IMAXSF). The pickup setting (51P01) and time-dial (51TD01) is set to 1 and 0 .05, respectively. The pickup characteristics move horizontally to fluctuate the current, while the time-dial characteristics move vertically to alter the operating time. Torque Control (51TC01) is set to 1 to facilitate directional control.

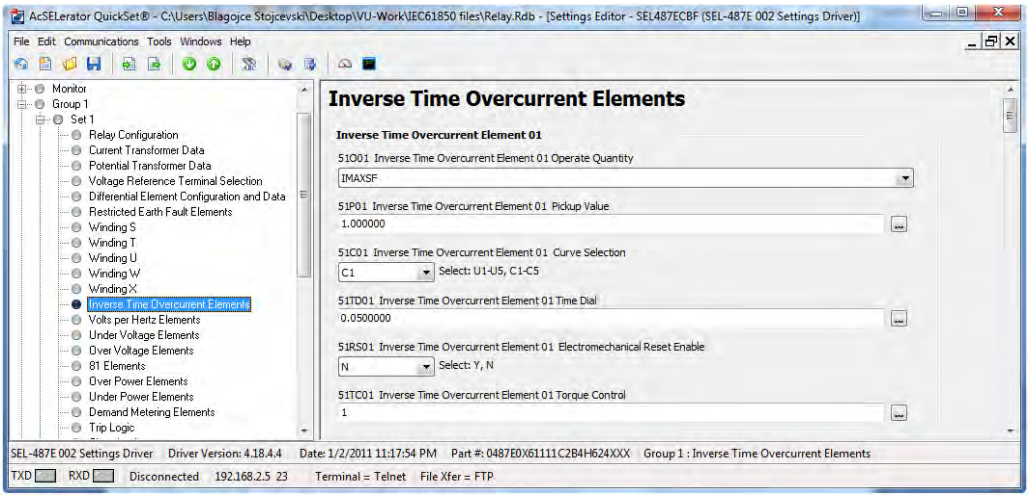


Figure 4.39: Directional 51 element

The *Trip Logic* form describes the equations for selectively tripping between unit and system faults. The Transformer Trip Timer (TRXFMR) and Trip Terminal S (TRS) is assigned to value PSV02, which opens the circuit breaker. Upon opening the circuit breaker, TRXFMR activates the Unlatch Transformer Trip Output (ULTXFMR), which remains asserted for the Minimum Trip Duration (TDURD). For Trip Terminal T (TRT) and U (TRU), the equation 50kP1 OR 50kQ1 specifies that during the event of a phase or negative sequence overcurrent element a fault is triggered. The Event Report (ER) setting is set to equation 50SQ1 OR 50TQ1 OR 50UQ1 to determine which events will cause the relay to initiate fault recording. Figure 4.40 illustrates the trip logic.

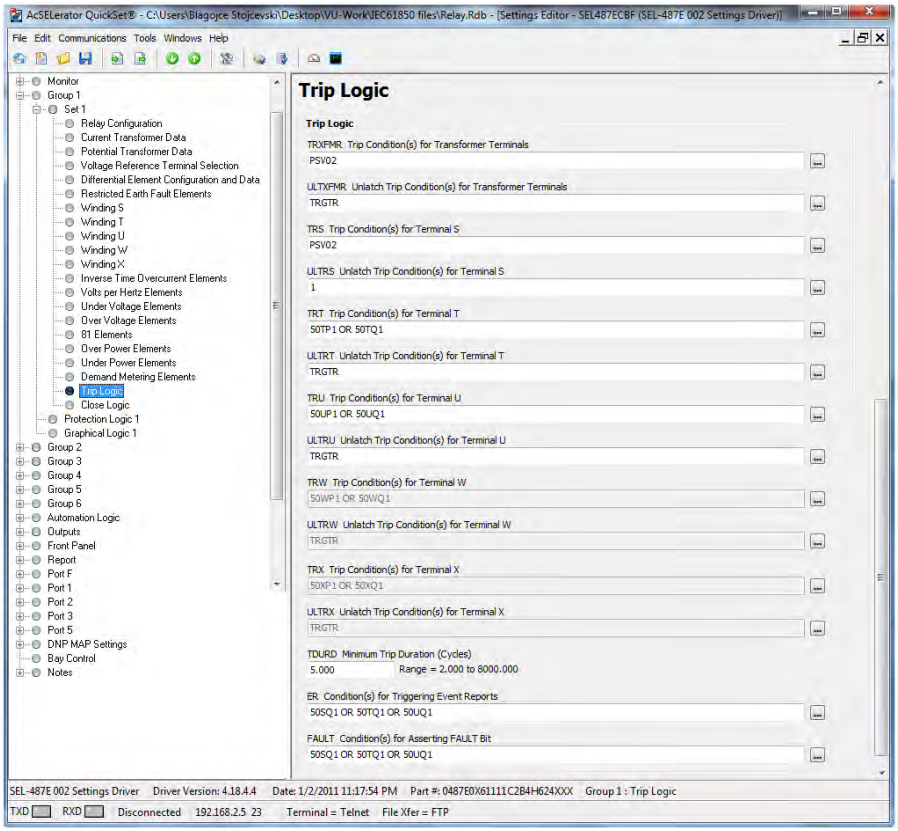
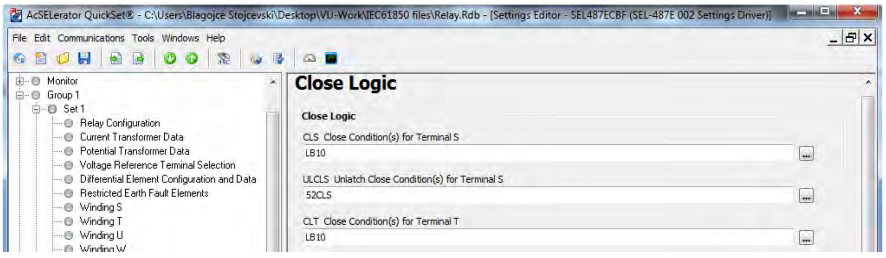


Figure 4.40: Trip logic

The *Close Logic* settings for Terminal S, T and U are set by default to local bit LB10 which controls the close operation at the front panel of the relay. The Unlatched Close (ULCLk) conditions are set to breaker auxiliary contact 52A or 52CLk, which asserts a logic 0. Figure 4.41 illustrates the Close Logic settings.



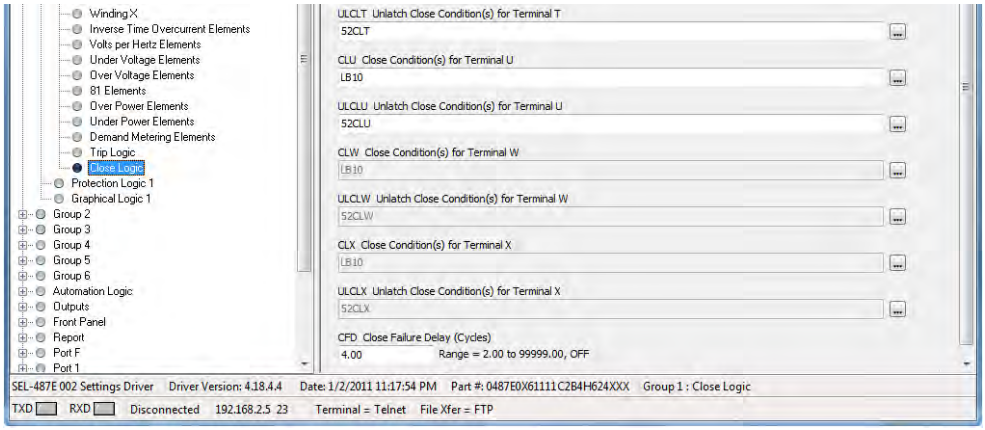


Figure 4.41: Close logic

The *Protection Free-Form Logic* facilitates in the use of front panel pushbuttons. Figure 4.42 illustrates the commands to open and close breakers S, T and U.

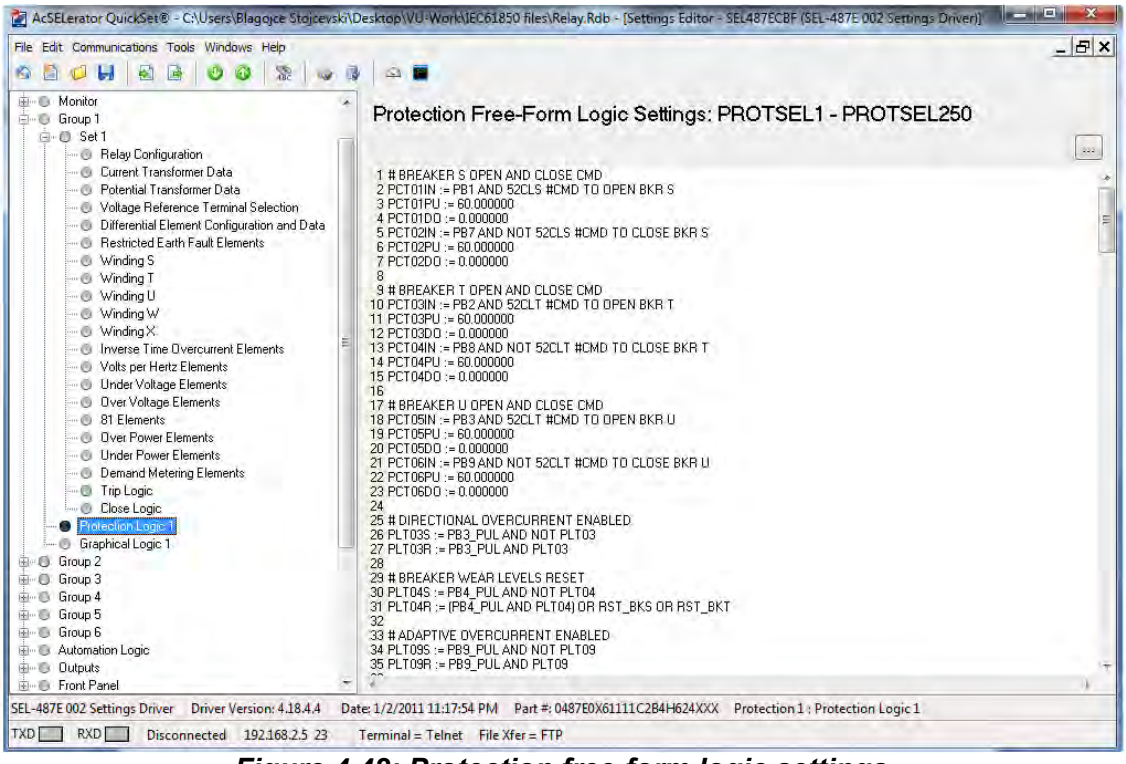


Figure 4.42: Protection free-form logic settings

The *Main Board Outputs* indicate the configuration of the output terminals (OUT101 - OUT108), which are used to trip and c lose the circuit breakers. Logical node OUT1GGIO17 and attributes Ind01.stVal - Ind08.stVal are associated to the Annunciation (ANN) element of the SEL-487E. OUT101 is appointed to pushbutton 7 of the SEL-487E to open breaker S, whereas OUT102 is appointed to pushbutton 1 to close breaker S. OUT103 - OUT106 is used for breakers T and U. OUT108 on the other hand is set for remote alarm status by equation NOT(SALARM OR HALARM).

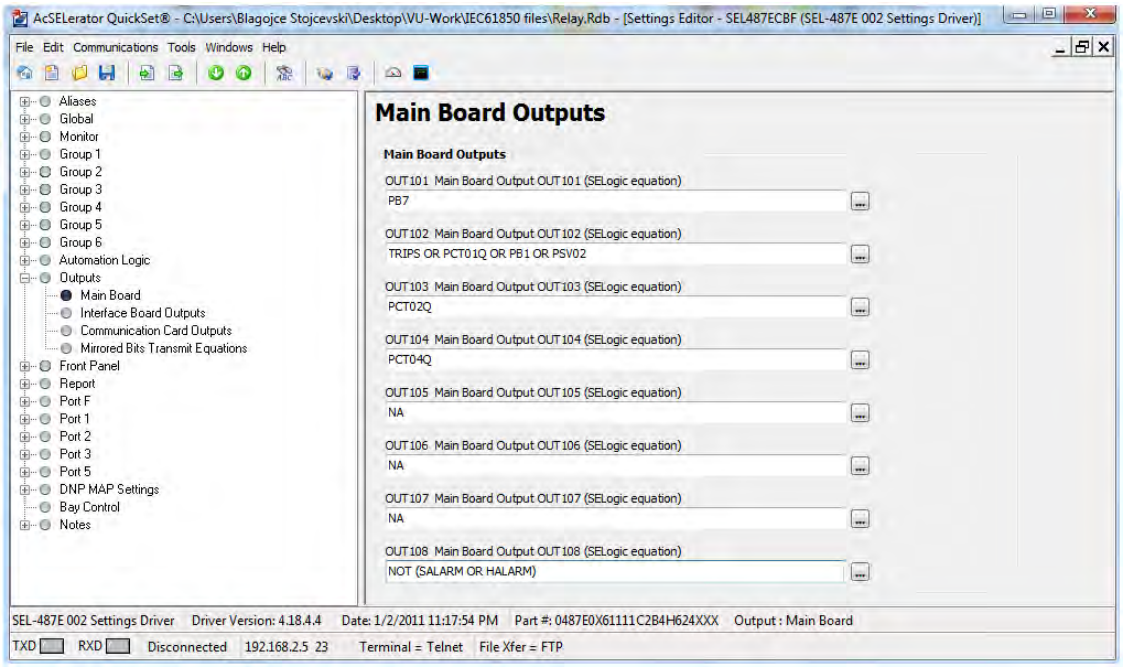
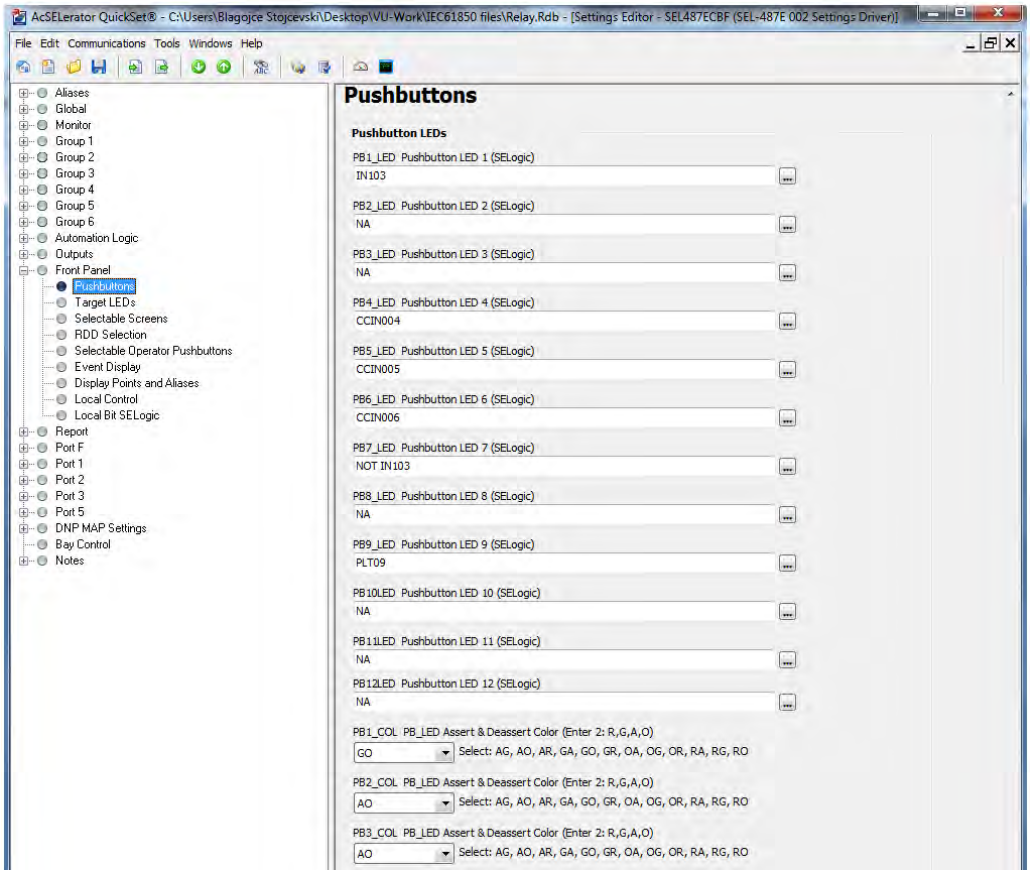


Figure 4.43: Main board outputs

The *Front Panel* menu uses 24 coloured programmable LEDs. PB*nn*COL (*nn* = 1-12) is set to red (R), green (G), amber (A), or off (O). A combination of colours may be used to distinguish between asserted and disserted pushbuttons (i.e. amber and off = AO).



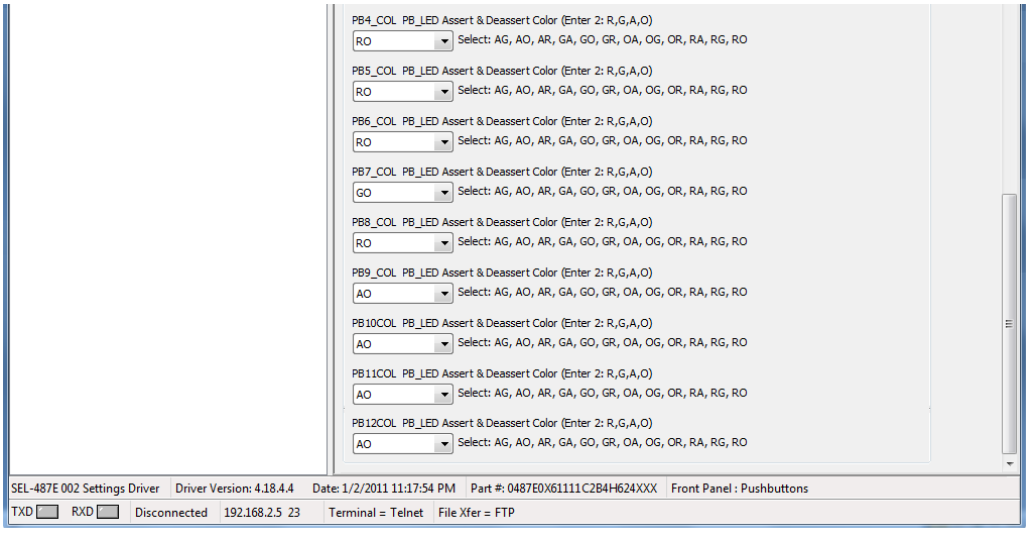


Figure 4.44: Pushbuttons

The PROTO setting parameter is used to select the type of protocol used across PORT F during virtual ports. DNP, MBA and MBB are each set to one port only. The SPEED is rated at 9600 baud, allowing the serial port hardware to synchronise, transmit and receive data at Pin 8 via the clock. The DATABIT setting is fixed to 8 bits, where the STOPBIT setting is set to default as 1 (as shown in Figure 4.45).

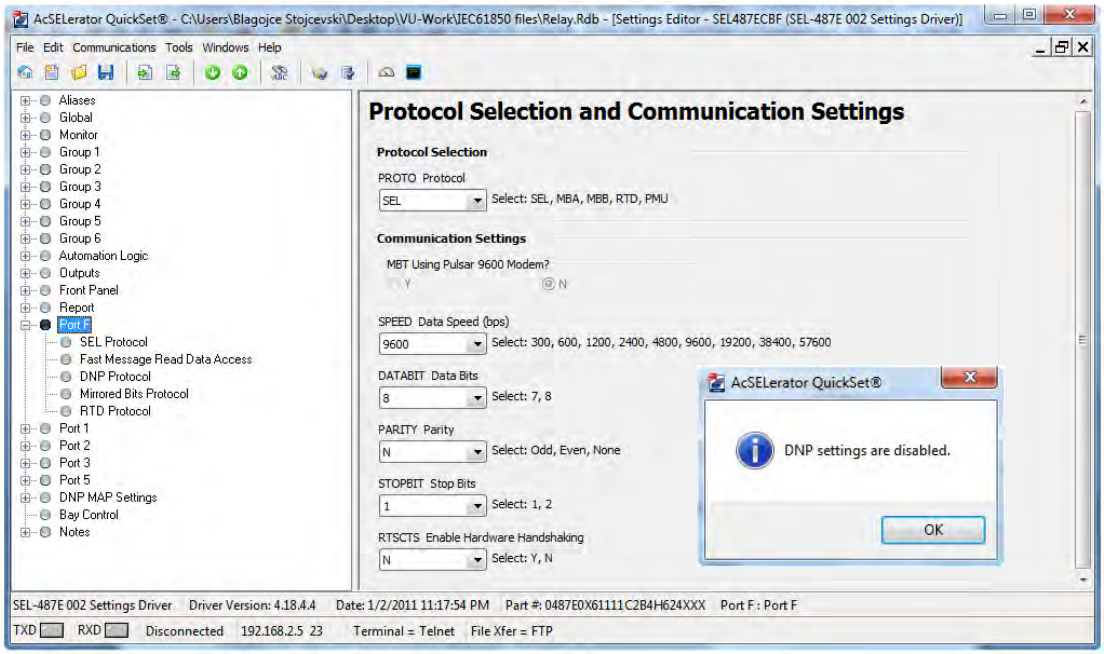


Figure 4.45: Protocol and communication settings

Group 1, Port 5 and Port F settings are updated to the relay. AcSELerator Architect is launched with the intent to subscribe and transmit the GOOSE messages. The ICD/CID files of the SEL-311L, P145 and REF615 are imported into the IED Palette window as illustrated in Figure 4.47.

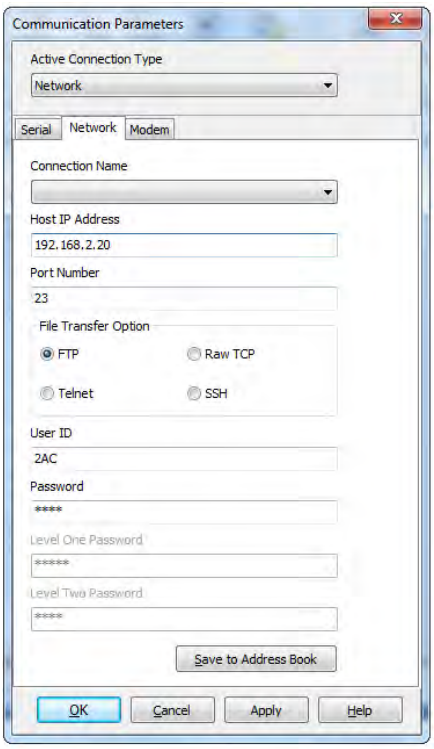


Figure 4.46: Communication port parameters

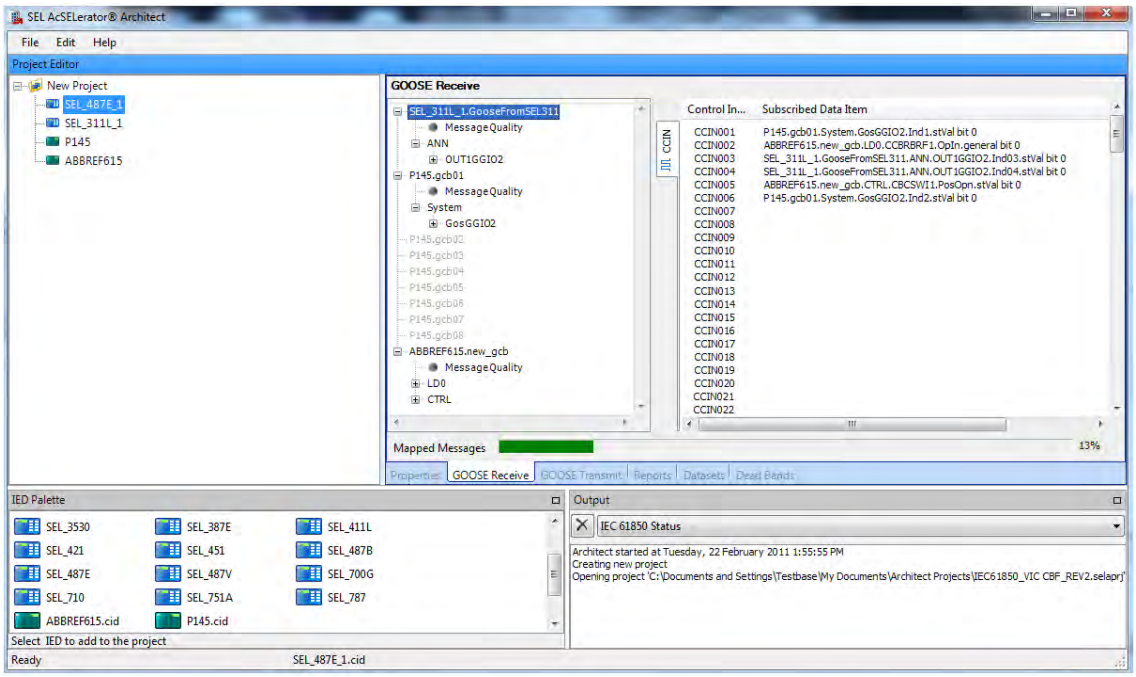


Figure 4.47: GOOSE receive

To transmit the configured GOOSE messages to the relay, the MAC Address, Application ID, VLAN ID and VLAN priority needs to be edited as shown in Figure 4.48. The APP ID is set to 0x0005 seeing as it is located on Port 5 of the RSG2200. The VLAN ID and VLAN priority are set to 5. The GOOSE ID is specified to SEL_487E_1.

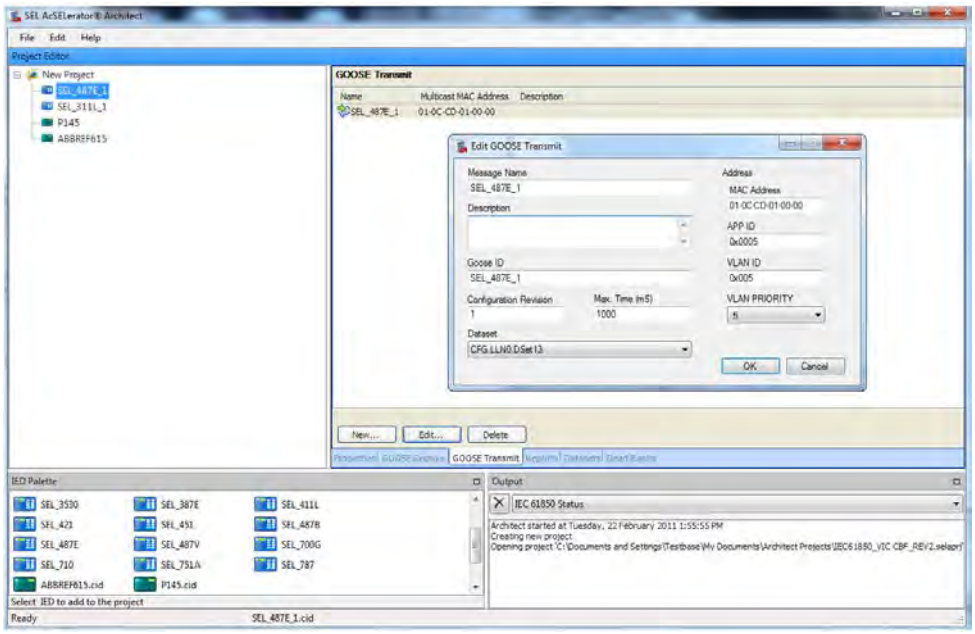


Figure 4.48: GOOSE transmit

The ICD/CID file is then sent to the FTP Address 192.168.2.20. The IEC61850 settings are transmitted as shown in Figure 4.49.

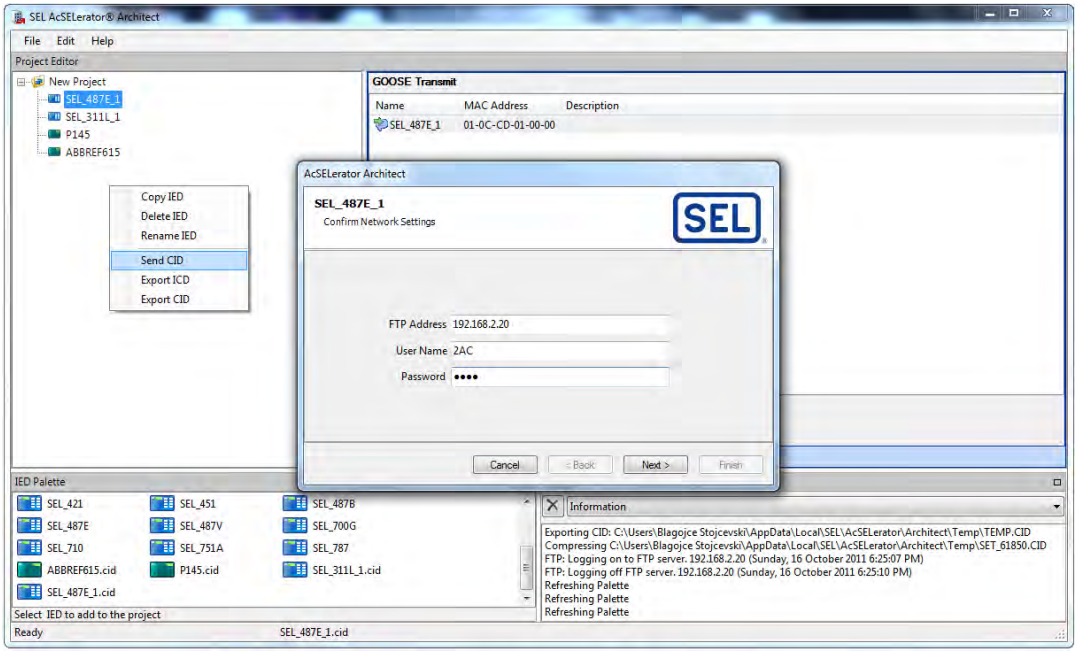


Figure 4.49: Sending ICD or CID files to the SEL-487E

4.5.4 REF615

The REF615 capitalises on the PCM600 and CCT600 Protection and Control IED Manager to read and write settings. A new project is created prior to setting the plant structure comprising of a substation, voltage and bay level as shown in Figure 4.50. Each level can be viewed to observe hardware properties, connection types and voltage ranges.

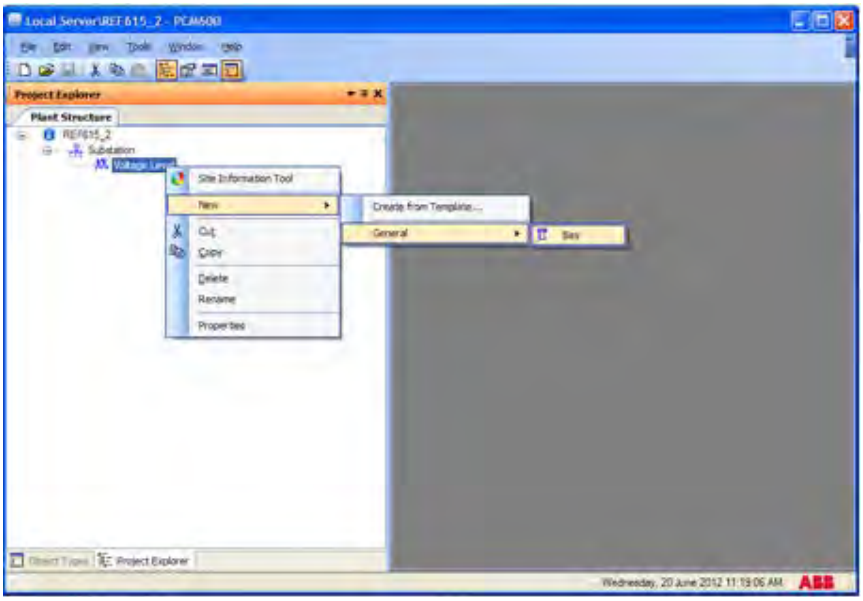


Figure 4.50: Substation, voltage and bay levels

There are two approaches when creating the relay object including using the context menu via the bay or through the object window. Right click on the bay node within the plant structure and select *New → Feeder IEDs → REF615*.

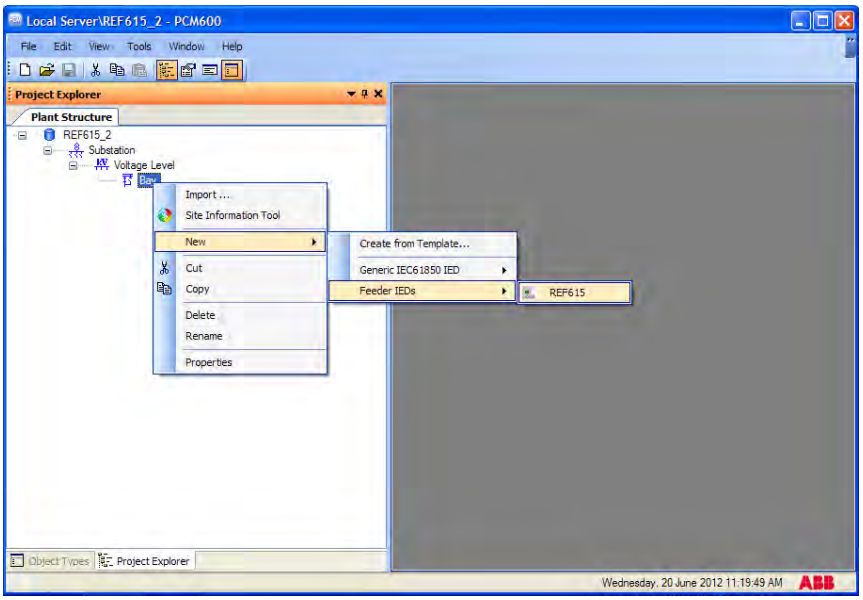


Figure 4.51: Object type of the relay

Configuring the IP Address, IED protocol, and communication provider is necessary to communicate to the relay (Figure 4.52). This is fulfilled through the *'Communication Wizard'* which assists in the basic set up of hardware properties either online or offline. The REF615 is set to IP address 192.168.2.10 and has a read-only communications provider when using the IEC61850 protocol. The '*Scan*' button is selected to detect the order code or serial of the relay (HBFFAEAGNBA1BNN2XC) which is sourced automatically from the ABB server.

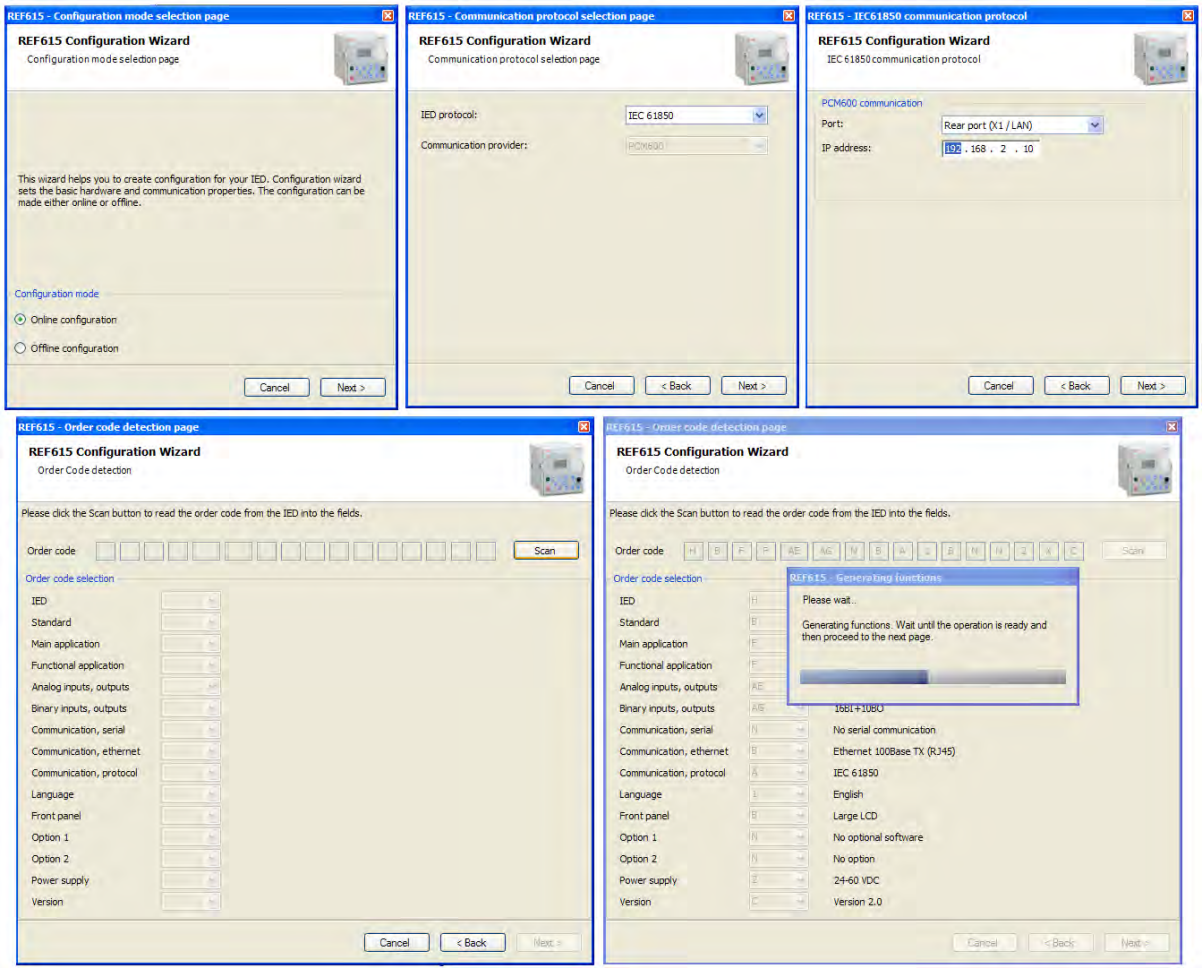


Figure 4.52: Communication configuration settings

A green '*tick*' symbol emerges adjacent to the Bay1 footer, where two sub-menus appear for the IED Configuration and Application Configuration. Right click Bay1 and select *'Read from IED*' as illustrated in Figure 4.53.

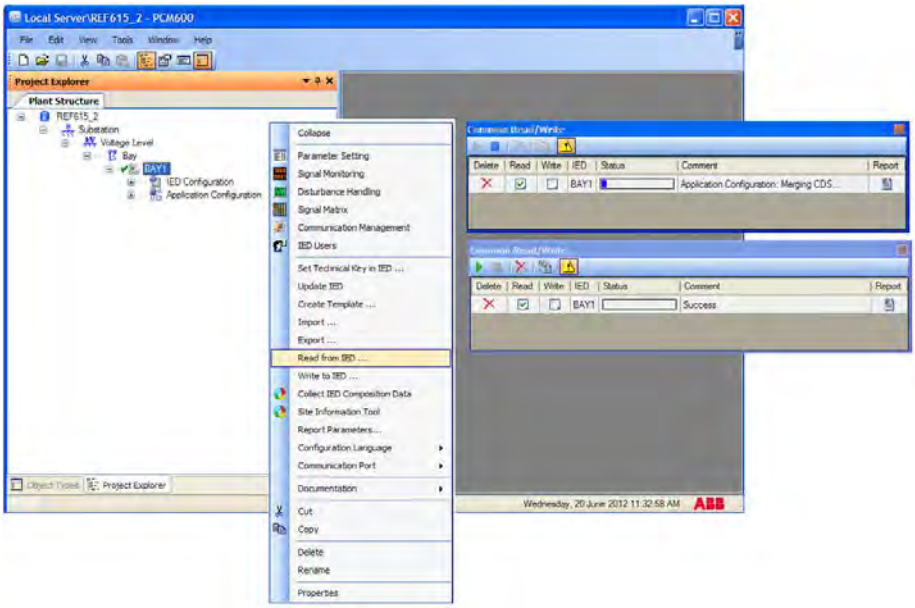


Figure 4.53: Read from IED

A list of all protection and logical node parameters specific to the REF615 become visible as shown in Figure 4.54. Once each parameter is set, right click and select *'Signal Matrix*'.

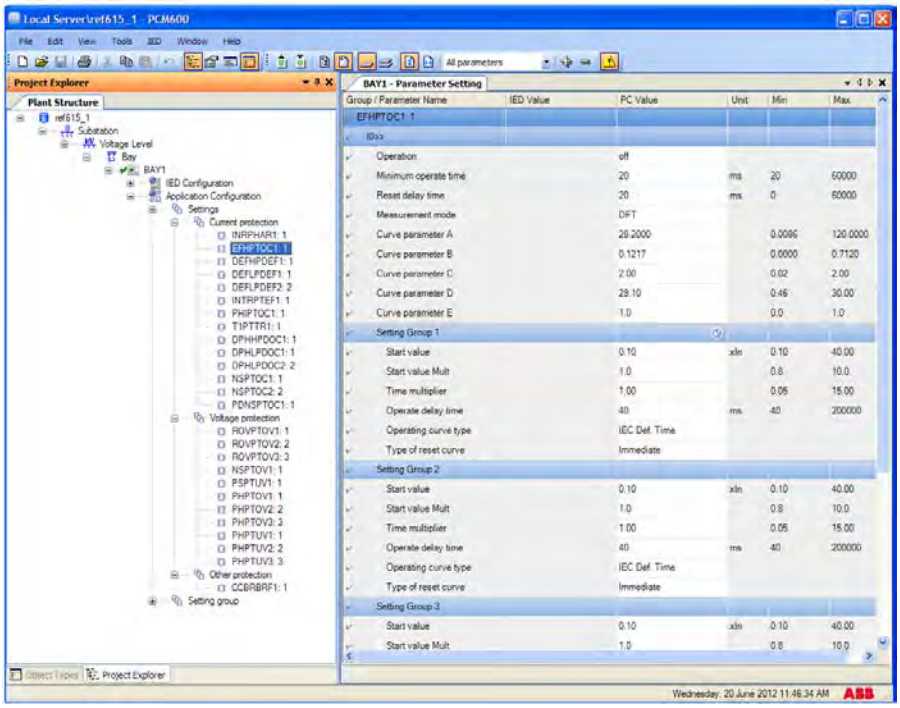


Figure 4.54: Parameter settings

The signal matrix is used to manually configure and connect input and output channels. The signal matrix for redundant channels is left empty and automatically updates itself when signals are lost (Figure 4.55).

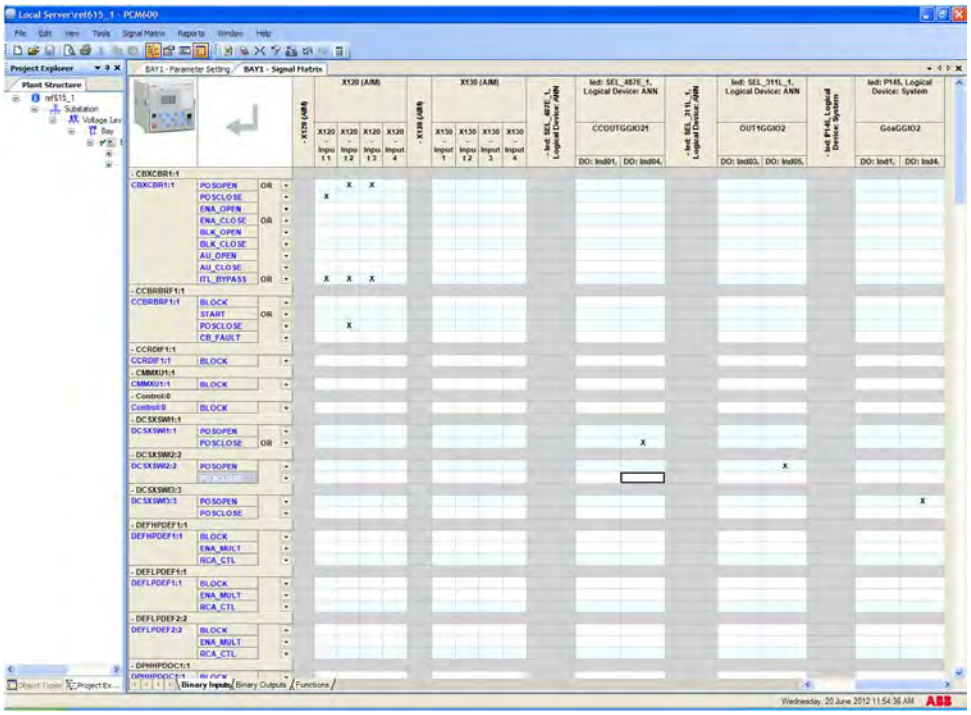


Figure 4.55: Signal matrix

Export the PCM600 project as an SCL file using a secondary file type such as PCM IED file *(.pcmi)*, IED Capability Description *(.icd)* or Configured IED Description *(.cid)* as shown in Figure 4.56.

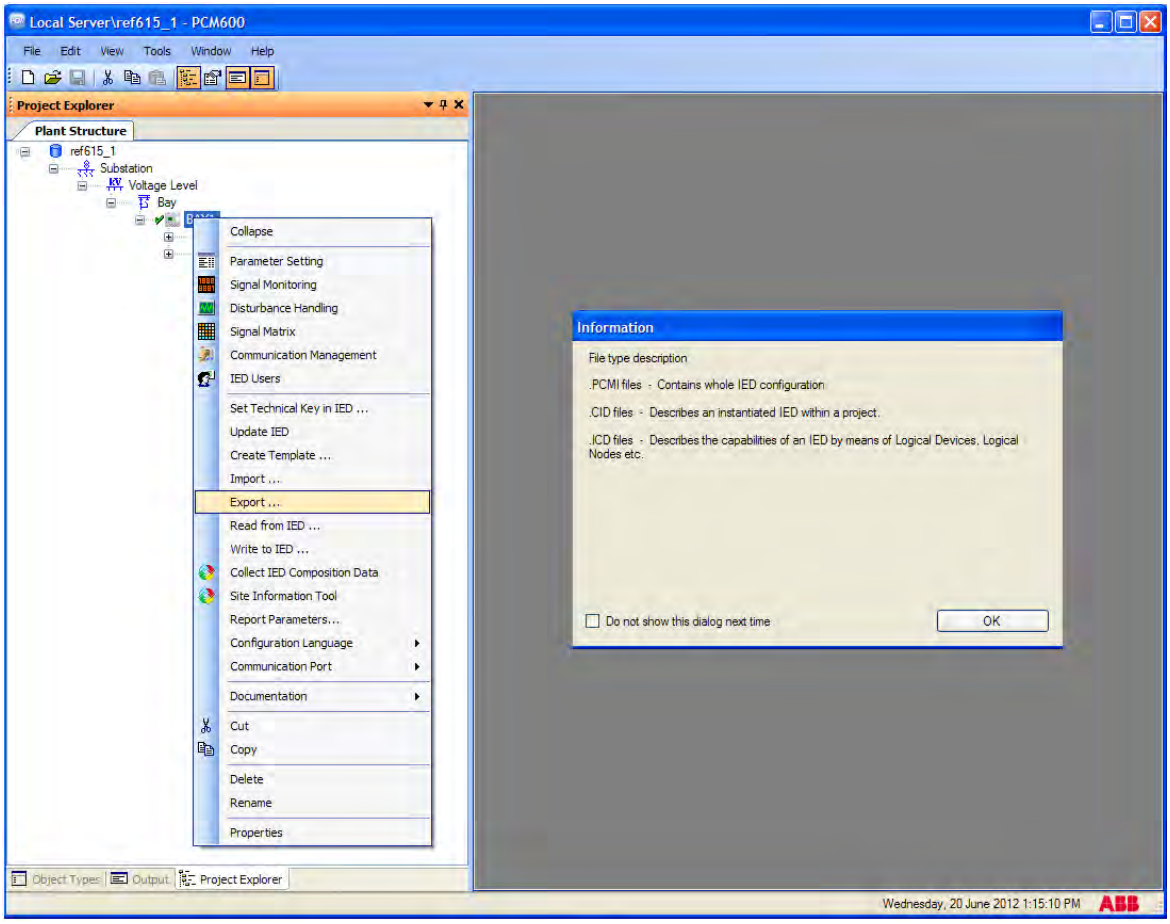


Figure 4.56: File type description in SCL file export

Start the CCT600 tool and import the SCL file. When the CCT600 tool is used for the first time you need to copy the license file to directory *C:\Program Files\IET\Bin\License*. Select *File → Create New Project* and give a name, browser folder and click OK.

Figure 4.57: New project CCT600

Technical keys (i.e. SEL_311L_1, SEL_487E_1 and P145) will become apparent in the Project Navigator window. These technical keys represent the SEL and Areva relays.

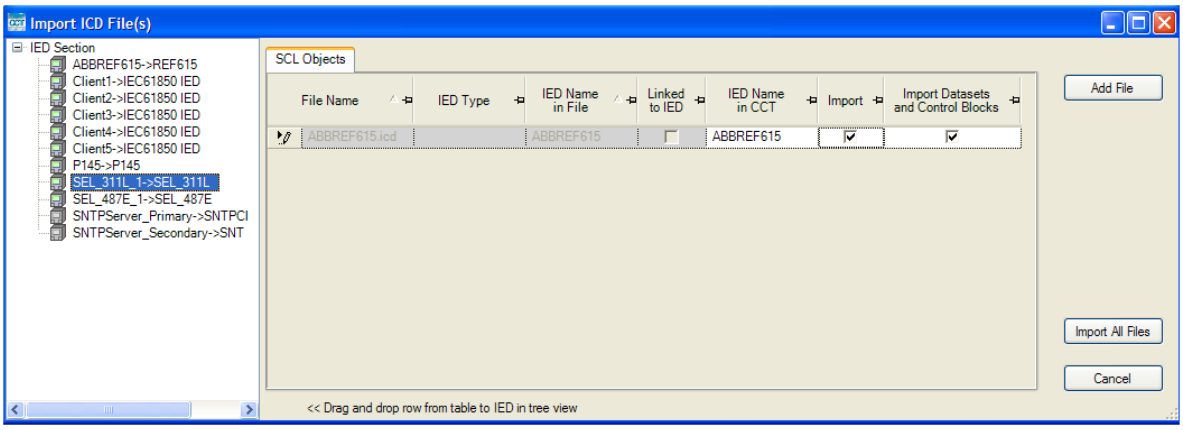


Figure 4.58: Importing SCL files

Logical nodes are symbolised with a red circle embracing characters LN. Each of these logical nodes need to be GOOSE engineered using the IED Data Model. This is achieved by dragging and dropping the GOOSE attributes (Int2.stVal, Int2.q, Int2.t and Int2.d) from the client relay to the recipient as shown in Figure 4.59.

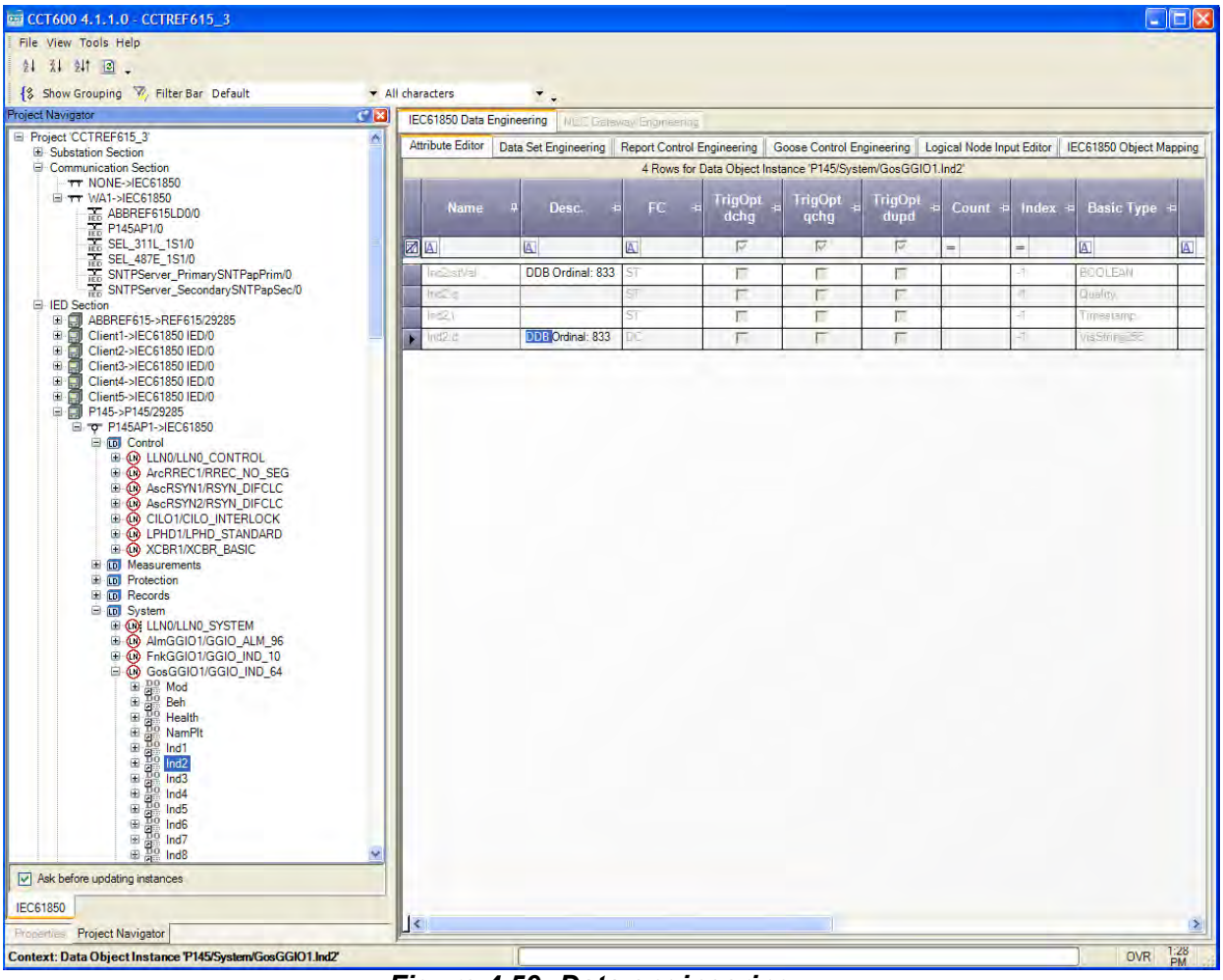


Figure 4.59: Data engineering

Select *Tools → IEC61850 Data Flow Engineering → Update Dataflow*. Export the SCL file from CCT600 by selecting *Tools → SCL Import/Export → Export SCL File*. Close CCT600 and import the SCL file to your PCM600 project. Select substation level and click import. Send the changes to the relay. Select '*Write to IED*' and note the relay will restart once the file is recognised.

4.5.5 P145

The P145 Feeder Management Relay draws on the Programmable Scheme Logic (PSL) editor of the MiCOM S1 Studio to graphically programme the functionality of optically isolated inputs, relay outputs and LED indicators for protection and control functions. A *'New System*' is created once the software is initiated, requiring a name and system path as shown in Figure 4.60.

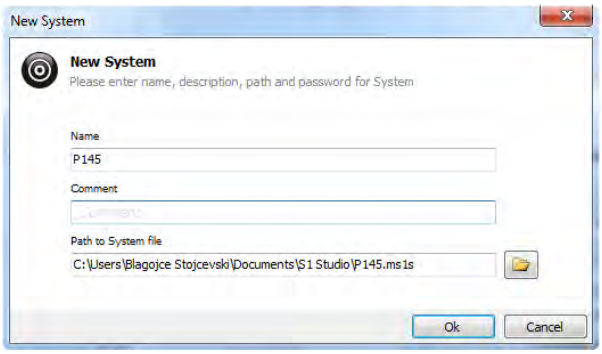


Figure 4.60: New system project file

The new system will appear in the Studio Explorer pallet. Right click *system [P145]* and create a substation level. Ensure to download all ICD files by selecting '*Extract All Records*' before generating the substation level. This will enable event and disturbance records as illustrated in Figure 4.61.

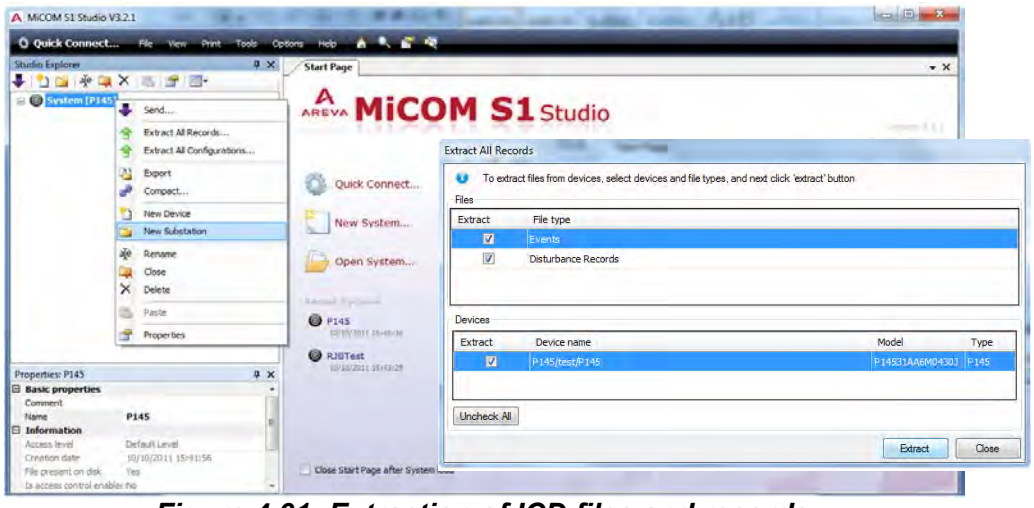


Figure 4.61: Extraction of ICD files and records

In the same way, select '*Extract All Configurations*' and wait for the file types of the device to surface. This will bring about a number of pallet options including connection settings, PSL, menu text, MCL 61850, measurements, events and disturbance records. Click the '*Settings*' folder and a file designation *P145.test.P145.000* will come into view exposing several operational settings that require parameter setup (Figure 4.62).

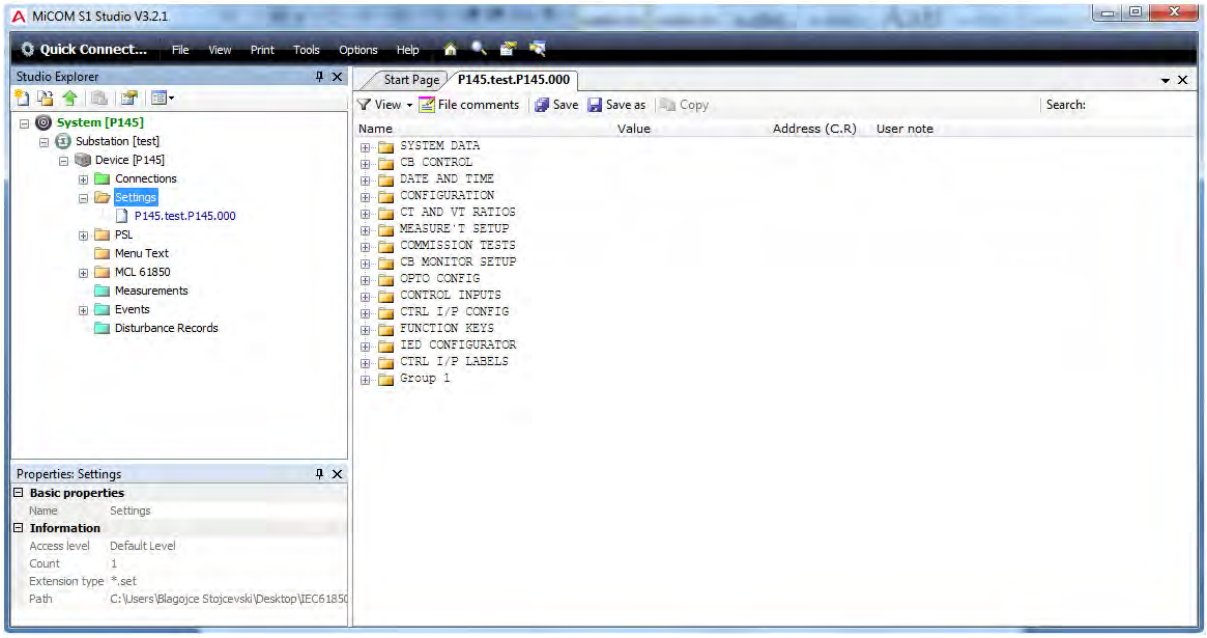


Figure 4.62: Operational settings

The *CB Control* setting is managed by optoisolated inputs, instead of function keys. The close and trip pulse times are set to 500ms, seeing as it is the minimum time permissible by the IED. The manual close delay is fixed to 10 seconds (Figure 4.63).

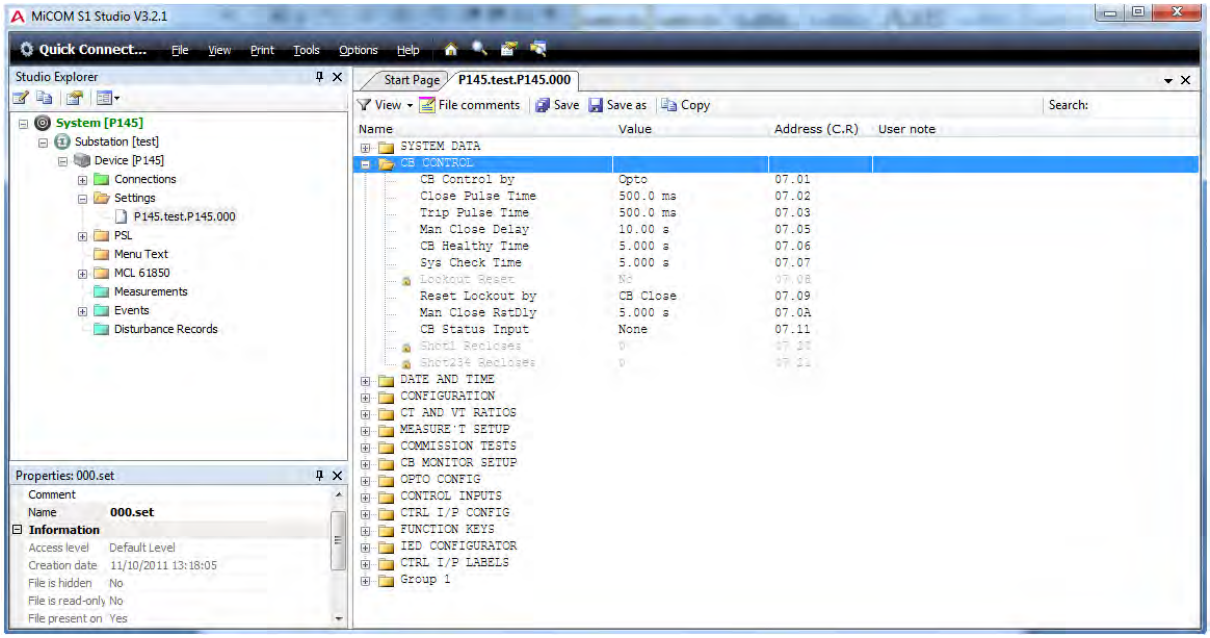


Figure 4.63: CB control

The *Configuration* settings are enabled and disabled for individual protection functions. Those settings that are enabled include overcurrent, negative sequence overcurrent, earth fault 1, negative sequence overvoltage, CB fail, fault locator, system checks and direct access as shown in Figure 4.64.

The overcurrent protection element provides four-stage non-directional overcurrent with independent time delay characteristics. The first two stages are chosen between inverse definite minimum time (IDMT) and definite time (DT) characteristics. They are supplied with a time hold facility, which may be set to zero or to a definite time value. Setting the timer to zero means that the overcurrent timer for that stage will reset instantaneously once the current falls below 95% of the current setting. If the timer has a value other than zero, the relay will repeatedly reset and not be able to trip until the fault becomes permanent. By using the timer hold facility the relay will integrate the fault current pulses, thereby reducing fault clearance times. The third and fourth stages are restricted to definite time characteristics only. The overcurrent protection element is distinctive in that it can be applied with only two phases and it will effectively derive the missing phase.

The Earth Fault 1 (EF1) element is used to measure currents directly from the system using a CT or residual connection. The residual connection is derived internally from the summation of three-phase currents. The detection of negative sequence overvoltage is an alternative to earth fault detection, which does not require any measurement of current. Instead it determines the input voltage rotation and magnitude of VTs. This is particularly advantageous in high impedance systems, where the voltage is measured at the secondary terminal through a broken delta connection. This causes a rise in neutral voltage with respect to earth, commonly referred to as the Neutral Voltage Displacement (NVD).

The fault locator element uses information from the current and voltage inputs to provide a distance to fault location characteristic. The sampled data from the analog input is written to a recurring buffer until a fault condition is detected. The data in the input buffer is frozen such that the buffer contains 6 cycles of pre-triggered data and 6 cycles of post-triggered data. When the fault calculation is complete the fault location

information is available in the fault recorder log. The element stores sampled data within a resolution of 24 samples per cycle.

The system check element deals with the monitoring of circuit breaker voltages. It carries out synchronism checks to determine whether the phase angle, frequency and voltage magnitude between vectors are within permitted limits.

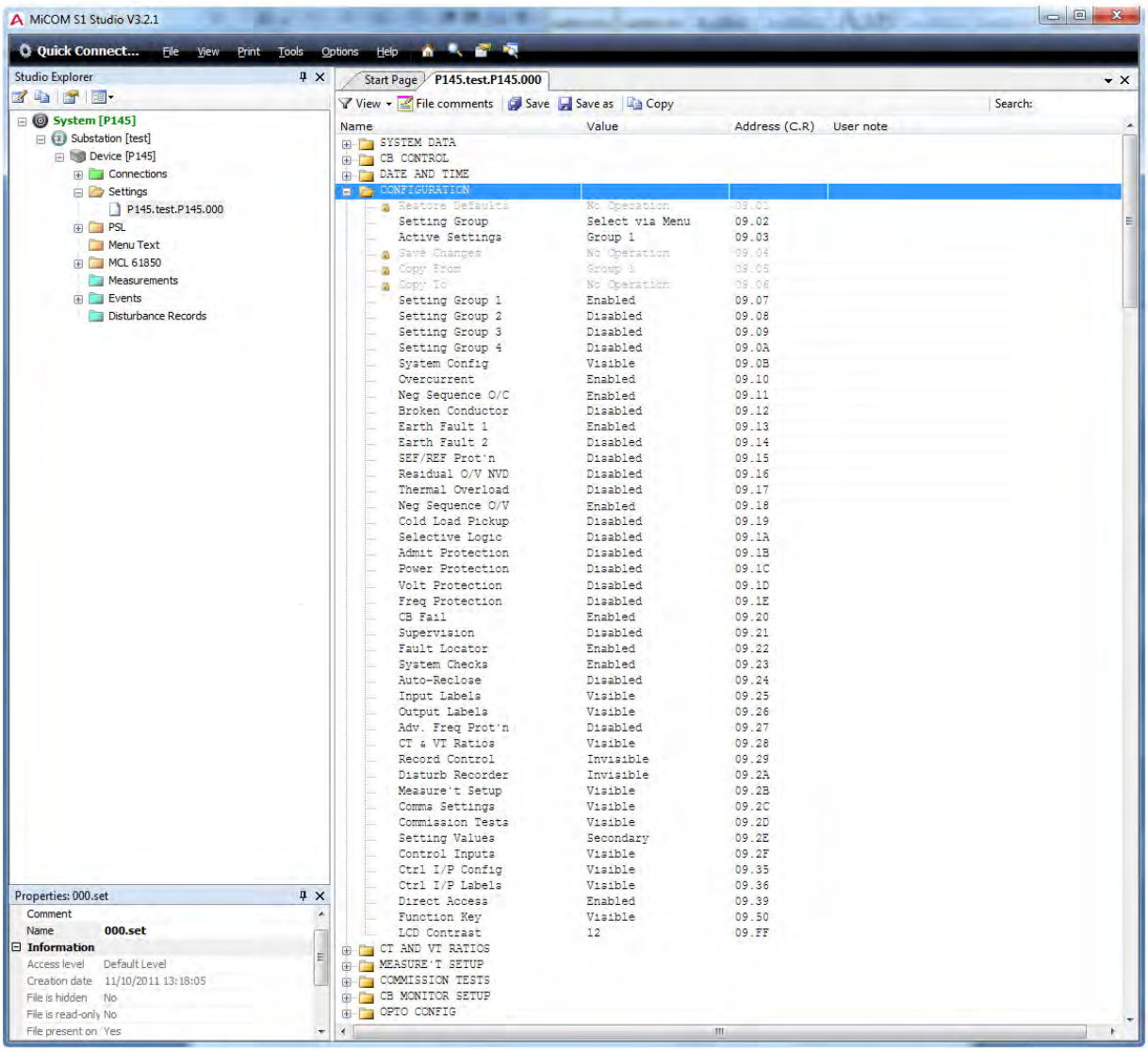


Figure 4.64: Configuration settings

The *Universal Optoisolated Input Logic* setting is programmed with a pick-up or drop-off characteristic of 60-80%. A logic '1' value is asserted for voltages ≥80% of the lower nominal voltage and a logic '0' is asserted for voltages ≤60% of the set upper nominal voltage. The lower voltage eliminates transitory pickups that occur when stray capacitances arise across a input. The nominal voltage is rated at 110/125V. Figure 4.65 illustrates the optoisolated input configurations.

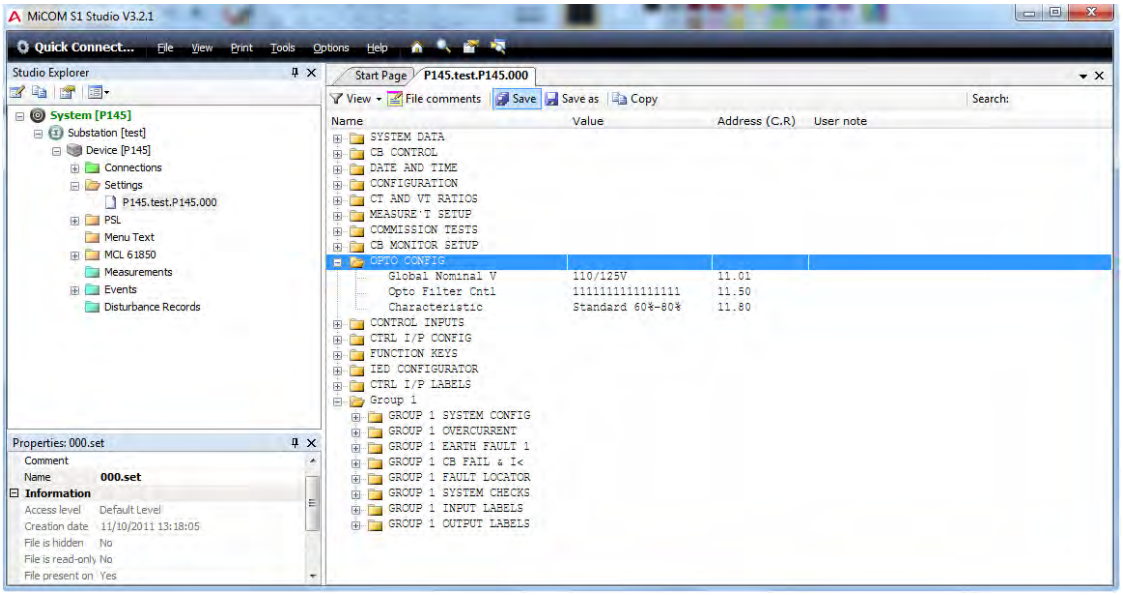


Figure 4.65: Universal optoisolated input logic

The *Control I/P Configuration* setting allows the user to configure the control inputs as either 'Latched' or 'Pushed'. A latched control input remains in the set condition until a reset command is given. A pushed control input stays energised for 10ms and resets automatically. These control inputs are individually assigned by logic '1' to the hotkey, in order to set and reset control commands. Figure 4.66 illustrates the control I/P configuration settings.

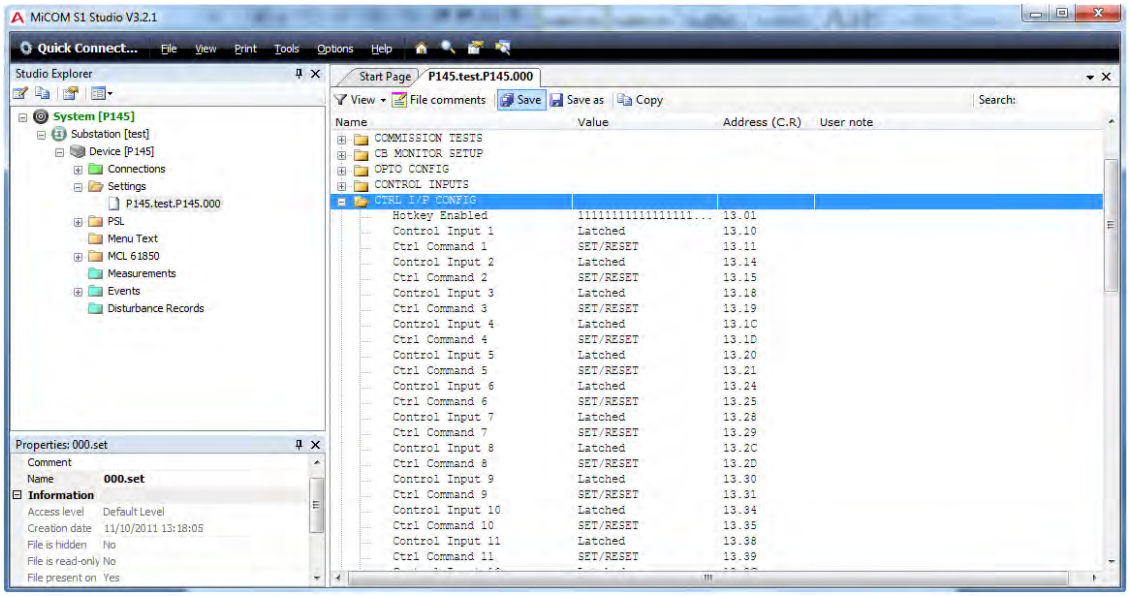


Figure 4.66: Control I/P configuration

The *Group 1 Overcurrent and Earth Fault 1* settings are both set with a non-directional IEC standard inverse operating characteristic. The Group 1 overcurrent setting has a minimum pickup current of 1A and a time multiplier setting of 0.5. The Group 1 earth

fault 1 setting has a pickup of 200mA and a TMS of 1. Zero sequence polarising is set to 5V. Figure 4.67 and Figure 4.68 illustrates the Group 1 overcurrent and earth fault 1 settings.

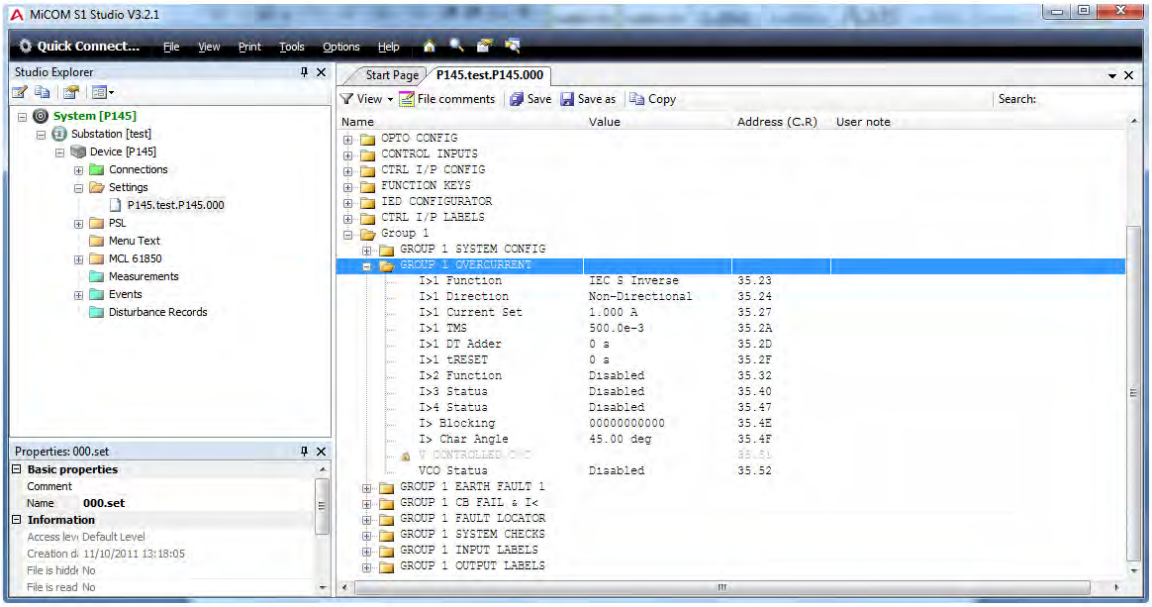


Figure 4.67: Group 1 (overcurrent)

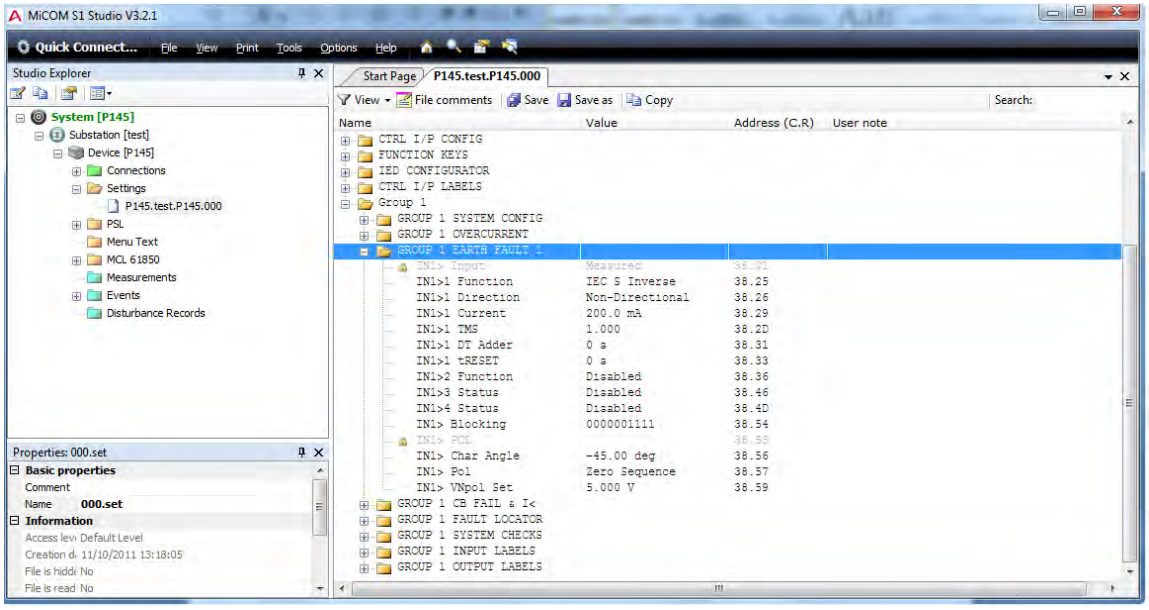


Figure 4.68: Group 1 (earth fault 1)

The *Group 1 Circuit Breaker Fail and Undercurrent* setting is activated by current, voltage or external protection elements. For current protection, the reset condition is used to determine if the CB is opened. For non-current protection, the reset criteria is selected by means of setting a CB fail condition. CB fail 1 is enabled with a timer of 200ms and a undercurrent value of 200mA. The undercurrent value is kept low as possible so that the circuit breaker poles may trigger a fault.

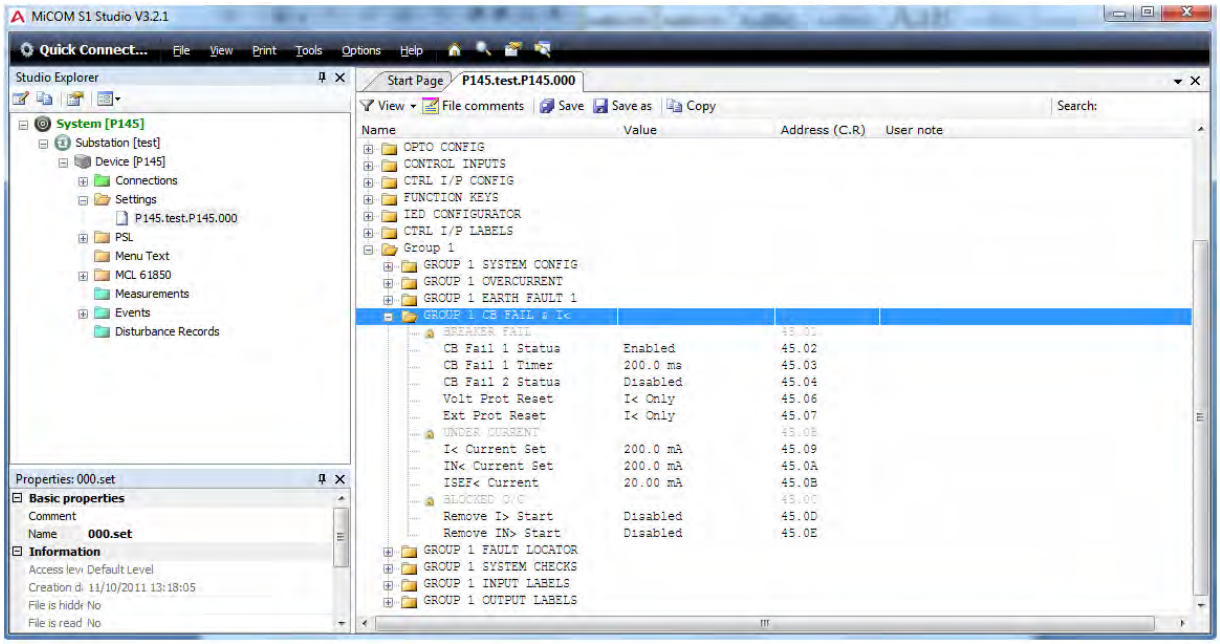


Figure 4.69: Group 1 (CB fail and I<)

The *Group 1 Fault Locator* setting is set with a line length of 300km and a positive sequence line impedance of 15Ω. The residual compensation factor (KZN) is set to 1. The residual impedance compensation magnitude and angle are calculated using equation 4.7. Figure 4.70 illustrates the Group 1 fault locator setting.

$$KZN_{\text{Residual}} = \frac{Z_{L0} - Z_{L1}}{3Z_{L1}} \qquad (4.7)$$

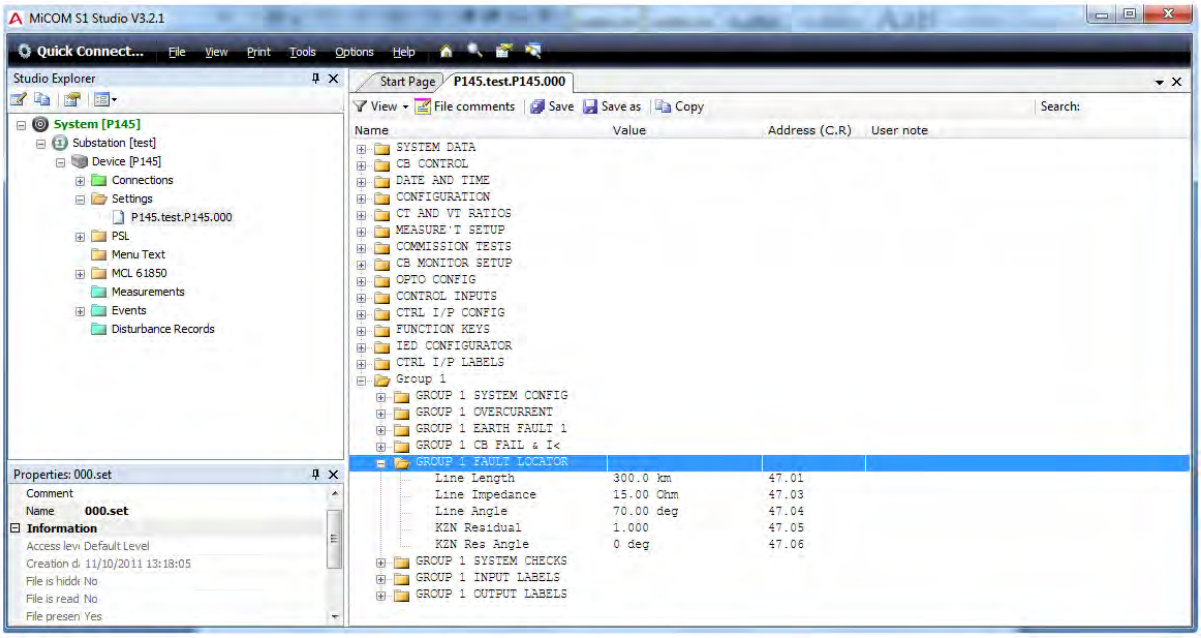
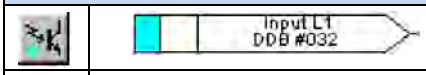
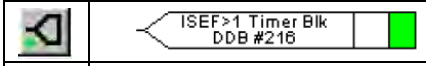
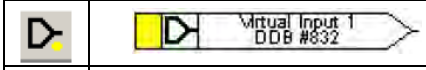
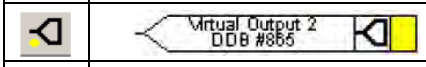
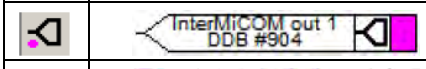
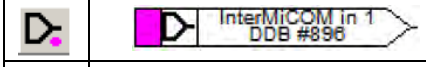
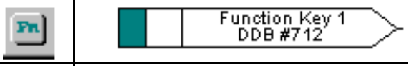
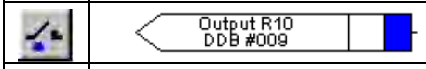
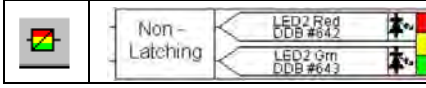


Figure 4.70: Group 1 (fault locator)

The PSL editor is invoked through the Studio Explorer pallet in order to map IED functionalities. Logic gates can be programmed to perform a range of different functions and can accept any number of inputs. Timers are used to create a delay or prepare logic outputs (i.e. creating a pulse of fixed duration on the output regardless of the length of the pulse at the input). The outputs of the PSL are associated to the LEDs on the front panel and rear contacts. Table 4.3 highlights some of the toolbar icons representing the signals of the PSL module.

Table 4.3: PSL editor toolbar icons

Icon	Description
	Optoisolated signal
	Input signal
	Output signal
	GOOSE In
	GOOSE Out
	Control In
	InterMiCOM out
	InterMiCOM in
	Function Key
	Fault Record Trigger
	LED signal
	Contact signal
	LED conditioner

Each signal is matched to a Digital Data Bus (DDB) number which is associated to a distinct logical node (Appendix A). For example, activating input signal *IN1>1 Trip* will declare DDB #261. This logical node is used to trip stage 1 earth faults. Figure 4.71 illustrates a top level perspective of the PSL mapping for the breaker failure scheme. Note that the DDB signals for trip in and trip out are combined together. Figures B.1 through to B.9 portray a close-up depiction of individual IED mappings as indicated in Appendix B. In order to map the functions of the IED, it is important to refer to Table A.8 which describes the role of each logical node icon.

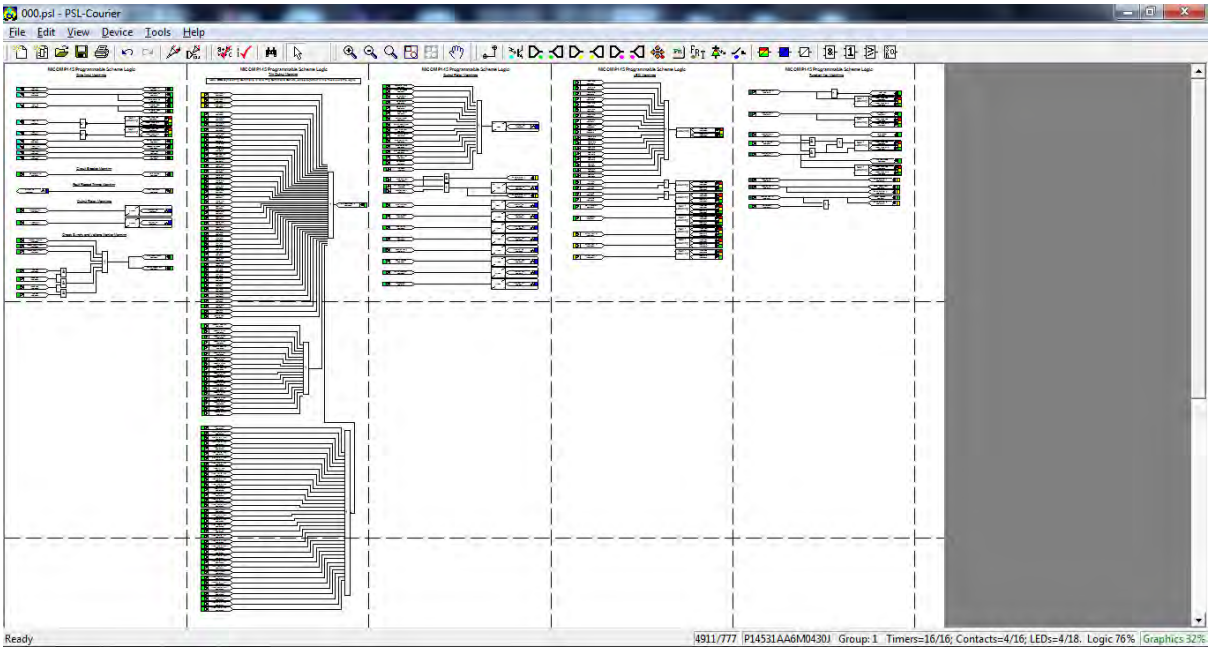


Figure 4.71: Top level PSL mapping

The '*Quick Connect*' icon is selected to allocate the device, port and connection parameters. The P145 is a Px40 device which performs protection requirements for MV to HV applications. An Ethernet port connection with IP address 192.168.2.15 is assigned for front and rear control. Access level 1 and 2 are set with password 'AAAA'. These two levels support read and write commands (i.e. opening and closing circuit breakers, resetting fault alarms and clearing event records). Access level 0 does not require a password considering it is an read only entry. Figure 4.72 illustrates the Quick Connect settings.

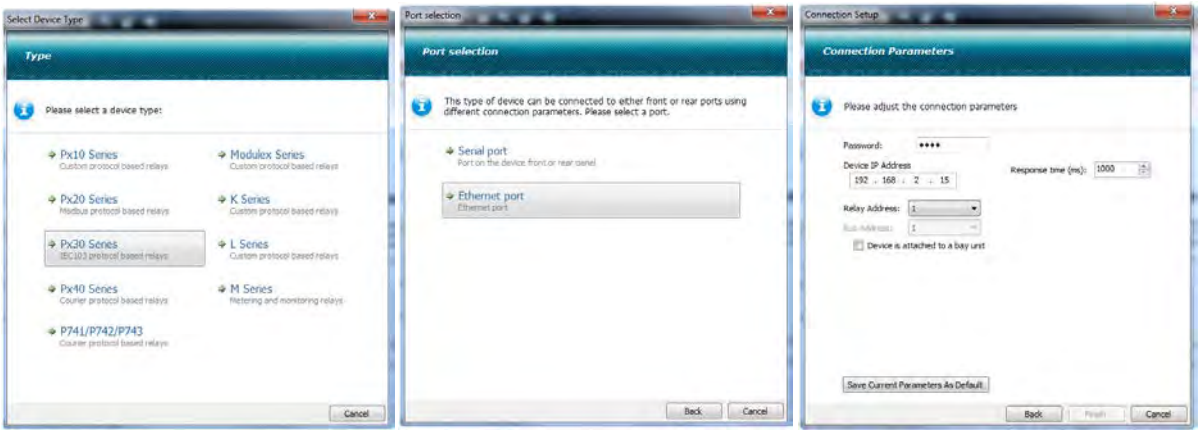


Figure 4.72: Quick connect settings

A '*New*' MCL 61850 file is created from the device context menu in the Studio Explorer. File *P145.test.P145.001* is compiled to configure datasets and subscribe/publish logical nodes using the IEC61850 IED Configurator. Figure 4.73 shows the communication settings of the relay where the media type is set to fibre.

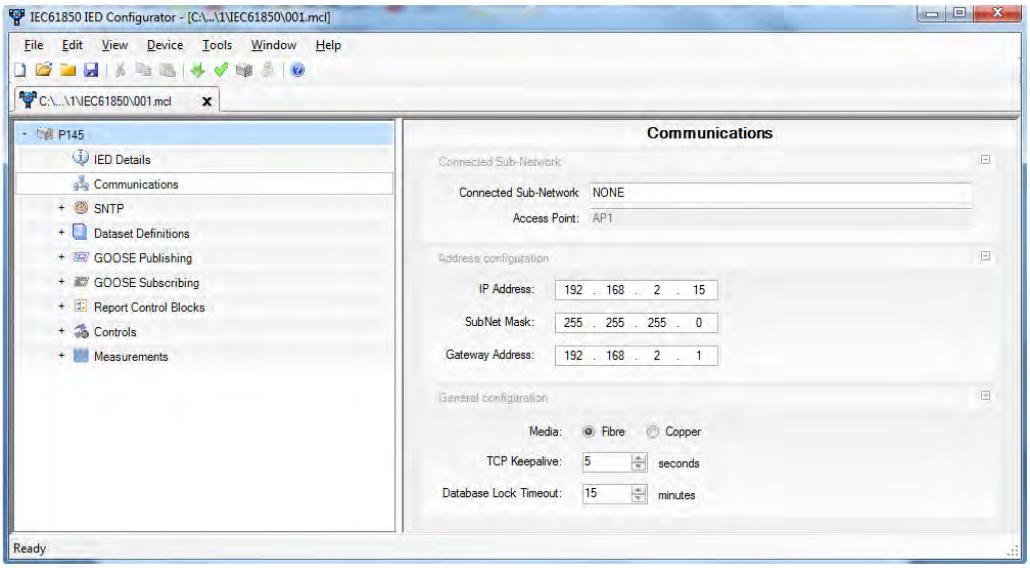


Figure 4.73: Communication settings

Datasets are added through the 'Data Definitions' selection where GosGGIO2 is associated with GOOSE outputs (Figure 4.74).

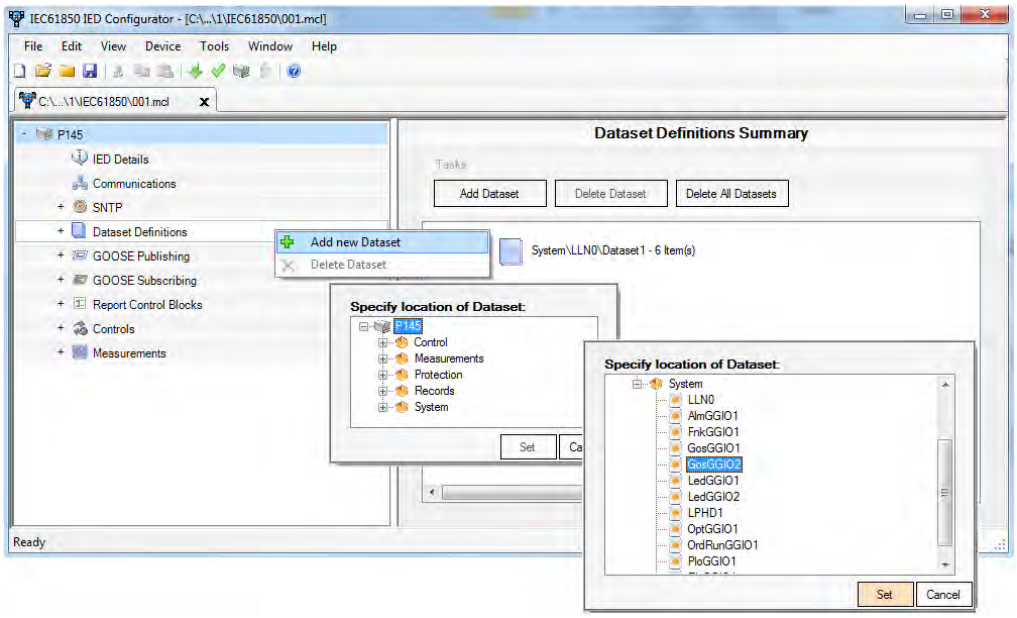


Figure 4.74: Dataset definitions

There are 32 GosGGIO2 outputs, of which only six are subscribed to perform circuit breakerstatus. These include data attributes Ind1.stVal (open SEL487E CB), Ind2.stVal (open SEL311L CB), Ind3.stVal (open REF615 CB), Ind4.stVal (close SEL487E CB), Ind5.stVal (close SEL311L CB) and Ind6.stVal (close REF615 CB).

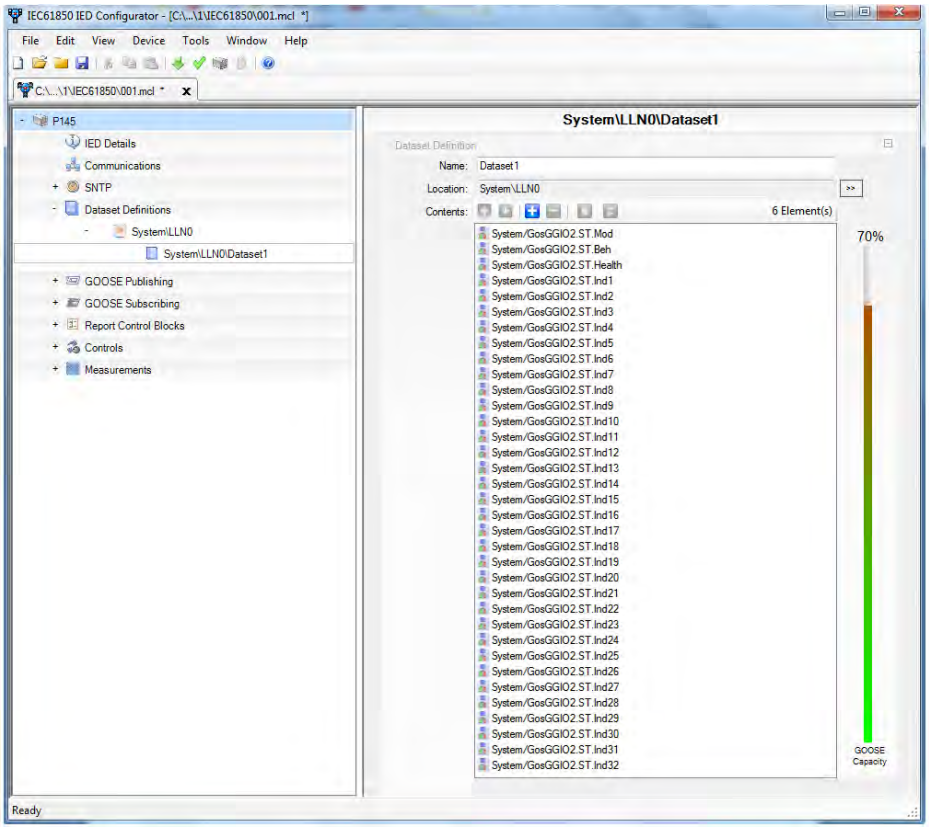


Figure 4.75: GosGGIO2 outputs

Figure 4.76 through to Figure 4.81 illustrate the GOOSE subscriptions. Each source path is composed of a logical device, logical node, function constraint, data name and attribute identifier as discussed in Figure 4.1. For example, if the source path is SEL_487E_1\ANN\CCOUTGGIO21\Ind01.stVal; the logical device is SEL_487E_1, the logical node is Annunciation (ANN), the function constraint is CCOUTGGIO21, the data name is Ind1 and the attribute identifier is stVal.

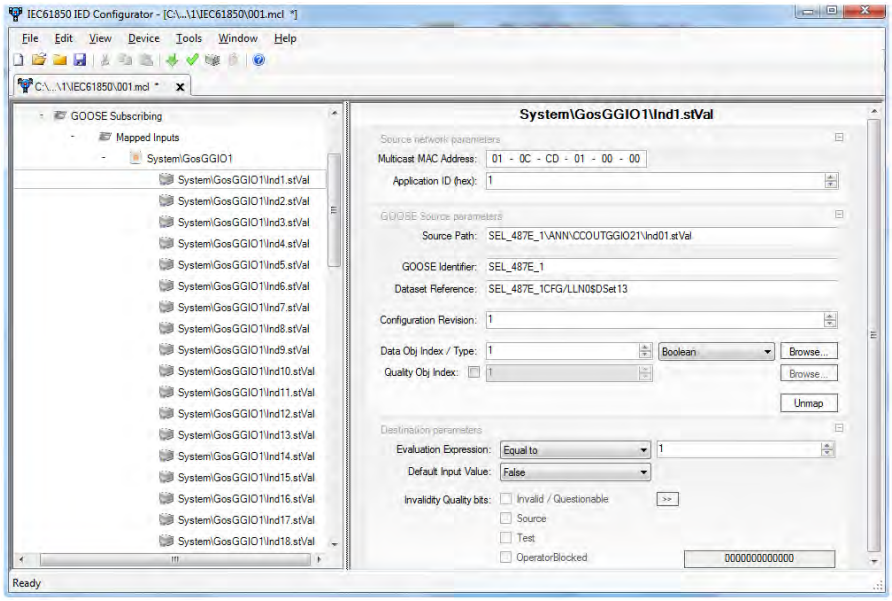


Figure 4.76: GOOSE subscription (Ind1.stVal)

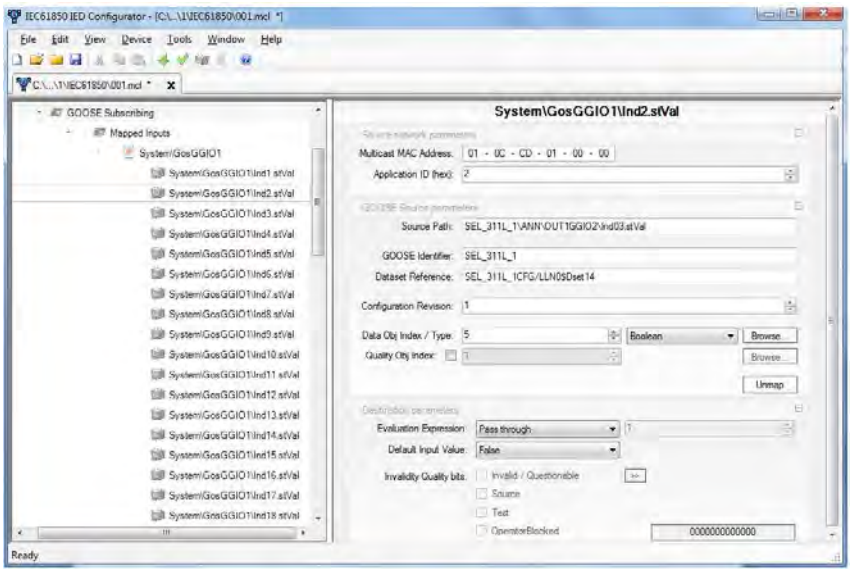


Figure 4.77: GOOSE subscription (Ind2.stVal)

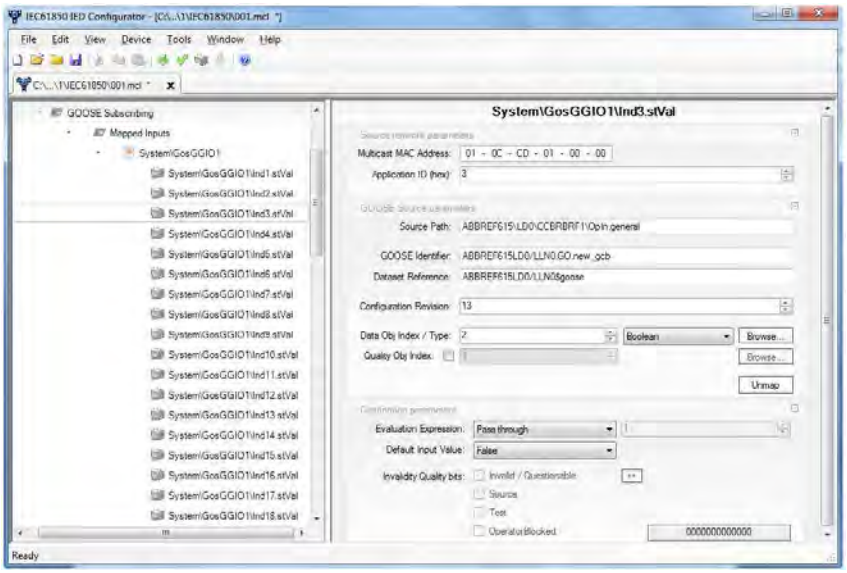


Figure 4.78: GOOSE subscription (Ind3.stVal)

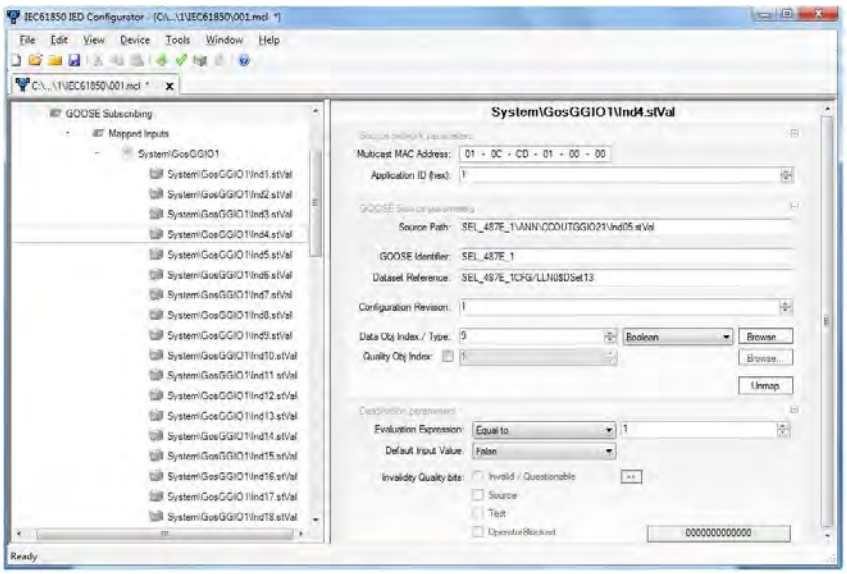


Figure 4.79: GOOSE subscription (Ind4.stVal)

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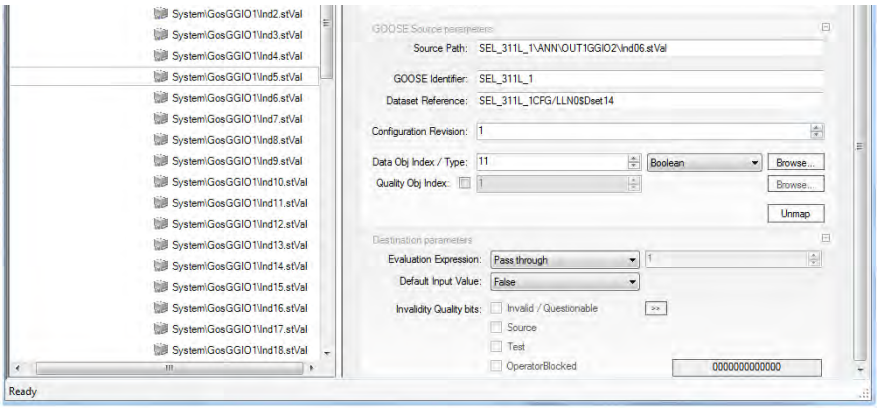

Figure 4.80: GOOSE subscription (Ind5.stVal)

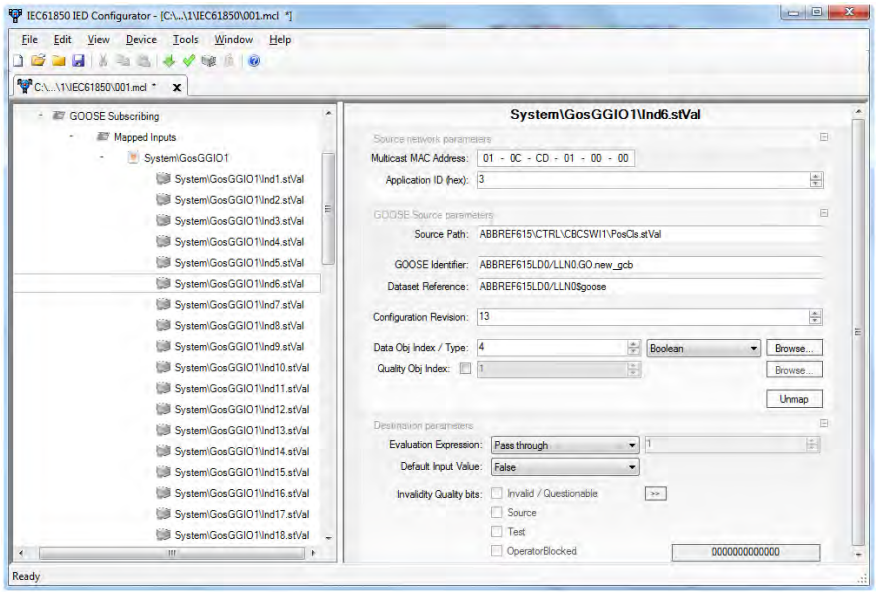

Figure 4.81: GOOSE subscription (Ind6.stVal)

To publish the GOOSE messages, the MAC Address, Application ID, VLAN ID and VLAN priority are entered as shown in Figure 4.82.

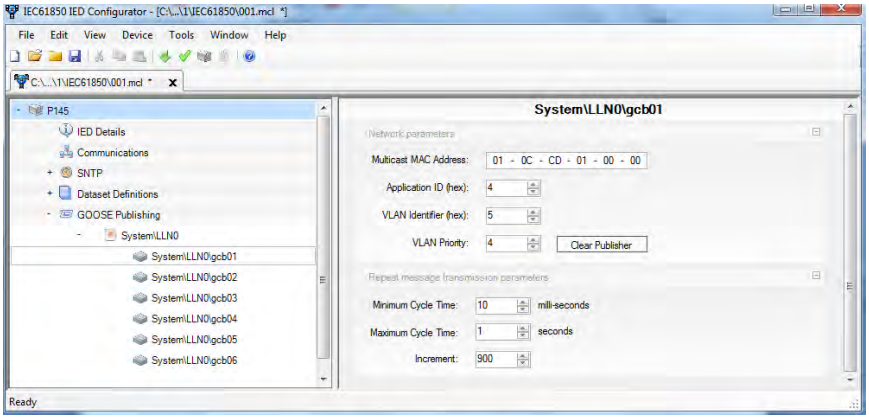

Figure 4.82: GOOSE publish

The ICD/CID file is then sent to the relay by selecting *Device → Send Configuration*.

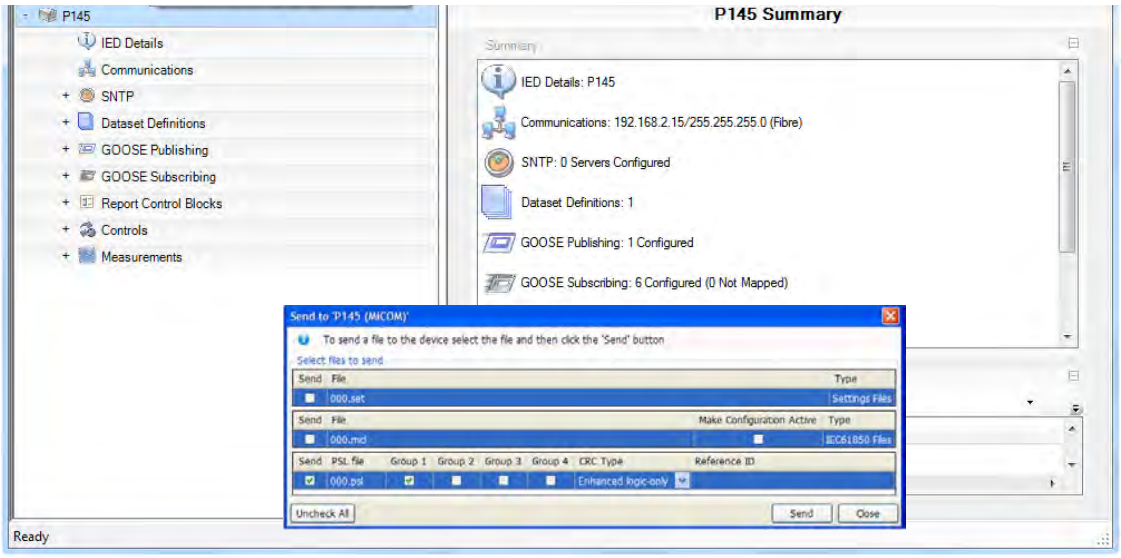

Figure 4.83: Sending CID file to the P145

4.5.6 SEL-2407

The SEL-2407 Satellite-Synchronised Clock makes use of the SEL-5860 Time Service application. The software supports both serial-port data and internal system settings for local-time. The SEL-2407 GPS clock requires the installation of a bullet antenna on the outer panel of the IEC61850 testing unit. A TNC connector coupled to the antenna allows for extra shielding and reliability. The antenna is concealed by a waterproof covering designed to withstand exposure of extreme temperatures, excessive vibration, rain and sunlight [42]. The antenna is positioned vertically so that the half-round radome has a 360º view of the sky. The antenna is capable of transmitting time signals as far as 4km over fibre optic cable [42]. Figure 4.84 illustrates the bullet antenna fixture.

Figure 4.84: Bullet antenna

The SEL-5860 Time Service application is easy to operate and takes a few simple steps

Figure 4.85. The rate of synchronisation is selected as *Every Minute* seeing as it provides polling of time events at predetermined intervals. The serial port is set as a communication (COM) port preference. The time zone obtains Universal Coordinated Time (UTC) offset information from the PC considering it acts as a server.

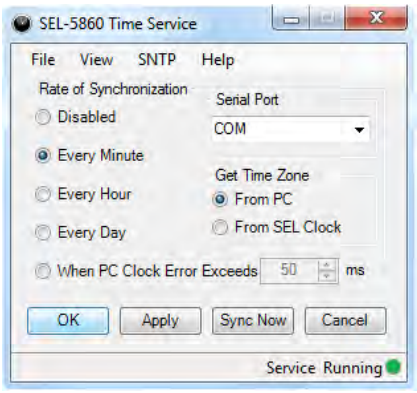

Figure 4.85: SEL-5860 time service

Once the *File → Start Service* command is selected and synchronisation is successful, the time service will display '*Service Running*' as shown in Figure 4.85. If there is an error or loss of communication, the software generates an Event Viewer which reports a warning message to the user. Depending on the type of Windows operating system or security policies, synchronisation can sometimes be blocked from the PC. In such an event, the SEL-5860 Time Service application should be set to automatically run settings via the control panel. This can be carried out by selecting '*Run*' from the start menu and entering the file source '*services.msc*'. A list of local services emerge in which the '*SEL-5860 Time Service*' banner must be right-clicked in order to change the '*Properties*'. The startup type is then customised from Manual to Automatic. Figure 4.86 illustrates a real-time representation of the SEL-2407.

Figure 4.86: Real-time operation of the SEL-2407

4.6 Verification Tests

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Scout software combines the ICD/CID files generated by the vendor specific tools into a single SCD file. The IED Scout software discovers the content of the data model by analysing the actual values of the dataset [45]. The software requires an OMICRON dongle to acquire full functionality when sniffing GOOSE messages. The CMC356 test set incorporates an auto crossover Ethernet cable (ETH1) to establish physical connection between the PC and test set. The test set must be associated to prevent forbidden users from accessing the device via the network. To establish association the '*Associate*' button on the back of the CMC356 is pressed. This leads to the immediate scan and capture of all four IEDs as shown in Figure 4.87. If the '*Subscribe*' button is clicked, the GOOSE ID (GoID), Application ID (AppID), Dataset Name (DatSet), binary digits and other functions are broadcast. The binary digits are used to monitor the change in logic (i.e. True '1', False '0') during the course of performing physical tests on the relays (i.e. pushing pushbuttons, tripping circuit breakers, etc). Table 4.3 illustrates the GOOSE Mapping Matrix of the overall system.

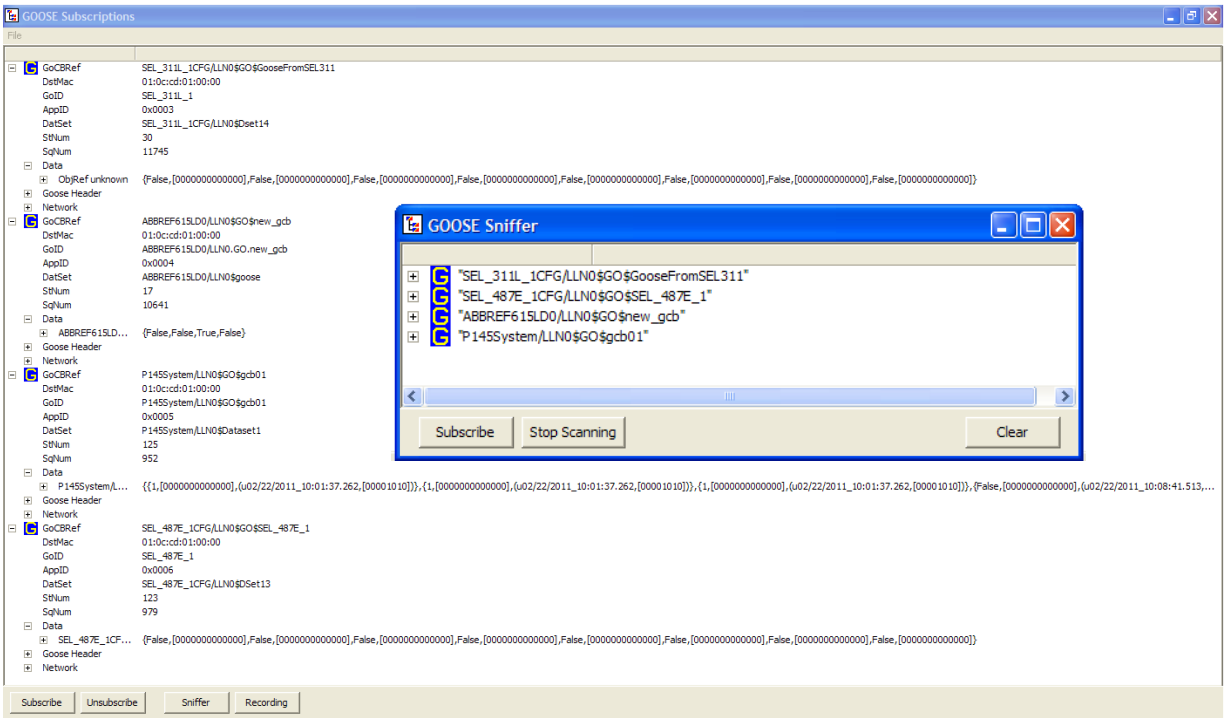


Figure 4.87: IED Scout capturing GOOSE messages

Table 4.4: GOOSE mapping matrix

GOOSE MAPPING MATRIX					Subscriber & Function: SEL 487-E						SEL 311-L						ABB REF615						Areva Micom P145					
				Action	Trip CB	Trip CB	Trip CB	PB LED 4	PB LED 5	PB LED 6	Trip CB	Trip CB	Trip CB	Text 1	Text 2	Text 3	Trip CB	Trip CB	Trip CB	LED 3	LED 4	LED 5	Trip CB	Trip CB	Trip CB	LED 6	LED 7	LED 8
NB: - All published GOOSE messages are Broadcast - Please see previous sheet for IED Information				Relay Input Reference (LD.LN.DataBit.DataType)	CCIN001 (ANN.CCINGGIO20.Ind001.stVal)	CCIN002 (ANN.CCINGGIO20.Ind002.stVal)	CCIN003 (ANN.CCINGGIO20.Ind003.stVal)	CCIN004 (ANN.CCINGGIO20.Ind004.stVal)	CCIN005 (ANN.CCINGGIO20.Ind005.stVal)	CCIN006 (ANN.CCINGGIO20.Ind006.stVal)	RB1 (CON.RBGGIO1.SPCSO01.stVal)	RB2 (CON.RBGGIO1.SPCSO02.stVal)	RB3 (CON.RBGGIO1.SPCSO03.stVal)	RB4 (CON.RBGGIO1.SPCSO04.stVal)	RB5 (CON.RBGGIO1.SPCSO05.stVal)	RB6 (CON.RBGGIO1.SPCSO06.stVal)	TRPPTRC1 (LD0.TRPPTRC1.Tr.general)	TRPPTRC1 (LD0.TRPPTRC1.Tr.general)	TRPPTRC1 (LD0.TRPPTRC1.Tr.general)	DCSXSWI1.Open (CTRL.DCSXSWI1.PosOpn.stVal)	DCSXSWI2.Open (CTRL.DCSXSWI2.PosOpn.stVal)	DCSXSWI3.Open (CTRL.DCSXSWI3.PosOpn.stVal)	Virtual Input 1 (System.GosGGIO1.Ind1.stVal)	Virtual Input 2 (System.GosGGIO1.Ind2.stVal)	Virtual Input 3 (System.GosGGIO1.Ind3.stVal)	Virtual Input 4 (System.GosGGIO1.Ind4.stVal)	Virtual Input 5 (System.GosGGIO1.Ind5.stVal)	Virtual Input 6 (System.GosGGIO1.Ind6.stVal)
Publisher Information																												
	Generated By	**Data Bit**	**SCL Name (IEDName.GooseID.LD.LN.DataBit.DataType)**																									
SEL 487-E	CB Fail	CCOUT1	SEL_487E_1.SEL_487E_1.ANN.CCOUTGGIO21.Ind01.stVal								x						x						x					
	SPARE	CCOUT2	SEL_487E_1.SEL_487E_1.ANN.CCOUTGGIO21.Ind02.stVal																									
	PB10	CCOUT3	SEL_487E_1.SEL_487E_1.ANN.CCOUTGGIO21.Ind03.stVal											x														
	PB11	CCOUT4	SEL_487E_1.SEL_487E_1.ANN.CCOUTGGIO21.Ind04.stVal																	x								
	PB12	CCOUT5	SEL_487E_1.SEL_487E_1.ANN.CCOUTGGIO21.Ind05.stVal																							x		
	Prot Trip/Inter-Trip Rec.	CCOUT6	SEL_487E_1.SEL_487E_1.ANN.CCOUTGGIO21.Ind06.stVal																									
SEL 311-L	OUT101 (SPARE)	OUT1GGIO1	SEL_311L_1.GooseFromSEL311.ANN.OUT1GGIO2.Ind01.stVal																									
	OUT102 (Prot Trip/Inter-Trip Rec.)	OUT1GGIO2	SEL_311L_1.GooseFromSEL311.ANN.OUT1GGIO2.Ind02.stVal																									
	OUT103 (CB Fail)	OUT1GGIO3	SEL_311L_1.GooseFromSEL311.ANN.OUT1GGIO2.Ind03.stVal				x											x						x				
	OUT104	OUT1GGIO4	SEL_311L_1.GooseFromSEL311.ANN.OUT1GGIO2.Ind04.stVal					x																				
	OUT105	OUT1GGIO5	SEL_311L_1.GooseFromSEL311.ANN.OUT1GGIO2.Ind05.stVal																		x							
	OUT106	OUT1GGIO6	SEL_311L_1.GooseFromSEL311.ANN.OUT1GGIO2.Ind06.stVal																								x	
ABB REF615	Prot Trip (Inv. TOC)	DPHLPTOC	ABBREF615.new_gcb.LD0.DPHLPTOC1.Op.general																									
	CB Fail	CCBRBRF1	ABBREF615.new_gcb.LD0.CCBRBRF1.OpIn.general			x						x													x			
	CB Open	CBCSWI1.Open	ABBREF615.new_gcb.CTRL.CBCSWI1.PosOpn.stVal						x						x													
	CB Closed	CBCSWI1.Closed	ABBREF615.new_gcb.CTRL.CBCSWI1.PosCls.stVal																									x
Areva Micom P145	CB Fail	Virtual Output 1	P145.gcb01.System.GosGGIO2.Ind1.stVal		x								x						x									
	FK8	Virtual Output 2	P145.gcb01.System.GosGGIO2.Ind2.stVal							x																		
	FK9	Virtual Output 3	P145.gcb01.System.GosGGIO2.Ind3.stVal													x												
	FK10	Virtual Output 4	P145.gcb01.System.GosGGIO2.Ind4.stVal																			x						
	SPARE	Virtual Output 5	P145.gcb01.System.GosGGIO2.Ind5.stVal																									
	Prot Trip/Inter-Trip Rec.	Virtual Output 6	P145.gcb01.System.GosGGIO2.Ind6.stVal																									

Device Name	IP Address	Broadcast MAC Address	VLAN ID	VLAN Priority	App ID	GoCB Ref	GOOSE ID	Dataset	Breaker Open Control	Breaker Close Control
SEL 487-E	192.168.2.20	01:0C:CD:01:00:00	5	5	6	SEL_487E_1CFG/LLN0GOSEL_487E_1	SEL_487E_1	SEL_487E_1CFG/LLN0$DSet13	PB1	PB2
SEL 311-L	192.168.2.5	01:0C:CD:01:00:00	5	5	3	SEL_311L_1CFG/LLN0GOGooseFromSEL311	SEL_311L_1	SEL_311L_1CFG/LLN0$Dset14	Front Controls	Front Controls
ABB REF615	192.168.2.10	01:0C:CD:01:00:00	5	5	4	ABBREF615LD0/LLN0GOnew_gcb	ABBREF615LD0/LLN0.GO.new_gcb	ABBREF615LD0/LLN0$goose	Front Controls	Front Controls
Areva Micom P145	192.168.2.15	01:0C:CD:01:00:00	5	5	5	P145System/LLN0GOgcb01	P145System/LLN0GOgcb01	P145System/LLN0$Dataset1	FK2	FK3

4.7 Troubleshooting

Although ultimately commissioning of the portable IEC61850 testing unit led to the interoperability between the SEL-311L, SEL-487E, REF615 and P145 relays; achieving such a goal came with some technical issues which delayed the progress of intended tasks. These include:

- Different relay manufacturers publishing their GOOSE messages in slightly different ways. The way in which most third party relays subscribe to these messages requires some modification (i.e. Device ID). This was compound by the fact that the GOOSE mapping process in the relay manuals is unclear, particularly when describing how to subscribe to third party devices. Manufacturers appear to deliberately omit this information. For example, in regards to the REF615 relay, quality attributes were not located after the status values of the data objects. To overcome this shortfall the dataset entries were set to single data attributes, such as stVal, instead of functional constraint data object structures by which the tool proposes by default.

- VLAN tags on the RSG2200 Ethernet switch were being stripped on outgoing GOOSE messages. This blocked vital GOOSE communication of the P145. To overcome this problem, it was necessary to update the P145 firmware which meant the relay needed to be physically dispatched back to the manufacturer. However, instead of choosing this option it was decided to disable the GVRP support on the RSG2200. This brought about the discovery that all ABB files require a GOOSE identifier of *ER101PR10LD0/LLN0.GO.GCB01* as shown in Figure 4.88.

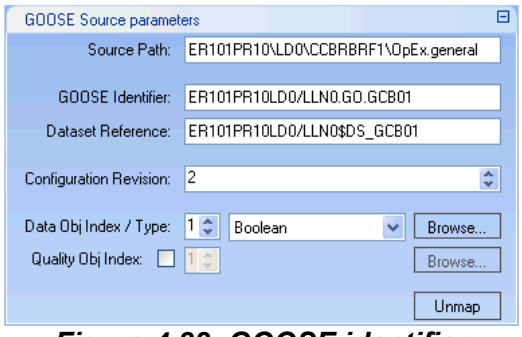


Figure 4.88: GOOSE identifier

- Restrictions in access levels for some relays made debugging and local control difficult. Nor engineer or admin rights were permitted. To overcome these problems, remote communication services were utilised via the offline mode.

- Overlooked wiring connections and human error resulted in some incorrect terminal connections. This was dealt by re-examining steps and inspecting AC and DC schematics.

4.8 Conclusion

This chapter confirmed interoperability between ABB, Areva and SEL devices by highlighting the steps necessary to configure the settings of the vendor specific software packages. A virtual wiring map was considered prior to system configuration in order to forecast GOOSE bits. The system performs breaker failure and enables fault location settings. The CMC356 test set captures GOOSE messages published on the network, in the form of CID or ICD files. These files are merged into a single SCD file, which contains the single line diagram of the substation. The RSG2200 Ethernet switch controls the IEDs via the management VLAN. GVRP support is disabled on the switch to prevent VLAN tags from being stripped on outgoing GOOSE messages.

Chapter 5 – Algorithm Derivation

5.1 Introduction

The purpose of this chapter is to investigate common types of unsymmetrical faults transpiring on overhead transmission lines including phase-to-phase, phase-to-ground and three-phase faults. A range of design and construction aspects are considered including conductor materials, line supports, insulators, string efficiency, corona, sag calculations and arcing. An innovative fault locator algorithm is derived using Discrete Fourier Transformation to determine the fault distance, arc resistance, total fault resistance and tower footing resistance. The algorithm is derived based on a square wave arc model.

5.2 Overhead Transmission Line Components

Overhead transmission lines consist of many components which are used to transmit and distribute electricity across short and long distances. These components offer considerable advantages over underground transmission lines including trouble-free access when carrying out repairs by the use of cranes or truck transporters, high visibility from ground structures, one-fifth the cost of installation and maintenance, and an operational life expectancy of 70 years [47]. In comparison, underground transmission lines require expensive excavation costs, rerouting of terrain to avoid obstruction of underground infrastructures (i.e. pipelines and sewages), environmental impacts on soil and vegetation, and an operational life expectancy of 30 years [48]. The continuous operation of overhead transmission lines depends on several factors including conductor materials, line supports, insulators, string efficiency, corona, sag properties and arcing.

5.2.1 Conductor Materials

Conductors come in many different types of materials ranging from copper, aluminium, aluminium steel-reinforced, galvanised steel and cadmium copper. Each conductor has a single inner rod surrounded by consecutive wires. These wires are twisted and spiralled in opposite directions. The total number of individual wires is determined by $3n(n+1)+1$, where n is the number of layers [49]. All conductors demand high electrical conductivity and high tensile strength to withstand mechanical stresses.

Copper conductors are exploited in hard solid form. This decreases electrical conductivity while increasing tensile strength. Copper has a high current density with a small cross-sectional area. Due to its high cost, copper is replaced by aluminium conductor material. Aluminium has a cross-sectional area 1.26 times greater than the diameter of copper. The increased cross-sectional area of aluminium creates a larger surface to wind pressure and transverse strength. This suggests the implementation of taller towers with the consequence of greater sag. Such towers do not need to be as sturdy as those used for copper conductors considering the gravity of aluminium (2.71 gm/cc) is lower than that of copper (8.9 gm/cc) [50].

Aluminium steel-reinforced conductor material is used to improve the tensile strength of aluminium and make it more suitable for long distance transmissions. The aluminium steel-reinforced conductor consists of a galvanised steel core surrounded by a number of aluminium strands as shown in Figure 5.1. The steel core takes a greater percentage of mechanical strength while the aluminium strands carry the bulk of current [51]. The cross-section of the two metals is 1:6. The benefit of this conductor is its lightweight, which produces smaller sags across longer spans.

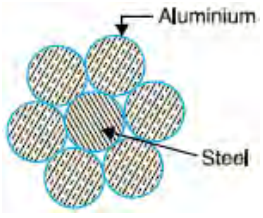


Figure 5.1: Aluminium steel-reinforced conductor cross-section

Galvanised steel conductor material is used for extra long distance transmissions exposed to abnormally high stresses. The galvanised steel conductor has poor conductivity and high resistance making it suitable for rural areas where the main consideration is cheapness. Cadmium copper contains 1-2% cadmium and 98-99%

copper. This percentage of cadmium is sufficient to increase the tensile strength by 50%, while the conductivity is reduced by 15% below that of pure copper [52].

5.2.2 Line Supports

Line supports are the supporting structures used to secure overhead conductors. These supports come in various types of pole and tower constructions including wood, steel, reinforced concrete and lattice steel. The choice of supporting structure depends on a number of characteristics such as the life span, cross-sectional area, line voltage, cost and local conditions.

Wood poles are the cheapest and most readily available. They are built from seasoned wood (i.e. sal or chir) and are widely used for distribution purposes in rural areas [53]. Wood poles have a tendency to rot beneath the ground resulting in foundation decay. To prevent such decomposition, wooden poles are impregnated with preservatives such as creosote oil. Figure 5.2 illustrates a double wood pole structure of type 'A' and 'H'. These poles are used to obtain a higher transverse strength as compared to single poles. The use of wood poles are restricted to a maximum voltage of 22kV.

Steel poles are an substitute to wood poles and are implemented in urban areas. These poles are more expensive but offer greater mechanical strength and improved structural life (i.e. 40-50 years). Steel poles come in three different categories including rail, tubular and rolled steel [54]. Such poles are painted in order to prevent corrosion.

Reinforced concrete poles (RCC) are feasible for spans between 80-200m. They offer good insulating properties and require no maintenance [55]. Figure 5.3 shows the composition of a single and double RCC pole. The main difficulty with RCC poles is the cost of transportation. As a result, such poles are manufactured on-site to limit expenditure.

Lattice steel towers are used for long distance transmissions (i.e. 300m and above) at higher voltages. Due to the towers robust construction it is capable of withstanding severe climate conditions. Tower footings are grounded by driving rods deep into the earth. This minimises lightning troubles as steel towers act as a lightning conductor [56]. Figure 5.4 illustrates a narrow-base lattice steel and broad-base lattice steel tower with transmissions at 110kV and 220kV, respectively.

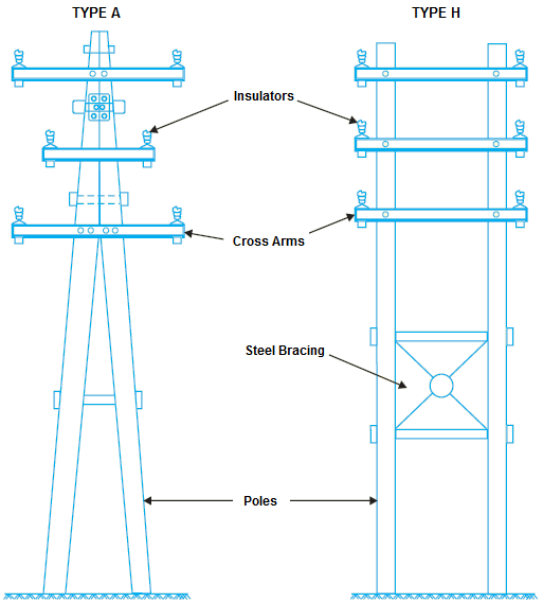


Figure 5.2: Wooden poles

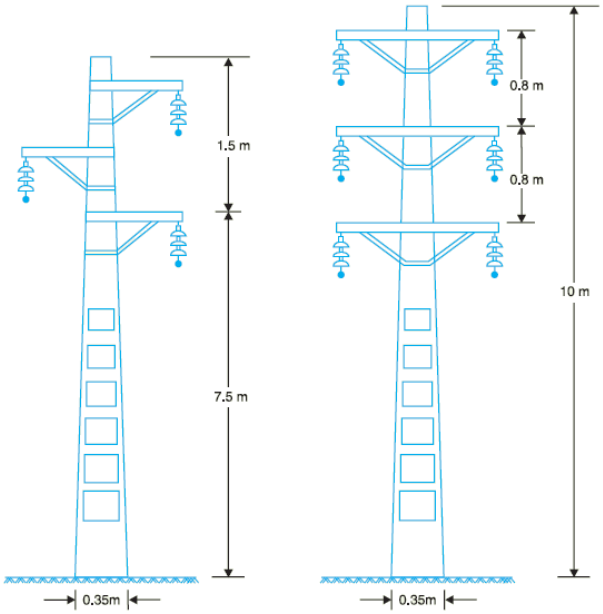


Figure 5.3: RCC poles

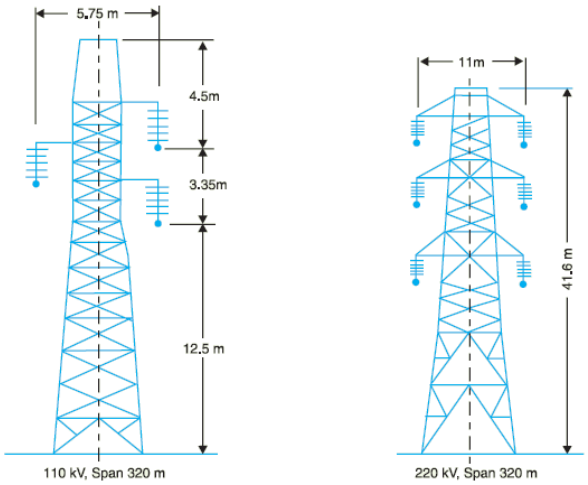


Figure 5.4: Lattice steel towers

5.2.3 Insulators

Insulators provide insulation between conductors and supports to prevent current leakage. Insulators have high mechanical strength in order to withstand conductor loads, high relative permittivity to ensure greater dielectric strength and a hi gher puncture to flashover ratio [57]. Porcelain is the most commonly used insulator material for overhead transmission lines, together with glass and steatite. Porcelain is produced by firing kaolin, feldspar and quartz mixtures at very high temperatures [58]. It is stronger than glass, less prone to temperature variations and emits fewer leakages.

The breakdown of an insulator occurs by either flashover or puncture. Flashover is when an arc takes place from the line conductor to the insulator pin. Puncture is when an arc originates from the conductor pin to the body of the insulator. Flashover will result in the insulator continuing to operate, whereas puncture will permanently destroy the insulator due to excessive heat [57]. For this reason, porcelain insulators are manufactured with a safety factor. The safety factor guarantees that flashover will arise prior to the insulator being punctured.

$$\text{Safety factor of insulator} = \frac{\text{Puncture strength}}{\text{Flashover voltage}} \tag{5.1}$$

Insulators are accessible in different types of assemblies including pin, suspension, strain and shackle [59]. Pin type insulators are secured to the cross-arm of a pole where an groove on the upper end of the insulator stores the conductor. Suspension type insulators consist of porcelain discs connected in series by metal links in the form of a string. The conductor is suspended beneath the string while the opposite end is secured to the cross-arm of the tower. These type of insulators have quite a f ew advantages over pin type insulators including each disc is designed for low voltage (i.e. 11kV); if any individual discs are damaged the whole string is not ineffective; the arrangement provides partial protection from lighting as conductors run below the cross-arm of steel towers; flexibility of the line is improved as insulator strings are free to swing in any direction where the stresses are minimal; and the overall cost is cheaper than in pin type insulators [59].

Strain insulators are used for vertical positioning of insulators where the line has a sharp bend (i.e. across long river spans). In such an event, the line tension is extremely high and strings are connected in parallel [59]. Shackle insulators are practical for horizontal connection of insulators, which are fixed on pole supports with a bolt. Figure 5.5 illustrates all four pin, suspension, strain and shackle insulators.

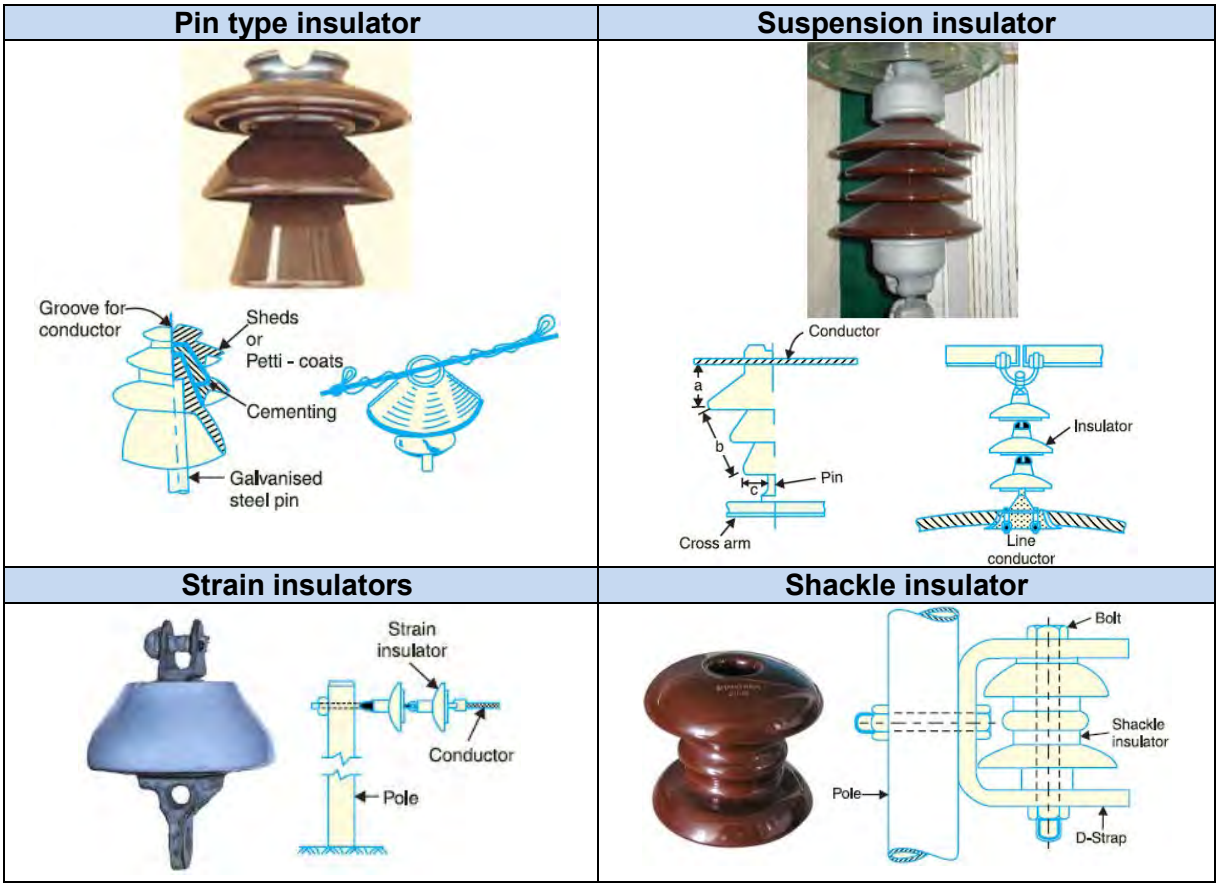


Figure 5.5: Pin, suspension, strain and shackle insulators

5.2.4 String Efficiency

String efficiency is the ratio of voltage across a string consisting of porcelain discs attached in series with metallic links [60]. The greater the string efficiency, the more uniform the potential distribution. Figure 5.6 illustrates a 3-disc string of suspension insulators. Each disc forms a mutual capacitance (C). If mutual capacitance was present by itself, the charging current and voltage will be identical through all discs. However, in actual practice, shunt capacitance (C_1) also exists between metal fittings. Due to shunt capacitance, charging current is not evenly distributed. The discs nearest to the line conductor have maximum voltage, whereas those closer to the cross-arm progressively decrease in voltage. Equation (5.2) presents the general formula for the string efficiency, where *n* is the number of discs in the string.

$$\text{String efficiency} = \frac{\text{Voltage across the string}}{\text{n} \times \text{Voltage across disc nearest to the conductor}} \quad (5.2)$$

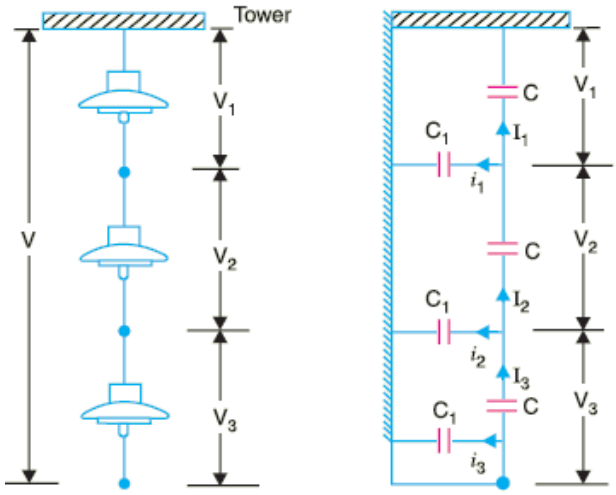


Figure 5.6: 3-disc string of insulators

If the insulator with the highest stress breaks down or flashover occurs, all consecutive insulators will stop working. Therefore, guard rings are used to improve string efficiency. Guard rings are metal rings that surround the base of the insulator (Figure 5.7). Guard rings introduce capacitances among metal fittings and line conductors. They are contoured in such a way that the shunt capacitance currents (i.e. i_1 and i_2) are equal to the metal fitting line capacitance currents (i.e. i'_1 and i'_2) [60]. This results in a charging current (I) flowing through each string.

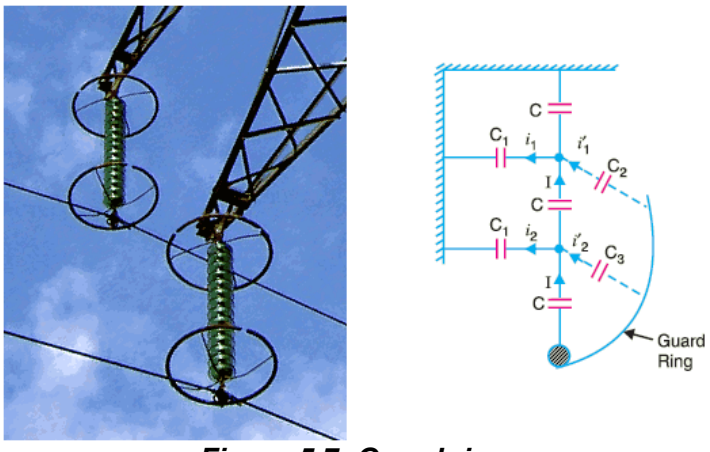


Figure 5.7: Guard ring

Other methods that can improve string efficiency include longer cross-arms and insulator grading. Longer cross-arms are highly dependent on the ratio of shunt capacitance to mutual capacitance (K). The smaller the value of K, the greater the string efficiency [61]. The value of K is decreased by reducing the shunt capacitance.

In order to reduce shunt capacitance, the distance between the conductor and tower must be increased using longer cross-arms. However, limitations due to the cost and tower strength prohibit the use of longer cross-arms. Alternatively, grading of insulators oversees the use of different sized insulators with assorted capacitance values [61]. The insulator with the smallest capacitance is placed at the top of the string.

5.2.5 Corona

Corona is an electrical discharge by which the ionisation of air surrounding a conductor glows bluish-purple. The discharge comes about when the potential gradient of the electric field is high enough to form a conductive region, but inadequate to cause breakdown or arcing [62]. If conductors are polished and smooth, the corona glow will be noticeable throughout the entire length of the line as illustrated in Figure 5.8. This has several disadvantages including loss of energy, ozone production and interference of neighbouring communications.

Figure 5.8: Corona effect

Corona is affected by the physical state of the atmosphere, conductor size, conductor spacing and line voltage [63]. In stormy weather, the number of ions is more than normal and as such corona occurs at much less voltage, relative to fairer weather. The conductor size and surface roughness decrease the value of breakdown voltage. The conductor spacing and line voltage both induce corona formation and reduce electrostatic stresses.

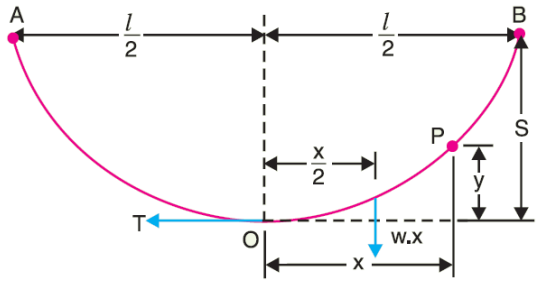
5.2.6 Sag and Tension

Conductors that are stretched uncontrollably between supports in a bid to save conductor material may reach an unsafe limit due to excessive tension. For the line not to break, conductors are allowed to have a sag or dip. The conductor sag is kept to a minimum in order to reduce conductor material and avoid extra pole height for

sufficient ground clearance. It is also desirable for the tension to be low in order to avert mechanical failures and to permit the use of fewer strong supports [64]. A low sag will result in a tight wire with high tension, whereas a low tension will imply a loose wire with increased sag. For this reason, it is standard practice to keep the conductor tension less than 50% of the overall tensile strength [64].

For equal height supports, the conductor sag between points *A* and *B* is in the shape of a parabola. Taking the lowest point *O* as the origin, the coordinates at point *P* are *x* and *y*. Assuming the curvature is not noticeable (i.e. OP=x), the two forces acting on segment *OP* are the tension (T) and weight (wx) at a distance of x/2. The maximum sag is governed by equation 5.3, where x=l/2 and y=S [64]. Figure 5.9, illustrates a conductor sag at equal heights.

$$\text{Sag} = \frac{w(l/2)^2}{2T} = \frac{wl^2}{8T} \tag{5.3}$$



l = Length of span, w = Weight per unit length of conductor, T = Tension in the conductor

Figure 5.9: Conductor sag at equal height supports

For hilly areas, conductors are suspended across unequal heights as shown in Figure 5.10. If *w* is the weight per unit length of the conductor, then the values of the sag S_1 and S_2 are calculated through distances x_1 and x_2 as stated in Equation 5.4 [64].

$$S_1 = \frac{wx_1^2}{2T} \text{ and } S_2 = \frac{wx_2^2}{2T}$$

$$x_1 + x_2 = l$$

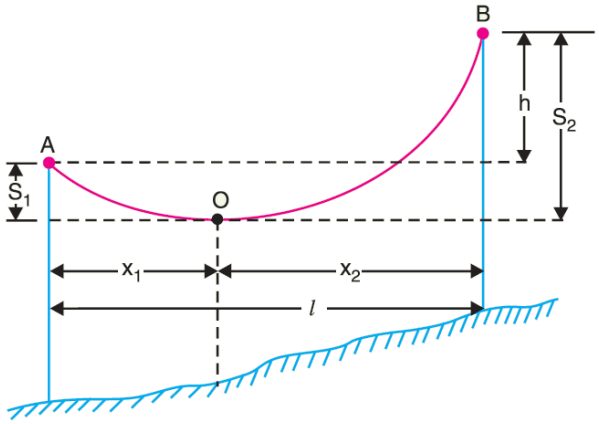
$$S_2 - S_1 = \frac{w}{2T}\left[x_2^2 - x_1^2\right] = \frac{w}{2T}(x_2 + x_1)(x_2 - x_1)$$

$$S_2 - S_1 = \frac{wl}{2T}(x_2 - x_1)$$

$$S_2 - S_1 = h$$

$$h = \frac{wl}{2T}(x_2 - x_1)$$

$$x_1 = \frac{l}{2} - \frac{Th}{wl}, \quad x_2 = \frac{l}{2} + \frac{Th}{wl} \tag{5.4}$$



l = Length of span, h = Difference in heights between two supports, T = Tension in the conductor
x_1 = Distance of support A from O, x_2 = Distance of support B from O

Figure 5.10: Conductor sag at unequal height supports

Factors that influence conductor sag and tension include conductor weight, effects of wind, ice loading and temperature variations. In the event of wind or ice loading, the weight of the ice acts vertically (i.e. in the same direction as the conductor weight) and the force of wind acts horizontally (i.e. at right angles to the conductor surface) [65]. The total force on the conductor is the vector sum of horizontal and vertical forces as illustrated in Figure 5.11.

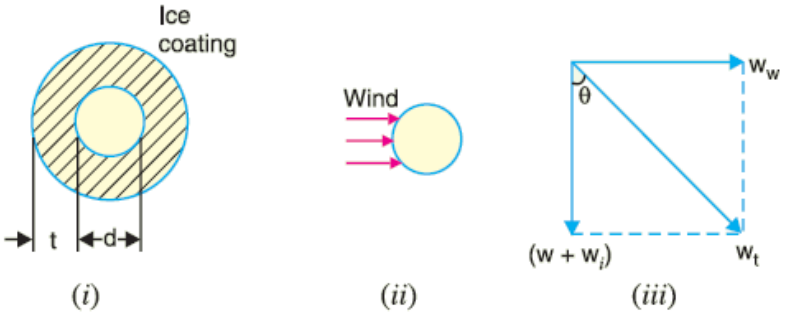


Figure 5.11: Wind and ice loading

The total weight of the conductor per unit length is:

$$w_t = \sqrt{(w + w_i)^2 + (w_w)^2} \tag{5.5}$$

where w = weight of conductor per unit length
= conductor material density x volume per unit length
w_i = weight of ice per unit length
= density of ice x volume of ice per unit length
= density of ice x $\frac{\pi}{4}\left[(d+2t)^2 - d^2\right] \times 1$
= density of ice x $\pi t(d+t)$
w_w = wind force per unit length

= wind pressure per unit area x projected area per unit length

= wind pressure x $[(d+2t)\times 1]$

5.2.7 Arcing

Arcing is the electrical breakdown of a normally nonconductive media that produces an self-sustaining plasma discharge. Arcing faults are categorised into two groups including free-burning arcs (i.e. those observed in overhead transmission lines) and constrained arcs (i.e. those analysed in circuit breakers) [66]. Arcing faults are separated into primary and secondary arcs. Primary arcs exist during a fault, where circuit breakers situated on transmission lines extinguish the arc. Secondary arcs occur on lines with single-pole switching. Single-pole switching is the practice where only the faulted phase is isolated, while the other two phases are left in operation [66]. The secondary arc is extinguished once the arc channel through the air becomes too long or overly de-ionised. The length of the arc is dependent on several factors such as the supply current, magnetic force acting on arc columns and atmospheric conditions [67]. Figure 5.12 illustrates an overhead transmission line arc.

Figure 5.12: Arcing phenomena

Arcs are purely resistive elements between a faulted line and ground. As the length of the arc increases continuously in air and the resistance increases, the arc voltage becomes non-linear.

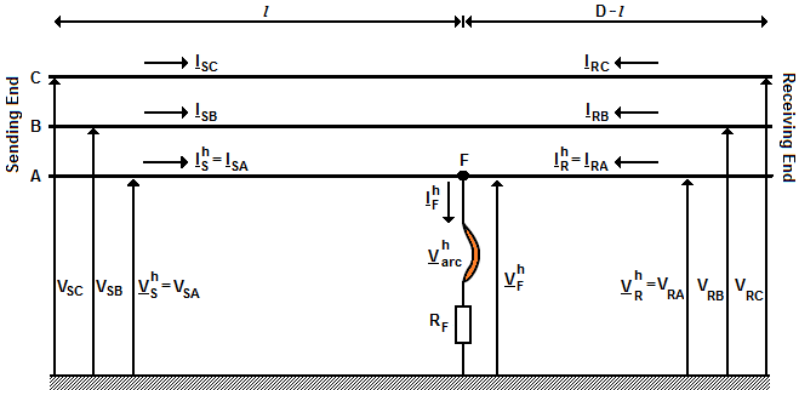
5.3 Proposed Algorithm

The proposed algorithm is developed for the case of a single phase-to-ground fault taking place on a three-phase overhead transmission line as shown in Figure 5.13. The algorithm is derived for short lines (0-100km) and long lines (100-300km). An arc

is formed across phase A of the line at a distance *l* from the sending end. Assuming the arc voltage has a rectangular wave shape [68], the characteristics of the arc are given by:

$$V_{arc}(t)=\sum_{h=1}^{\infty}\frac{4V_{arc(pk)}}{h\pi}\sin(h\omega t+h\varphi_1) \tag{5.6}$$

where *h* is the harmonic order; $V_{arc(pk)}$ is the peak arc voltage; ω is the fundamental radian frequency and φ_1 is the fundamental phase angle.



F = fault location, *l* = fault distance, *D* = line length, *S* = sending end, R = receiving end,
$\underline{V_S}^h$, $\underline{V_R}^h$ = hth harmonics of the voltages, $\underline{I_S}^h$, $\underline{I_R}^h$ = hth harmonics of the currents,
$\underline{V}^h_{arc}$ = hth harmonic of the arc voltage at the fault point, $\underline{V_F}^h$ = hth harmonic of the fault voltage,
$\underline{I_F}^h$ = hth harmonic of the fault current, R_F = fault resistance

Figure 5.13: Proposed fault model

The hth harmonic of the arc voltage amplitude is:

$$\underline{V}^h_{arc}=\frac{4}{\pi h}V_{arc}=k^hV_{arc} \tag{5.7}$$

where k^h is the harmonic coefficient.

The hth harmonic of the fault voltage is:

$$\underline{V}^h_F=\underline{V}^h_{arc}+R_F\underline{I}^h_F \tag{5.8}$$

where $\underline{I}^h_F$ is the hth harmonic of the fault arc current.

The fundamental arc voltage in phasor form is:

$$\underline{V}^1_{arc}=\underline{k}^1V_{arc}=k^1\angle\varphi^1V_{arc}=\frac{k^1V_{arc}\underline{I}^1_F}{\left|\underline{I}^1_F\right|}=R_{arc}\underline{I}^1_F \tag{5.9}$$

where R_{arc} is the fundamental harmonic arc resistance.

Combining equation (5.8) and (5.9) represents the general fault formula:

$$\underline{V}^1_F=(R_{arc}+R_F)\underline{I}^1_F=R_T\underline{I}^1_F \tag{5.10}$$

where R_T is the total fault resistance.

A block diagram showing each step of the algorithm derivation process is illustrated in Figure 5.14.

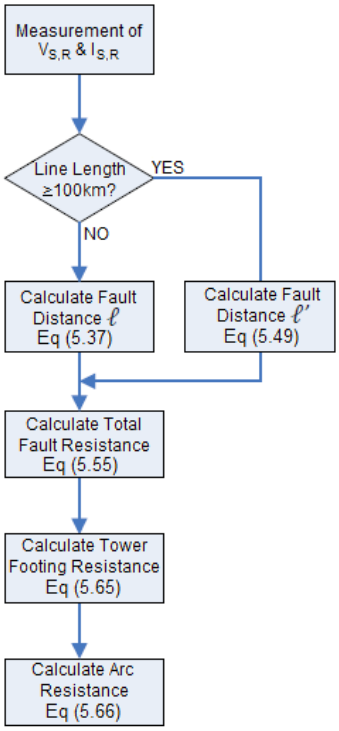
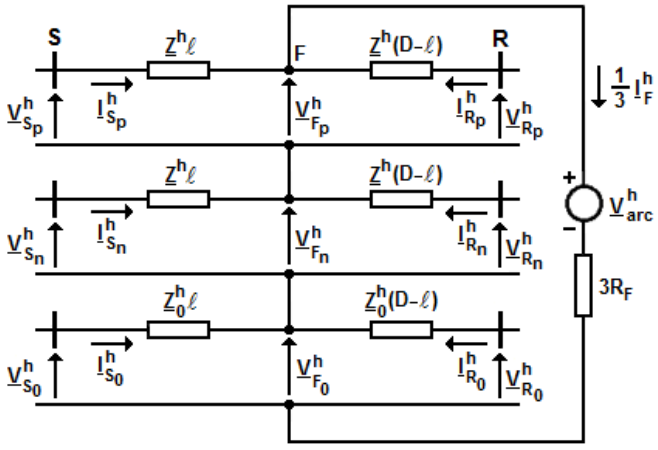


Figure 5.14: Algorithm block diagram

5.3.1 Calculation of the Fault Distance

Figure 5.15 illustrates an unsymmetrical three-phase circuit connecting the single-phase equivalents of the positive (p), negative (n) and zero (0) sequence circuits. The circuit neglects the use of shunt capacitances between 0-100km.



$\underline{V}_{Sp,n,0}^h$, $\underline{V}_{Rp,n,0}^h$ = h[th] harmonic of the positive, negative and zero-sequence voltages

$\underline{I}_{Sp,n,0}^h$, $\underline{I}_{Rp,n,0}^h$ = h[th] harmonic of the positive, negative and zero-sequence currents

$\underline{V}_{Fp,n,0}^h$ = h[th] harmonic of the positive, negative and zero-sequence components of the faulted phase voltage at the fault point

$\underline{Z}^h$ = h[th] harmonic of the positive or negative-sequence line impedance

$\underline{Z}_0^h$ = h[th] harmonic of the zero-sequence line impedance

Figure 5.15: Sequence line diagram (with neglected shunt capacitances)

The following derivations can be made from Figure 5.15:

$$\underline{V}_{S_p}^{h} = \underline{Z}^{h}\ell\underline{I}_{S_p}^{h} + \underline{V}_{F_p}^{h} \tag{5.11}$$

$$\underline{V}_{S_n}^{h} = \underline{Z}^{h}\ell\underline{I}_{S_n}^{h} + \underline{V}_{F_n}^{h} \tag{5.12}$$

$$\underline{V}_{S_0}^{h} = \underline{Z}_0^{h}\ell\underline{I}_{S_0}^{h} + \underline{V}_{F_0}^{h} \tag{5.13}$$

$$\underline{V}_{R_p}^{h} = \underline{Z}^{h}(D-\ell)\underline{I}_{R_p}^{h} + \underline{V}_{F_p}^{h} \tag{5.14}$$

$$\underline{V}_{R_n}^{h} = \underline{Z}^{h}(D-\ell)\underline{I}_{R_n}^{h} + \underline{V}_{F_n}^{h} \tag{5.15}$$

$$\underline{V}_{R_0}^{h} = \underline{Z}_0^{h}(D-\ell)\underline{I}_{R_0}^{h} + \underline{V}_{F_0}^{h} \tag{5.16}$$

Combining equation (5.11) to (5.13) and (5.14) to (5.16) produces the h^{th} harmonic phase voltage at the sending and receiving terminals:

$$\underline{V}_{S}^{h} = \underline{Z}^{h}\left(\underline{I}_{S}^{h} + \underline{k}_{Z}^{h}\underline{I}_{S_0}^{h}\right)\ell + \underline{V}_{F}^{h} \tag{5.17}$$

$$\underline{V}_{R}^{h} = \underline{Z}^{h}\left(\underline{I}_{R}^{h} + \underline{k}_{Z}^{h}\underline{I}_{R_0}^{h}\right)(D-\ell) + \underline{V}_{F}^{h} \tag{5.18}$$

where $\underline{k}_{Z}^{h} = (\underline{Z}_0^{h} - \underline{Z}^{h})/\underline{Z}^{h}$ is the zero sequence compensation factor.

Rewriting equation (5.17) and (5.18) for the fundamental harmonic gives:

$$\underline{V}_{S}^{1} = \underline{Z}^{1}\left(\underline{I}_{S}^{1} + \underline{k}_{Z}^{1}\underline{I}_{S_0}^{1}\right)\ell + \underline{V}_{F}^{1} \tag{5.19}$$

$$\underline{V}_{R}^{1} = \underline{Z}^{1}\left(\underline{I}_{R}^{1} + \underline{k}_{Z}^{1}\underline{I}_{R_0}^{1}\right)(D-\ell) + \underline{V}_{F}^{1} \tag{5.20}$$

Substituting equation (5.10) into (5.19) and (5.20) yields:

$$\underline{I}_{F}^{1}R_{T} + \underline{Z}^{1}\left(\underline{I}_{S}^{1} + \underline{k}_{Z}^{1}\underline{I}_{S_0}^{1}\right)\ell = \underline{V}_{S}^{1} \tag{5.21}$$

$$\underline{I}_{F}^{1}R_{T} - \underline{Z}^{1}\left(\underline{I}_{R}^{1} + \underline{k}_{Z}^{1}\underline{I}_{R_0}^{1}\right)\ell = \underline{V}_{R}^{1} - \underline{Z}^{1}\left(\underline{I}_{R}^{1} + \underline{k}_{Z}^{1}\underline{I}_{R_0}^{1}\right)D \tag{5.22}$$

where the two unknowns are the fault distance (ℓ) and the total fault resistance (R_T).

Rearranging (5.21) and (5.22) with the intent of eliminating R_T, the fault distance becomes:

$$\ell_{0\text{-}100\text{km}} = \frac{\underline{V}_{S}^{1} - \underline{V}_{R}^{1} + \underline{Z}^{1}\left(\underline{I}_{R}^{1} + \underline{k}_{Z}^{1}\underline{I}_{R_0}^{1}\right)D}{\underline{Z}^{1}\left[\underline{I}_{S}^{1} + \underline{I}_{R}^{1} + \underline{k}_{Z}^{1}\left(\underline{I}_{S_0}^{1} + \underline{I}_{R_0}^{1}\right)\right]} \tag{5.23}$$

Figure 5.16 illustrates an updated diagram of Figure 5.15, where the shunt capacitances are added. The circuit is used to derive the fault distance (ℓ') for line lengths between 100-300km.

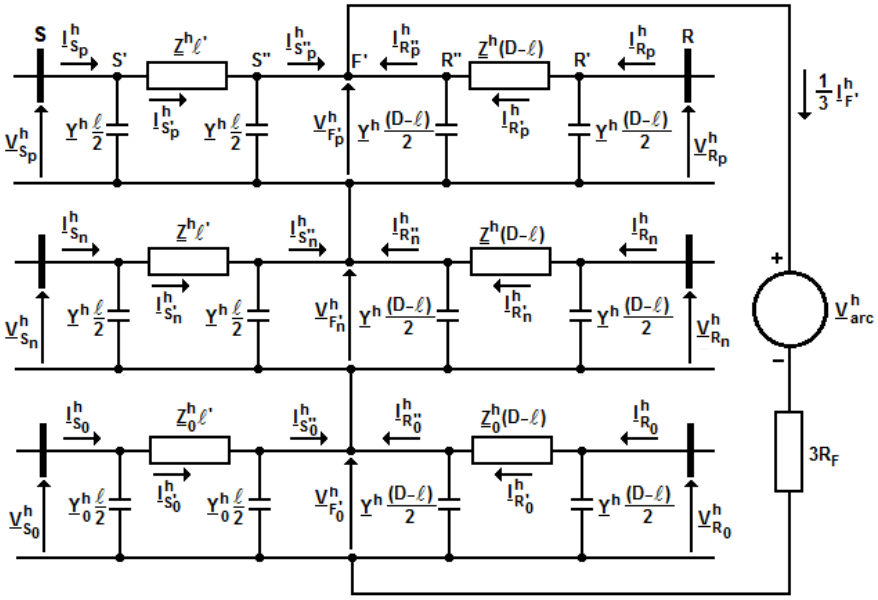


Figure 5.16: Sequence line diagram (with included shunt capacitances)

The currents at point S' are determined using equation (5.23):

$$\underline{I}^{h}_{S'_p} = \underline{I}^{h}_{S_p} - \underline{V}^{h}_{S_p}\,\underline{Y}^{h}\,\frac{\ell}{2} \tag{5.24}$$

$$\underline{I}^{h}_{S'_n} = \underline{I}^{h}_{S_n} - \underline{V}^{h}_{S_n}\,\underline{Y}^{h}\,\frac{\ell}{2} \tag{5.25}$$

$$\underline{I}^{h}_{S'_0} = \underline{I}^{h}_{S_0} - \underline{V}^{h}_{S_0}\,\underline{Y}^{h}_{0}\,\frac{\ell}{2} \tag{5.26}$$

where $\underline{I}^{h}_{S'_{p,n,0}}$ is the positive, negative and zero sequence currents flowing through the shunt admittances.

Adding these equations together provides:

$$\underline{I}^{h}_{S'} = \underline{I}^{h}_{S} - \left(\underline{V}^{h}_{S} + \underline{k}^{h}_{Y}\,\underline{V}^{h}_{S_0}\right)\underline{Y}^{h}_{Z}\,\frac{\ell}{2} \tag{5.27}$$

where $\underline{Y}^{h}_{Z} = (\underline{Y}^{h}_{0} - \underline{Y}^{h})/\underline{Y}^{h}$ is the zero sequence compensation factor of the voltages.

The voltages are derived as:

$$\underline{V}^{h}_{S_p} = \underline{Z}^{h}\,\ell'\,\underline{I}^{h}_{S'_p} + \underline{V}^{h}_{F'_p} \tag{5.28}$$

$$\underline{V}^{h}_{S_n} = \underline{Z}^{h}\,\ell'\,\underline{I}^{h}_{S'_n} + \underline{V}^{h}_{F'_n} \tag{5.29}$$

$$\underline{V}^{h}_{S_0} = \underline{Z}^{h}_{0}\,\ell'\,\underline{I}^{h}_{S'_0} + \underline{V}^{h}_{F'_0} \tag{5.30}$$

Combining equations (5.28), (5.29) and (5.30) provides the h^{th} harmonic phase voltage at the sending and receiving terminals:

$$\underline{V}_S^h = \underline{Z}^h\left(\underline{I}_{S'}^h + \underline{k}_Z^h \underline{I}_{S'_0}^h\right)\ell' + \underline{V}_{F'}^h \tag{5.31}$$

$$\underline{V}_R^h = \underline{Z}^h\left(\underline{I}_{R'}^h + \underline{k}_Z^h \underline{I}_{R'_0}^h\right)\left(D - \ell'\right) + \underline{V}_{F'}^h \tag{5.32}$$

Rewriting equations (5.31) and (5.32) for the fundamental harmonic produces:

$$\underline{V}_S^1 = \underline{Z}^1\left(\underline{I}_{S'}^1 + \underline{k}_Z^1 \underline{I}_{S'_0}^1\right)\ell' + \underline{V}_{F'}^1 \tag{5.33}$$

$$\underline{V}_R^1 = \underline{Z}^1\left(\underline{I}_{R'}^1 + \underline{k}_Z^1 \underline{I}_{R'_0}^1\right)\left(D - \ell'\right) + \underline{V}_{F'}^1 \tag{5.34}$$

The resultant is the fault distance formula:

$$\ell'_{100\text{-}300\text{km}} = \frac{\underline{V}_S^1 - \underline{V}_R^1 + \underline{Z}^1\left(\underline{I}_{R'}^1 + \underline{k}_Z^1 \underline{I}_{R'_0}^1\right)D}{\underline{Z}^1\left[\underline{I}_{S'}^1 + \underline{I}_{R'}^1 + \underline{k}_Z^1\left(\underline{I}_{S'_0}^1 + \underline{I}_{R'_0}^1\right)\right]} \tag{5.35}$$

Although equations (5.23) and (5.35) are alike, they are not the same. The difference lies in the calculation of I'_{S0} and I'_{S1} for equation (5.23) and $I'_{S'0}$ and $I'_{S'1}$ for equation (5.35). The fault distance (ℓ') can be used for both long lines and short lines, whereas the fault distance (ℓ) is used strictly for short lines only.

5.3.2 Calculation of the Total Fault Resistance

The total fault resistance is derived from equation (5.10) where $R_T = R_{arc} + R_F$. Rearranging equations (5.30) and (5.35) results in the zero sequence fault voltage:

$$\underline{V}_{F'_0}^1 = \underline{V}_{S_0}^1 - \underline{Z}_0^1 \ell' \underline{I}_{S'_0}^1 \tag{5.36}$$

The corrected zero sequence current is:

$$\underline{I}_{S''_0}^1 = \underline{I}_{S_0}^1 - \underline{V}_{S_0}^1 \underline{Y}_0^1 \frac{\ell'}{2} - \underline{V}_{F'_0}^1 \underline{Y}_0^1 \frac{\ell'}{2} \tag{5.37}$$

$$\underline{I}_{R''_0}^1 = \underline{I}_{R_0}^1 - \underline{V}_{R_0}^1 \underline{Y}_0^1 \frac{\ell'}{2} - \underline{V}_{F'_0}^1 \underline{Y}_0^1 \frac{\ell'}{2} \tag{5.38}$$

The single phase-to-ground fault current is:

$$\underline{I}_{F'}^1 = 3\left(\underline{I}_{S''_0}^1 + \underline{I}_{R'_0}^1\right) \tag{5.39}$$

Combining equations (5.33) and (5.35) results in the positive and negative sequence fault voltage:

$$\underline{V}^1_{F'} = \underline{V}^1_S - \underline{Z}^1\left(\underline{I}^1_{S'} + \underline{k}^1_z \underline{I}^1_{S'_0}\right)\ell' \tag{5.40}$$

The total fault resistance is:

$$R_T = \frac{\underline{V}^1_{F'}}{\underline{I}^1_{F'}} = \frac{\underline{V}^1_S - \underline{Z}^1\left(\underline{I}^1_{S'} + \underline{k}^1_Z \underline{I}^1_{S'_0}\right)\ell'}{3\left(\underline{I}^1_{S'_0} + \underline{I}^1_{R'_0}\right)} \tag{5.41}$$

5.3.3 Calculation of the Tower Footing Resistance

The tower footing resistance is calculated by using equation (5.31) for the third harmonic:

$$\underline{V}^3_{F'} = \underline{V}^3_S - \underline{Z}^3\left(\underline{I}^3_{S'} + \underline{k}^3_z \underline{I}^3_{S'_0}\right)\ell' \tag{5.42}$$

The current at point S' is determined through equation (5.23):

$$\underline{I}^3_{S'} = \underline{I}^3_S - \left(\underline{V}^3_S + \underline{k}^3_Y \underline{V}^3_{S_0}\right)\underline{Y}^3\frac{\ell'}{2} \tag{5.43}$$

$$\underline{I}^3_{S'_0} = \underline{I}^3_{S_0} - \underline{V}^3_{S_0}\underline{Y}^3_0\frac{\ell'}{2} \tag{5.44}$$

The zero sequence current values at point S" are:

$$\underline{I}^3_{S''_0} = \underline{I}^3_{S_0} - \underline{V}^3_{S_0}\underline{Y}^3_0\frac{\ell'}{2} - \underline{V}^3_{F'_0}\underline{Y}^3_0\frac{\ell'}{2} \tag{5.45}$$

$$\underline{I}^3_{R''_0} = \underline{I}^3_{R_0} - \underline{V}^3_{R_0}\underline{Y}^3_0\frac{\ell'}{2} - \underline{V}^3_{F'_0}\underline{Y}^3_0\frac{\ell'}{2} \tag{5.46}$$

This produces the fault current and fault voltage:

$$\underline{I}^3_{F'} = 3\left(\underline{I}^3_{S''_0} + \underline{I}^3_{R''_0}\right) \tag{5.47}$$

$$\underline{V}^3_{F'} = \underline{k}^3 V_{arc} + R_F \underline{I}^3_{F'} \tag{5.48}$$

Substituting equations (5.42) into (5.47) and (5.48) provides:

$$V_{arc} = \frac{\underline{V}^3_S}{\underline{k}^3} - \frac{\underline{Z}^3\left(\underline{I}^3_{S'} + \underline{k}^3_Z \underline{I}^3_{S'_0}\right)}{\underline{k}^3}\ell - \frac{\left(\underline{I}^3_{S''_0} + \underline{I}^3_{R''_0}\right)}{\underline{k}^3}R_F$$

$$\Rightarrow \mathrm{Im}\frac{\underline{V}^3_S}{\underline{k}^3} - \mathrm{Im}\frac{\underline{Z}^3\left(\underline{I}^3_{S'} + \underline{k}^3_Z \underline{I}^3_{S'_0}\right)}{\underline{k}^3}\ell - \mathrm{Im}\frac{\left(\underline{I}^3_{S''_0} + \underline{I}^3_{R''_0}\right)}{\underline{k}^3}R_F = 0 \tag{5.49}$$

Noting that electrical arcs are purely resistive elements with no reactance, it can be alleged that the arc voltage has no imaginary component ($\mathrm{Im}\{V_{arc}\}=0$), resulting in a tower footing resistance of:

$$R_F = \frac{\mathrm{Im}\dfrac{\underline{V}_S^3}{\underline{k}^3} - \mathrm{Im}\dfrac{\underline{Z}^3\left(\underline{I}_{S'}^3 + \underline{k}_Z^3\underline{I}_{S'_0}^3\right)}{\underline{k}^3}\ell}{\mathrm{Im}\dfrac{\underline{I}_{S''_0}^3 + \underline{I}_{R''_0}^3}{\underline{k}^3}} \tag{5.50}$$

Combining the absolute fault distance of equation (5.35) into (5.50) yields:

$$R_F = \frac{\mathrm{Im}\dfrac{\underline{V}_S^3}{\underline{k}^3} - \mathrm{Im}\dfrac{\underline{Z}^3\left(\underline{I}_{S'}^3 + \underline{k}_Z^3\underline{I}_{S'_0}^3\right)}{\underline{k}^3}\bullet\dfrac{\underline{V}_{S'}^1 + \underline{V}_R^1 + \underline{Z}^1\left(\underline{I}_{R'}^1 + \underline{k}_Z^1\underline{I}_{R'_0}^1\right)D}{\underline{Z}^1\left[\underline{I}_{S'}^1 + \underline{I}_{R'}^1 + \underline{k}_Z^1\left(\underline{I}_{S'_0}^1 + \underline{I}_{R'_0}^1\right)\right]}}{\mathrm{Im}\dfrac{\underline{I}_{S''_0}^3 + \underline{I}_{R''_0}^3}{\underline{k}^3}} \tag{5.51}$$

5.3.4 Calculation of the Arc Resistance

The unknown arc resistance is calculated using Equation (5.41) and (5.51). If the fault is a permanent metallic fault with no arc, then $R_T = R_F$ and $R_{arc} = 0$.

$$R_{arc} = R_T - R_F \tag{5.52}$$

5.4 Conclusion

This chapter focused on the manual derivation of an innovative fault locator algorithm aimed at determining the fault distance, arc resistance, total fault resistance and tower footing resistance. The algorithm is viable for single phase-to-ground faults in overhead transmission lines. The algorithm is proposed for distances between 0-300km using Discrete Fourier Transformation. The algorithm relies on voltage and current data obtained from IEDs at both ends of the transmission line by using digital fault recording capabilities such as file transfer based on the IEC61850 protocol. All simulation and practical tests are discussed in the following chapter.

No approximations are required during the development of the fault locator algorithm seeing as the algorithm is developed using raw data signals. This means all signals such as voltages, currents and harmonics are taken directly from the IEDs and ATL in real-time as it provides a more realistic approach, as opposed to a theoretical representation. No extra transducers are necessary as the ATL operates at 400V.

Chapter 6 – Testing & Results

6.1 Introduction

The purpose of this chapter is to validate the algorithm presented in Chapter 5 as being true and accurate by performing automated tests using a 300km Artificial Transmission Line. The CMC356 test set is configured to the SEL-311L to generate fault recordings. Tests are carried out using OMICRON's Test Universe software at different line segments, where mutual coupling is considered. The chapter presents various fault waveforms, R-X plots, relay reaches and harmonics.

6.2 Experimental Setup

The experimental setup required to test the algorithm demands the use of several equipment. The most important is the Artificial Transmission Line which is divided into four segments, each 75km apart, totalling 300km. The ATL is equipped with three current transformers rated at 25/5A, four electric cooling fans, a thermostat for temperature control, a single contactor for automated features, and a s eries of inductors, capacitors and resistors. The resistors and capacitors across all four segments are set to R=2.5Ω and C=0.2x10^{-6}F. The inductors conversely have distinct values of L=44x10^{-6}H for segment 1 and L=35x10^{-6}H for segments 2-4. Figure 6.1 illustrates the front view panel of the ATL.

Figure 6.1: Artificial transmission line (front view)

Figure 6.2 shows the internal wiring connections.

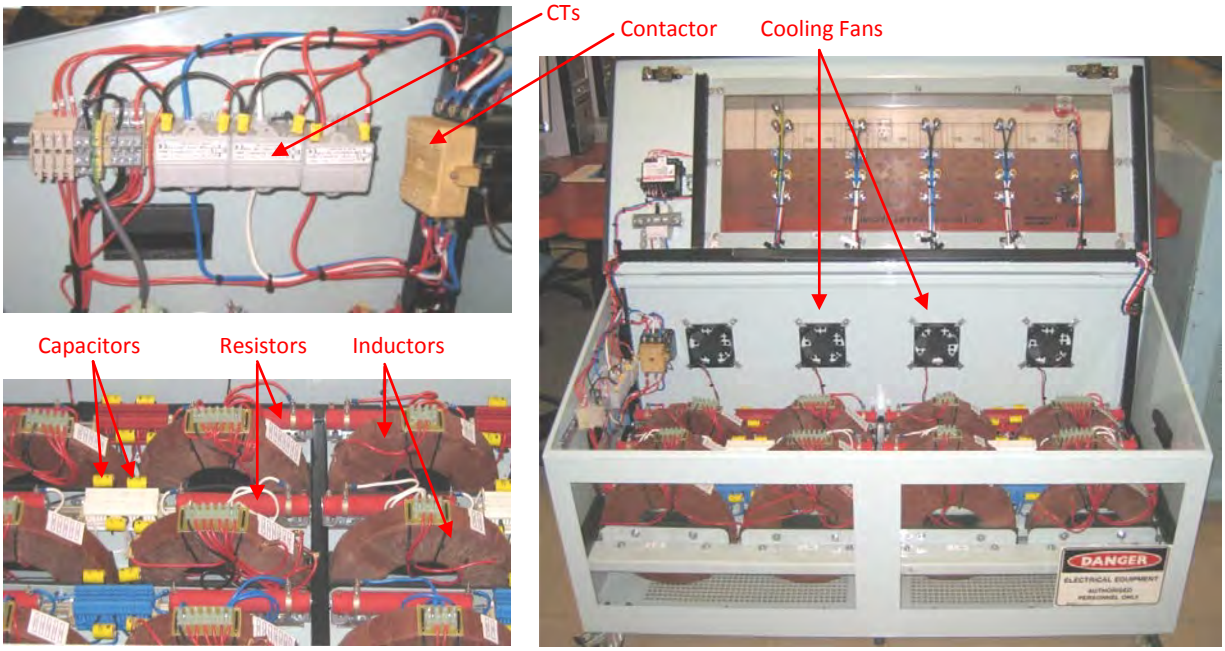


Figure 6.2: Artificial transmission line (internal view)

Figure 6.3 depicts the circuit diagram of the ATL.

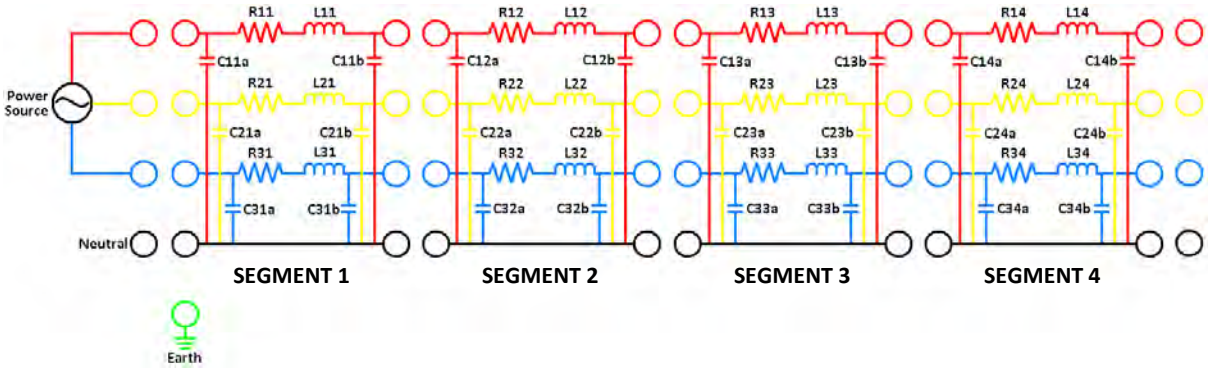


Figure 6.3: ATL circuit diagram

The ATL when originally designed did not consider the effect of mutual coupling. To ensure the algorithm is as accurate as possible, this factor is taken into consideration. The objective is to build a prototype which can be connected together with the ATL comprising of several chokes and power resistors (Figure 6.5). Mutual coupling is dependent on the k-factor. This factor is often referred to as the ground impedance matching factor, residual compensation factor and ear th factor. The k-factor is considered constant for a particular line and is generally independent of the length. The k-factor expresses the relationship between the line impedance (Z_L) and earth return path (Z_E) by separating the circuit of Figure 6.3 into two loops, a phase-to-phase and phase-to-ground as shown in Figure 6.4.

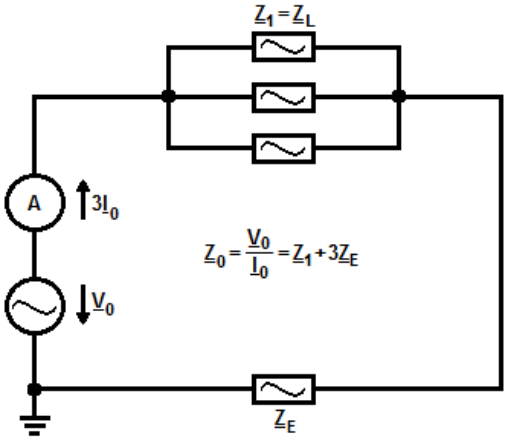


Figure 6.4: ATL equivalent diagram

The line impedance (Z_L) is assigned to the positive sequence impedance (Z_1):

$$\underline{Z}_L = \underline{Z}_1 \tag{6.1}$$

The earth return impedance (Z_E) is:

$$\underline{Z}_E = \frac{\underline{Z}_0 - \underline{Z}_1}{3} \tag{6.2}$$

The complex impedances of Z_E and Z_L in their real and imaginary forms are:

$$\frac{R_E}{R_L} \quad \text{and} \quad \frac{X_E}{X_L} \tag{6.3}$$

The line resistance and line inductance for each segment is derived as:

$$Z_{1(0\text{-}75\text{km})} = R_1 + jX_{L1} \;\square\; 28.873\cos(69.64^\circ) + j28.873\sin(69.64^\circ) \tag{6.4}$$

$$\square\; 10.0454 + j27.0692$$

$$80\%\text{ of } R_1 \text{ and } X_{L1} \text{ is } 8.03632 + j21.6554$$

$$\square\; R = 8.03632\Omega$$

$$X_{L1} = 2\pi fL \;\square\; 21.6554 = 2\pi(50) \times L$$

$$\square\; L = \frac{21.6554}{2\pi \times 50}$$

$$\square\; L = 68.9313\text{mH}$$

$$Z_{2(75\text{-}150\text{km})} = R_2 + jX_{L2} \;\square\; 45.812\cos(65.64^\circ) + j45.812\sin(65.64^\circ) \tag{6.5}$$

$$\square\; 18.896 + j41.7334$$

$$80\%\text{ of } R_2 \text{ and } X_{L2} \text{ is } 15.1168 + j33.3867$$

$$\square\; R = 15.1168\Omega$$

$$X_{L2} = 2\pi fL \;\square\; 33.3867 = 2\pi(50) \times L$$

$$\square\; L = \frac{33.3867}{2\pi \times 50}$$

$$\square\; L = 106.273\text{mH}$$

$$Z_{3(150\text{-}225\text{km})} = R_3 + jX_{L3} \;\square\; 75.047\cos(65.10^\circ) + j75.047\sin(65.10^\circ) \qquad (6.6)$$

$$\square\; 31.5975 + j68.0709$$

$$80\%\text{ of } R_3 \text{ and } X_{L3} \text{ is } 25.278 + j54.4567$$

$$\square\; R = 25.278\Omega$$

$$X_{L2} = 2\pi fL \;\square\; 54.4567 = 2\pi(50) \times L$$

$$\square\; L = \frac{54.4567}{2\pi \times 50}$$

$$\square\; L = 173.341\text{mH}$$

$$Z_{4(225\text{-}300\text{km})} = R_4 + jX_{L4} \;\square\; 97.344\cos(65.09^\circ) + j97.344\sin(65.09^\circ) \qquad (6.7)$$

$$\square\; 41.0007 + j88.2881$$

$$80\%\text{ of } R_4 \text{ and } X_{L4} \text{ is } 32.8006 + j70.6305$$

$$\square\; R = 32.8006\Omega$$

$$X_{L4} = 2\pi fL \;\square\; 70.6305 = 2\pi(50) \times L$$

$$\square\; L = \frac{70.6305}{2\pi \times 50}$$

$$\square\; L = 224.824\text{mH}$$

Following the calculation of each R and L value, components were purchased and soldered into the metal enclosure shown in Figure 6.5. The chokes all have a maximum current of I_{max}=4A.

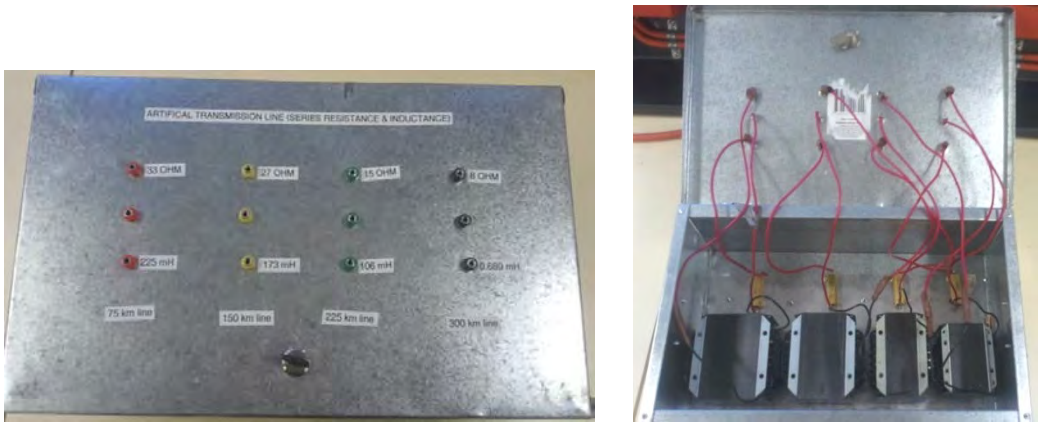


Figure 6.5: Power resistor and choke connections

The ATL is run using a main switchboard that transmits power to a transformer bank. The main switchboard is connected as shown in Figure 6.6 using coloured leads and a control cable.

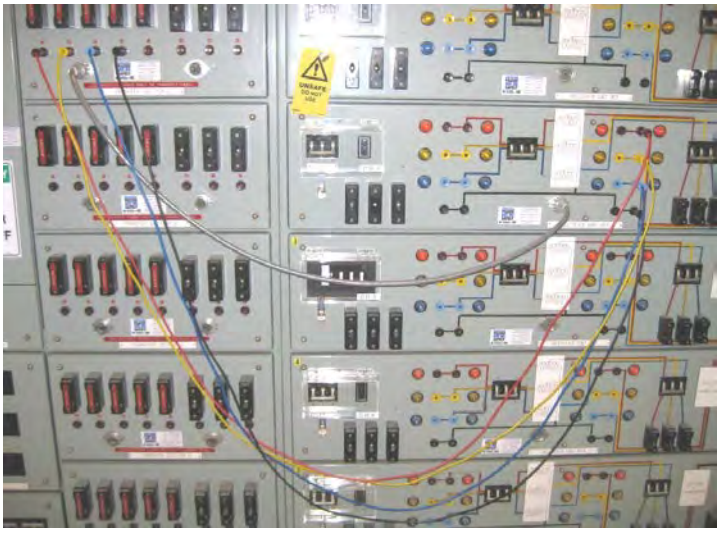


Figure 6.6: Main switchboard connections

The input side of the transformer bank is connected to individual CTs. The red, yellow and blue wires symbolise the three-phase channels, the black wire represents the neutral channel and the green wire signifies the earth channel. Tap one of each CT is connected to neutral; tap two is connected to the SEL-311L; tap three is connected to the power source terminals of the ATL; and tap four is connected to the transformer bank inputs (Figure 6.7). The output side of the transformer bank is connected to transfer terminals 1,2,3,4. These terminals distribute power back into the main switchboard.

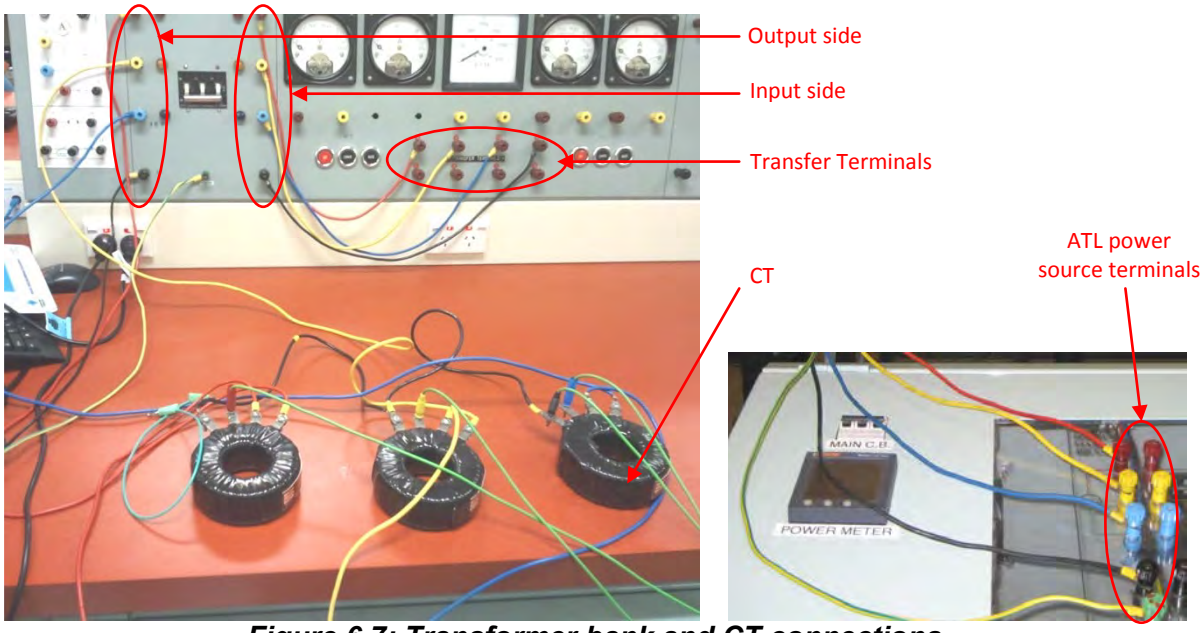


Figure 6.7: Transformer bank and CT connections

Figure 6.8 illustrates the complete experimental setup required to test the algorithm. The analog inputs of the CMC356 test set are connected to the sending end of the ATL. To generate a single phase-to-ground fault, a connection between phase A and ground needs to be made. Once automated tests have been carried out, leads can be repositioned to other segments of the line in order to record fault locations at different distances. The CMC356 test set is used to communicate and accurately transfer data between the sending and receiving ends.

Figure 6.8: Complete experimental setup

The OMICRON CMC356 test set co-ordinates data between the relays and the two ends of the line using four simple steps including (refer to Figure 6.9):

1. Connecting the CMC to the parallel port of the PC for data exchange.
2. Connecting the analog outputs of the CMC to the transducer inputs of the test object in order to read currents and voltages.
3. Connecting the binary outputs or transistor outputs of the CMC to the binary inputs of the test object to read the binary signals of the test object.
4. Connecting the binary inputs of the CMC to the binary outputs of the test object in order to load the output data of the test object.

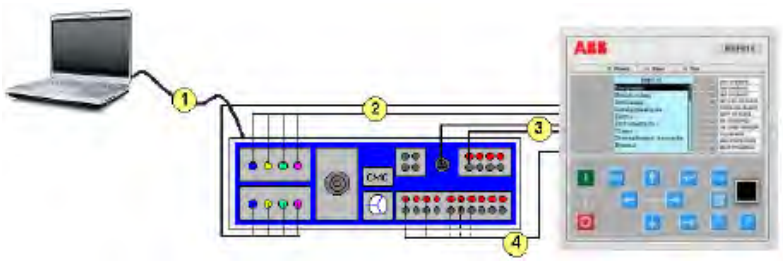


Figure 6.9: Co-ordination between the CMC356 and relays

The CMC356 can configure GOOSE messages (Figure 6.10):

1. Using an SCL file from the engineering process or system configurator.
2. Using an SCL file created from the IEDs self description.
3. Online GOOSE sniffing.
4. Manual configuration of the subscription.

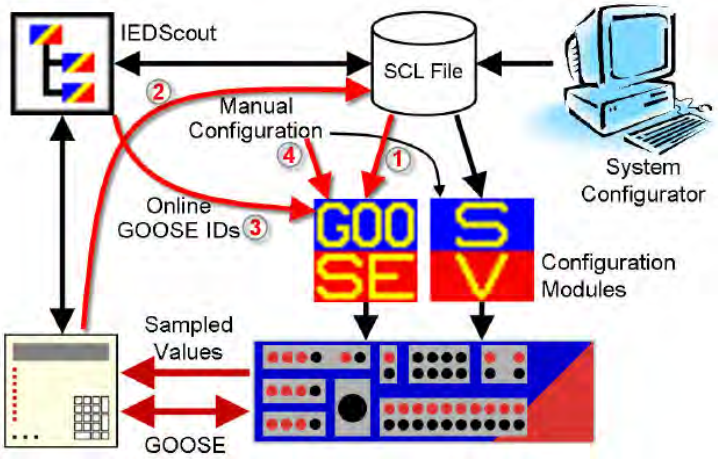


Figure 6.10: Setting up a GOOSE configuration using the CMC356

If using the SCL file through the system configurator, it must be obtainable. If it is not available, an SCL file needs to be imported using OMICRON's GOOSE Configuration module by selecting *File → Import Configuration*. The SCL file is parsed until all contained GOOSE definitions are offered in the dialog. The GOOSE messages can be individually selected for subscription, simulation, or both. Figure 6.11 illustrates the SCL file import.

Figure 6.11: SCL file importing

After the SCL file has been imported the GOOSE messages have to be mapped to binary inputs. Select the binary inputs to be mapped and move the data item from the received GOOSE message window by dragging & dropping it into the inputs window. Repeat this until all mappings have been established as illustrated in Figure 6.12.

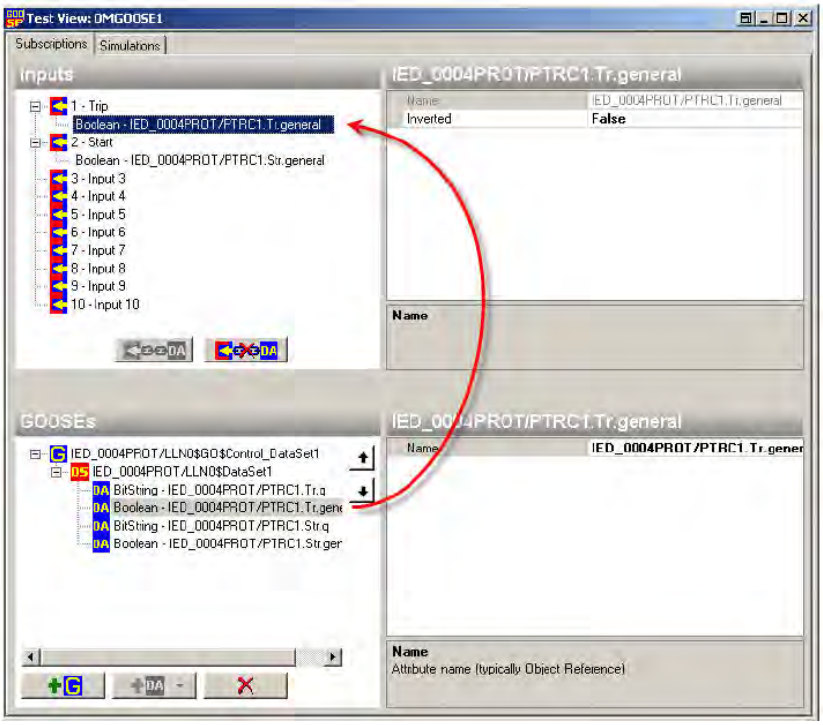


Figure 6.12: Mapping GOOSE to binary inputs using the CMC356

If no SCL file is available, a SCL file needs to be created using the IEDs self description. When creating a SCL file from the IED, OMICRON's *IEDScout* must be applied. The IED must initially be defined.

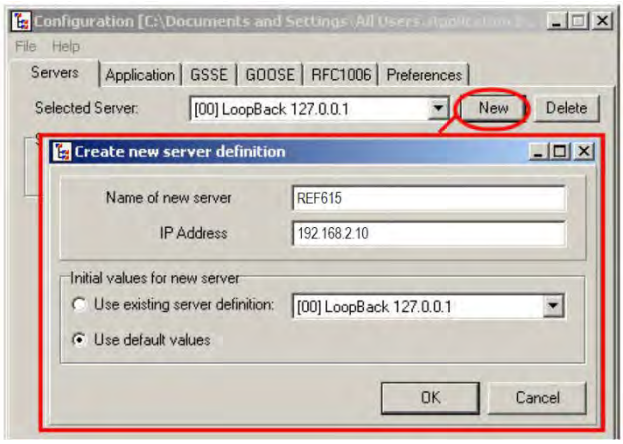


Figure 6.13: Defining a new sever

The next step is to discover the IED by selecting the '*Discover*' function in the main window of *IEDScout* and connecting it to the server.

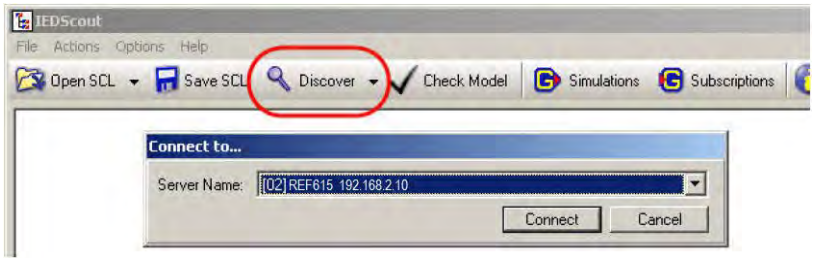


Figure 6.14: Discovering the sever

The software should read out the self description of the IED. This data can be saved in SCL format by selecting *File → Save SCL*. The SCL file obtained this way can be imported within the system configurator.

Figure 6.15: Saving an SCL file

6.3 Results

The algorithm is tested using OMICRON's Test Universe software at a voltage of 400kV. All parameters are entered using the TransPlay application. This section will focus only on results obtained for the fault distance, arc resistance, total fault resistance and tower footing resistance. Appendix D provides detailed analysis of simulated R-X plots, relay reaches and harmonics.

6.2.1 Short Line Tests (0-100km)

Figures 6.16 and 6.17 illustrates the line voltages and currents at both the sending and receiving terminals of the ATL for a single phase-to-ground arcing fault with a sample frequency of f_s=3.2kHz (64 samples per 20ms cycle). V_{SA}, V_{SB}, V_{SC} and I_{SA}, I_{SB}, I_{SC} are the three phase voltage and current signals at the sending end. V_{RA}, V_{RB}, V_{RC} and I_{RA}, I_{RB}, I_{RC} are the three phase voltage and current signals at the receiving end. Assuming the fault is at 10km, the fault current at the sending end can be seen to be slightly larger than the fault current at the receiving end. This is due to the fault being picked up closer to the sending end.

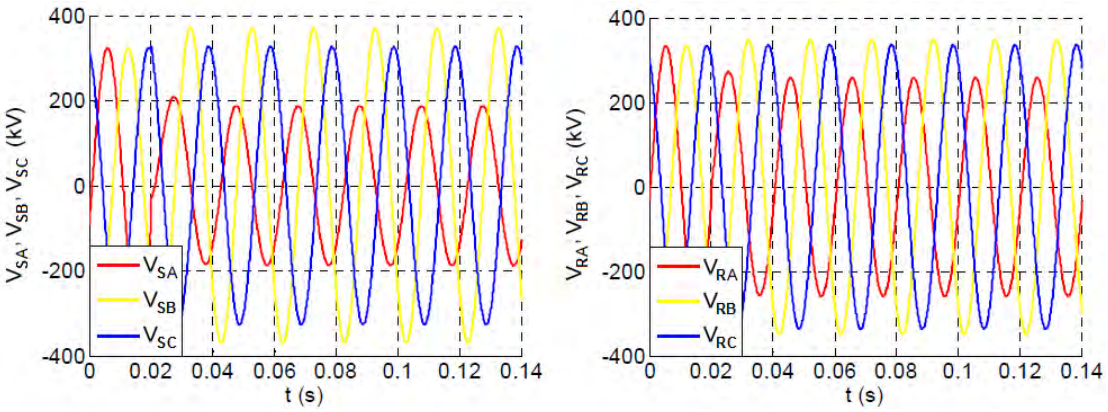


Figure 6.16: Line voltages at the sending and receiving terminals

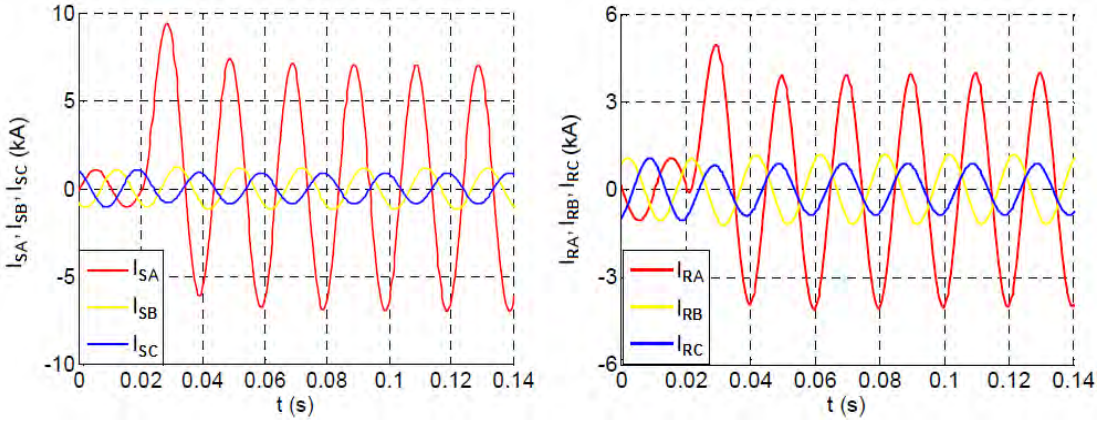


Figure 6.17: Line currents at the sending and receiving terminals

The arc voltage is assumed to have a distorted rectangular waveshape with an amplitude of V_{arc}=4kV as shown in Figure 6.18. The value of 4kV is obtained under the assumption that the arc length or distance between arc electrodes is 3.25m and the arc voltage gradient is 12.5V/cm.

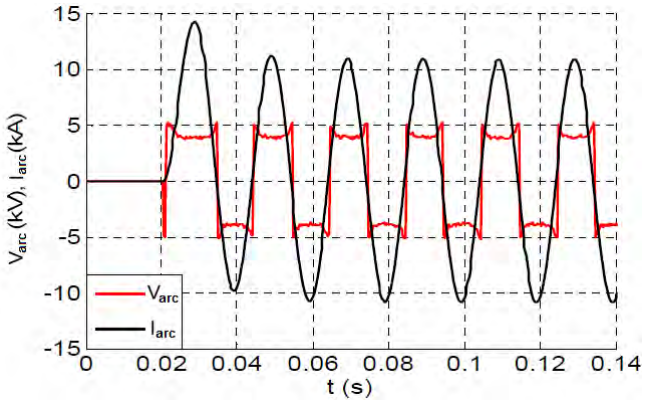


Figure 6.18: Fault arc voltage and current

The arc resistance (R_{arc}) is determined as the ratio of the fundamental arc voltage and fundamental arc current harmonic amplitudes:

$$R_{arc} = \frac{V_{arc}^{1}}{I_{arc}^{1}} \tag{6.8}$$

Figure 6.19 illustrates the arc resistance for four different cases in which the tower footing resistance is modified from case to case. R_F is set to 10, 20, 50 and 80Ω. In practice, such high R_F values are caused by extreme weather conditions where heavy tree branches fall on overhead transmission lines. The diagram on the left shows the theoretical results derived for R_{arc}, whereas the diagram on the right represents the practical results obtained using the ATL. The theoretical results are calculated using equation (5.66) resulting in 0.48, 0.58, 1 and 1.57Ω. In both case, the arc voltage is the same, but the arc current fluctuates leading to different arc resistances.

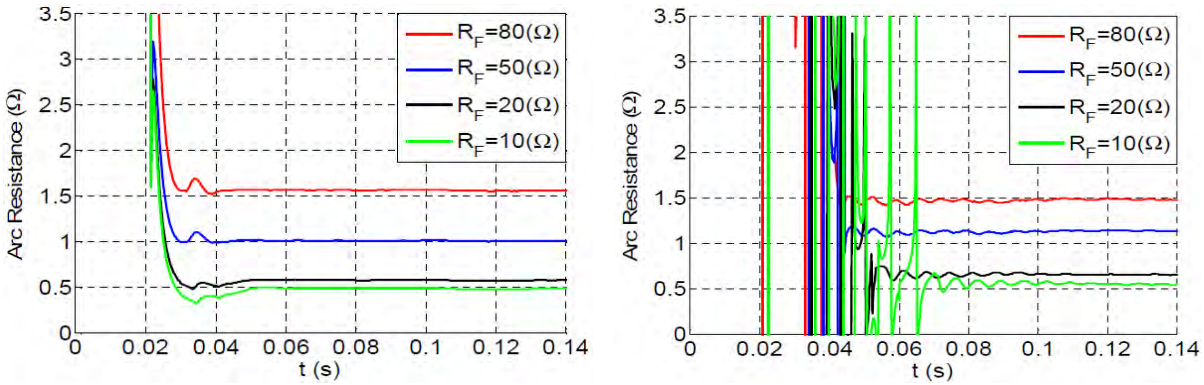


Figure 6.19: Theoretical and practical arc resistance simulations (R_{arc})

The results achieved in Figure 6.19 suggest good accuracy. Although there is a slight discrepancy between the simulations, the arc model used to derive the proposed algorithm is thought to be purely rectangular, whereas the arc simulated practically on the ATL is in effect a distorted rectangular wave shape as shown in Figure 6.18.

Figure 6.20 demonstrates the fault distances recorded at 10, 20, 50 and 80km. The tower footing resistance is set to R_F=8Ω.

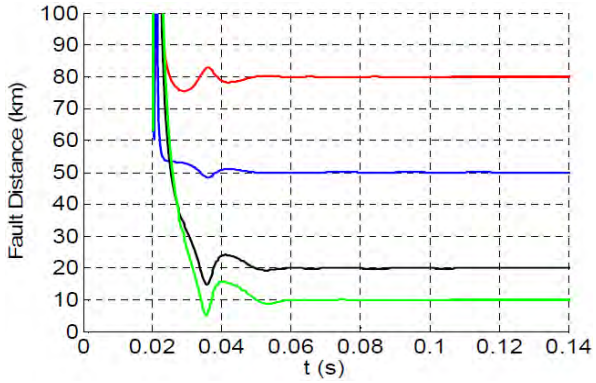


Figure 6.20: Fault distance (l = 10, 20, 50 and 80km)

Figure 6.21 depicts the total fault resistance with varying tower footing resistances. The total fault resistance is the sum of the fault resistance and the arc resistance.

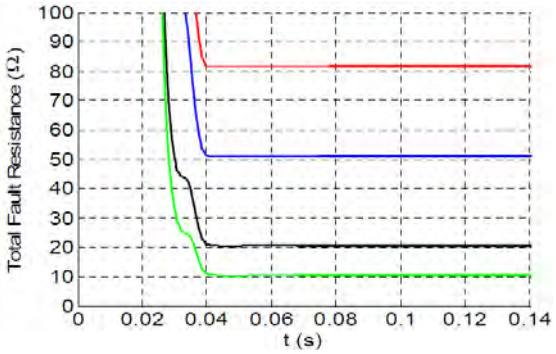


Figure 6.21: Total fault resistance (R_T)

Figure 6.22 illustrates the tower footing resistance.

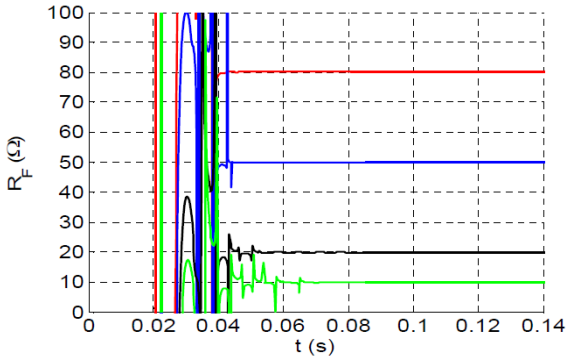


Figure 6.22: Tower footing resistance (R_F)

In all cases, the algorithm accurately determined the fault distance, arc resistance, total fault resistance and tower footing resistance. Table 6.1 summarises the findings.

Even though the majority of faults on overhead transmission lines are transient arcing faults, some faults are permanent metallic faults that do not produce an arc. If the proposed algorithm is to be used for other applications apart from fault location, it is important that it is able to distinguish between transient and permanent faults. A single phase-to-ground permanent metallic non-arcing fault with the fault resistance set at R_F=20Ω is simulated at 10km via the sending end. Figure 6.23 represents the algorithm output where all unknown parameters are determined. The algorithm suitably establishes that the arc resistance is R_{arc}=0Ω.

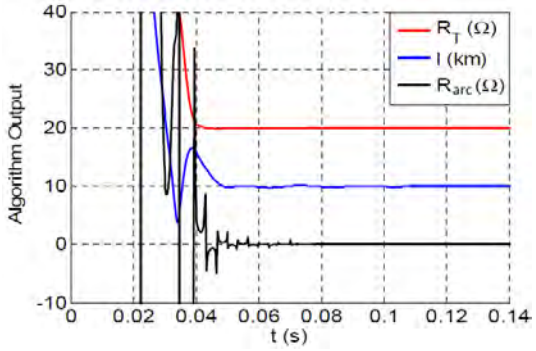


Figure 6.23: Algorithm output for a non-arcing fault (l=10km, R_F=20Ω, R_{arc}=0)

6.2.2 Long Line Tests (100-300km)

To assess the performance of the algorithm on long lines where shunt capacitances are included, the voltage and current data sampled at each end of the line is injected into the ATL using the CMC356 test set.

Comparing the algorithm outputs of the second and third columns of Table 6.1, the fault distance (ℓ') derived using Equation (5.49) is seen to be more accurate than

the fault distance (ℓ) derived using Equation (5.37). The inaccuracies in the calculation of ℓ in the first stage are caused by the shunt capacitance of the line and the inaccuracies for ℓ' in the second stage is due to ℓ being inexact, therefore causing minor inaccuracies in the shunt admittance.

Table 6.1: Algorithm outputs for both short and long line (D=300km)

Actual Fault Distance (km)	Algorithm Outputs				
	ℓ (km)	ℓ' (km)	R_F (Ω)	R_{arc} (Ω)	R_T (Ω)
10	8.757	10.19	7.92	0.535	8.46
20	18.08	20.18	7.93	0.550	8.48
50	47.14	50.15	7.93	0.547	8.48
100	98.62	100.0	7.94	0.491	8.43
150	150.6	149.7	7.92	0.547	8.48
200	203.1	199.3	7.93	0.547	8.48
250	255.8	248.9	7.93	0.491	8.43
280	285.6	278.9	7.95	0.430	8.38

In the first stage, tests proved that the algorithm underestimated the fault distance when the faults were nearer to the sending end o f the line (ℓ <150km) and overestimated the fault distance when the faults were closer to the receiving end (ℓ ≥150km). In the second stage, the algorithm overestimated the fault distance when the faults were closer to the sending end (ℓ <150km) and underestimated the fault distance when the faults were closer to the receiving end (ℓ ≥150km). This could arise from a number of reasons, mainly component errors in the ATL. To improve the accuracy even further a third stage can be derived and tested. However, given the almost precise accuracy of the results from the second stage, the necessity of a third stage is questionable.

6.4 Conclusion

This chapter validated that the proposed algorithm is viable for the application of an single phase-to-ground arcing fault by testing it on a 300km Artificial Transmission Line. In each case, the algorithm was slightly inaccurate in its calculation of R_F, although the error in the calculation was reduced as the fault distance was increased. The calculation of the total fault resistance remained constant, only dipping somewhat for the final case for a fault at 280km. The values of R_{arc} remained reasonably constant apart from in the last two cases where a combination of an increased value of R_F and decreased value of R_T led to a reduction in the value of R_{arc}. The fault arc waveforms have an accuracy error of 0.02-0.05%.

Chapter 7 – Conclusion

7.1 Introduction

The IEC61850 standard is the first and only standard to consider all communication needs within Substation Automation Systems. Many transmission companies have adopted the standard in newly built Greenfield substations, while distribution companies have been more reluctant to embrace the protocol due to legacy issues associated with older Brownfield substations. The IEC61850 defines strict interoperability guidelines between functions and devices independent of the product manufacturer to provide control, monitoring and protection advantages. The IEC61850 does not restrict the use of any other protocol (i.e. MODBUS or DNP3) given that Ethernet switches support both fibre and copper interconnections. The IEC61850 replaces hardwired links between IEDs by using GOOSE messages for data communication over the network. Such advances have put pressure on utilities to develop faster and more accurate fault location algorithms for the application of overhead transmission lines. This chapter presents the final remarks and future work of the research.

7.2 Major Benefits

Three major accomplishments have been satisfied throughout the research including the construction of a portable IEC61850 testing unit; GOOSE interoperability between three different vendors (ABB, Areva and SEL); and the derivation and testing of an innovative fault locator algorithm for single phase-to-ground faults on overhead transmission lines.

A detailed description of all hardware inventory and wiring schematics used to assemble the portable IEC61850 testing unit was elaborated in Chapter 3. Traditional substations deployed copper wiring using trip contacts on relays to isolate circuit breaker coils. With IEC61850, copper wiring is reduced dramatically to only a few serial links and GOOSE messages are sent across fibre optic cables to trip contacts. This upgrade offers several benefits including reduced wiring costs, higher data performance and automated link status.

Chapter 4 exposed the individual and overall system configurations of GOOSE messages using vendor specific software tools. A virtual wiring map was considered prior to system setup of the IEDs to execute a breaker failure scheme. GOOSE messages were subscribed and published in the form of ICD/CID files. These files were merged into a single SCD file by sniffing the network. The portable IEC61850 testing unit has the benefit of enabling dummy circuit breakers to be tripped, along with information exchange of multiple IEDs. Users can assign object names and data attributes using logical nodes.

Chapter 5 and 6 demonstrated the manual derivation, simulation and practical testing of an innovative single phase-to-ground fault locator algorithm. The proposed algorithm determined not only the fault distance, but also the arc resistance, total fault resistance and tower footing resistance of short and long lines between 0-300km. This is an advantage over conventional numerical algorithms that can only locate the fault distance. The algorithm was derived using a simple square wave arc model employing voltage and current data at each end of the Artificial Transmission Line. The accuracy of the algorithm was assessed using fault simulations carried out by OMICRON's Test Universe software. The benefit of carrying out both practical and simulated tests is that practical tests produce exact results, whereas simulated tests produce rough estimates. The algorithm was proven to be feasible.

7.3 Future Work

Although significant achievements have been made throughout the thesis, some research aspects can be further developed for future work. Cyber security is one of these recommendations where SCADA systems and IT networks have been under

constant attack by malware and cyber criminals. In May 2013, a US power utility was reportedly targeted with over 10,000 cyber attacks [69]. Due to the enormity of these threats, it is imperative that power utilities invest additional time and resources by frequently upgrading technologies that support the prevention of cyber security risks.

Wireless systems such as routers and Ethernet switches are obvious targets for cyber criminals. A large number of electricity companies make use of wireless systems as they believe features such as firewalls and proxy servers will protect devices from prohibited users. However, many utilities fail to recognise that without the installation of extra security applications, the most amateur of hackers can access a company's personal data in a number of minutes via the use of a laptop computer and downloadable software tools from the internet.

This reality for the most part is based on the view that SCADA systems were not originally designed to take onboard the concept of security. Engineers believed that such systems will not be used with any other device on the network and that only authorised personnel will have access to system data. This proved not to be the case. At present, SCADA systems transmit data by means of modems. These modems behave as an additional pathway for hackers to access confidential data given that each modem dials out a specific dialog, which if harnessed correctly can scrutinise system logins. Hackers can shut down entire electrical grids and self-destruct generators. Dedicated encryption topologies and simulated cyber attacks using the portable IEC61850 testing unit is a consideration to be explored.

Another proposal is the direct communication of process bus switchgear through sampled data values compliant to IEC61850-9-2. Much of the progress till date on IEC61850 has been based on station and bay level communications between HMI computers, Ethernet switches and IEDs. The station and bay levels are only a part of the standard, with IEC61850-9-2 being largely unexplored. IEC61850-9-2 brings Non-Conventional Instrument Transformer Technology (NCIT) into the process bus, breaking the constraints of conventional CTs and VTs. The main aim for future work is to improve synchronisation between digital sources and switchgear that transmit sampled data over the network using IEEE 802.

Last but not least, is the development of new approaches for fault detection, isolation and restoration of overhead and underground transmission lines. Although the thesis focused strictly on unsymmetrical single phase-to-ground faults, the study can further be broadened to incorporate different types of fault scenarios which can be tested using the 300km Artificial Transmission Line. The research should concentrate towards understanding the elongation effects of free-burning arcs, while taking into account harmonics.

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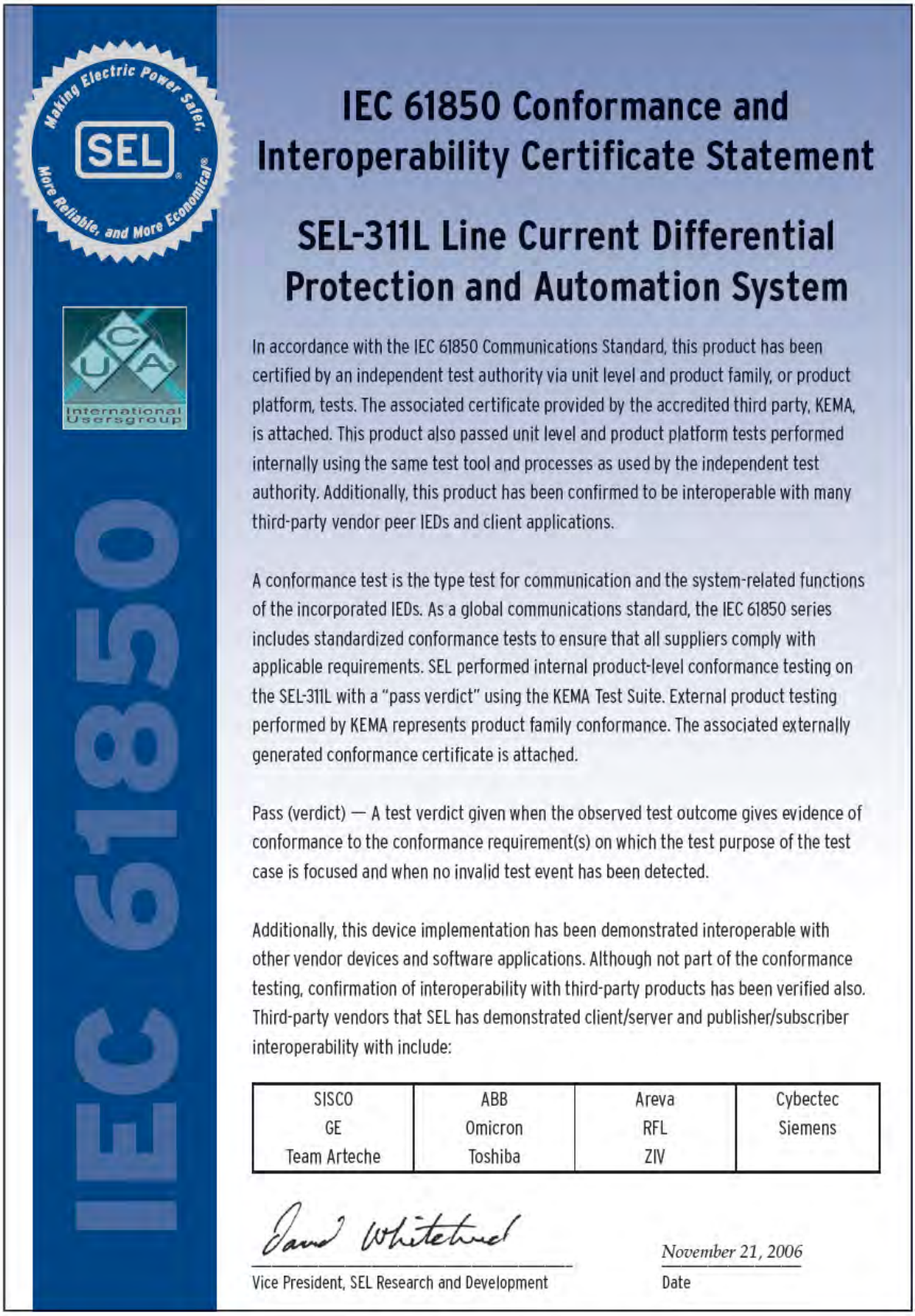
APPENDIX A

A.1 Conformance Certificates



IEC 61850 Conformance and Interoperability Certificate Statement

SEL-311L Line Current Differential Protection and Automation System

In accordance with the IEC 61850 Communications Standard, this product has been certified by an independent test authority via unit level and product family, or product platform, tests. The associated certificate provided by the accredited third party, KEMA, is attached. This product also passed unit level and product platform tests performed internally using the same test tool and processes as used by the independent test authority. Additionally, this product has been confirmed to be interoperable with many third-party vendor peer IEDs and client applications.

A conformance test is the type test for communication and the system-related functions of the incorporated IEDs. As a global communications standard, the IEC 61850 series includes standardized conformance tests to ensure that all suppliers comply with applicable requirements. SEL performed internal product-level conformance testing on the SEL-311L with a "pass verdict" using the KEMA Test Suite. External product testing performed by KEMA represents product family conformance. The associated externally generated conformance certificate is attached.

Pass (verdict) — A test verdict given when the observed test outcome gives evidence of conformance to the conformance requirement(s) on which the test purpose of the test case is focused and when no invalid test event has been detected.

Additionally, this device implementation has been demonstrated interoperable with other vendor devices and software applications. Although not part of the conformance testing, confirmation of interoperability with third-party products has been verified also. Third-party vendors that SEL has demonstrated client/server and publisher/subscriber interoperability with include:

SISCO GE Team Arteche	ABB Omicron Toshiba	Areva RFL ZIV	Cybectec Siemens

David Whitehead

Vice President, SEL Research and Development

November 21, 2006

Date

IEC 61850 Conformance and Interoperability Certificate Statement

SEL-487E Transformer Protection Relay

In accordance with the IEC 61850 Communications Standard, this product has been certified by an independent test authority via unit level and product family or product platform tests. The associated certificate, No. 30620245, provided by the accredited third party, KEMA, is attached. This product also passed unit level and product platform tests performed internally using the same test tool and processes as used by the independent test authority. Additionally, this product has been confirmed to be interoperable with many third-party vendor peer IEDs and client applications.

A conformance test is the type test for communication and the system-related functions of the incorporated IEDs. As a global communications standard, the IEC 61850 series includes standardized conformance tests to ensure that all suppliers comply with applicable requirements. These requirements include MMS, GOOSE, SCL, and Time Services. SEL performed internal product-level conformance testing on the SEL-487E with a "pass verdict" using the KEMA Test Suite and internal standardized tests. These tests include Time Synchronization and File Transfer.

Compatible global standards for time services and data access have also been tested for compliance and interoperability. GPS-based time synchronization provides microsecond accuracy. These have been demonstrated compatible with standard software available on virtually all laptops, workstations, and servers throughout industry and the world.

Additionally, this device implementation has been demonstrated interoperable with other IEC 61850 vendor devices and software applications. Although not part of the conformance testing, confirmation of interoperability with third-party products has been verified also. Third-party vendors that SEL has demonstrated client/server and publisher/subscriber interoperability with include:

SISCO	ABB	Areva	Cybectec
GE	Omicron	RFL	Siemens
Team Arteche	Toshiba	ZIV	

David Whitehead

Vice President, SEL Research and Development

September 4, 2008

Date

IEC 61850 Certificate Level A[1]

No. 30920420-Consulting 09-1712

Issued to:
ABB Oy
Distribution Automation
Muottitie 2 A
FI-65101 Vaasa
Finland

For the product:
615 series
Software version: 2.0.3
Hardware revision: C

Issued by: KEMA

The product has not shown to be non-conforming to:

IEC 61850-6, 7-1, 7-2, 7-3, 7-4 and 8-1

Communication networks and systems in substations

The conformance test has been performed according to IEC 61850-10 with product's protocol, model and technical issue implementation conformance statements: "RE_615_IEC61850_PICS_756465_ENc", "RE_615_IEC61850_MICS_756467_ENd", "RE_615_IEC61850_TICS_ 756466_ENc" and product's extra information for testing: "RE_615_IEC61850_PIXIT_756464_ENe".

The following IEC 61850 conformance blocks have been tested with a positive result (number of relevant and executed test cases / total number of test cases as defined in the UCA International Users Group Device Test procedures v2.2):

1	Basic Exchange (20/24)	9a	GOOSE Publish (7/12)
2	Data Sets (3/6)	9b	GOOSE Subscribe (9/10)
4+	Setting Group Definition (10/11)	12a	Direct Control (6/11)
5	Unbuffered Reporting (14/18)	12d	Enhanced SBO Control (11/19)
6	Buffered Reporting (16/20)	13	Time Synchronization (3/4)
		14	File Transfer (4/7)

This Certificate includes a summary of the test results as carried out at ABB Oy in Finland with UniCAsim 61850 version 3.19.02 with test suite 3.19.01 and UniCA 61850 analyzer 4.18.02. The test is based on the UCA International Users Group Device Test Procedures version 2.2. This document has been issued for information purposes only, and the original paper copy of the KEMA report: No. 30920420-Consulting 09-1711 will prevail.

The test has been carried out on one single specimen of the products as referred above and submitted to KEMA by ABB Oy. The manufacturer's production process has not been assessed. This Certificate does not imply that KEMA has certified or approved any product other than the specimen tested.

Arnhem, July 27, 2009

W. Strabbing
Manager Intelligent Networks and Communication

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Senior Test Engineer

1 Level A - Independent Test lab with certified ISO 9000 or ISO 17025 Quality System

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Applicable Test Procedures from the UCA International Users Group Device Test Procedures version 2.2

Conformance Block	Mandatory	Conditional
1: Basic Exchange	Ass1, Ass2, Ass3, AssN2, AssN3, AssN4, AssN5 Srv1, Srv2, Srv3, Srv4, Srv5, SrvN1abcd, SrvN4	Srv6, Srv7, Srv8, SrvN1e, SrvN2, SrvN3
2: Data Sets	Dset1, Dset10a, DsetN1ae	
4+: Setting Group Definition	Sg1, Sg2, Sg3a, Sg3b, Sg4 SgN1a, SgN1b, SgN2, SgN3, SgN4	
5: Unbuffered Reporting	Rp1, Rp2, Rp3, Rp4, Rp7, Rp10 RpN1, RpN2, RpN3, RpN4	Rp5, Rp8, RpN5, RpN6
6: Buffered Reporting	Br1, Br2, Br3, Br4, Br7, Br8, Br9, Br12 BrN1, BrN2, BrN3, BrN4, BrN5	Br5, Br10, BrN6
9a: GOOSE publish	Gop2, Gop3, Gop4, Gop7	Gop1, Gop6, GopN1
9b: GOOSE subscribe	Gos1a, Gos2, Gos3, GosN1, GosN2, GosN3, GosN4, GosN5, GosN6	
12a: Direct control	CltN3, CtlN8, DOns1, DOns3	Ctl2, CtlN11
12d: Enhanced SBO control	Ctl3, CltN1, CltN2, CltN3, CltN4, CtlN9 SBOes1, SBOes2, SBOes3	Ctl2, CtlN11
13: Time sync	Tm1, Tm2, TmN1	
14: File transfer	Ft1, Ft2ab, FtN1ab, Ft4	Ft2c, FtN1c

The conformance test was executed with following 615 series IED variants using the same software version and hardware revision.

REF615, RED615, RET615 and REM615

IEC 61850 Certificate Level A[1]

No. 30710079-Consulting 07-1458

Issued to:
Areva T&D
St. Leonards Avenue
ST17 4LX Stafford
United Kingdom

For the product:
Areva MiCOM P145
Feeder Management Relay
Firmware version 40A

Issued by: KEMA

The product has not shown to be non-conforming to:

IEC 61850-6, 7-1, 7-2, 7-3, 7-4 and 8-1

Communication networks and systems in substations

The conformance test has been performed according to IEC 61850-10 with product's protocol, model and technical issue implementation conformance statements: "MiCOM P145 Feeder Management Relay, Software version D2.1, Hardware Version J or K, PICS & MICS P145/EN PX/H65" and product's extra information for testing: "MiCOM P145 Feeder Management Relay, Software version D2.1, Hardware Version J or K, PIXIT P145/EN PX/H65".

The following IEC 61850 conformance blocks have been tested with a positive result (number of relevant and executed test cases / total number of test cases as defined in the UCA International Users Group Device Test procedures v1.1):

1	Basic Exchange (15/24)	9b	GOOSE Subscribe (10/10)
2	Data Sets (3/6)	12a	Direct Control (7/11)
5	Unbuffered Reporting (13/18)	12c	Enhanced Direct Control (7/13)
6	Buffered Reporting (16/20)	12d	Enhanced SBO Control (12/19)
9a	GOOSE Publish (5/12)	13	Time Synchronization (3/5)

This certificate includes a summary of the test results as carried out at KEMA in Arnhem with UniCAsim 61850 version 2.15.00 with test suite 2.15.00 and UniCA 61850 analyzer 4.15. The test is based on the UCA International Users Group Device Test Procedures version 1.1. This document has been issued for information purposes only, and the original paper copy of the KEMA report: No. 30710079-Consulting 07-1455 will prevail.

The tests have been carried out on one single specimen of the products as referred above and submitted to KEMA by Areva. The manufacturer's production process has not been assessed. This Certificate does not imply that KEMA has certified or approved any product other than the specimen tested.

Arnhem, July 12, 2007

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Applicable Test Procedures from the UCA International Users Group Device Test Procedures version 1.1

Conformance Block	Mandatory	Conditional
1: Basic Exchange	Ass1, Ass2, Ass3, AssN2, AssN3, AssN4, AssN5 Srv1, Srv2, Srv3, Srv4, Srv5, SrvN1abcd, SrvN4	Srv8
2: Data Sets	Dset1, Dset10a, DsetN1ae	
5: Unbuffered Reporting	Rp1, Rp2, Rp3, Rp4, Rp7, Rp10 RpN1, RpN2, RpN3, RpN4	Rp5, Rp8, Rp9
6: Buffered Reporting	Br1, Br2, Br3, Br4, Br7, Br8, Br9, Br12 BrN1, BrN2, BrN3, BrN4, BrN5	Br5, Br10, Br11
9a: GOOSE publish	Gop2, Gop3, Gop4, Gop7	Gop1
9b: GOOSE subscribe	Gos1a, Gos2, Gos3, GosN1, GosN2, GosN3, GosN4, GosN5, GosN6	Gos1b
12a: Direct control	CtlN3, CtlN8 DOns1, DOns3	Ctl2, CtlN10, CtlN11
12c: Enhanced Direct Control	CtlN3, CtlN8 DOes2, DOes5	Ctl2, CtlN10, CtlN11
12d: Enhanced SBO control	Ctl3, CtlN1, CtlN2, CtlN3, CtlN4, CtlN9 SBOes1, SBOes2, SBOes3	Ctl2, CtlN10, Ctln11
13: Time sync	Tm1, Tm2, TmN1	

A.2 Inventory List

A.2.1 SEL-311L Line Current Differential Protection & Automation System

The SEL-311L contains an advanced line current differential system that is easy to set and apply, while providing sub-cycle operation and superior fault resistance coverage. It is suitable for protection of any transmission line or underground cable where digital communication in the form of either a 56/64kb channel or dedicated fibre optic interface is available. The SEL-311L enables up to four zones of phase and ground mho distance backup elements, along with four zones of ground quadrilateral distance elements. Figure A.1 illustrates the SEL-311L relay with its corresponding functional overview.

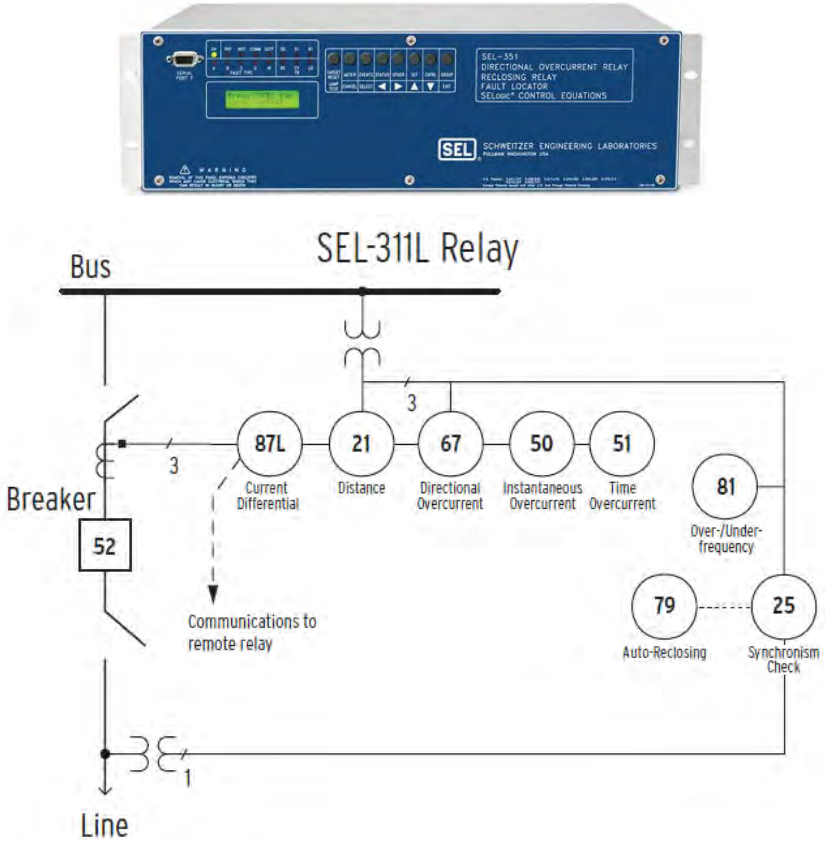


Figure A.1: SEL-311L relay and functional overview

The differential protection elements within the SEL-311L measure phase and sequence components from each line terminal as shown in Figure A.2. Because line charging current has a very low negative-sequence component, negative sequence differential current protection allows for high sensitivity without compromising security. The phase elements provide high-speed protection for severe or balanced faults. This allows rapid operation under heavy load flow conditions when system stability may be critical.

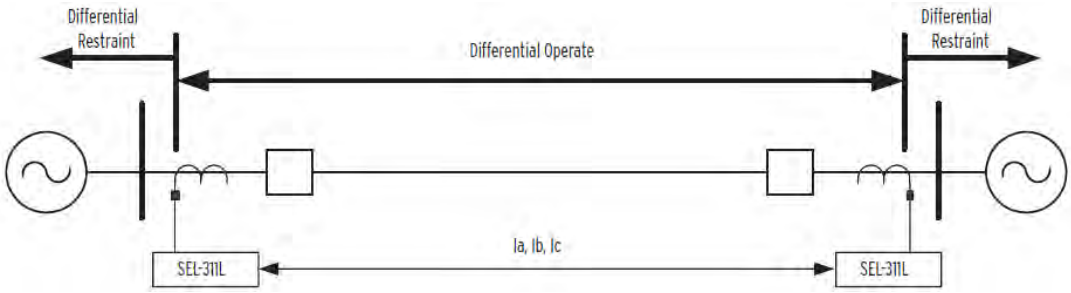


Figure A.2: Differential element operate and restraint regions

The vector ratio of the local ($\overrightarrow{I_L}$) and remote ($\overleftarrow{I_R}$) currents within the complex plane, known as the alpha plane, is shown in Figure A.3, Figure A.4, Figure A.5 and Figure A.6. For load and external faults with no CT or communication errors, the vector ratio of remote current to local current is –1 or 1∠180°. Errors introduced from CTs cause the ratio to appear at different locations within the complex ratio plane.

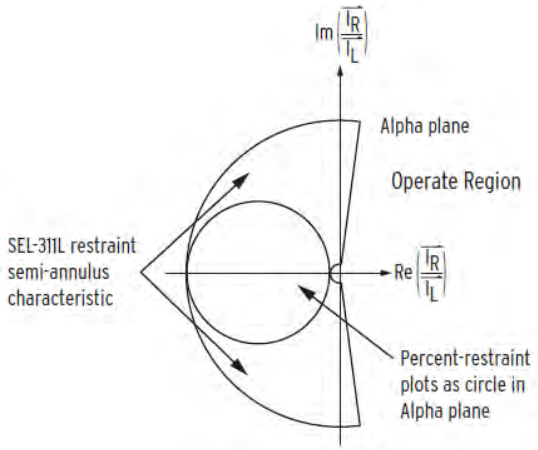


Figure A.3: Operate and restraint regions

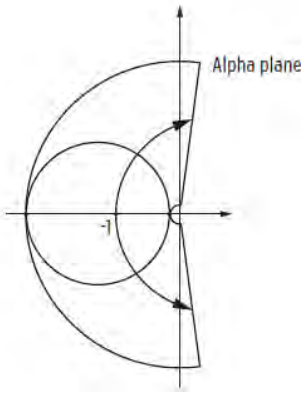


Figure A.4: Channel asymmetry

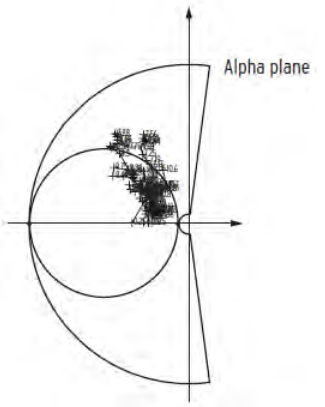


Figure A.5: Current transformer saturation

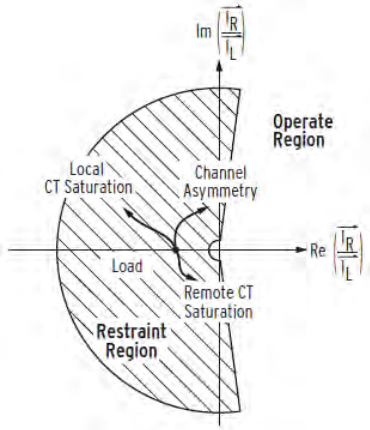


Figure A.6: System conditions

CT saturation, channel asymmetry and other effects during faults outside the protected zone produce shifts in the magnitude and angle of the ratio. The restraint characteristic provides proper control for these conditions and detects high-impedance faults and

outfeed faults that occur within the protected zone. The restraint region is adjusted both in angular extent and radial reach. The differential protection elements are insensitive to CT saturation effects due to different CT characteristics at the line ends or remnant CT flux. This prevents tripping on through faults and allows the use of existing CTs at each line end. The SEL-311L current connections add very little burden, which permits line current differential protection to be added to multiuse CTs without degradation of accuracy.

Figure A.7 and Figure A.8 illustrate the front and rear panel diagrams of the relay. The front panel user interface has a two-line 16 character LCD, 16 LED status and target indicators and 8 pushbuttons for local communication. The LCD shows event metering, setting and relay self-test status information and allows IED setting changes without the need for a data terminal. The LCD is controlled by GOOSE messages, pushbuttons and programmed display points.

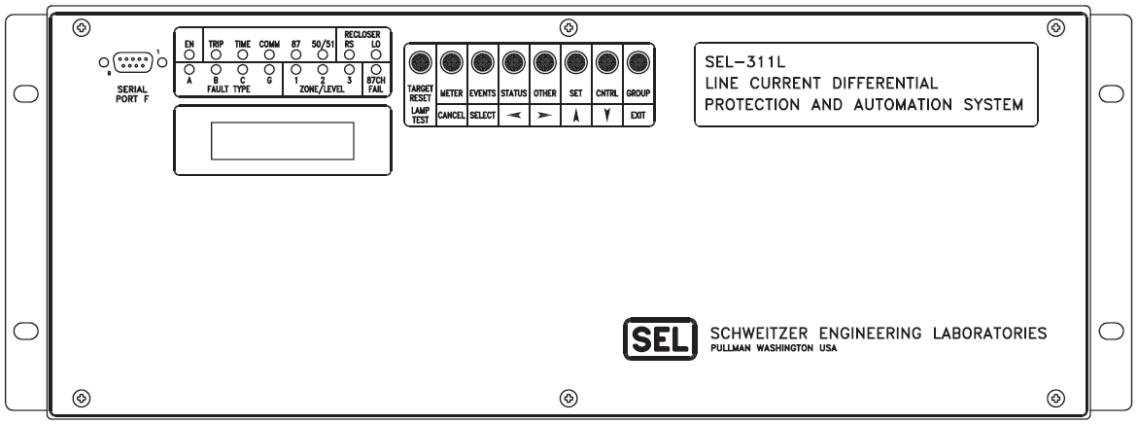


Figure A.7: Rack-mount front panel

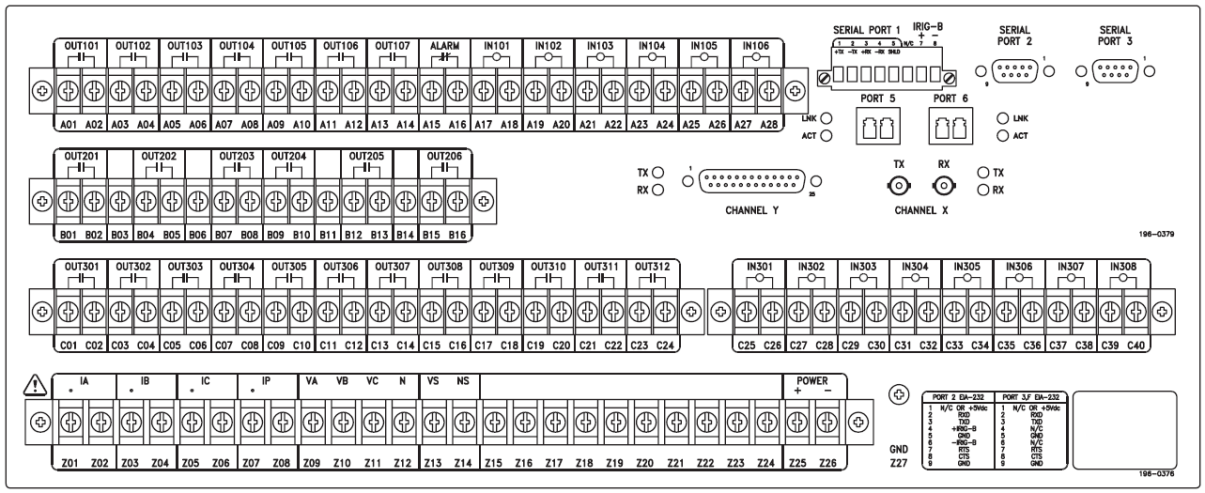


Figure A.8: Rear panel with 10/100BASE-T and 100BASE-FX Ethernet

Table A.1 represents the LED functions of the front panel display.

Table A.1: Description of target LEDs

Target LED	Function
EN	Relay powered properly and self-test satisfactory.
TRIP	Indication that a trip occurred.
TIME	Time-delayed trip.
COMM	Communication assisted trip.
87	Line current differential trip.
50/51	Instantaneous and time-overcurrent trip.
RECLOSER	RS - Ready for reclose cycle. LO - Control in lockout state.
FAULT TYPE	A, B, C - Phases involved in fault. G - Ground involved in fault.
ZONE/LEVEL	1-3 - Trip by Zone 1 and 3 distance elements and/or Level 1 and 3 overcurrent elements.
87CH FAIL	Failure of active differential channel.

The wiring diagram of Figure A.9 highlights the inputs, outputs and communication ports.

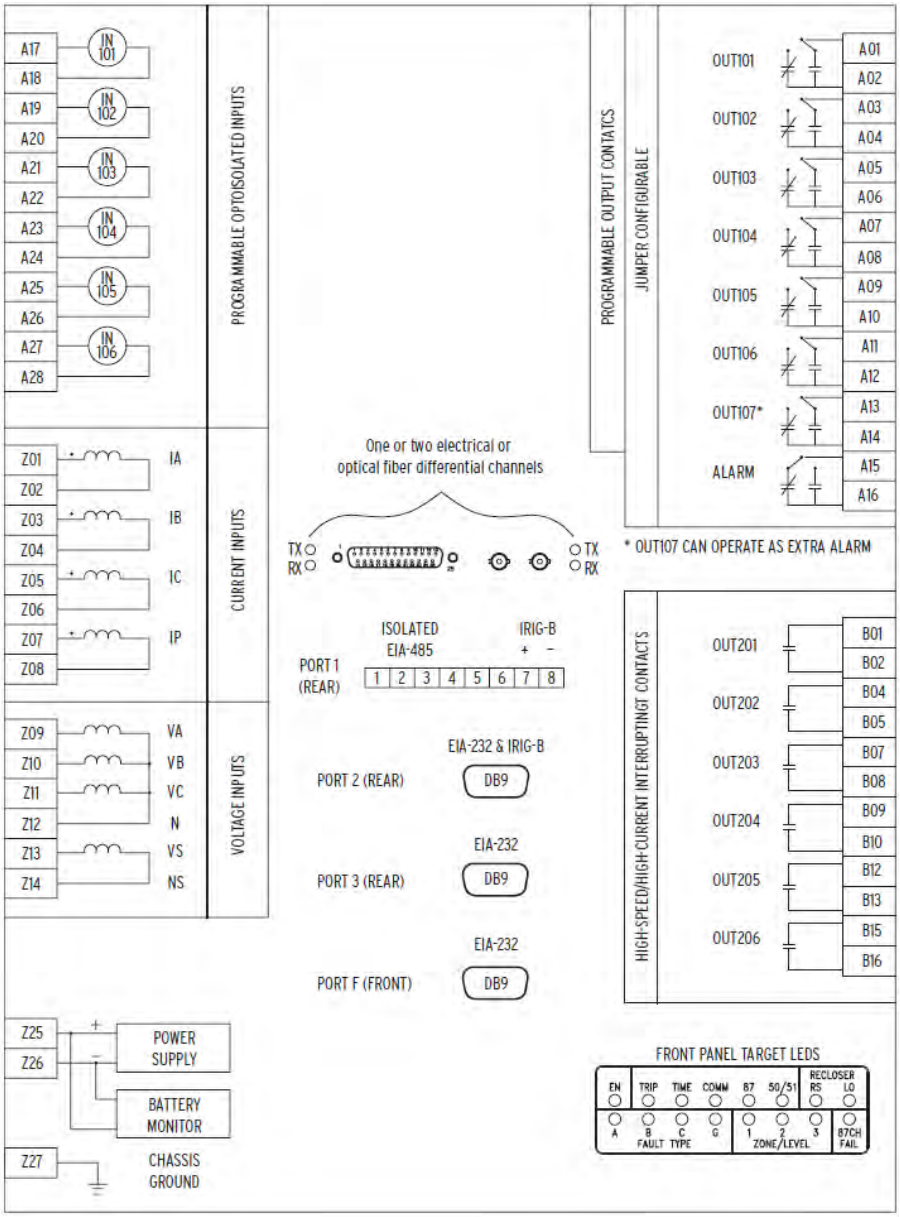
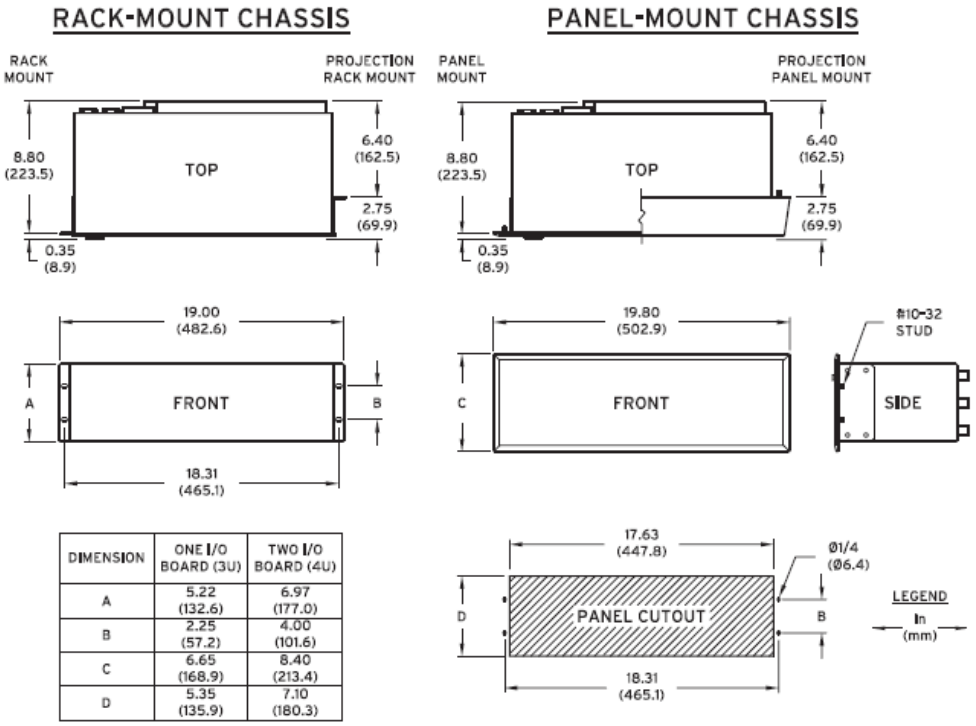


Figure A.9: Wiring diagram

Figure A.10 illustrates the mounting dimensions of the SEL-311L.



DIMENSION	ONE I/O BOARD (3U)	TWO I/O BOARD (4U)
A	5.22 (132.6)	6.97 (177.0)
B	2.25 (57.2)	4.00 (101.6)
C	6.65 (168.9)	8.40 (213.4)
D	5.35 (135.9)	7.10 (180.3)

Figure A.10: Mounting dimensions

Additional technical data is shown in Table A.2.

Table A.2: Technical data

General	
Terminal Connections	Rear Screw-Terminal Tightening Torque Minimum: 0.9 Nm, Maximum: 1.4 Nm Terminals or stranded copper wire. Ring terminals are recommended. Minimum temperature rating of 105ºC.
AC Current Input	Nominal: 5A Continuous: 15A, linear to 100A symmetrical Thermal Rating: 500A for 1 second, 1250A for 1 cycle Measurement Range: 0.5-96A Burden: 0.27 VA at 5A, 2.51 VA at 15A Nominal: 1A Continuous: 3A, linear to 20A symmetrical Thermal Rating: 100A for 1 second, 250A for 1 cycle Measurement Range: 0.1-19.2A Burden: 0.13 VA at 1A, 1.31 VA at 3A
AC Voltage Inputs	Nominal: 67 V_{L-N} three-phase four-wire connection Continuous: 150 V_{L-N} Measurement Range: 365 Vac for 10 seconds Burden: 0.13 VA at 67V, 0.45 VA at 120V
Power Supply	Input Voltage Rated: 125/250 Vdc or Vac, Range: 85-350 Vdc or 85-264 Vac Rated:48/125 Vdc or 125 Vac, Range: 38-200 Vdc or 85-140 Vac Rated: 24/48 Vdc, Range: 18-60 Vdc polarity dependent Power Consumption: <25W
Control Outputs	Standard Make: 30A Carry: 6A continuous carry at 70ºC, 4A continuous carry at 85ºC 1s Rating: 50A MOV Protection (maximum voltage): 270 Vac, 360 Vdc, 40 J Pickup/Dropout Time: <5ms Break Capacity (10,000 operations): 48 Vdc, 0.50A, L/R=40ms 125 Vdc, 0.30A, L/R=40ms 250 Vdc, 0.20A, L/R=40ms Cyclic Capacity (2.5 cycle/second): 48 Vdc, 0.50A, L/R=40ms 125 Vdc, 0.30A, L/R=40ms 250 Vdc, 0.20A, L/R=40ms

Optoisolated Inputs	250 Vdc: Pickup 200-300 Vdc; dropout 150 Vdc 220 Vdc: Pickup 176-264 Vdc; dropout 132 Vdc 125 Vdc: Pickup 105-150 Vdc; dropout 75 Vdc 110 Vdc: Pickup 88-132 Vdc; dropout 66 Vdc 48 Vdc: Pickup 38.4-60 Vdc; dropout 28.8 Vdc 24 Vdc: Pickup 15-30 Vdc
Frequency and Rotation	System Frequency: 50 or 60 Hz Phase Rotation: ABC or ACB Frequency Tracking: 40.1-65 Hz
Serial Communication Ports	EIA-232: 1 Front, 2 Rear EIA-485: 1 Rear, 2100 Vdc isolation Baud Rate: 300-38400
Ethernet Communications Ports	FTP to Card: 1 server session (supports IEC 61850 CID files) Telnet to Card: 1 serve session (support SEL ASCII) Telnet to Host: 1 server session (supports SEL ASCII, SEL Compressed ASCII, Fast Meter and Fast Operate) IEC61850: 6MMS sessions, 16 incoming GOOSE messages, 8 outgoing GOOSE messages
Protocol Stacks	TCP/IP, OSI
Ports (PORT 5 and PORT 6)	PORT 5 is supported PORT 6 will be enabled with a future firmware are upgrade
Physical Layer Options (PORT 5 and PORT 6)	10/100BASE-T: 10/100 Mbps, RJ-45 connector 100BASE-FX: 100 Mbps, LC connector
Indicators (PORT 5 and PORT 6)	Link: Green LED is on when the link is operational Activity: Red LED blinks when there is transmit or receive activity
Time-Code Input	Relay accepts demodulated IRIG-B time-code input as Port 1 or 2. Synchrophasor: ±10µs, Other: ±5ms
Operating Temperature	-40º to +85ºC
Weight	Rack Unit: 8.3 kilograms
Relay Elements	
Line Current Differential (87L) Elements	87L Enable Levels (Difference or Total Current) Phase Setting Range: OFF, 1.00 to 10.00A, 0.01A steps Negative-Sequence Setting Range: OFF, 0.50 to 5.00A, 0.01A steps Zero-Sequence Setting Range: OFF, 0.50 to 5.00A, 0.01A steps Accuracy: ±3% ±0.01 I_{NOM} Restraint Characteristics (Outer Radius) Radius Range: 2 to 8 in steps of 0.1 Angle Range: 90-270º in steps of 1º Accuracy: ±5% of radius setting, ±3º of angle setting Differential Current Alarm Setting Setting Range: OFF, 0.5 to 10.0A, 0.1A steps Accuracy: ±3% of ±0.01 I_{NOM}
Substation Battery Voltage Monitor Specifications	Pickup Range: 20-300 Vdc, 1 Vdc steps Pickup Accuracy: ±2% ±2 Vdc of setting
Timer Specifications	Reclosing Relay Pickup: 0.00-999999.00 cycles, 0.25-cycle steps Other Timers: 0.00-16000.00 cycles, 0.25-cycle steps Pickup/Dropout Accuracy for All Timers: ±0.25 cycle and ±0.1% of setting
Mho Phase Distance Elements	Zones 1-4 Impedance Reach Setting Range: OFF, 0.05 to 64.00Ω secondary, 0.01Ω steps (5A nominal) OFF, 0.25 to 320.00Ω secondary, 0.01Ω steps (1A nominal) Accuracy: ±5% of setting at line angle for 30 ≤ SIR ≤ 60 ±3% of setting at line angle for SIR < 60 Transient Overreach: <5% of setting plus steady-state accuracy Zones 1-4 Phase-to-Phase Current Fault Detectors (FD) Setting Range: 0.5-170 A_{p-p} secondary, 0.01A steps (5A nominal) 0.1-34 A_{p-p} secondary, 0.01A steps (1A nominal) Accuracy: ±0.05A and ±3% of setting (5A nominal) ±0.01A and ±3% of setting (1A nominal) Transient Overreach: <5% of pickup
Mho and Quadrilateral Ground Distance Elements	Zones 1-4 Impedance Reach Mho Element Reach: OFF, 0.05 to 64Ω secondary, 0.01Ω steps (5A nom) OFF, 0.25 to 320Ω secondary, 0.01 Ω steps (1A nom) Quadrilateral Reactance Reach: OFF, 0.05 to 64Ω secondary, 0.01Ω steps (5A nominal) OFF, 0.25 to 320Ω secondary, 0.01Ω steps (1A nominal) Quadrilateral Resistance Reach: OFF, 0.05 to 50Ω secondary, 0.01Ω steps (5A nominal) OFF, 0.25 to 250Ω secondary, 0.01Ω steps (1A nominal) Accuracy: ±5% of setting at line angle for 30 ≤ SIR ≤ 60 ±3% of setting at line angle for SIR < 30 Transient Overreach: <5% of setting plus steady-state accuracy Zones 1-4 Phase and Residual Current Fault Detectors (FD) Setting Range: 0.5-100A secondary, 0.01A steps (5A nominal)

	0.1-20A secondary, 0.01A steps (1A nominal) Accuracy: ±0.05A and ±3% of setting (5A nominal) ±0.01A and ±3% of setting (1A nominal) Transient Overreach: <5% of pickup
Undervoltage and Overvoltage Elements	Pickup Range: OFF, 0-150V, 0.01V steps (various elements) OFF, 0-260V, 0.01V steps (phase-to-phase elements) Steady-State Pickup Accuracy: ±1V and ±5% of setting Transient Overreach: <5% of pickup
Instantaneous/Definite-Time Overcurrent Elements	Pickup Range: OFF, 0.25-100A, 0.01A steps (5A nominal) OFF, 0.05-20A, 0.01A steps (1A nominal) Steady-State Pickup Accuracy: ±0.05A and ±3% of setting (5A nominal) ±0.01A and ±3% of setting (1A nominal) Transient Overreach: <5% of pickup Time Delay: 0-16000 cycles, 0.25-cycle steps Timer Accuracy: ±0.25 cycle and ±0.1% of setting
Time-Overcurrent Elements	Pickup Range: 0.25-16A, 0.01A steps (5A nominal) 0.05-3.20A, 0.01A steps (1A nominal) Steady-State Pickup Accuracy: ±0.05A and ±3% of setting (5A nominal) ±0.01A and ±3% of setting (1A nominal) Time Dial Range: 0.50-1.00, 0.01 steps (IEC) Curve Timing Accuracy: ±1.50 cycles and ± 4% of curve time for current between 2 and 30 multiples of pickup
Definite-Time Overfrequency or Underfrequency (81) Elements	Pickup Range: 41-65 Hz, 0.01 Hz steps Pickup Time: 32ms at 60 Hz (max) Time Delays: 2-16000 cycles, 0.25-cycle steps

A.2.2 SEL-487E Transformer Differential Relay

The SEL-487E Transformer Differential Relay provides three-phase differential protection of up to five restraint current inputs. The relay is made up of 24 analog channels separated into three groups. Group 1 consists of 15 phase current input channels. Group 2 features 3 single-phase (neutral) current input channels. Group 3 presents 6 dual three-phase voltage input channels. The SEL-487E offers current protection elements such as adaptive-slope phase percentage restraint differential, negative-sequence percentage restraint differential, voltage polarised breaker failure, negative and zero sequence time overcurrent, and busbar mismatch protection for CT ratios as high as 25:1. The secondary phase input current of winding S and X must be set to 1A or 5A. The relay has a sampling rate of 1kHz-8kHz.

Figure A.11: SEL-487E relay

The SEL-487E can monitor and control as many as 24 incoming and 8 outgoing GOOSE messages using the IEC61850 data server. The incoming GOOSE

messages are pre-defined using logical node objects and can manage up to 128 control bits at a latency of <3ms. Outgoing GOOSE messages can be configured with Boolean or analog data to isolate external breakers, switches and other devices. Figure A.12 demonstrates a simplified functional overview of the relay. Table A.3 describes the protection functions and ANSI device numbers of the SEL-487E.

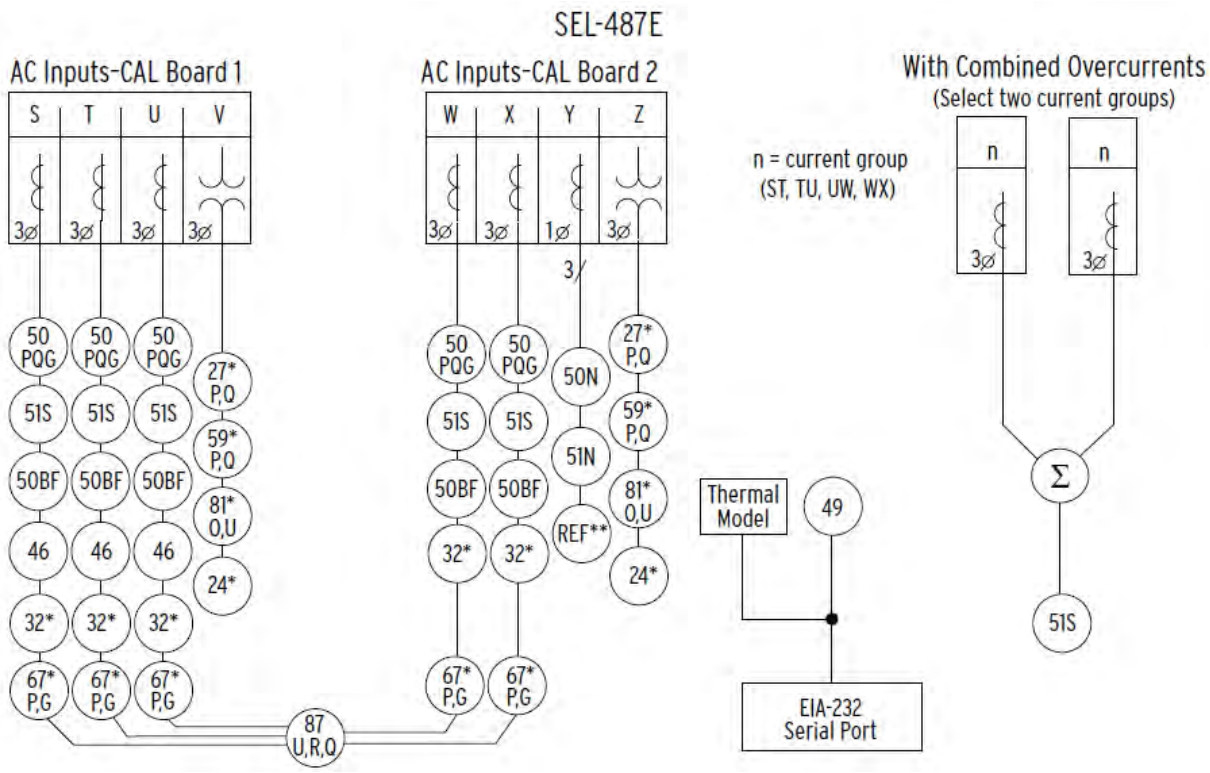


Figure A.12: Functional overview

Table A.3: Protection functions

ANSI Device Number	Description
87U	Unrestrained differential element
87R	Restrained differential element
87Q	Negative-sequence differential element
50	Instantaneous overcurrent element (P=Phase, Q=Negative sequence, N=Neutral)
51S	Adaptive time-overcurrent element
50BF	Breaker failure element
46	Current unbalance
32	Directional power element
67	Directional overcurrent element
81	Frequency element (O=Over, U=Under)
27	Undervoltage element
59	Overcoltage element
24	Volt/Hertz element
49	Thermal element
G, N, P, Q, R, S, U	(G) Ground, (N) Neutral, (P) Phase, (Q) Negative Sequence, (R) Restrained, (S) Adaptive, (U) Unrestrained

Figure A.13 illustrates the rear panel diagram.

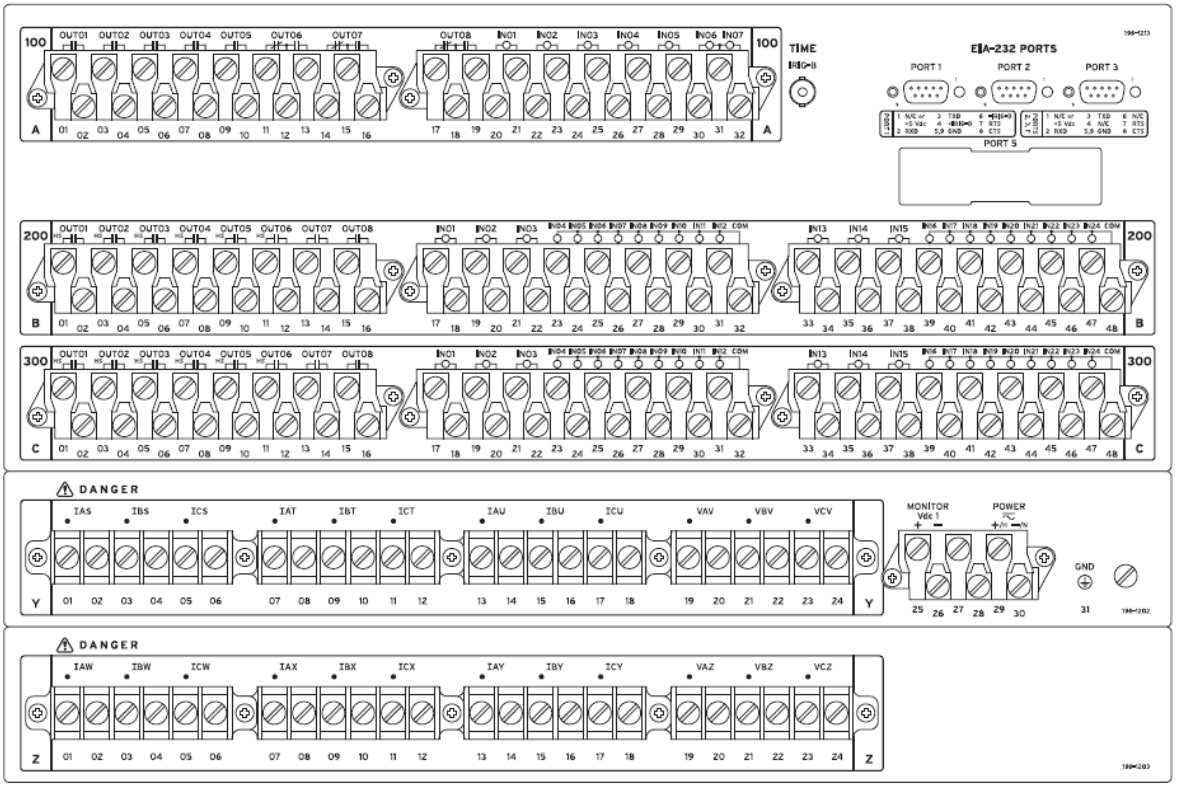
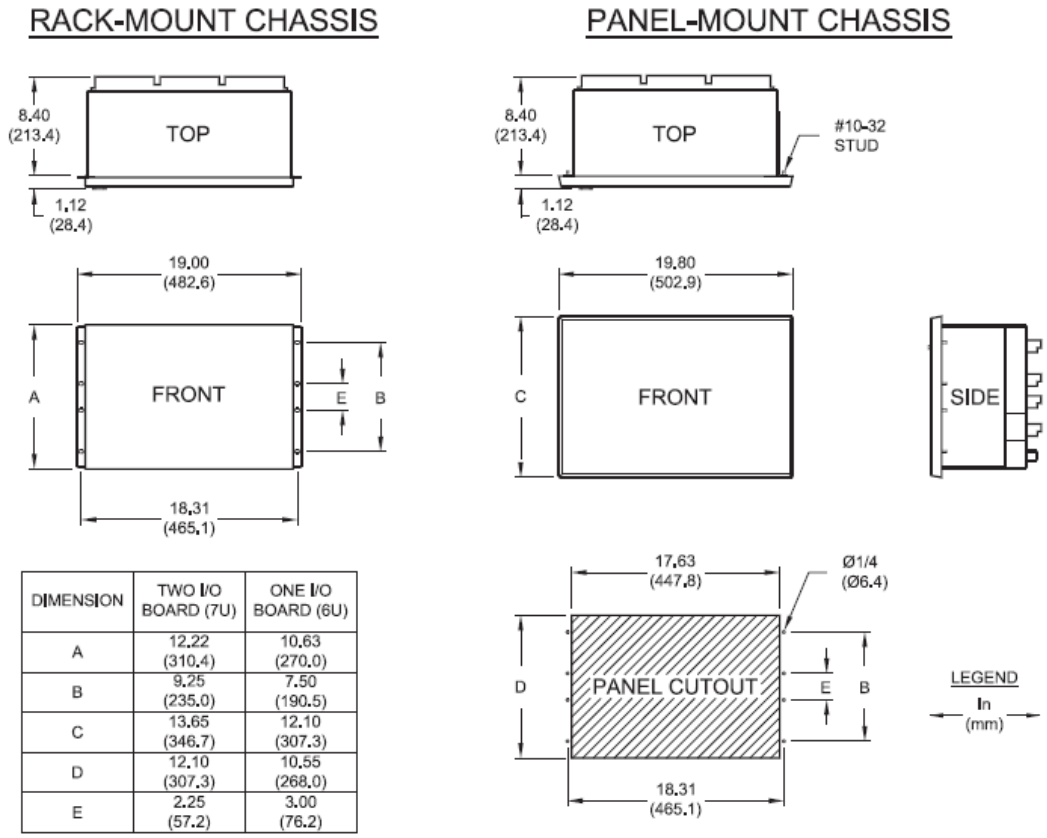


Figure A.13: Rear panel

Figure A.14 illustrates mounting dimensions of the SEL-487E.



DIMENSION	TWO I/O BOARD (7U)	ONE I/O BOARD (6U)
A	12.22 (310.4)	10.63 (270.0)
B	9.25 (235.0)	7.50 (190.5)
C	13.65 (346.7)	12.10 (307.3)
D	12.10 (307.3)	10.55 (268.0)
E	2.25 (57.2)	3.00 (76.2)

Figure A.14: Mounting dimensions

Table A.4 summarises technical data.

Table A.4: Technical data

General	
AC current inputs (secondary circuits)	Continuous Thermal Rating 5A nominal: 15A, 1A nominal: 3A Saturation Current (Linear) Rating 5A nominal: 100A, 1A nominal: 20A One-Second Thermal Rating 5A nominal: 500A, 1A nominal: 100A One-Cycle Thermal Rating 5A nominal: 1250A peak 1A nominal: 250A peak Burden Rating 5A nominal: ≤0.5VA at 5A, 2.51VA at 15A 1A nominal: ≤0.1VA at 1A, 1.31VA at 3A Minimum A/D Current Limit (peak) 5A nominal: 247.5A 1A nominal: 49.5A Sampling Rate: 8kHz Rated Voltage (U_e): 240 Vac Rated Insulation Voltage (U_i): 300 Vac Rotation: ABC, ACB
AC Voltage Inputs	Burden: <0.5VA at 67V Nominal Frequency Rating: 50±5Hz, 60±5Hz Frequency Tracking: tracks between 40-65Hz, below 40Hz = 40Hz, above 65Hz = 65Hz Maximum Slew Rate: 15Hz/s
Power Supply	125/250 Vdc or 120/230 Vac DC Range: 85-300 Vdc DC Burden: < 35W AC Range: 85-264 Vac AC Burden: <180VA at pf=0.2 Nominal Frequency: 50/60Hz 48/125 Vdc or 120 Vac DC Range: 38-140 Vdc DC Burden: <35W AC Range: 85-140 Vac AC Burden: <170 VA at pf=0.2 Nominal Frequency: 50/60Hz
Control Outputs	Rated Insulation Voltage (U_i): 300 Vac, 470 Vdc Dielectric Test Voltage: 2500 Vac Rated Impulse Voltage (U_{imp}): 5000V Continuous Carry: 6A at 70ºC, 4A at 85ºC Operating Time (coil energisation to contact closure, resistive load) Pickup time (resistive load): ≤6ms maximum Dropout time (resistive load): ≤6ms maximum Break Capacity: 24 Vdc, 0.75A, L/R=40ms; 48 Vdc, 0.50A, L/R=40ms; 125 Vdc, 0.30A, L/R=40ms; 250 Vdc, 0.20A, L/R=40ms Minimum Current Rating: 10mA Update Rate: 1/8 cycle
High-Current Contact Output Ratings	Rated Insulation Voltage (U_i): 300Vac, 470 Vdc Rated Carry: 6A at 70ºC and 4A at 85ºC continuous carry One Second Thermal Rating: 50A Operating Time (coil energisation to contact closure, resistive load) Pickup time (resistive load): ≤6ms maximum Dropout time (resistive load): ≤8ms maximum
Optoisolated Digital Inputs	
General	Sampling Rate: 2kHz Rated Insulation Voltage (U_i): 300 Vac Dielectric Test Voltage: 2500 Vac or 3100 Vdc Rated Impulse Voltage (U_{imp}): 5000V Main Board: 5 independent, 2 common, level sensitive optoisolated INT2: 8 independent, level-sensitive optoisolated INT4: 18 common, 6 independent, level sensitive optoisolated INT7: 8 independent, level-sensitive optoisolated INT8: 8 independent, level-sensitive optoisolated
DC Digital Input Ratings	Voltage Options: 48, 110, 125, 220, 250V DC Threshold: 48 Vdc (Pickup 38.4-60.0 Vdc; Dropout below 28.8 Vdc)

	110 Vdc (Pickup 88.0-132.0 Vdc; Dropout below 66.0 Vdc) 125 Vdc (Pickup 105-150 Vdc; Dropout below 75 Vdc) 220 Vdc (Pickup 176-264 Vdc; Dropout below 132 Vdc) 250 Vdc (Pickup 200-300 Vdc; Dropout below 150 Vdc) Current Drawn: 5mA at nominal voltage, 8mA for 110V option
AC Digital Input Ratings	Rated Frequency: 50±5Hz, 60±5Hz 48 Vdc (Pickup 32.8-60.0 Vac; Dropout below 20.3 Vac) 110 Vdc (Pickup 75.1-132.0 Vac; Dropout below 46.6 Vac) 125 Vdc (Pickup 89.6-150.0 Vac; Dropout below 53.0 Vac) 220 Vdc (Pickup 150.3-264.0 Vac; Dropout below 93.2 Vac) 250 Vdc (Pickup 170.6-300.0 Vac; Dropout below 106.0 Vac) Current Drawn: 5mA at nominal voltage, 8mA for 110V option System frequency: 50/60Hz Phase rotation: ABC or ACB
Communications Ports	EIA-232: 1 Front and 3 Rear Serial Data Speed: 300-57600bps Fibre Optic (Mode: Multi, Wavelength: 820nm, Source: LED, Connector type: ST, Sys. Gain (dB): 5), (Mode: Single, Wavelength: 1300nm, Source: LED, Connector type: ST, Sys. Gain (dB): 13) Min. TX Pwr. (dBm): -15.8 to +19 Max. TX Pwr. (dBm): 12-14 RX Sens. (dBm): -34.4 to +32 Sys. Gain (dB): 513 IRIG Time Input Demodulated IRIG-B time code (Nominal Voltage: 5 Vdc± 10%, Maximum Voltage: 8 Vdc, Input Impedance: 332Ω ± 10%, Isolation: 1.5 kV_{RMS} for 1 minute) Terminal Connections Rear Screw-Terminal Tightening Torque (Minimum: 1.0 Nm, Maximum 2.0 Nm)
Event Reports	
High-Resolution Data	Rate: 8000, 4000, 2000, 1000 samples/second Output Format: Binary COMTRADE
Event Reports	Length: 15/30 cycles Maximum Duration: 2 seconds of back-to-back event reports and a total of 5 seconds Resolution: 1/4 and 1/8 samples/cycle Digital Inputs: 2kHz
Event Summary	Storage: 100 summaries
Breaker History	Storage: 128 histories
Sequential Events Recorder	Storage: 1000 entries Trigger Elements: 250 relay elements
Relay Element Pickup Ranges and Accuracies	
Differential Elements (General)	Number of Zones: 1 (A, B and C elements) Number of Windings: 5 TAP Pickup: (0.1-32.0) x I_{NOM} A secondary TAP Range: $TAP_{MAX}/TAP_{MIN} \leq 35$ Time-Delay Accuracy: ±0.1% plus ±0.125 cycle
Differential Elements (Restraint)	Pickup Range: 0.1-4.0 per unit Pickup Accuracy: 1A nominal (±5% ±0.02A), 5A nominal (±5% ±0.10A) Pickup Time: 1.25 minimum cycle, 1.38 typical cycle, 1.5 maximum cycle Slope 1 (Setting range: 5-100%, Accuracy: ±5% ±0.02 x I_{NOM} Slope 2 (Setting range: 5-100%, Accuracy: ±5% ±0.02 x I_{NOM}
Differential Elements (Unrestraint)	Pickup Range: (1.0-20.0) x TAP Pickup Accuracy: ±5% of user setting, ±0.02 x I_{NOM} A Pickup Time: 0.7 minimum cycle, 0.85 typical cycle, 1.2 maximum cycle
Harmonic Elements (2nd, 4th, 5th)	Pickup Range: OFF, 5−100% of fundamental Pickup Accuracy: 1A nominal (±5% ±0.02A), 5A nominal (±5% ±0.10A) Time-Delay Accuracy: ±0.1% plus ±0.125 cycle
Negative-Sequence Differential Element	Pickup Range: 0.05−1 per unit Slope Range: 5−100% Pickup Accuracy: ±5% of user setting, ±0.02 x I_{NOM} A Maximum Pickup/Dropout Time: 4 cycles Winding Coverage: 2%
Incremental Restraint and Operating Threshold Current Supervision	Setting Range: 0.1−10.0 per unit Accuracy: ±5% ±0.02 x I_{NOM}
Open-Phase Detection Logic	3 elements per winding (S, T, U, W, X) Pickup Range (1A nominal: 0.05−1.00A, 5A nominal: 0.25-5.00A) Maximum Pickup/Dropout Time: 0.625 cycle
Restricted Earth Fault (REF)	
Operating Quantity	Select: IY1, IY2, IY3
Restraint Quantity	Select: 3i0S, 3i0T, 3i0U, 3i0W and 3I0X

	Pickup Range: 0.05−5 per unit, 0.02−0.05 positive-sequence ratio factor Pickup Accuracy (1A nominal: 0.01A, 5A nominal: 0.05A) Maximum Pickup/Dropout Time: 1.75 cycles
Instantaneous/Definite-Time Overcurrent Elements (50)	Phase- and Negative-Sequence, Ground-Residual Elements Pickup Range 5A nominal: 0.25-100A secondary, 0.01A steps 1A nominal: 0.05-20A secondary, 0.01A steps Accuracy (Steady State) 5A nominal: ±0.05A plus ±3% of setting 1A nominal: ±0.01A plus ±3% of setting Transient Overreach (phase and ground residual) 5A nominal: ±5% of setting, ±0.10A 1A nominal: ±5% of setting, ±0.02A Transient Overreach (negative sequence) 5A nominal: ±6% of setting, ±0.10A 1A nominal: ±6% of setting, ±0.02A Time-Delay Range: 0.00-16000.00 cycles, 0.125 cycle steps Time Accuracy: ±0.25 cycle plus ±0.1% of setting Maximum Pickup/Dropout Time: 1.5 cycles
Combined Time-Overcurrent Elements (51)	Pickup Range (5A nominal: 0.25-16A secondary, 0.01A steps) (1A nominal: 0.05-3.20A secondary, 0.01A steps) Accuracy (Steady State) (5A nominal: ±0.05A plus ±3% of setting) (1A nominal: ±0.01A plus ±3% of setting) Transient Overreach (5A nominal: ±5% of setting, ±0.10A) (1A nominal: ±5% of setting, ±0.20A) Transient Overreach (5A nominal: ±5%, ±0.10A) (1A nominal: ±5%, ±0.02A) Maximum Pickup Time: 1.5 cycles
Directional Overpower / Underpower Element	Operating Quantities: OFF, 3PmF, 3QmF, 3PqpF, 3QqpF Pickup Range: -20000VA (secondary) to 20000VA (secondary, 0.01 steps) Pickup Accuracy: ±3% of setting and ±5VA, power factor > ±0.5 at nominal frequency Time Delay Range: 0.000-16000 cycles, 0.25 cycle increment Time Delay Accuracy: ±0.1% of setting ±0.25 cycle
Bay Control	Breakers: 5 (maximum) Disconnects (Isolators): 8 (maximum)

A.2.3 REF615 Feeder Protection & Control Relay

The REF615 Feeder Protection & Control relay is perfectly aligned for the protection, control, measurement and s upervision of utility and i ndustrial power distribution systems. The IED offers directional and non-directional overcurrent and thermal overload protection, directional and non-directional earth-fault protection, sensitive earth-fault protection, phase discontinuity protection, transient/intermittent earth-fault protection, overvoltage and undervoltage protection, residual overvoltage protection, positive sequence undervoltage and negative sequence overvoltage protection. The IED offers three-pole multi-shot autoreclose functions for overhead line feeders and features three light detection channels for arc fault protection of circuit breaker, busbar and cable switchgear. Figure A.15, illustrates the REF615 relay.

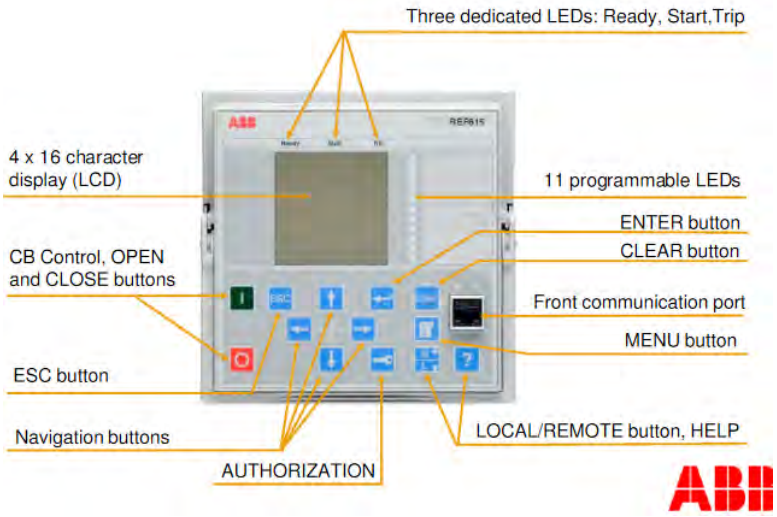


Figure A.15: REF615 relay

The IED is established with a disturbance recorder featuring up to 12 analog and 64 binary channels. The analog channels are set to trigger sudden waveform trends above or below the set value. The binary channels are set to start recording on the rising or falling edge of the binary signal. By default, the binary channels are set to record external or internal IED signals (i.e. start or trip signals, external blocking and control signals). The recorded information is stored in a non-volatile memory and can be uploaded for subsequent fault analysis.

To collect Sequence-of-Event (SoE) information, the IED incorporates the capacity of storing 50 event codes with time stamps. The memory storage retains its data in case the IED temporarily loses its auxiliary supply. The event log facilitates detailed pre- and post-fault analysis of feeder faults and disturbances. The REF615 has the capacity to store the records up-to-the-minute. Each record comprises of current, voltage, angle values, start times and time stamps. The IED supports the IEC61850, IEC60870-5-103, Modbus and DNP3 communication protocols.

Table A.5 summarises critical technical data for the relay.

Table A.5: Technical data

Dimensions	
Width	Frame: 179.8mm, Case: 164mm
Height	Frame: 177mm, Case: 160mm
Depth	194mm (153mm + 41mm)
Weight	IED: 3.5kg, Spare unit: 1.8kg
Power Supply	
U_{aux} nominal	Type 1: 100, 110, 120, 220, 240V AC at 50/60Hz 48, 60, 110, 125, 220, 250V DC Type 2: 24, 30, 48, 60V DC
U_{aux} variation	Type 1: 38 ... 110% of U_n (38 ... 264V AC) 80 ... 120% of U_n (38.4 ... 300V DC)

	Type 2: 50 ... 120% of U_n (12 ... 72V DC)
Start-up threshold	Type 2: 19.2V DC (24V DC x 80%)
Burden of auxiliary voltage supplier under quiescent (P_q)/operating condition	Type 1: 250V DC - 8.5W (nominal)/-14.1W (max) 240V AC - 10.2W (nominal)/-16.1W (max) Type 2: 60V DC - 6.7W (nominal)/-12.9W (max)
Ripple in the DC auxiliary voltage	Max 12% of the DC value (at frequency of 100 Hz)
Maximum interruption time in the auxiliary DC voltage without resetting the IED	Type 1: 100V DC: 84ms, 100V AC:116ms Type 2: 48V DC: 68ms
Fuse type	T4A/250V
Binary Inputs	
Operating range	±20% of the rated voltage
Rated voltage	24 ... 250V DC
Current drain	1.6 ... 1.9mA
Power consumption	31.0 ... 570.0mW
Threshold voltage	18 ... 176V DC
Reaction time	3ms
Signal outputs and IRF output	
Rated voltage	250V AC/DC
Continuous contact carry	5A
Make and carry for 3.0s	10A
Make and carry 0.5s	15A
Breaking capacity when the control-circuit time constant L/R < 40ms, at 48/110/220V DC	1A / 0.25A / 0.15A
Minimum contact load	100mA at 24V AC/DC
Single-pole power output relays	
Rated voltage	250V AC/DC
Continuous contact carry	8A
Make and carry for 3.0s	15A
Make and carry for 0.5s	30A
Breaking capacity when the control-circuit time constant L/R < 40ms, at 48/110/220V DC, at 48/110/220V DC	5A / 3A / 1A
Minimum contact load	100mA at 24V AC/DC
Lens sensor and optical fibre for arc protection	
Fibre-optic cable including lens	1.5m, 3.0m or 5.0m
Normal service temperature range of the lens	-40 ... + 100ºC
Maximum service temperature range of the lens, max 1h	+140ºC
Minimum permissible bending radius of the connection fibre	100mm
Environmental conditions	
Operating temperature range	-25 ... + 55ºC (continuous)
Short-time service temperature range	-40 ... + 85ºC (<16h)
Relative humidity	<93%, non-condensing
Atmospheric pressure	86 ... 106kPa
Altitude	Up to 2000m
Transport/storage temperature range	-40 ... + 85ºC
Front port Ethernet interfaces	
TCP/IP protocol	Standard Ethernet CAT 5 cable with RJ-45 connector 10 MBits/s
Three-phase non-directional overcurrent protection (PHxPTOC)	
Operation accuracy	PHLPTOC: Depending on the frequency of the current measured f_n ±2Hz; ±1.5% of the set value or ±0.002 x I_n PHHPTOC and PHIPTOC: ±1.5% of set value or ±0.002 x I_n (at currents in the range of 0.1 ... 10 x I_n); ±5.0% of the set value (at currents in the range of 10 ... 40 x I_n)
Reset time	<40ms
Reset ratio	Typical 0.96
Retardation time	<30ms
Operate time accuracy in definite time mode	±1.0% of the set value or ±20ms
Operate time accuracy in inverse time mode	±5.0% of the theoretical value or ±20ms
Suppression of harmonics	RMS: No suppression DFT: -50dB at f = n x f_n, where n = 2, 3, 4, 5
Three-phase non-directional overcurrent protection (PHxPTOC) main settings	
Start value	PHLPTOC: Range 0.05 ... 5.00 x I_n, Step 0.01 PHHPTOC: Range 0.10 ... 40.00 x I_n, Step 0.01 PHIPTOC: Range 1.00 ... 40.00 x I_n, Step 0.01
Time multiplier	PHLPTOC: Range 0.05 ... 15.00, Step 0.05 PHHPTOC: Range 0.05 ... 15.00, Step 0.05
Operate delay time	PHLPTOC: Range 40 ... 200000 ms, Step 10

	PHHPTOC: Range 40 ... 200000 ms, Step 10 PHIPTOC: Range 20 ... 200000 ms, Step 10
Operating curve type	PHLPTOC: Definite or inverse time (Curve type 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 17, 18, 19) PHHPTOC: Definite or inverse time (Curve type 1, 3, 5, 9, 10, 12, 15, 17) PHIPTOC: Definite time
Three-phase directional over current protection (DPHxPDOC)	
Operation accuracy	DPHLPDOC: Depending on t he frequency of the current/voltage measured f_n ±2Hz. Current ±1.5% of the set value or ±0.002 x I_n. Voltage ±1.5% of the set value or ±0.002 x U_n. Phase angle ±2º. DPHHPDOC: Current ±1.5% of the set value or ±0.002 x I_n (at currents in the range of 0.1 ... 10 x I_n), ±5.0% of the set value (At currents in the range of 10 ... 40 x I_n). Voltage ±1.5% of the set value or ±0.002 x U_n. Phase angle ±2º.
Start time	I_{Fault} = 2.0 x set start value (Minimum 37ms, Typical 40ms, Maximum 42ms)
Reset time	<40ms
Reset ratio	Typical 0.96
Retardation time	<35ms
Operate time accuracy in definite time mode	±1.0% of the set value or ±20ms
Operate time accuracy in inverse time mode	±5.0% of the theoretical value or ±20ms
Suppression of harmonics	DFT: -50dB at f = n x f_n, where n = 2, 3, 4, 5, ...
Three-phase directional overcurrent protection (DPHxPDOC) main settings	
Start value	DPHxPDOC: Range 0.05 ... 5.00 x I_n, Step 0.01
Time multiplier	DPHxPDOC: Range 0.05 ... 15.00, Step 0.05
Operate delay time	DPHxPDOC: Range 40 ... 200000ms, Step 10
Directional mode	DPHxPDOC: 1 = Non-directional, 2 = Forward, 3 = Reverse
Characteristic angel	DPHxPDOC: -179 ... 180 degrees
Operating curve type	DPHLPDOC: Definite or inverse time (Curve type 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19) DPHHPTOC: Definite or inverse time (Curve type 1, 3, 5, 9, 10, 12, 15, 17)
Non-directional EF protection (EFxPTOC)	
Operation accuracy	EFLPTOC: Depending on the frequency of the current measured f_n: ±2Hz, ±1.5% of the set value or ±0.002 x I_n EFHPTOC and EFIPTOC: ±1.5% of set value or ±0.0002 x I_n (at currents in the range of 0.1 ... 10 x I_n), ±5.0% of the set value (at currents in the range of 10 ... 40 x I_n)
Reset time	<40ms
Reset ratio	Typical 0.96
Retardation time	<30ms
Operate time accuracy in definite time mode	±1.0% of the set value or ±20ms
Operate time accuracy in inverse time mode	±5.0% of the theoretical value or ±20ms
Non-directional EF protection (EFxPTOC) main settings	
Start value	EFLPTOC: Range 0.010 ... 5.000 x I_n, Step 0.005 EFHPTOC: Range 0.10 ... 40.00 x I_n, Step 0.01 EFIPTOC: Range 1.00 ... 40.00 x I_n, Step 0.01
Time multiplier	EFLPTOC: Range 0.05 ... 15.00, Step 0.05 EFHPTOC: Range 0.15 ... 15.00, Step 0.05
Operate delay time	EFLPTOC: Range 40 ... 200000ms, Step 10 EFHPTOC: Range 40 ... 200000ms, Step 10 EFIPTOC: Range 20 ... 200000ms, Step 10
Operating curve type	EFLPTOC: Definite or inverse time (Curve type 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 19) EFHPTOC: Definite or inverse time (Curve type 1, 3, 5, 9, 10, 12, 15, 17) EFIPTOC: Definite time
Transient/intermittent earth-fault protection (INTRPTEF)	
Operation accuracy (U_O criteria with transient protection)	Depending on the frequency of the current measured f_n ±2Hz, ±1.5% of the set value or ±0.002 x U_n
Operate time accuracy	±1.0% of the set value or ±20ms
Three-phase overvoltage protection (PHPTOV)	
Operating accuracy	Depending on the frequency of the voltage measured f_n ±2Hz, ±1.5% of the set value or ±0.002 x U_n
Start time	U_{Fault} = 1.1 x set start value Minimum 22ms, Typical 24ms, Maximum 26ms
Reset time	<40ms
Reset ratio	Depends on the set relative hysteresis
Retardation time	<35ms
Operating time accuracy in definite time mode	±1.0% of the set value or ±20ms

Operating time accuracy in inverse time mode	±5.0% of the theoretical value or ±20ms
Suppression of harmonics	DFT: -50dB at f = n x f_n, where n = 2, 3, 4, 5, ...
Three-phase overvoltage protection (PHPTOV) main settings	
Start value	PHPTOV: Range 0.05 ... 1.60 x U_n, Step 0.01
Time multiplier	PHPTOV: Range 0.05 ... 15, Step 0.05
Operate delay time	PHPTOV: Range 40 ... 300000ms, Step 10
Operating curve type	PHPTOV: Definite or inverse time (Curve type 5, 15, 17, 18, 19, 20)
Three-phase undervoltage protection (PHPTUV)	
Operating accuracy	Depending on the frequency of the voltage measured f_n ±2Hz, ±1.5% of the set value or ±0.002 x U_n
Start time	U_{Fault} = 0.9 x set start value Minimum 62ms, Typical 64ms, Maximum 66ms
Reset time	<40ms
Reset ratio	Depends on the set relative hysteresis
Retardation time	<35ms
Operating time accuracy in definite time mode	±1.0% of the set value or ±20ms
Operating time accuracy in inverse time mode	±5.0% of the theoretical value or ±20ms
Suppression of harmonics	DFT: -50dB at f = n x f_n, where n = 2, 3, 4, 5, ...
Three-phase undervoltage protection (PHPTUV) main settings	
Start value	PHPTUV: Range 0.05 ... 1.20 x U_n, Step 0.01
Time multiplier	PHPTUV: Range 0.05 ... 15.00, Step 0.05
Operate delay time	PHPTUV: Range 60 ... 300000ms, Step 10
Operating curve type	PHPTUV: Definite or inverse time (Curve type 5, 15, 17, 18, 19, 20)
Positive sequence undervoltage protection (PSPTUV)	
Operating accuracy	Depending on the frequency of the voltage measured f_n ±2Hz, ±1.5% of the set value or ±0.002 x U_n
Start time	U_{Fault} = 0.99 x set start value Minimum 51ms, Typical 53ms, Maximum 54ms U_{Fault} = 0.9 x set start value Minimum 43ms, Typical 45ms, Maximum 46ms
Reset time	<40ms
Reset ratio	Depends on the set relative hysteresis
Retardation time	<35ms
Operating time accuracy in definite time mode	±1.0% of the set value or ±20ms
Operating time accuracy in inverse time mode	±5.0% of the theoretical value or ±20ms
Suppression of harmonics	DFT: -50dB at f = n x f_n, where n = 2, 3, 4, 5, ...
Positive sequence undervoltage protection (PSPTUV) main settings	
Start value	PSPTUV: Range 0.010 ... 1.200 x U_n, Step 0.001
Operate delay time	PSPTUV: Range 40 ... 120000ms, Step 10
Voltage block value	PSPTUV: Range 0.01 ... 1.0 x U_n, Step 0.01
Negative sequence overvoltage protection (NSPTOV)	
Operating accuracy	Depending on the frequency of the voltage measured f_n ±2Hz, ±1.5% of the set value or ±0.002 x U_n
Start time	U_{Fault} = 1.1 x set start value Minimum 33ms, Typical 35ms, Maximum 37ms U_{Fault} = 2.0 x set start value Minimum 24ms, Typical 26ms, Maximum 28ms
Reset time	<40ms
Reset ratio	Typical 0.96
Retardation time	<35ms
Operating time accuracy in definite time mode	±1.0% of the set value or ±20ms
Suppression of harmonics	DFT: -50dB at f = n x f_n, where n = 2, 3, 4, 5, ...
Negative sequence overvoltage protection (NSPTOV) main settings	
Start value	NSPTOV: Range 0.010 ... 1.000 x U_n, Step 0.001
Operate delay time	NSPTOV: Range 40 ... 120000ms, Step 1
Residual overvoltage protection (ROVPTOV)	
Operating accuracy	Depending on the frequency of the voltage measured f_n ±2Hz, ±1.5% of the set value or ±0.002 x U_n
Start time	U_{Fault} = 1.1 x set start value Minimum 29ms, Typical 31ms, Maximum 32ms
Reset time	<40ms
Reset ratio	Typical 0.96
Retardation time	<35ms
Operating time accuracy in definite time mode	±1.0% of the set value or ±20ms
Suppression of harmonics	DFT: -50dB at f = n x f_n, where n = 2, 3, 4, 5, ...
Residual overvoltage protection (ROVPTOV) main settings	
Start value	ROVPTOV: Range 0.010 ... 1.000 x U_n, Step 0.001
Operate delay time	ROVPTOV: Range 40 ... 300000ms, Step 1
Negative phase-sequence overcurrent protection (NSPTOC)	

Operating accuracy	Depending on the frequency of the current measured f_n ±2Hz, ±1.5% of the set value or ±0.002 x I_n
Start time	U_{Fault} = 2 x set start value Minimum 22ms, Typical 24ms, Maximum 25ms U_{Fault} = 10 x set start value Minimum 14ms, Typical 16ms, Maximum 17ms
Reset time	<40ms
Reset ratio	Typical 0.96
Retardation time	<35ms
Operating time accuracy in definite time mode	±1.0% of the set value or ±20ms
Operate time accuracy in inverse time mode	±5.0% of the theoretical value or ±20ms
Negative phase-sequence overcurrent protection (NSPTOC) main settings	
Start value	NSPTOC: Range 0.01 ... 5.00 x I_n, Step 0.01
Time multiplier	NSPTOC: Range 0.05 ... 15.00, Step 0.05
Operate delay time	NSPTOC: Range 40 ... 200000ms, Step 10
Circuit breaker failure protection (CCBRBRF)	
Operation accuracy	Depending on the frequency of the current measured f_n ±2Hz, ±1.5% of the set value or ±0.002 x I_n
Operate time accuracy	±1.0% of the set value or ±20ms
Circuit breaker failure protection (CCBRBRF) main settings	
Current value (Operating phase current)	CCBRBRF: Range 0.05 ... 1.00 x I_n, Step 0.05
Current value Res (Operating residual current)	CCBRBRF: Range 0.05 ... 1.00 x I_n, Step 0.05
CB failure mode (Operating mode of function)	CCBRBRF: 1=Current, 2=Breaker status, 3=Both
CB fail trip mode	CCBRBRF: 1=Off, 2=Without check, 3=Current check
Retrip time	CCBRBRF: Range 0 ... 60000ms, Step 10
CB failure delay	CCBRBRF: Range 0 ... 60000ms, Step 10
CB fault delay	CCBRBRF: Range 0 ... 60000ms, Step 10
Three-phase thermal overload (T1PTTR)	
Operation accuracy	Depending on t he frequency of the current measured f_n ±2Hz, Current measurement ±1.5% of the set value or ±0.002 x I_n (at currents in the range of 0.01 ... 4.00 x I_n)
Operate time accuracy	±2.0% of the theoretical value or ±0.50s
Three-phase thermal overload (T1PTTR) main settings	
Env temperature Set (Ambient temperature used when the AmbSens is set to Off)	T1PTTR: Range -50 ... 100ºC, Step 1
Current multiplier (Current multiplier when function is used for parallel lines)	T1PTTR: Range 1 ... 5, Step 1
Current reference	T1PTTR: Range 0.05 ... 4.00 x I_n, Step 0.01
Temperature rise (End temperature rise above ambient)	T1PTTR: Range 0.0 ... 200ºC, Step 0.1
Time constant (Time constant of the line in seconds)	T1PTTR: Range 60 ... 60000s, Step 1
Maximum temperature (temperature level for operate)	T1PTTR: Range 20 ... 200ºC, Step 0.1
AAlarm value (Temperature level for start (alarm))	T1PTTR: Range 20 ... 150ºC, Step 0.1
Reclose temperature (Temperature for reset of block reclose after operate)	T1PTTR: Range 20 ... 150ºC, Step 0.1
Initial temperature (Temperature raise above ambient temperature at startup)	T1PTTR: Range -50 ... 100ºC, Step 0.1
Three-phase inrush current detection (INRPHAR)	
Operation accuracy	At the frequency f=f_n Current measurement ±1.5% of the set value or ±0.002 x I_n Ratio I2f/I1f measurement ±5.0% of the set value
Reset time	+35ms / -0ms
Reset ratio	Typical 0.96
Operate time accuracy	+35ms / -0ms
Arc protection (ARCSARC)	
Operation accuracy	±3% of the set value or ±0.01 x I_n
Operate time	Operation mode (Light+current): Min 9ms, Typ 12ms, Max 15ms Operation mode (Light only): Min 9ms, Typ 10ms, Max 12ms
Reset time	<40ms
Reset ratio	Typical 0.96
Arc protection (ARCSARC) main settings	
Phase start value (Operating phase current)	ARCSARC: Range 0.50 ... 40.00 x I_n, Step 0.01
Ground start value (Operating residual current)	ARCSARC: Range 0.05 ... 8.00 x I_n, Step 0.01
Operation mode	ARCSARC: 1=Light+current, 2=Light only, 3=BI controlled
Autoreclosure (DARREC)	
Operate time accuracy	±1.0% of the set value or ±20ms
Three-pole current measurement (CMMXU)	

Operation accuracy	Depending on the frequency of the current measured f_n ±2Hz, ±0.5% or ±0.002 x I_n (at currents in the range of 0.01 ... 4.00 x I_n)
Suppression of harmonics	DFT: -50dB at f = n x f_n, where n = 2, 3, 4, 5, ... RMS: No suppression
Current sequence components (CSMSQI)	
Operation accuracy	Depending on the frequency of the current measured f/f_n = ±2Hz, ±1.0% or ±0.002 x I_n (at currents in the range of 0.01 ... 4.00 x I_n)
Suppression of harmonics	DFT: -50dB at f = n x f_n, where n = 2, 3, 4, 5, ...
Three-phase voltage measurement (VMMXU)	
Operation accuracy	Depending on the frequency of the current measured f_n ±2Hz at voltages in the range of 0.01 ... 1.15 x U_n
Suppression of harmonics	DFT: -50dB at f = n x f_n, where n = 2, 3, 4, 5, ... RMS: No suppression

A.2.4 P145 Feeder Management Relay

The P145 is a feeder management relay designed for a wide-range of overhead distribution and transmission voltage levels. It has 10 function keys offering operator control for applications such as auto-reclose, breaker failure and remote communications. The P145 incorporates a series of non-protection features in order to aid with power systems diagnosis and fault analysis. Figure A.16 depicts the P145.

Figure A.16: P145 relay

Figure A.17 and Table A.6 represent the functional overview and protection functions.

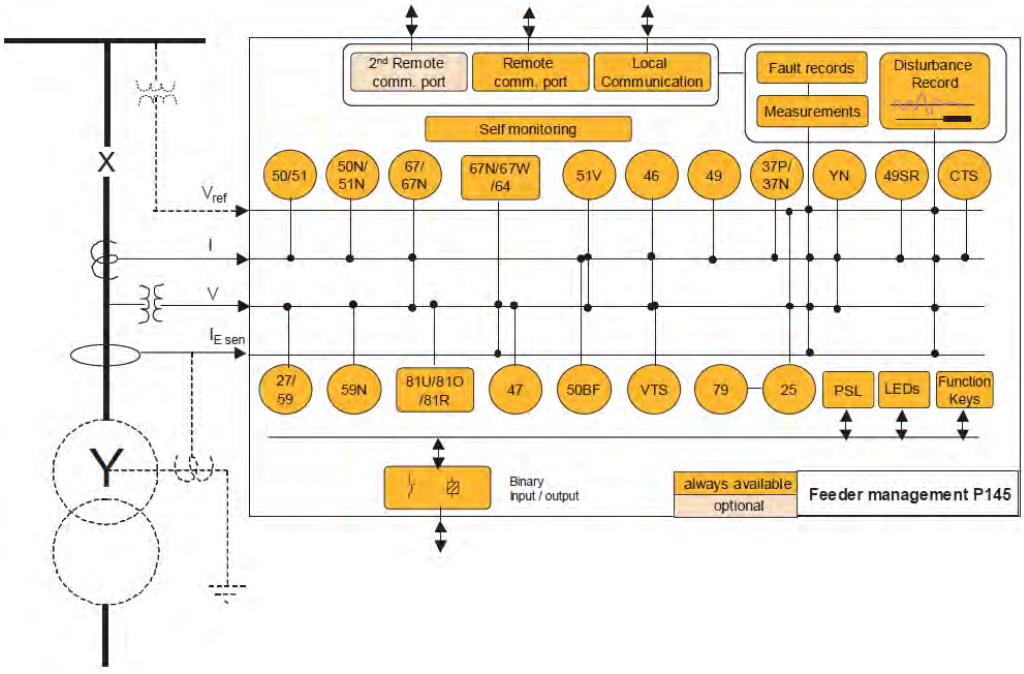


Figure A.17: Functional overview

Table A.6: Protection functions

ANSI Device Number	Description
50/51/67	Six overcurrent measuring stages are provided for each phase and are selectable to be either non-directional, directional forward or directional reverse. Stages 1, 2 and 5 may be set Inverse Definite Minimum Time (IDMT) or Definite Time (DT); stages 3, 4 and 6 may be set DT only.
50N/51N/67N	Three independent earth fault elements are provided for sensitive earth fault protection. Each element is equipped with four stages which are independently selectable to be either non-directional, directional forward or directional reverse. Either zero sequence or negative sequence polarising are available for the earth fault elements.
67N/67W	The Sensitive Earth Fault element can be configured as an Icosϕ, Isinϕ or VIcosϕ (Wattmetric) element for application to isolated and compensated networks.
51V	Voltage controlled overcurrent functionality is available on the first two stages of the overcurrent function. It provides backup protection for remote phase to phase faults by increasing the sensitivity of stages 1 and 2 of the overcurrent protection.
YN	Neutral admittance protection - operates from the SEF CT or EF CT to provide single stage admittance, conductance and susceptance elements.
64	Restricted earthfault is configurable as a high impedance or low impedance element.
BOL	Blocked overcurrent logic is available on each stage of the overcurrent and earth fault including sensitive earth fault elements. This consists of start outputs and block inputs that can be used to implement busbar blocking schemes.
SOL	Selective overcurrent provides the capability of temporarily altering (i.e. raising) the time settings of stages 3 and 4 of the phase overcurrent, earth fault and sensitive earth fault elements.
CLP	Cold load pick-up may be used to transiently raise the settings, for both overcurrent and earth fault protection elements, following closure of the circuit breaker.
46	Four stages are provided and can be selected to be either non-directional, directional forward or directional reverse and provides remote backup protection for both phase to earth and phase to phase faults.
49	RMS thermal overload (single/dual time constant) protection that provides thermal characteristics, which is suitable for both cables and transformers. Both Alarm and trip stages are provided.
37P/37N	Phase, neutral and sensitive earth fault undercurrent elements are available with the circuit breaker fail function.
27	Undervoltage 2-stage element, configurable as phase-to-phase or phase-to-neutral measuring. Stage 1 may be selected as either IDMT or DT and stage 2 is DT only.
59	Overvoltage 2-stage element, configurable as either phase-to-phase or phase-to-neutral measuring. Stage 1 may be selected as either IDMT or DT and stage 2 is DT only.
59N	Residual overvoltage (Neutral displacement) is a two-stage element selectable as either IDMT or DT.
47	Negative sequence overvoltage protection with a definite time delayed element to provide tripping or interlocking upon detection of unbalanced supply voltages.
81U/O/R	A 4-stage underfrequency and 2-stage overfrequency.
81U/O (Adv)	9-stage underfrequency and 9-stage overfrequency (advanced).
81R (Adv)	9-stage advanced rate of change of frequency element (df/dt) (advanced).
81RF (Adv)	9-stage frequency supervised rate of change of frequency element (f+df/dt) (advanced).
81RAV (Adv)	9-stage average rate of frequency (f + ΔF/Δt) (advanced).
46BC	Broken conductor (open jumper) used to detect open circuit faults using the ratio of I2/I1.
32R/32L/32O	Phase segregated under/over power protection. Two stages of power protection are provided and each stage can be independently configured to operate as over power or under power and forward or reverse direction. The relay provided a standard 3-phase power protection element and also a single-phase power protection element.
50BF	A 2-stage circuit breaker failure with 1 or 3 pole initiation inputs.
VTS	Voltage transformer supervision (1, 2 & 3 phase fuse failure detection) to prevent mal-operation of voltage dependent protection elements upon loss of a VT input signal.
CTS	Current transformer supervision to prevent mal-operation of current dependent protection elements upon loss of a CT input signal.
49SR	Silicon rectifier overload protection.
79	4 shot three pole auto-reclose with check sync., external initiation and sequence co-ordination capability.
25	Check synchronising (2-stage) with advanced system spilt features and breaker closing compensation time.

Figure A.18 illustrates the mounting dimensions.

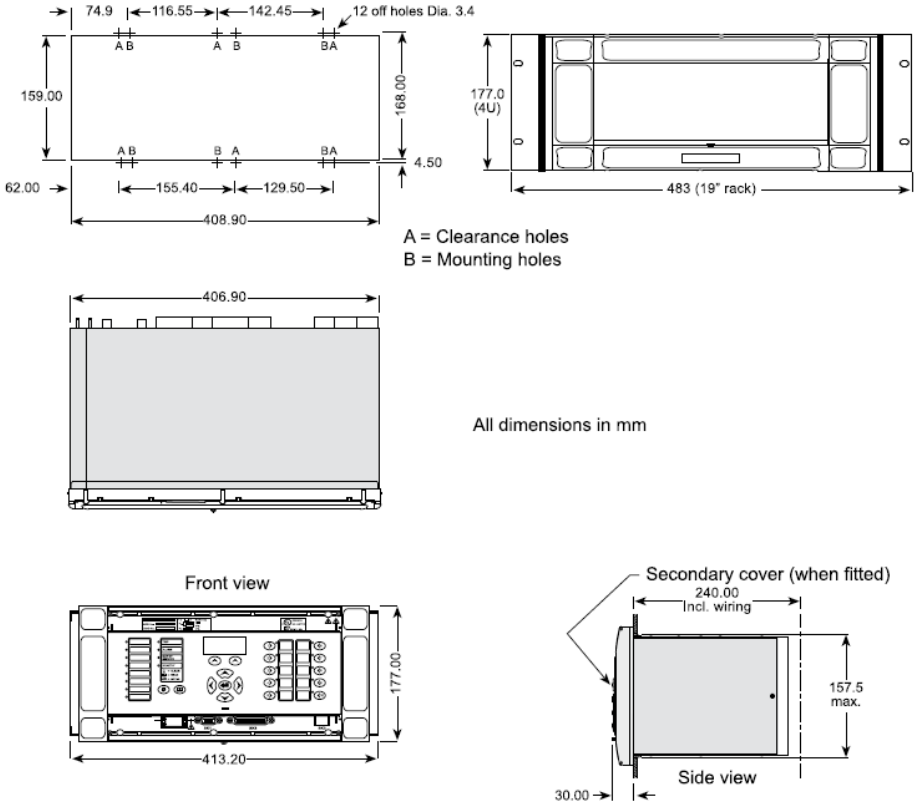


Figure A.18: Mounting dimensions

Table A.7 lists the technical data of the relay.

Table A.7: Technical data

Mechanical Specifications	
Design	Mounting is front of panel flush mounting, or 19“ rack.
Weight	9.2 kg
Terminals	
AC Current and Voltage Measuring Inputs	Located on heavy duty (black) terminal block: Threaded M4 terminals, for ring lug connection. CT inputs have integral safety shorting, upon removal of the terminal block.
General Input/Output Terminals	For power supply, opto inputs, output contacts and COM1 rear communications. Located on general purpose (grey) blocks: Threaded M4 terminals, for ring lug connection.
Case Protective Earth Connection	Two rear stud connections, threaded M4. Must be earthed (grounded) for safety, minimum earth wire size 2.5mm^2.
Front Port Serial PC Interface	EIA(RS)232 DTE, 9 pin D-type female connector. Courier protocol for interface to MiCOM S1software. Isolation to ELV level. Maximum cable length 15m.
Front Download/Monitor Port	EIA(RS)232, 25 pin D-type female connector. For firmware downloads. Isolation to ELV level.
Rear Communications Port	EIA(RS)485 signal levels, two wire connections located on general purpose block, M4 screw. For screened twisted pair cable, multi-drop, 1000m max. For K-Bus, IEC-870-5-103, or DNP3 protocol. Isolation to SELV level.
Optional Second Rear Communications Port	EIA(RS)232, 9 pin D-type female connector, socket SK4. Courier protocol: K-Bus, EIA(RS)232, or EIA(RS)485 connection. Isolation to SELV level.
Optional Rear IRIG-B Interface modulated or un-modulated	BNC socket. Isolation to SELV level. 50 ohm coaxial cable.
Optional Rear Fibre Connection for SCADA/DCS	BFOC 2.5 - interface for glass fibre, as per IEC 874-10. 850nm short-haul fibre, one Tx and one Rx. For Courier, IEC-870-5-103, DNP3 or MODBUS protocol.
10BaseT/100BaseTX Communications	Interface in accordance with IEEE802.3 and IEC61850. Isolation: 1.5kV Connector type: RJ45

	Cable type: Screened Twisted Pair (STP)
100 Base FX Interface	Interface in accordance with IEEE802.3 and IEC61850. Wavelength: 1300nm Fibre: multi-mode 50/125µm or 62.5/125µm Connector style: BFOC 2.5
Ratings	
AC Measuring Inputs	Nominal frequency: 50 and 60 Hz Operating range: 45 to 65Hz Phase rotation: ABC
AC Current	Nominal current (In): 1 and 5 A dual rated. (1A and 5A inputs use different transformer tap connections, check correct terminals are wired). Nominal burden per phase: < 0.15 VA at In Thermal withstand: continuous 4 In, for 10s: 30 In, for 1s; 100 In Linear to 64 In (non-offset AC current).
AC Voltage	Nominal voltage (Vn): 100 to 120 V or 380 to 480V phase-phase (min. 196 Vac, max. 560 Vac). Nominal burden per phase: < 0.02 VA at Vn. Thermal withstand: continuous 2 Vn, for 10s: 2.6 Vn
Power Supply	
Auxiliary Voltage (Vx)	Vx: 24 to 48 Vdc; 48 to 110 Vdc, and 40 to100Vac (rms); 110 to 250 Vdc, and 100 to 240Vac (rms)
Operating Range	19 to 65V (dc only); 37 to 150V (dc), 32 to 110V (ac); 87 to 300V (dc), 80 to 265V (ac). With a tolerable ac ripple of up to 12% for a dc supply, per IEC 60255-11: 1979.
Nominal Burden	Quiescent burden: 11W. (Extra 1.25W when fitted with second rear courier). Additions for energised binary inputs/outputs: Per opto input: 0.09W (24 to 54V), 0.12W (110/125V), 0.19W (220/120V). Per energised output relay: 0.13W
Power-up Time	Time to power up <11s.
Power Supply Interruption	Per IEC 60255-11: 1979 The relay will withstand a 20ms interruption in the DC auxiliary supply, without de-energising. Per IEC 61000-4-11: 1994 The relay will withstand a 20ms interruption in an AC auxiliary supply, without de-energising.
Battery Backup	Front panel mounted Type ½ AA, 3.6V (SAFT advanced battery reference LS14250) Battery life (assuming relay energised for 90% time) >10 years
Field Voltage Output	Regulated 48Vdc Current limited at 112mA maximum output
Digital (“Opto”) Inputs	Universal opto inputs with programmable voltage thresholds (24/27, 30/34, 48/54, 110/125, 220/250V). May be energised from the 48V field voltage, or the external battery supply. Rated nominal voltage: 24 to 250Vdc Operating range: 19 to 265Vdc Withstand: 300Vdc, 300Vrms. Peak current of opto input when energized is 3.5mA (0-300V)
Output Contacts	
Standard Contacts	General purpose relay outputs for signalling, tripping and alarming: Continuous Carry Ratings (Not Switched): Maximum continuous current: 10A (UL: 8A) Short duration withstand carry: 30A for 3s, 250A for 30ms Rated voltage: 300 V Make & Break Capacity: DC: 50W resistive, DC: 62.5W inductive (L/R = 50ms), AC: 2500VA resistive (cos ϕ = unity) AC: 2500VA inductive (cos ϕ = 0.7) Make, Carry: 30A for 3 secs, dc resistive, 10,000 operations (subject to the above limits of make/break capacity and rated voltage) Make, Carry & Break: 30A for 200ms, ac resistive, 2,000 operations (subject to the above limits of make/break capacity & rated voltage) 4A for 1.5 secs, dc resistive, 10,000 operations (subject to the above limits of make/break capacity & rated voltage) 0.5A for 1 sec, dc inductive, 10,000 operations (subject to the above limits of make/break capacity & rated voltage) 10A for 1.5 secs, ac resistive/inductive, 10,000 operations (subject to the above limits of make/break capacity & rated voltage) Durability: Loaded contact: 10 000 operations minimum Unloaded contact: 100 000 operations minimum

	Operate Time: Less than 5ms Reset Time: Less than 5ms
High Break Contacts	Continuous Carry Ratings (Not Switched): Maximum continuous current: 10A Short duration withstand carry: 30A for 3s, 250A for 30ms Rated voltage: 300 V Make & Break Capacity: DC: 7500W resistive DC: 2500W inductive (L/R = 50ms) Make, Carry: 30A for 3 secs, dc resistive, 10,000 operations (subject to the above limits of make/break capacity & rated voltage) Make, Carry & Break: 30A for 3 secs, dc resistive, 5,000 operations (subject to the above limits of make/break capacity & rated voltage) 30A for 200 ms, dc resistive, 10,000 operations (subject to the above limits of make/break capacity & rated voltage) 10A (*), dc inductive, 10,000 operations (subject to the above limits of make/break capacity & rated voltage) Durability: Loaded contact: 10 000 operations minimum Unloaded contact: 100 000 operations minimum Operate Time: Less than 0.2ms Reset Time: Less than 8ms
Watchdog Contacts	Non-programmable contacts for relay healthy/relay fail indication. Breaking capacity: DC: 30W resistive DC: 15W inductive (L/R = 40ms) AC: 375VA inductive (cos ϕ = 0.7)
IRIG-B 12X Interface Modulated	External clock synchronization per IRIG standard 200-98, format B12X. Input impedance 6kΩ at 1000Hz Modulation ratio: 3:1 to 6:1 Input signal, peak-peak: 200mV to 20V
IRIG-B 00X Interface Un-modulated	External clock synchronization per IRIG standard 200-98, format B00X. Input signal TTL level Input impedance at dc 10kΩ
Three-phase overcurrent Protection	
Accuracy	Additional tolerance X/R ratios: ±5% over X/R 1…90 Overshoot: <30ms
Inverse Time Characteristic	
Accuracy	DT Pick-up: Setting ±5% Minimum IDMT trip level: 1.05 x setting ±5% Drop-off: 0.95 x setting ±5% IDMT shape: ±5% or 40ms whichever is greater IEEE reset: ±5% or 50ms whichever is greater DT operation: ±2% or 50ms, whichever is greater DT reset: ±5% Directional boundary (RCA ±90%): ±2% hysteresis
Earth/Sensitive Fault Protection	
Earth Fault 1	DT Pick-up: Setting ±5% Minimum IDMT trip level: 1.05 x Setting ±5% Drop-off: 0.95 x Setting ±5% IDMT shape: ±5% or 40ms whichever is greater IEEE reset: ±5% or 50ms whichever is greater DT operation: ±2% or 50ms whichever is greater DT reset: ±5% Repeatability: 2.5%
Earth Fault 2	DT Pick-up: Setting ±5% Minimum IDMT Trip level: 1.05 x Setting ±5% Drop-off: 0.95 x Setting ±5% IDMT shape: ±5% or 40ms whichever is greater IEEE reset: ±10% or 40ms whichever is greater DT operation: ±2% or 50ms whichever is greater DT reset: ±2% or 50ms whichever is greater Repeatability: ±5%
SEF	DT Pick-up: Setting ±5% Minimum IDMT Trip level: 1.05 x Setting ±5% Drop-off: 0.95 x Setting ±5% IDMT shape: ±5% or 40ms whichever is greater IEEE reset: ±7.5% or 60ms whichever is greater DT operation: ±2% or 50ms whichever is greater DT reset: ±5% Repeatability: ±5%

REF	Pick-up: Setting formula ±5% Drop-off: 0.80 x setting formula ±5% Operating time: <60ms High pick up: Setting ±5% High operating time: <30ms Repeatability: <15%
Wattmetric SEF	Pick-up For P=0W ISEF> ±5% or P> ±5% Drop off: For P>0W (0.95 x ISEF>) ±5% or 0.9 x P> ±5% Boundary accuracy: ±5% with 1o hysteresis Repeatability: 5%
SEF Cos(PHI)	Pick-up: Setting ±5% for angles RCA±60 Drop-off: 0.90 x Setting IDMT shape: ±5% or 50ms whichever is greater IEEE reset: ±7.5% or 60ms whichever is greater DT operation: ±2% or 50ms whichever is greater DT reset: ±5% Repeatability: 2%
SEF Sin(PHI)	Pick-up: Setting ±5% for angles from RCA±60 to RCA±90 Drop-off: 0.90 x Setting IDMT shape: ±5% or 50ms whichever is greater IEEE reset: ±7.5% or 60ms whichever is greater DT operation: ±2% or 50ms whichever is greater DT reset: ±5% Repeatability: 2%
Zero Polarising	Operating pick-up: ±2%o of RCA ±90% Hysteresis: <3 VN > Pick-up: Setting ±10% VN > Drop-off: 0.9 x Setting ±10%
Negative Polarising	Operating Pick-up: ±2%o of RCA ±90% Hysteresis: <3 VN 2 > Pick-up: Setting ±10% VN 2 > Drop-off: 0.9 x Setting ±10% I2 > Pick up: Setting ±10% I2 > Drop-off: 0.9 x Setting ±10%
Negative Sequence Overcurrent	
Accuracy	DT Pick-up: Setting ±5% Minimum IDMT trip level: 1.05 x Setting ±5% Drop-off: 0.95 x Setting ±5% IDMT shape: ±5% or 40ms whichever is greater IEEE reset: ±5% or 50ms whichever is greater DT operation: ±2% or 50ms, whichever is greater DT reset: ±5% Directional boundary (RCA ±90%): ±2% hysteresis 2º
Reverse/Low Forward/Over Power Protection	
Accuracy	Pick-up: Setting ±10% Reverse/Over Power drop off: 0.95 x Setting ±10% Low forward Power drop off: 1.05xSetting+10% Angle variation pick-up: Expected pick-up angle ±2 degree Angle variation drop-off: Expected drop-off angle ±2.5 degree Operating time: ±2% or 50ms whichever is greater Repeatability: <5% Disengagement time: <50ms tRESET: ±5% Instantaneous operating time: < 50ms
Sensitive Reverse/Low Forward/Over Power (1 Phase)	
Accuracy	Pick-up: Setting ±10% Reverse/Over power Drop-off: 0.9 of setting ±10% Low forward power Drop-off: 1.1 of Setting ±10% Angle variation Pick-up: Expected pick-up angle ±2 degree Angle variation Drop-off: Expected drop-off angle ±2.5% degree Operating time: ±2% or 50ms whichever is greater Repeatability: <5% Disengagement time: <50ms tRESET: ±5% Instantaneous operating time: <50ms
Under Voltage Protection	
Accuracy	DT Pick-up: Setting ±5% IDMT Pick-up: Setting ±5% Drop-off: 1.02 x Setting ±5% IDMT shape: ±2% or 50ms whichever is greater DT operation: ±2% or 50ms whichever is greater

	Reset: <75ms Repeatability: <1%
Over Voltage Protection	
Accuracy	DT Pick-up: Setting ±5% IDMT Pick-up: Setting ±5% Drop-off: 0.98 x Setting ±5% IDMT shape: ±2% or 50ms whichever is greater DT operation: ±% or 50ms whichever is greater Reset: <75ms Repeatability: <1%
Rate of Change of Voltage (dv/dt) Protection	
Accuracy for 110V VT	Tolerance: 1% or 0.07, whichever is greater Pick-up: Setting ± tolerance Drop-off: (Setting - 0.07) ± tolerance for positive direction Drop-off: (Setting + 0.07) ± tolerance for negative direction Operating time at50Hz: [(Avg.cycle*20)+60]ms Reset time at 50Hz: 40ms
Neutral Displacement/Residual Voltage	
Accuracy	Pick-up: Setting ±5% or 1.05 x Setting ±5% Drop-off: 0.95 x Setting ±5% IDMT shape: ±5% or 65ms whichever is greater DT operation: ±2% or 20ms whichever is greater <55ms Reset: <35ms Repeatability: <10%
Under-frequency Protection	
Accuracy	Pick-up: Setting ±0.025Hz Drop-off: 1.05 x Setting ±0.025Hz DT operation: ±2% or 50ms whichever is greater
Over-frequency Protection	
Accuracy	Pick-up: Setting ±0.025Hz Drop-off: 0.95 x Setting ±0.025Hz DT operation: ±2% or 50ms whichever is greater

Table A.8 demonstrates digital data bus (DDB) signals for the Programmable Scheme Logic (PSL) editor.

Table A.8: DDB logical nodes

DDB No.	Text	Source	Description
0	Output Label 1 (Setting)	Output Conditioner	Output signal from output Relay 1 when activated
31	Output Label 32 (Setting)	Output Conditioner	Output signal from output Relay 32 when activated
32	Opto Label 1 (Setting)	Opto Input	From opto input 1 - when opto energized
63	Opto Label 32 (Setting)	Opto Input	From opto input 32 - when opto energized
64 - 71			Unused
72	Relay Cond. 1	PSL	Input to Relay Output Conditioner
73	Relay Cond. 2	PSL	Input to Relay Output Conditioner
74	Any Trip	PSL	Input to Relay Output Conditioner
75	Relay Cond. 4	PSL	Input to Relay Output Conditioner
103	Relay Cond. 4	PSL	Input to Relay Output Conditioner
104 - 111			Unused
112	Timer in 1	PSL	Input to Auxiliary Timer 1
127	Timer in 16	PSL	Input to Auxiliary Timer 16
128	Timer out 1	Auxiliary Timer	Output from Auxiliary Timer 1
129 - 242	Timer out 2 …15	Auxiliary Timer	Output from Auxiliary Timer 2 …15
143	Timer out 16	Auxiliary Timer	Output from Auxiliary Timer 16
144	Fault REC TRIG	PSL	Input Trigger for Fault Recorder
145	SG-opto Invalid	Group Selection	Setting group selection opto inputs have detected an invalid (disabled) settings group
146	Prot'n. Disabled	Commissioning Test	Protection disabled - typically out of service due to test mode
147	F out of Range	Frequency Tracking	Frequency Out of Range Alarm
148	VT Fail Alarm	VT Supervision	VTS Indication alarm- failed VT (fuse blow) detected by VT supervision
149	CT Fail Alarm	CT Supervision	CTS Indication Alarm (CT supervision alarm)
150	CB Fail Alarm	CB Fail	Circuit Breaker Fail Alarm
151	I^ Maint. Alarm	CB Monitoring	Broken Current Maintenance Alarm - circuit breaker cumulative duty alarm set-point
152	I^ Lockout Alarm	CB Monitoring	Broken Current Lockout Alarm - circuit breaker

			cumulative duty has been exceeded
153	CB Ops Maint.	CB Monitoring	No of Circuit Breaker Operations Maintenance Alarm - indicated due to circuit breaker trip operations threshold
154	CB Ops Lockout	CB Monitoring	No of Circuit Breaker Operations Maintenance Lockout - excessive number of circuit breaker trip operations, safety lockout
155	CB Op Time Maint.	CB Monitoring	Excessive Circuit Breaker Operating Time Maintenance Alarm - excessive operation time alarm for the circuit breaker (slow interruption time)
156	CB Op Time Lock	CB Monitoring	Excessive Circuit Breaker Operating Time Lockout Alarm - excessive operation time alarm for the circuit breaker (too slow interruption)
157	Fault Freq. Lock	CB Monitoring	Excessive fault frequency Lockout Alarm
158	CB Status Alarm	CB Status	Indication of problems by Circuit Breaker state monitoring - example defective auxiliary contacts
159	Man CB Trip Fail	CB Status	Circuit Breaker Failed to Trip (after a manual/ operator trip command)
160	Man CB Cls. Fail	CB Status	Circuit Breaker Failed to Close (after a manual/operator or auto-reclose close command)
161	Man CB Unhealthy	CB Status	Manual Circuit Breaker Unhealthy Output signal indicating that the circuit breaker has not closed successfully after a manual close command. (A successful close also requires The Circuit Breaker Healthy signal to reappear within the "healthy window" timeout)
162	Man No Check Sync.	CB Status	Indicates that the check synchronism signal has failed to appear for a manual close
163	AR Lockout	Auto-reclose	Indicates an Auto-reclose Lockout condition - no further auto-reclosures possible until resetting
164	AR CB Unhealthy	Auto-reclose	Auto-reclose Circuit Breaker unhealthy signal, output from auto-reclose logic. Indicates during auto-reclose in progress, if the Circuit Breaker has not become healthy within the Circuit Breaker Healthy time window
165	AR No Sys. Checks	Auto-reclose	Indicates during auto-reclose in progress, if system checks have not been satisfied within the Check Synchronizing time window
166	System Split	Check Sync.	System Split Alarm – will be raised if the system is split (remains permanently out of synchronism) for the duration of the system split timer
167	SR User Alarm 1	PSL	Triggers User Alarm 1 message to be alarmed on LCD display (self-resetting)
199	SR User Alarm 32	PSL	Triggers User Alarm 32 message to be alarmed on LCD display (self-resetting)
200	MR User Alarm 34	PSL	Triggers User Alarm 34 message to be alarmed on LCD display (manual-resetting)
202	MR User Alarm 36	PSL	Triggers User Alarm 36 message to be alarmed on LCD display (manual-resetting)
203	I>1 Timer Block	PSL	Block Phase Overcurrent Stage 1 Time Delay
204	I>2 Timer Block	PSL	Block Phase Overcurrent Stage 2 Time Delay
205	I>3 Timer Block	PSL	Block Phase Overcurrent Stage 3 Time Delay
206	I>4 Timer Block	PSL	Block Phase Overcurrent Stage 4 Time Delay
207			Unused
208	IN1>1 Timer Blk.	PSL	Block Earth Fault Measured Stage 1 Time Delay
209	IN1>2 Timer Blk.	PSL	Block Earth Fault Measured Stage 2 Time Delay
210	IN1>3 Timer Blk.	PSL	Block Earth Fault Measured Stage 3 Time Delay
211	IN1>4 Timer Blk.	PSL	Block Earth Fault Measured Stage 4 Time Delay
212	IN2>1 Timer Blk.	PSL	Block Earth Fault Derived Stage 1 Time Delay
213	IN2>2 Timer Blk.	PSL	Block Earth Fault Derived Stage 2 Time Delay
214	IN2>3 Timer Blk.	PSL	Block Earth Fault Derived Stage 3 Time Delay
215	IN2>4 Timer Blk.	PSL	Block Earth Fault Derived Stage 4 Time Delay
216	ISEF>1 Timer Blk.	PSL	Block Sensitive Earth Fault Stage 1 Time Delay
217	ISEF>2 Timer Blk.	PSL	Block Sensitive Earth Fault Stage 2 Time Delay
218	ISEF>3 Timer Blk.	PSL	Block Sensitive Earth Fault Stage 3 Time Delay
219	ISEF>4 Timer Blk.	PSL	Block Sensitive Earth Fault Stage 4 Time Delay
220	VN>1 Timer Blk.	PSL	Block Residual Overvoltage Stage 1 Time Delay
221	VN>2 Timer Blk.	PSL	Block Residual Overvoltage Stage 2 Time Delay
222	V<1 Timer Block	PSL	Block Phase Undervoltage Stage 1 Time Delay
223	V<2 Timer Block	PSL	Block Phase Undervoltage Stage 2 Time Delay
224	V>1 Timer Block	PSL	Block Phase Overvoltage Stage 1 Time Delay

225	V>2 Timer Block	PSL	Block Phase Overvoltage Stage 2 Time Delay
226	CLP Initiate	PSL	Initiate Cold Load Pickup
227	Ext. Trip 3ph	PSL	External Trip 3 phase - allows external protection to initiate breaker fail, circuit breaker condition monitoring statistics, and internal auto-reclose (if enabled)
228	CB Aux. 3ph(52-A)	PSL	52-A (CB closed)CB Auxiliary Input (3 phase)
229	CB Aux. 3ph(52-B)	PSL	52-B (CB open)CB Auxiliary Input (3 phase)
230	CB Healthy	PSL	Circuit Breaker Healthy (input to auto-recloser - that the CB has enough energy to allow re.closing)
231	MCB/VTS	PSL	VT supervision input - signal from external miniature Circuit Breaker showing MCB tripped
232	Init. Trip CB	PSL	Initiate tripping of circuit breaker from a manual Command
233	Init. Close CB	PSL	Initiate closing of Circuit Breaker from a manual Command
234	Reset Close Dly.	PSL	Reset Manual Circuit Breaker Close Time Delay
235	Reset Relays/LED	PSL	Reset Latched Relays & LEDs (manual reset of any lockout trip contacts, auto-reclose lockout, and LEDs)
236	Reset Thermal	PSL	Reset Thermal State to 0%
237	Reset Lockout	PSL	Manual control to reset auto-recloser from lockout
238	Reset CB Data	PSL	Reset Circuit Breaker Maintenance Values
239	Block A/R	PSL	Block the Auto-reclose function from an external input
240	Live Line Mode	PSL	Auto-reclose Live Line Mode Operation-switches the auto-reclose out of service and protection functions are not blocked. If DDB is active, the scheme is forced to Live Line Mode, irrespective of the Auto-reclose Mode Select setting and Auto Mode and Telecontrol input DDBs
241	Auto Mode	PSL	Auto-recloser Auto Mode Operation-switches the auto-reclose in service
242	Telecontrol Mode	PSL	Telecontrol Mode Operation selection-whereby the Auto and Non-Auto modes of auto-reclose can be selected remotely
243	I>1 Trip	Phase Overcurrent	1st Stage Overcurrent Trip 3ph
244	I>1 Trip A	Phase Overcurrent	1st Stage Overcurrent Trip A
245	I>1 Trip B	Phase Overcurrent	1st Stage Overcurrent Trip B
246	I>1 Trip C	Phase Overcurrent	1st Stage Overcurrent Trip C
247	I>2 Trip	Phase Overcurrent	2nd Stage Overcurrent Trip 3ph
248	I>2 Trip A	Phase Overcurrent	2nd Stage Overcurrent Trip A
249	I>2 Trip B	Phase Overcurrent	2nd Stage Overcurrent Trip B
250	I>2 Trip C	Phase Overcurrent	2nd Stage Overcurrent Trip C
251	I>3 Trip	Phase Overcurrent	3rd Stage Overcurrent Trip 3ph
252	I>3 Trip A	Phase Overcurrent	3rd Stage Overcurrent Trip A
253	I>3 Trip B	Phase Overcurrent	3rd Stage Overcurrent Trip B
254	I>3 Trip C	Phase Overcurrent	3rd Stage Overcurrent Trip C
255	I>4 Trip	Phase Overcurrent	4th Stage Overcurrent Trip 3ph
256	I>4 Trip A	Phase Overcurrent	4th Stage Overcurrent Trip A
257	I>4 Trip B	Phase Overcurrent	4th Stage Overcurrent Trip B
258	I>4 Trip C	Phase Overcurrent	4th Stage Overcurrent Trip C
259			Unused
260	Broken Line Trip	Broken Conductor	Broken Conductor Trip
261	IN1>1 Trip	Earth Fault 1	1st Stage Measured Earth Fault Trip
262	IN1>2 Trip	Earth Fault 1	2nd Stage Measured Earth Fault Trip
263	IN1>3 Trip	Earth Fault 1	3rd Stage Measured Earth Fault Trip
264	IN1>4 Trip	Earth Fault 1	4th Stage Measured Earth Fault Trip
265	IN2>1 Trip	Earth Fault 2	1st Stage Derived Earth Fault Trip
266	IN2>2 Trip	Earth Fault 2	2nd Stage Derived Earth Fault Trip
267	IN2>3 Trip	Earth Fault 2	3rd Stage Derived Earth Fault Trip
268	IN2>4 Trip	Earth Fault 2	4th Stage Derived Earth Fault Trip
269	ISEF>1 Trip	Sensitive Earth Fault	1st Stage Sensitive Earth Fault Trip
270	ISEF>2 Trip	Sensitive Earth Fault	2nd Stage Sensitive Earth Fault Trip
271	ISEF>3 Trip	Sensitive Earth Fault	3rd Stage Sensitive Earth Fault Trip
272	ISEF>4 Trip	Sensitive Earth Fault	4th Stage Sensitive Earth Fault Trip
273	IREF> Trip	Restricted Earth Fault	Restricted Earth Fault Trip
274	VN>1 Trip	Residual Overvoltage	1st Stage Residual Overvoltage Trip
275	VN>2 Trip	Residual Overvoltage	2nd Stage Residual Overvoltage Trip
276	Thermal Trip	Thermal Overload	Thermal Overload Trip

277	V2> Trip	Neg. Sequence O/V	Negative Sequence Overvoltage Trip
278	V<1 Trip	Undervoltage	1st Stage Phase Undervoltage Trip 3ph
279	V<1 Trip A/AB	Undervoltage	1st Stage Phase Undervoltage Trip A/AB
280	V<1 Trip B/BC	Undervoltage	1st Stage Phase Undervoltage Trip B/BC
281	V<1 Trip C/CA	Undervoltage	1st Stage Phase Undervoltage Trip C/CA
282	V<2 Trip	Undervoltage	2nd Stage Phase Undervoltage Trip 3ph
283	V<2 Trip A/AB	Undervoltage	2nd Stage Phase Undervoltage Trip A/AB
284	V<2 Trip B/BC	Undervoltage	2nd Stage Phase Undervoltage Trip B/BC
285	V<2 Trip C/CA	Undervoltage	2nd Stage Phase Undervoltage Trip C/CA
286	V>1 Trip	Overvoltage	1st Stage Phase Overvoltage Trip 3ph
287	V>1 Trip A/AB	Overvoltage	1st Stage Phase Overvoltage Trip A/AB
288	V>1 Trip B/BC	Overvoltage	1st Stage Phase Overvoltage Trip B/BC
289	V>1 Trip C/CA	Overvoltage	1st Stage Phase Overvoltage Trip C/CA
290	V>2 Trip	Overvoltage	2nd Stage Phase Overvoltage Trip 3ph
291	V>2 Trip A/AB	Overvoltage	2nd Stage Phase Overvoltage Trip A/AB
292	V>2 Trip B/BC	Overvoltage	2nd Stage Phase Overvoltage Trip B/BC
293	V>2 Trip C/CA	Overvoltage	2nd Stage Phase Overvoltage Trip C/CA
294	Any Start	All protection	Any Start
295	I>1 Start	Phase Overcurrent	1st Stage Overcurrent Start 3ph
296	I>1 Start A	Phase Overcurrent	1st Stage Overcurrent Start A
297	I>1 Start B	Phase Overcurrent	1st Stage Overcurrent Start B
298	I>1 Start C	Phase Overcurrent	1st Stage Overcurrent Start C
299	I>2 Start	Phase Overcurrent	2nd Stage Overcurrent Start 3ph
300	I>2 Start A	Phase Overcurrent	2nd Stage Overcurrent Start A
301	I>2 Start B	Phase Overcurrent	2nd Stage Overcurrent Start B
302	I>2 Start C	Phase Overcurrent	2nd Stage Overcurrent Start C
303	I>3 Start	Phase Overcurrent	3rd Stage Overcurrent Start 3ph
304	I>3 Start A	Phase Overcurrent	3rd Stage Overcurrent Start A
305	I>3 Start B	Phase Overcurrent	3rd Stage Overcurrent Start B
306	I>3 Start C	Phase Overcurrent	3rd Stage Overcurrent Start C
307	I>4 Start	Phase Overcurrent	4th Stage Overcurrent Start 3ph
308	I>4 Start A	Phase Overcurrent	4th Stage Overcurrent Start A
309	I>4 Start B	Phase Overcurrent	4th Stage Overcurrent Start B
310	I>4 Start C	Phase Overcurrent	4th Stage Overcurrent Start C
311	VCO Start AB	Voltage Controlled O/C	Voltage Controlled Overcurrent Start AB
312	VCO Start BC	Voltage Controlled O/C	Voltage Controlled Overcurrent Start BC
313	VCO Start CA	Voltage Controlled O/C	Voltage Controlled Overcurrent Start CA
314			Unused
315	IN1>1 Start	Earth Fault 1	1st Stage Measured Earth Fault Start
316	IN1>2 Start	Earth Fault 1	2nd Stage Measured Earth Fault Start
317	IN1>3 Start	Earth Fault 1	3rd Stage Measured Earth Fault Start
318	IN1>4 Start	Earth Fault 1	4th Stage Measured Earth Fault Start
319	IN2>1 Start	Earth Fault 2	1st Stage Derived Earth Fault Start
320	IN2>2 Start	Earth Fault 2	2nd Stage Derived Earth Fault Start
321	IN2>3 Start	Earth Fault 2	3rd Stage Derived Earth Fault Start
322	IN2>4 Start	Earth Fault 2	4th Stage Derived Earth Fault Start
323	ISEF>1 Start	Sensitive Earth Fault	1st Stage Sensitive Earth Fault Start
324	ISEF>2 Start	Sensitive Earth Fault	2nd Stage Sensitive Earth Fault Start
325	ISEF>3 Start	Sensitive Earth Fault	3rd Stage Sensitive Earth Fault Start
326	ISEF>4 Start	Sensitive Earth Fault	4th Stage Sensitive Earth Fault Start
327	VN>1 Start	Residual Overvoltage	1st Stage Residual Overvoltage Start
328	VN>2 Start	Residual Overvoltage	2nd Stage Residual Overvoltage Start
329	Thermal Alarm	Thermal Overload	Thermal Overload Alarm
330	V2> Start	Neg. Sequence O/V	Negative Sequence Overvoltage Start
331	V<1 Start	Undervoltage	1st Stage Phase Undervoltage Start 3ph
332	V<1 Start A/AB	Undervoltage	1st Stage Phase Undervoltage Start A/AB
333	V<1 Start B/BC	Undervoltage	1st Stage Phase Undervoltage Start B/BC
334	V<1 Start C/CA	Undervoltage	1st Stage Phase Undervoltage Start C/CA
335	V<2 Start	Undervoltage	2nd Stage Phase Undervoltage Start 3ph
336	V<2 Start A/AB	Undervoltage	2nd Stage Phase Undervoltage Start A/AB
337	V<2 Start B/BC	Undervoltage	2nd Stage Phase Undervoltage Start B/BC
338	V<2 Start C/CA	Undervoltage	2nd Stage Phase Undervoltage Start C/CA
339	V>1 Start	Overvoltage	1st Stage Phase Overvoltage Start 3ph
340	V>1 Start A/AB	Overvoltage	1st Stage Phase Overvoltage Start A/AB
341	V>1 Start B/BC	Overvoltage	1st Stage Phase Overvoltage Start B/BC
342	V>1 Start C/CA	Overvoltage	1st Stage Phase Overvoltage Start C/CA
343	V>2 Start	Overvoltage	2nd Stage Phase Overvoltage Start 3ph

344	V>2 Start A/AB	Overvoltage	2nd Stage Phase Overvoltage Start A/AB
345	V>2 Start B/BC	Overvoltage	2nd Stage Phase Overvoltage Start B/BC
346	V>2 Start C/CA	Overvoltage	2nd Stage Phase Overvoltage Start C/CA
347	CLP Operation	Cold Load Pickup	Indicates the Cold Load Pickup logic is in operation
348	I> BlockStart	CBF & POC	I> Blocked Overcurrent Start
349	IN/SEF>Blk Start	CBF & IN1/IN2/SEF	IN/ISEF> Blocked Overcurrent Start
350	VTS Fast Block	VT Supervision	VT Supervision Fast Block - blocks elements which would otherwise mal-operate immediately a fuse failure event occurs
351	VTS Slow Block	VT Supervision	VT Supervision Slow Block - blocks elements which would otherwise mal-operate some time after a fuse failure event occurs
352	CTS Block	CT Supervision	CT Supervision Block (current transformer supervision)
353	Bfail1 Trip 3ph	CB Fail	tBF1 Trip 3Ph - three phase output from circuit breaker failure logic, stage 1 timer
354	Bfail2 Trip 3ph	CB Fail	tBF2 Trip 3Ph - three phase output from circuit breaker failure logic, stage 2 timer
355	Control Trip	CB Control	Control Trip - operator trip instruction to the circuit breaker, via menu, or SCADA. (Does not operate for protection element trips)
356	Control Close	CB Control	Control Close command to the circuit breaker. Operates for a manual close command (menu, SCADA), and additionally is driven by the auto-reclose close command
357	Close in Prog.	CB Control	Control Close in Progress - the relay has been given an instruction to close the circuit breaker, but the Manual Close timer Delay has not yet finished timing out
358	Block Main Prot.	Auto-reclose	Auto-reclose block Main Protection during auto-reclose cycle. Can be used to block external protection via relay output contacts
359	Block SEF Prot.	Auto-reclose	Auto-reclose block Sensitive Earth Fault Protection during auto-reclose cycle. Can be used to block external protection via relay output contacts
360	AR In Progress	Auto-reclose	Auto-reclose In Progress
361	AR In Service	Auto-reclose	Auto-reclose In/Out of service - the auto-reclose function has been enabled either in the relay menu, or by an opto input
362	Seq. Counter = 0	Auto-reclose	Auto-reclose sequence counter is at zero - no previous faults have been cleared within recent history. The sequence count is at zero because no reclaim times are timing out, and the auto-recloser is not locked out. The recloser is awaiting the first protection trip, and all programmed cycles are free to follow
363	Seq. Counter = 1	Auto-reclose	The first fault trip has happened in a new auto-reclose sequence. Dead time 1, or reclaim time 1 are in the process of timing out
366	Seq. Counter = 4	Auto-reclose	Auto-reclose sequence counter is at 4. This means that the initial fault trip happened, and then 3 trips followed, moving the counter on to 4
367	Successful Close	Auto-reclose	Successful Re-closure indication. The circuit breaker was re-closed by the auto-reclose function, and stayed closed. This indication is raised at the expiry of the reclaim time
368	Dead T in Prog.	Auto-reclose	Indicates Dead Time in Progress
369	Protection Lockt.	Auto-reclose	Indicates a Protection Lockout of auto-reclose when the AR is set to Live Line or Non Auto mode
370	Reset Lckout Alm.	Auto-reclose	Auto-reclose Reset Lockout Alarm indication
371	Auto Close	Auto-reclose	Auto-reclose command to the circuit breaker
372	A/R Trip Test	Auto-reclose	Auto-reclose trip test which initiates an auto-reclose cycle
373	IA< Start	Undercurrent	A phase Undercurrent Start
374	IB< Start	Undercurrent	B phase Undercurrent Start
375	IC< Start	Undercurrent	C phase Undercurrent Start
376	IN< Start	Undercurrent	Earth Fault Undercurrent Start
377	ISEF< Start	Undercurrent	Sensitive Earth Fault Undercurrent Start
378	CB Open 3 ph	CB Status	Three phase Circuit breaker Open Status
379	CB Closed 3 ph	CB Status	Three phase Circuit breaker Closed Status
380	All Poles Dead	Poledead	Pole dead logic detects 3 phase breaker open Condition

381	Any Pole Dead	Poledead	Pole dead logic detects at least one breaker pole open
382	Pole Dead A	Poledead	Phase A Pole Dead
383	Pole Dead B	Poledead	Phase B Pole Dead
384	Pole Dead C	Poledead	Phase C Pole Dead
385	VTS Acc. Ind.	VT Supervision	Voltage Transformer Supervision Accelerate Indication signal form a fast tripping voltage dependent function used to accelerate indications when the indicate only option is selected
386	VTS Volt Dep.	VT Supervision input	Outputs from any function that utilizes the system voltage, if any of these elements operate before a VTS is detected, the VTS is blocked from operation. The outputs include starts and trips
387	VTS Ia>	VT Supervision	VTS A phase current level detector is over threshold
388	VTS Ib>	VT Supervision	VTS B phase current level detector is over threshold
389	VTS Ic>	VT Supervision	VTS C phase current level detector is over threshold
390	VTS Va>	VT Supervision	VTS A phase voltage level detector is over threshold
391	VTS Vb>	VT Supervision	VTS B phase voltage level detector is over threshold
392	VTS Vc>	VT Supervision	VTS C phase voltage level detector is over threshold
393	VTS I2>	VT Supervision	VTS negative sequence current level detector is over threshold
394	VTS V2>	VT Supervision	VTS negative sequence voltage level detector is over threshold
395	VTS Ia delta>	VT Supervision	Superimposed A phase current over threshold
396	VTS Ib delta>	VT Supervision	Superimposed B phase current over threshold
397	VTS Ic delta >	VT Supervision	Superimposed C phase current over threshold
398	CBF SEF Trip	Breaker Fail Fixed Logic	Internal signal for the Circuit Breaker Fail logic to indicate general Sensitive Earth Fault Trip condition
399	CBF Non I Trip	Breaker Fail Fixed Logic	Internal signal for the Circuit Breaker Fail logic to indicate general Non Current based Protection Trip
400	CBF SEF Trip-1	Breaker Fail Fixed Logic	Internal signal for the Circuit Breaker Fail logic to indicate a Sensitive Earth Fault Stage Trip condition
401	CBF Non I Trip-1	Breaker Fail Fixed Logic	Internal signal for the Circuit Breaker Fail logic to indicate Non Current Protection Stage Trip
402	Man Check Sync.	PSL	Input to the Circuit Breaker Control Logic to indicate manual check synchronization conditions are satisfied
403	AR SysChecks OK	PSL	Input to the auto-reclose logic to indicate auto-reclose check synchronization conditions are satisfied
404	Lockout Alarm	CB Monitoring	Composite Lockout Alarm
405	Pre-Lockout	CB Monitoring	Pre-Lockout Alarm indicates the auto-reclose will lockout on the next shot
406	Freq. High	Frequency Tracking	Frequency tracking detects frequency above the allowed range
407	Freq. Low	Frequency Tracking	Frequency tracking detects frequency below the allowed range
408	Stop Freq. Track	Fixed Logic	Stop Frequency Tracking signal - indicates under legitimate conditions when the relay suspends frequency tracking on the instruction of the protection elements
409	Start N	EF1/EF2/SEF/VN/YN	Composite Earth Fault Start
410	Field Volts Fail	Field Voltage Monitor	48V Field Voltage Failure
411	Freq. Not Found	Frequency Tracking	Frequency Not Found by the frequency tracking
412	F<1 Timer Block	PSL	Block Underfrequency Stage 1 Timer
413	F<2 Timer Block	PSL	Block Underfrequency Stage 2 Timer
414	F<3 Timer Block	PSL	Block Underfrequency Stage 3 Timer
415	F<4 Timer Block	PSL	Block Underfrequency Stage 4 Timer
416	F>1 Timer Block	PSL	Block Overfrequency Stage 1 Timer
417	F>2 Timer Block	PSL	Block Overfrequency Stage 2 Timer
418	F<1 Start	Frequency Protection	Under frequency Stage 1 Start
419	F<2 Start	Frequency Protection	Under frequency Stage 2 Start
420	F<3 Start	Frequency Protection	Under frequency Stage 3 Start
421	F<4 Start	Frequency Protection	Under frequency Stage 4 Start
422	F>1 Start	Frequency Protection	Over frequency Stage 1 Start
423	F>2 Start	Frequency Protection	Over frequency Stage 2 Start
424	F<1 Trip	Frequency Protection	Under frequency Stage 1 Trip
425	F<2 Trip	Frequency Protection	Under frequency Stage 2 Trip
426	F<3 Trip	Frequency Protection	Under frequency Stage 3 Trip
427	F<4 Trip	Frequency Protection	Under frequency Stage 4 Trip
428	F>1 Trip	Frequency Protection	Over frequency Stage 1 Trip

429	F>2 Trip	Frequency Protection	Over frequency Stage 2 Trip
430	YN> Timer Block	PSL	Block Overadmittance Timer
431	GN> Timer Block	PSL	Block Overconductance Timer
432	BN> Timer Block	PSL	Block Oversusceptance Timer
433	YN> Start	Admittance Protection	Overadmittance Start
434	GN> Start	Admittance Protection	Overconductance Start
435	BN> Start	Admittance Protection	Oversusceptance Start
436	YN> Trip	Admittance Protection	Overadmittance Trip
437	GN> Trip	Admittance Protection	Overconductance Trip
438	BN> Trip	Admittance Protection	Oversusceptance Trip
439	Ext. AR Prot. Trip	PSL	Initiate Auto-reclose from an external protection device trip
440	Ext. AR Prot. Strt.	PSL	Initiate Auto-reclose from an external protection device start
441	Test Mode	PSL	Initiate Test Mode which takes the relay out of service and allows secondary injection testing of the relay
442	Inhibit SEF	PSL	Inhibit Sensitive Earth Fault Protection - All Stages
443	Live Line	Voltage Monitors	Indicates Live Line condition is detected
444	Dead Line	Voltage Monitors	Indicates Dead Line condition is detected
445	Live Bus	Voltage Monitors	Indicates Live Bus condition is detected
446	Dead Bus	Voltage Monitors	Indicates Dead Bus condition is detected
447	Check Sync. 1 OK	Check Synchronization	Check Sync. Stage 1 OK
448	Check Sync. 2 OK	Check Synchronization	Check Sync. Stage 2 OK
449	SysChks Inactive	Check Synchronization	System Checks Inactive (output from the check synchronism, and other voltage checks)
450	CS1 Enabled	PSL	Check Sync. Stage 1 Enabled
451	CS2 Enabled	PSL	Check Sync. Stage 2 Enabled
452	SysSplit Enabled	PSL	System Split function Enabled
453	DAR Complete	PSL	Delayed Auto-reclose Complete
454	CB In Service	PSL	Circuit breaker is In Service
455	AR Restart	PSL	Auto-reclose Restart input to initiate an auto-reclose cycle irrespective of the normal AR interlock conditions
456	AR In Progress 1	Auto-reclose	Auto-reclose In Progress indication which is active during AR cycle and is reset by the ‘DAR Complete’ DDB if mapped or otherwise by the ‘AR in Progress’ DDB
457	DeadTime Enabled	PSL	Dead Time Enabled
458	DT OK To Start	PSL	Dead Time OK To Start input to the dead time initiation logic. Allows an interlock condition besides CB open and protection reset to ‘prime’ the dead time logic
459	DT Complete	Auto-reclose	Dead Time Complete indication and operates at the end of the set dead time period
460	Reclose Checks	Auto-reclose	Re-close Checks indicates the dead time logic is ‘primed’
461	Circuits OK	PSL	Input to the auto-reclose logic to indicate Live/Dead Circuit conditions are satisfied when AR with ‘Live/Dead Ccts’ is enabled
462	AR Sync. Check	Auto-reclose	Auto-reclose Check Synchronism OK (system checks passed)
463	AR SysChecksOK	Auto-reclose	Auto-reclose System Check OK conditions are confirmed by the system checks function
464	AR Init. TripTest	PSL	Initiates a trip and auto-reclose cycle and is usually mapped to an opto input
465	Monitor Block	PSL	For IEC-870-5-103 protocol only, used for "Monitor Blocking" (relay is quiet - issues no messages via SCADA port)
466	Command Block	PSL	For IEC-870-5-103 protocol only, used for "Command Blocking" (relay ignores SCADA commands)
467	ISEF>1 Start 2	Sensitive Earth Fault	1st Stage Sensitive Earth Fault second Start indication
468	ISEF>2 Start 2	Sensitive Earth Fault	2nd Stage Sensitive Earth Fault second Start Indication
469	ISEF>3 Start 2	Sensitive Earth Fault	3rd Stage Sensitive Earth Fault second Start Indication
470	ISEF>4 Start 2	Sensitive Earth Fault	4th Stage Sensitive Earth Fault second Start indication
471	CS1 Slipfreq.>	Check Synchronization	Operates when 1st Stage Check Sync. slip

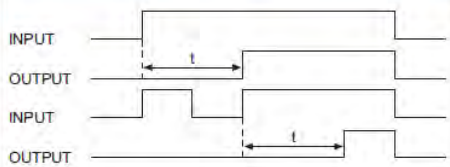
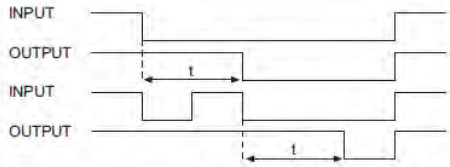
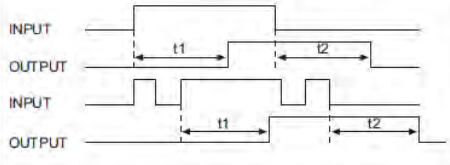
			frequency is above the Check Sync. 1 Slip Frequency setting
472	CS1 Slipfreq.<	Check Synchronization	Operates when 1st Stage Check Sync. slip frequency is below the Check Sync. 1 Slip Frequency setting
473	CS2 Slipfreq.>	Check Synchronization	Operates when 2nd Stage Check Sync. slip frequency is above the Check Sync. 2 Slip Frequency setting
474	CS2 Slipfreq.<	Check Synchronization	Operates when 2nd Stage Check Sync. slip frequency is below the Check Sync. 2 Slip Frequency setting
475	Time Sync.	PSL	Time Synchronism by Opto pulse
476	df/dt> Inhibit	PSL	Inhibit input for the Rate of change of Frequency function
477	df/dt>1 Tmr. Blk.	PSL	Block Rate of change of Frequency Stage 1Timer
478	df/dt>2 Tmr. Blk.	PSL	Block Rate of change of Frequency Stage 2 Timer
479	df/dt>3 Tmr. Blk.	PSL	Block Rate of change of Frequency Stage 3 Timer
480	df/dt>4 Tmr. Blk.	PSL	Block Rate of change of Frequency Stage 4 Timer
481	df/dt>1 Start	df/dt Protection	1st Stage Rate of change of Frequency Start indication
482	df/dt>2 Start	df/dt Protection	2nd Stage Rate of change of Frequency Start indication
483	df/dt>3 Start	df/dt Protection	3rd Stage Rate of change of Frequency Start indication
484	df/dt>4 Start	df/dt Protection	4th Stage Rate of change of Frequency Start indication
485	df/dt>1 Trip	df/dt Protection	1st Stage Rate of change of Frequency Trip
486	df/dt>2 Trip	df/dt Protection	2nd Stage Rate of change of Frequency Trip
487	df/dt>3 Trip	df/dt Protection	3rd Stage Rate of change of Frequency Trip
488	df/dt>4 Trip	df/dt Protection	4th Stage Rate of change of Frequency Trip
489	CS Vline<	Check Synchronization	Indicates the Line voltage is less than the Check Sync. undervoltage setting
490	CS Vbus<	Check Synchronization	Indicates the Bus voltage is less than the Check Sync. undervoltage setting
491	CS Vline>	Check Synchronization	Indicates the Line voltage is greater than the Check Sync. overvoltage setting
492	CS Vbus>	Check Synchronization	Indicates the Bus voltage is greater than the Check Sync. overvoltage setting
493	CS Vline>Vbus	Check Synchronization	Indicates that the Line voltage is greater than Bus voltage + Check Sync. differential voltage setting
494	CS Vline<Vbus	Check Synchronization	Indicates the Bus voltage is greater than Line voltage + Check Sync. differential voltage setting
495	CS1 Fline>Fbus	Check Synchronization	Indicates the Line frequency is greater than the Bus frequency + Check Sync. 1 Slip Frequency setting where Check Sync. 1 Slip Control is set to Frequency
496	CS1 Fline<Fbus	Check Synchronization	Indicates the Bus frequency is greater than Line frequency + Check Sync. 1 Slip Frequency setting where Check Sync. 1 Slip Control is set to Frequency
497	CS1 Ang. Not OK +	Check Synchronization	Indicates the Line angle leads the bus angle and falls in range + CS1 Phase Angle (deg.) to 180°
498	CS1 Ang. Not OK -	Check Synchronization	Indicates if the Line angle lags the bus angle and falls in range - CS1 Phase Angle (deg.) to -180°
499	External Trip A	PSL	External Trip A input
500	External Trip B	PSL	External Trip B input
501	External Trip C	PSL	External Trip C input
502	External Trip EF	PSL	External Trip Earth Fault input
503	External TripSEF	PSL	External Trip Sensitive Earth Fault input
504	I2> Inhibit	PSL	Inhibit all Negative Sequence Overcurrent stages
505	I2>1 Tmr. Blk.	PSL	Block Negative Sequence Overcurrent Stage 1Timer
506	I2>2 Tmr. Blk.	PSL	Block Negative Sequence Overcurrent Stage 2 Timer
507	I2>3 Tmr. Blk.	PSL	Block Negative Sequence Overcurrent Stage 3 Timer
508	I2>4 Tmr. Blk.	PSL	Block Negative Sequence Overcurrent Stage 4 Timer
509	I2>1 Start	Neg. Sequence O/C	1st Stage Negative Sequence Overcurrent Start
510	I2>2 Start	Neg. Sequence O/C	2nd Stage Negative Sequence Overcurrent Start
511	I2>3 Start	Neg. Sequence O/C	3rd Stage Negative Sequence Overcurrent Start
512	I2>4 Start	Neg. Sequence O/C	4th Stage Negative Sequence Overcurrent Start
513	I2>1 Trip	Neg. Sequence O/C	1st Stage Negative Sequence Overcurrent Trip

514	I2>2 Trip	Neg. Sequence O/C	2nd Stage Negative Sequence Overcurrent Trip
515	I2>3 Trip	Neg. Sequence O/C	3rd Stage Negative Sequence Overcurrent Trip
516	I2>4 Trip	Neg. Sequence O/C	4th Stage Negative Sequence Overcurrent Trip
517	V2> Accelerate	PSL	Input to Accelerate Negative Sequence Overvoltage (V2> Protection) instantaneous operating time
518	Trip LED	PSL	Input to Trigger Trip LED (other than Relay 3)
519	CS2 Fline>Fbus	Check Synchronization	Indicates the Line frequency is greater than the Bus Frequency + Check Sync. 2 Slip Frequency setting where Check Sync. 2 Slip Control is set to Frequency
520	CS2 Fline<Fbus	Check Synchronization	Indicates the Bus frequency is greater than Line Frequency + Check Sync. 2 Slip Frequency setting where Check Sync. 2 Slip Control is set to Frequency
521	CS2 Ang. Not OK +	Check Synchronization	Indicates the Line angle leads the bus angle and falls in range + Check Sync. 2 Phase Angle (deg.) to 180°
522	CS2 Ang. Not OK -	Check Synchronization	Indicates the Line angle lags the bus angle and falls in range - Check Sync. 2 Phase Angle (deg.) to -180°
523	CS Ang. Rot ACW	Check Synchronization	The direction of rotation of line angle, using bus as a reference, is anti-clockwise (ACW)
524	CS Ang. Rot CW	Check Synchronization	The direction of rotation of line angle, using bus as a reference, is clockwise (CW)
525	Blk. Rmt. CB Ops	PSL	Block Remote CB Trip/Close Commands
526	SG Select x1	PSL	Setting Group Selector X1 (low bit)-selects SG2 if only DDB 526 signal is active. SG1 is active if both DDB 526 & DDB 527=0 SG4 is active if both DDB 526 & DDB 527=1
527	SG Select 1x	PSL	Setting Group Selector 1X (high bit)-selects SG3 if only DDB 527 is active. SG1 is active if both DDB 526 & DDB 527=0 SG4 is active if both DDB 526 & DDB 527=1
528	IN1> Inhibit	PSL	Inhibit Earth Fault 1 Protection
529	IN2> Inhibit	PSL	Inhibit Earth Fault 2 Protection
530	AR Skip Shot 1	PSL	When active skips the first auto-reclose shot in an auto-reclose cycle
531	Logic 0 Ref.	Reference DDB Signal	Logic zero reference DDB signal
532 - 639	Unused		
640	LED1 Red	Output Conditioner	Programmable LED 1 Red is energized
641	LED1 Grn.	Output Conditioner	Programmable LED 1 Green is energized
654	LED8 Red	Output Conditioner	Programmable LED 8 Red is energized
655	LED8 Grn.	Output Conditioner	Programmable LED 8 Green is energized
656	FnKey LED1 Red	Output Conditioner	Programmable Function Key LED 1 Red is energized
657	FnKey LED1 Grn.	Output Conditioner	Programmable Function Key LED 1 Green is energized
674	FnKey LED10 Red	Output Conditioner	Programmable Function Key LED 10 Red is energized
675	FnKey LED10 Grn.	Output Conditioner	Programmable Function Key LED 10 Green is energized
676	LED1 Con R	PSL	Assignment of input signal to drive output LED 1Red
677	LED1 Con G	PSL	Assignment of signal to drive output LED 1Green.To drive LED1 Yellow DDB 676 and DDB 677 must be driven at the same time
690	LED8 Con R	PSL	Assignment of signal to drive output LED 8Red
691	LED8 Con G	PSL	Assignment of signal to drive output LED 8 Green. To drive LED8 Yellow DDB 690 and DDB 691 must be active at the same time
692	FnKey LED1 ConR	PSL	Assignment of signal to drive output Function Key LED 1 Red. This LED is associated with Function Key 1
693	FnKey LED1 ConG	PSL	Assignment of signal to drive output Function Key LED 1 Green. This LED is associated with Function Key 1. To drive function key LED, yellow DDB 692 and DDB 693 must be active at the same time
710	FnKey LED10 ConR	PSL	Assignment of signal to drive output Function Key LED 10 Red. This LED is associated with Function Key 10
711	FnKey LED10 ConG	PSL	Assignment of signal to drive output Function Key LED 10 Green. This LED is associated with Function Key 10. To drive function key LED1 yellow, DDB 710

			and DDB 711 must be active at the same time
712	Function Key 1	Function Key	Function Key 1 is activated. In 'Normal' mode it is high on keypress and in 'Toggle' mode remains high/low on single keypress
721	Function Key 10	Function Key	Function Key 10 is activated. In 'Normal' mode it is high on keypress and in 'Toggle' mode remains high/low on single keypress
722 - 768			Unused
800	Control Input 1	Control Input Command	Control Input 1 - for SCADA and menu commands into PSL
831	Control Input 32	Control Input Command	Control Input 32 - for SCADA and menu commands into PSL
832	Virtual Input 1	GOOSE Input Command	GOOSE Input 1 (reserved for future use when IEC61850 implemented)
833 - 862	Virtual Input 2-31	GOOSE Input Command	GOOSE Input 1 - allows binary signals that are mapped to virtual inputs to interface into PSL (reserved for future use when IEC61850 implemented)
863	Virtual Input 32	GOOSE Input Command	GOOSE Input 2-31 - allows binary signals that are mapped to virtual inputs to interface into PSL (reserved for future use when IEC61850 implemented)
864	Virtual Output 1	PSL	GOOSE Input 32 - allows binary signals that are mapped to virtual inputs to interface into PSL (reserved for future use when IEC61850 implemented)
865 - 894	Virtual Output 2 - 31	PSL	GOOSE Output 2 - 31 - output allows user to control a binary signal which can be mapped via SCADA protocol output to other devices
895	Virtual Output 32	PSL	GOOSE Output 32 - output allows user to control a binary signal which can be mapped via SCADA protocol output to other devices

Table A.9 and Table A.10 illustrate general logic gate and timer symbols.

Table A.9: Logic timers

Logic Symbols	Explanation	Time Chart
t / 0	Delay on pick-up timer, t	
0 / t	Delay on drop-off timer, t	
t1 / t2	Delay on pick-up/drop-off timer	

t	Pulse timer	INPUT OUTPUT t INPUT OUTPUT t
t	Pulse pick-up falling edge	INPUT OUTPUT t
t	Pulse pick-up raising edge	INPUT OUTPUT t
Latching	Latch	INPUT OUTPUT
Dwell / Timer	Dwell timer	INPUT OUTPUT t INPUT OUTPUT t
Straight	**Straight (non latching):** Hold value until input reset signal	INPUT OUTPUT

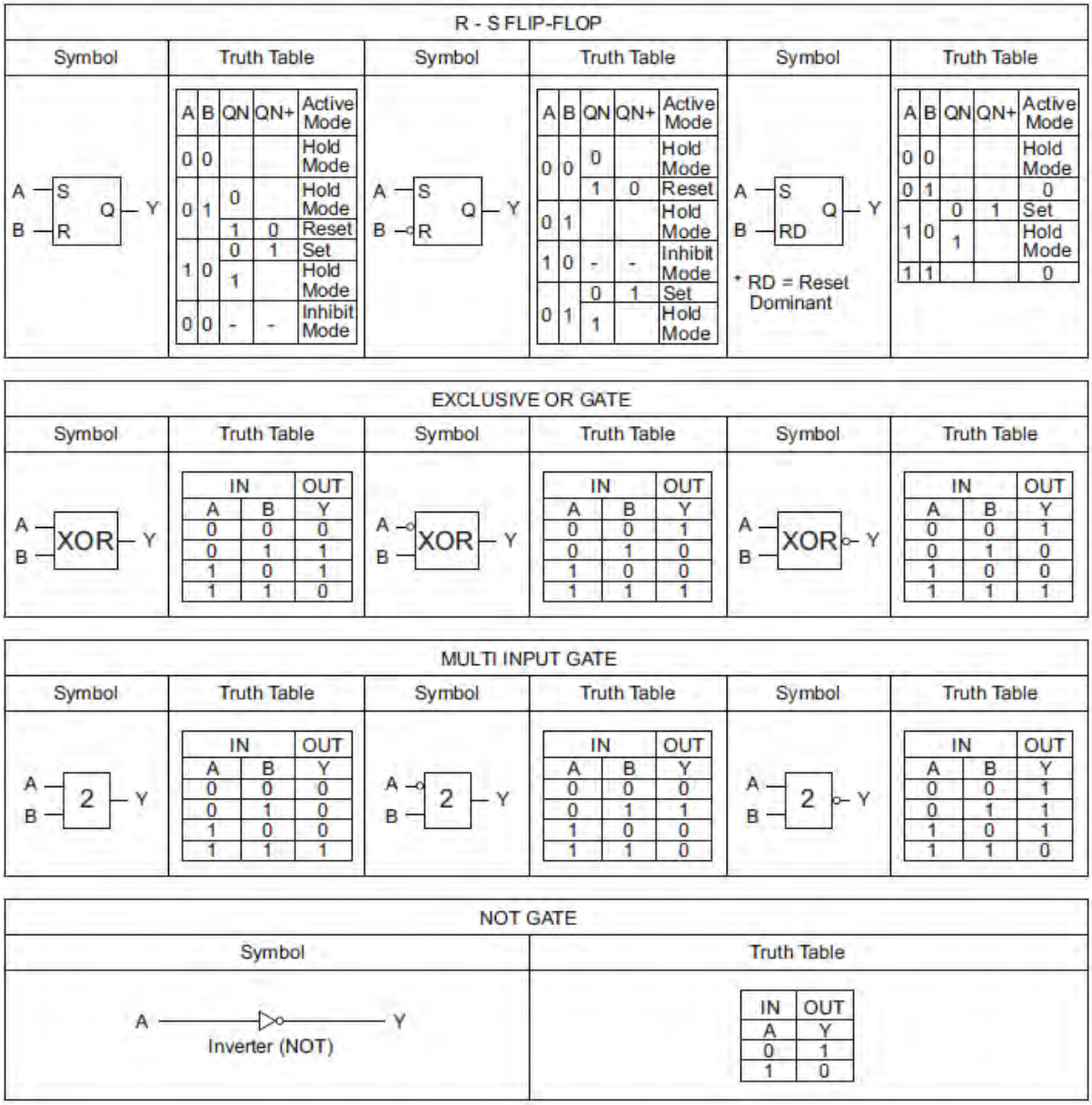
Table A.10: Logic gates

AND GATE

Symbol	Truth Table	Symbol	Truth Table	Symbol	Truth Table
A, B → & → Y	IN / OUT 0 1 0 0 1 0 0 1 0 1 0 0 1 1 1	A, B → & → Y	IN / OUT A B Y 0 0 0 0 1 1 1 0 0 1 1 0	A, B → & → Y	IN / OUT A B Y 0 0 1 0 1 1 1 0 1 1 1 0

OR GATE

Symbol	Truth Table	Symbol	Truth Table	Symbol	Truth Table
A, B → 1 → Y	IN / OUT A B Y 0 0 0 0 1 1 1 0 1 1 1 1	A, B → 1 → Y	IN / OUT A B Y 0 0 1 0 1 1 1 0 0 1 1 1	A, B → 1 → Y	IN / OUT A B Y 0 0 1 0 1 0 1 0 0 1 1 0



A.2.5 RSG2200 9-Port Managed Gigabit Ethernet Backbone Switch

The RSG2200 is an industrially hardened, fully managed, modular Ethernet switch specifically designed to operate in substation utility environments. The RSG2200's superior hardware design coupled with the ROS software provides improved system reliability and advanced networking features making it ideally suited for creating Ethernet networks for mission-critical, real-time, control applications. The RSG2200 offers modular flexibility at 1000BaseX fibre and 10/100/1000BaseTX copper port combinations. Optional front or rear mount connectors make the RSG2200 highly versatile and can support multiple fibre connections (SFP, GBIC, LC, SC) without loss of port density. Figure A.19 illustrates the RSG2200 Ethernet switch.

Figure A.19: RSG2200 Ethernet switch

The RSG2200 is equipped with a comprehensible display panel designed to provide rapid status information across each port for problem-solving and troubleshooting. It features:

- RS232 console port for 'out of band' console access and configuration;
- Power supply and alarm status indications;
- Convenient port status indications conveying Link-Activity, Duplex and Speed via push-button control;
- System reset using the 'Mode' button (5 seconds).

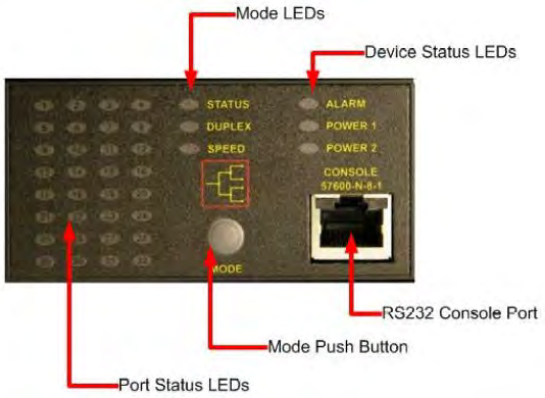


Figure A.20: RSG2200 Ethernet switch

Table A.11 and Table A.12 define the device status and port status LED colours.

Table A.11: Device status LED colours

LED	Colour	Description
PS1/PS2	Green	Power supply operating normal
	Red	Power supply failure
	Off	No power supply installed
Alarm	Red	Alarm exist - login to web management interface to determine alarm code
	Off	No alarm exist

Table A.12: Port status LED colours

LED	Colour	Description
Status	Green (Solid)	Link
	Green (Blinking)	Activity
	Off	No Link
Duplex	Green (Solid)	Full-Duplex operation
	Orange (Solid)	Half-Duplex operation
	Off	No Link
Speed	Green (Blinking)	1000Mb/s
	Green (Solid)	100Mb/s
	Orange (Solid)	10Mb/s
	Off	No Link

The RSG2200 can be connected with several types of fibre optic connectors as shown in Figure A.21. The Transmit (TX) and Receive (RX) connections of each port must be properly matched. If the connectors are populated on the bottom row of the RSG2200, the transceiver orientation must be reversed (i.e. RX and TX need to be upturned).

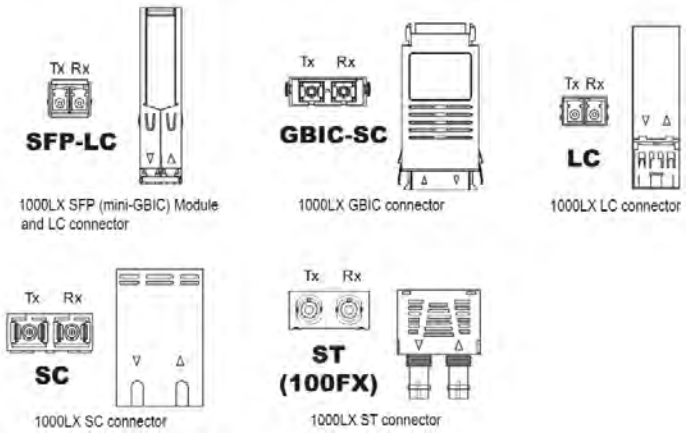


Figure A.21: Fibre optic connectors

The device is rack mounted using panel adapter assemblies, which allow the chassis to be mounted to a standard 2.5cm rail using the grooves. A space of 4.4cm should be kept free above the Ethernet switch to allow for small amount of convectional airflow. Any increase in airflow will result in a r eduction of ambient temperature, leading to long-lasting reliability of equipment within the rack. Figure A.22 illustrates the mounting dimensions of the Ethernet switch.

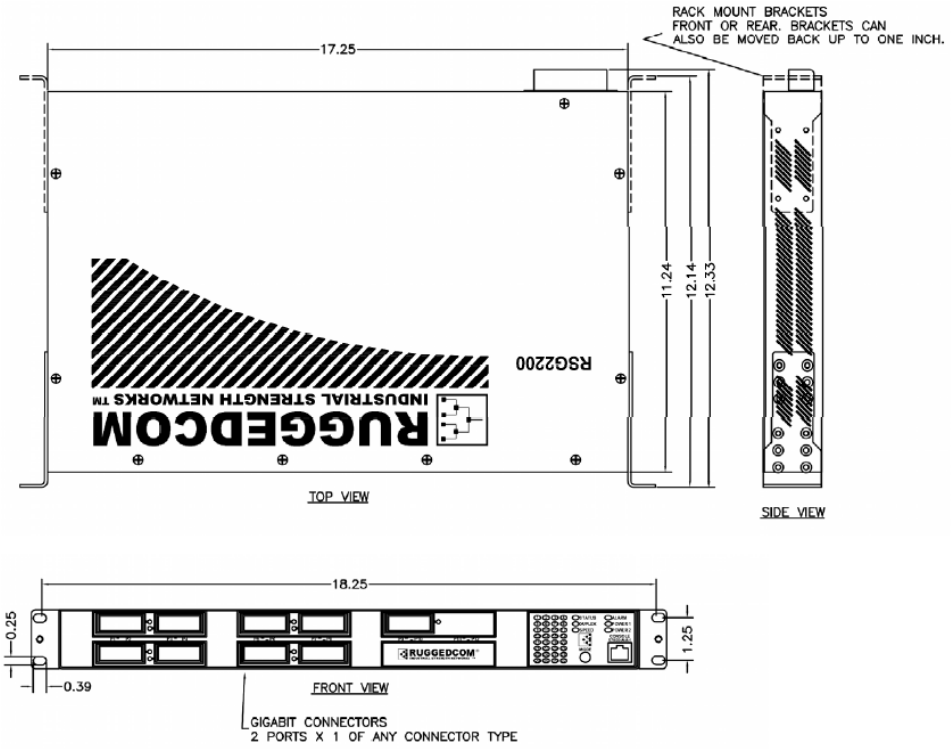


Figure A.22: Mounting dimensions

The RSG2200 supports dual redundant power supplies – 'Power Supply 1 (PS1)' and 'Power Supply 2 (PS2)'. The connections for PS1, PS2 and the fail-safe are located on the terminal blocks and are secured by means of Phillip screws or Phoenix plugs. The terminal blocks have a compression plate allowing bare wire connections or crimped terminal lugs. A #6 size ring lug is used to ensure secure, reliable connections under severe shock or vibration. The safety cover must be re-attached after wiring to ensure preventative measures. Figure A.23 and Figure A.24 illustrate the Phillip screw and Phoenix plug terminal blocks.

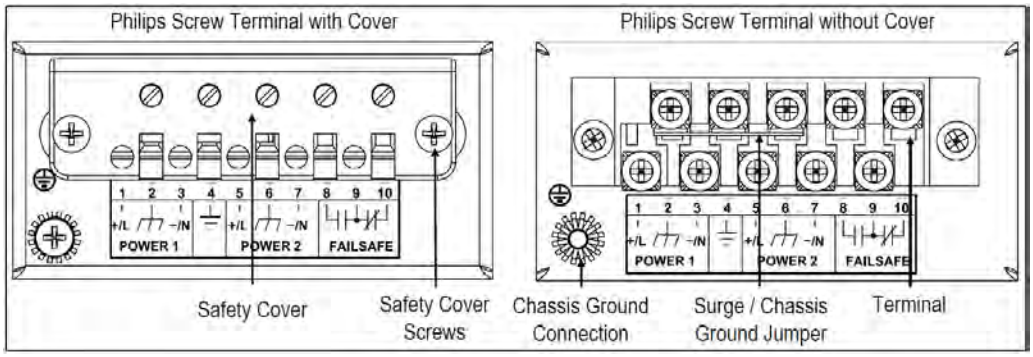


Figure A.23: Phillip screw terminal block

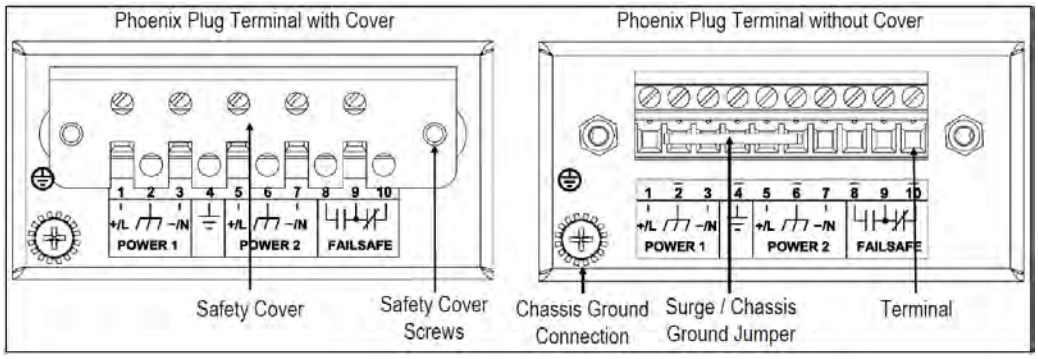


Figure A.24: Phoenix plug terminal block

The chassis ground connection requires a #6-32 screw. It is recommended to terminate the ground connection in a #6 ring lug and to use a torque setting not exceeding 1.7 Nm.

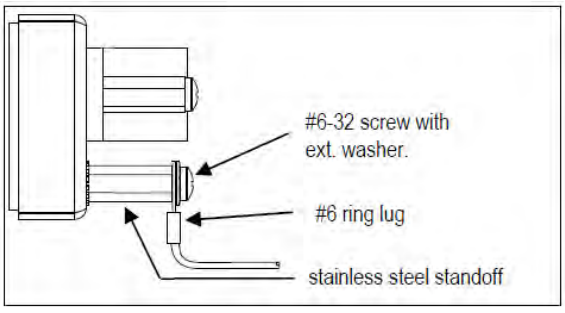


Figure A.25: Chassis ground connection

Table A.13 summarises the terminal block descriptions for power connections.

Table A.13: Power terminal block description

Terminal	Description	Usage
1	PS1 Live / +	**PS1 Live / +** is connected to the positive (+) terminal if the power source is DC or to the (Live) terminal if the power source is AC.
2	PS1 Surge Ground	**PS1 Surge Ground** is connected to the Chassis Ground via a jumper on the terminal block. Surge Ground is used as the ground conductor for all surge and transient suppression circuitry. Surge Ground must be disconnected from Chassis Ground during HIPOT (dielectric strength) testing.
3	PS1 Neutral / -	**PS1 Neutral / -** is connected to the negative (-) terminal if the power source is DC or to the (Neutral) terminal if the power source is AC.
4	Chassis Ground	**Chassis Ground** is connected to the Safety Ground terminal for AC inputs or the ground bus for DC inputs. Chassis ground connects to both power supply surge grounds via a removable jumper.
5	PS2 Live / +	**PS2 Live / +** is connected to the positive (+) terminal if the power source is DC or to the (Live) terminal if the power source is AC.
6	PS2 Surge Ground	**PS2 Surge Ground** is connected to the Chassis Ground via a jumper on the terminal block. Surge Ground is used as the ground conductor for all surge and transient suppression circuitry. Surge Ground must be disconnected from Chassis Ground during HIPOT (dielectric strength) testing.
7	PS2 Neutral / -	**PS2 Neutral / -** is connected to the negative (-) terminal if the power source is DC or to the (Neutral) terminal if the power source is AC.
8	Relay NO Contact	Normally open, failsafe relay contact.
9	Relay Common	Failsafe relay common contact.
10	Relay NC Contact	Normally closed, failsafe relay contact.

Figure A.26 depicts typical AC and DC wiring connections for the terminal blocks.

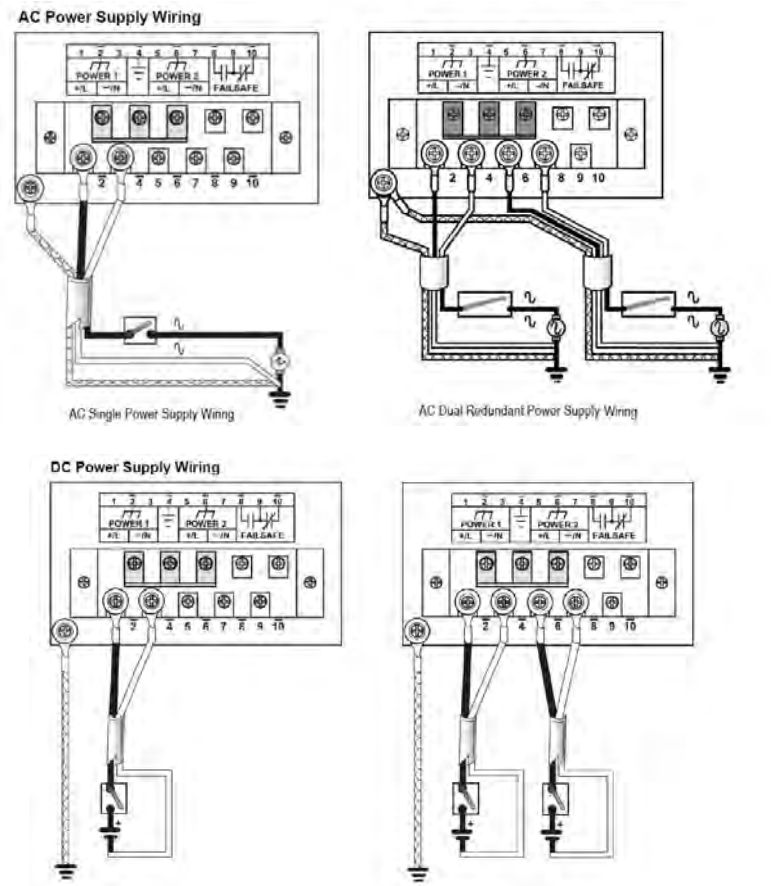


Figure A.26: Power supply wiring

The Ethernet switch comprises of twenty-four 10/100BaseTX ports that connect to a CAT-5 UTP cable with RJ45 male connectors. The RJ45 connectors facilitate auto-negotiation, auto-polarity and auto-crossover functions. Figure A.27 and Table A.14 illustrate the RJ45 port pin arrangement.

Table A.14: RJ45 Ethernet pin assignment

10/100BaseTx Pin-out	
Pin	Description
1	RX +
2	RX -
3	TX +
6	TX -
4, 5, 7, 9	NC

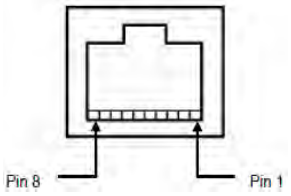


Figure A.27: RJ45 port pin configuration

A.2.6 SEL-2407 Satellite-Synchronised Clock

The SEL-2407 synchronised clock is used for basic sequence-of-event and fault recording using mission-critical processes such as detailed event analysis and synchrophasor measurements. The SEL-2407 comes equipped with a GPS antenna. The antenna is designed for pole mounting on a 2. 54cm straight threaded socket, which allows the antenna cable to be routed inside the pole, protecting the cable connection and adding reliability. The antenna is mounted to the side panel of the portable IEC61850 testing unit and supplied with a Gas Tube Coaxial Surge Protector to balance the difference in potential that can occur between the centre conductor and the shield of the coaxial cable between the antenna and clock.

Figure A.28: SEL-2407 clock

The Gas Tube Coaxial Surge Protector is firmly mounted at the entrance of the enclosure and the clock is grounded to the common earth to avoid ground-rise potential damage as illustrated in Figure A.29. A C960 cable is required between the SEL-2407

and surge protector, allowing for a installation variability of 10-20% with respect to the cable length.

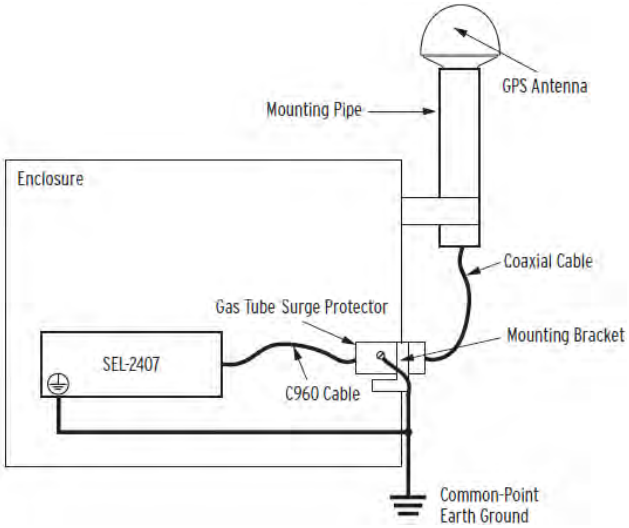


Figure A.29: Surge-protector installation

The SEL-2407 has three front panel status LED indicators as shown in Table A.15. These indicators annunciate the current status of the clock. The 'Holdover' signifies the operating mode in which the clock has lost satellite transmission and is operating on the internal clock.

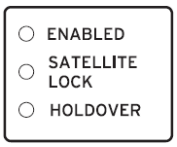


Table A.15: Front-panel status LED indicators

LED	Colour	Description
Enabled	Green	All self tests are passing.
	Yellow	All self tests are passing and the clock is in Force-Time-Quality mode or manual time mode.
Satellite Lock	Green	Clock is tracking three or more satellites.
Holdover	Green	Clock is in holdover mode and the time quality is <±1µs.
	Yellow	Clock is in holdover mode and the time quality is between ±1µs and ±100µs.
	Red	Clock is in holdover mode and the time output is greater than ±100µs.

All settings for the SEL-2407 are performed through Dual In-Line Package (DIP) control switches located behind the front panel of the device as illustrated in Figure A.30. To access these switches, disconnect the input power from the clock and remove the front panel by loosening the four captive screws.

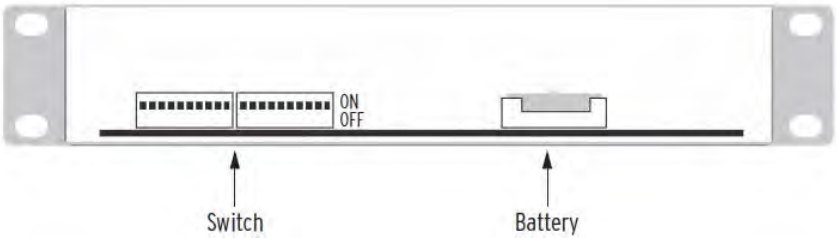


Figure A.30: Control (DIP) switch and battery location

The control switches are labelled 1-20 starting from the left hand side. The control switch settings are listed in Table A.16.

Table A.16: Control (DIP) switch and battery location

Switch	Function
1	ON = Password protection disabled (only use to reset password when lost). OFF = Password protection enabled.
2	ON = **ALARM** output does not include loss of satellite lock. OFF = Adds loss of satellite lock to **ALARM** output.
3, 4	**ALARM** output - Clock function: OFF | OFF | = Normal ALARM operation ON | OFF | = 1 pulse per 30 seconds OFF | ON | = 1 pulse per minute ON | ON | = 1 pulse per hour
5	IRIG output format for options OUT4, OUT5, OUT6, MOD, and serial and fibre ports. ON = Extended IEEE 1344 and IEEE C37.118 IRIG-BXX0 format. OFF = Standard IRIG-BXX2 format.
6, 7 8, 9 10, 11	OUT 1 configuration: OUT 2 configuration: OUT 3 configuration: OFF | ON | = IRIG-B002 format OFF | OFF | = 1 PPS select ON | OFF | = 1k PPS select ON | ON | = IRIG-B000 format with IEEE 1344 and IEEE C37.118 extensions
12 - 17	Local Time Offset: 12 | ON | = Add to UTC | OFF | = Subtract from UTC 13 | ON | = 8 hour increment 14 | ON | = 4 hour increment 15 | ON | = 2 hour increment 16 | ON | = 1 hour increment 17 | ON | = 1/2 hour increment
18	ON = Daylight-Saving Time (DST): advance and return local time display by one hour. OFF = Daylight-Saving Time (DST): always display local standard time.
19	ON = Even parity for IRIG-B000. OFF = Odd parity for IRIG-B000: default position.
20	OUT6 to UTC configuration and ASCII FOR command: ON = OUT6 set to UTC IRIG-B000 format and ASCII FOR commands enabled. OFF = OUT6 to standard format and ASCII FOR commands disabled.

The SEL-2407 provides both modulated (IRIG-B12X) and unmodulated (IRIG-B00X) IRIG-B outputs. The last digit, either 2 or 0, indicates the coded expression. IRIG-B is the serial data format consisting of a 1 s econd frame that contains 100 p ulses divided into fields. The time-synchronised device decodes the second, minute, hour and day fields and sets the internal clock time upon detecting valid time data in the IRIG time mode. The SEL-2407 has one rear EIA-232 serial port and an fibre optic port. Pinout functions for both ports are shown in Table A.17. Pin 4 and Pin 6 is used to output a demodulated IRIG-B signal via control switch 5. The time accuracy of this signal is ±1µs peak.

Table A.17: Pinout functions

Pin	Function
1	+5 Vdc
2	RXD
3	TXD
4	+IRIG-B
5	GND
6	-IRIG-B
7	RTS
8	CTS
9	GND

Figure A.31 illustrates the panel-mount dimensions of the SEL-2407.

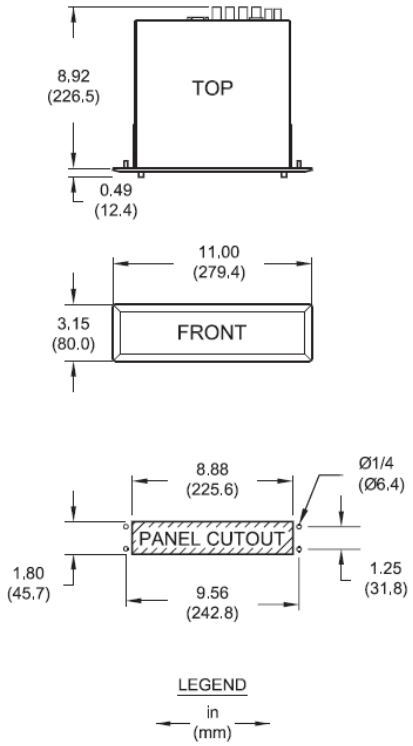


Figure A.31: Panel-mount dimensions

Table A.18 illustrates significant technical data for the clock.

Table A.18: Technical data

Receiver	
Satellite tracking	12-channel continuous tracking 1575.42MHz
Acquisition times	Hot, warm, cold start: 135s
Clock accuracy (UTC time)	1 PPS: ±100ns average, ±500ns peak Demodulated IRIG-B: ±100ns average, ±500ns peak Modulated IRIG-B: ±1µs peak Serial port BX command: ±500µs peak
Holdover stability	±0.08ppm for 20 minutes (from −40º to +80ºC)
Antenna requirements	5V active antenna, 35dB preamp
Electrical output drive levels	
Demodulated IRIG-B/PPS	TTL (OUT1-OUT6): 120mA, 3.5Vdc, 25Ω
Modulated IRIG-B (MOD)	40mA, 4.75Vpp, 25Ω
Serial Port	TTL (Pin 4/Pin 6): 2.5mA, 2.4Vdc, 1kΩ
Alarm contact	
From C carry	6A, Rated voltage: 250 Vdc or 190 Vac
Pulse mode	<10µs
Power supply	
Rating	(24, 48, 125, 250) Vdc, (120, 230) Vac, 50/60Hz

Range	18-300 Vdc or 85-264 Vac
Burden	<10W
Serial Port	
EIA-232 DB-9 Female	Fixed 9600bps, 8 data bits, no parity, 1 stop bit, +5 Vdc, 0.5A, 150 minute timeout, fixed
Fibre Port	
Optical interface connector	ST
Optical protocol	SEL-2812 compatible
Port speed (data rate)	9600 bps
Fibre optic link budget	15 dB
IRIG-B delay	15µs plus 5µs per kilometre of fibre
Optical source	850nm VCSEL transmitter Typical transmitter level: -12 dBm Maximum output level: -3 dBm
Dimensions	
H x W x D	4.45cm x 21.59cm x 23.37cm (1.75in x 8.5in x 9.2in)

A.2.7 SEL-2725 Unmanaged Ethernet Switch

The SEL-2725 is an unmanaged five-port Ethernet switch which uses an copper-to-fibre optic multiport media converter to connect between Ethernet 10/100Base-T and dual-fibre 100BASE-FX ports. The SEL-2725 has no configurable settings and only requires the use of an 1.5mm^2 (16AWG) wire to connect to the power supply. The power supply will stop operation when the input voltage is too low, thus requiring the use of a circuit breaker or overcurrent device rated at a maximum current of 15A.

Figure A.32: SEL-2725 Ethernet switch

Figure A.33 illustrates the mounting dimensions of the SEL-2725.

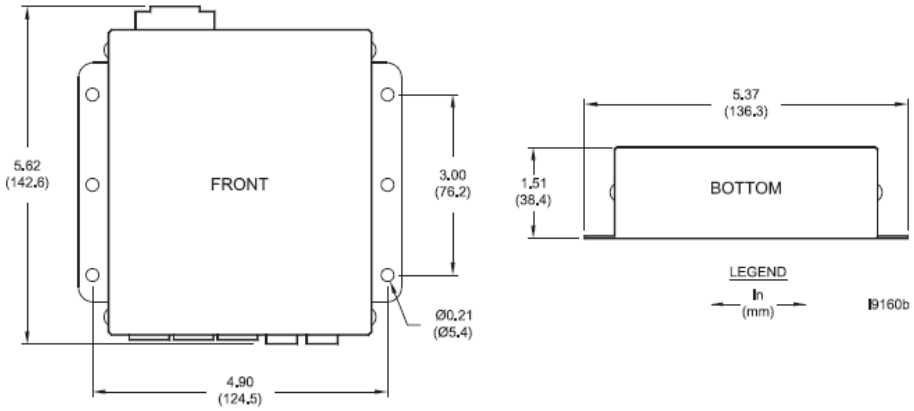


Figure A.33: Mounting dimensions

Table A.19 illustrates technical data.

Table A.19: Technical data

General	
LED indicators	Power (green), link/activity (green per port), full duplex/collision (yellow per port)
Network	IEEE802.3u: 100BASE-T and 100BASE-FX IEEE 802.3: 10 BASE-T 1EEE 802.x: Flow control Address table: 100 MAC addresses
RJ-45 ports	Recommended cable: Category 5(e) shielded twisted pair Auto Negotiation: 10 or 100Mbs, full- or half-duplex and MDI/MDI-X crossover
Fibre optics	100Mbs full duplex Multimode option: Connector type LC, Max distance 2Km Singlemode option: Connector type LC, Max distance 15Km
Environmental	
Operating temperature	-40º to +85ºC (-40º to +185ºF)
Relative humidity	0 to 95% non-condensing
Altitude	2000m
Power supply	12 Vdc (Voltage range 9-30 Vdc, Power consumption <5W) 24/48 Vdc (Voltage range 18-60 Vdc, Power consumption <5W) 125/250 Vdc or 110/240 Vac (Voltage range 85-275 Vdc or 85-264 Vac at 50/60Hz, Power consumption <5W)

A.2.8 CMC356 Universal Relay Test Set & Commissioning Tool

The CMC356 test set is used for testing of protection relays. It has six powerful current sources (three-phase mode: up to 64A/860VA per channel) making the unit capable of testing high-burden relays with excessive power demands. The CMC356 allows wiring and plausibility checks of current transformers by using primary injection. The test set can either be operated by the Test Universe software running on a PC or by the front panel control device CMControl. Figure A.34 and Figure A.35 illustrate the front and rear panels of the device.

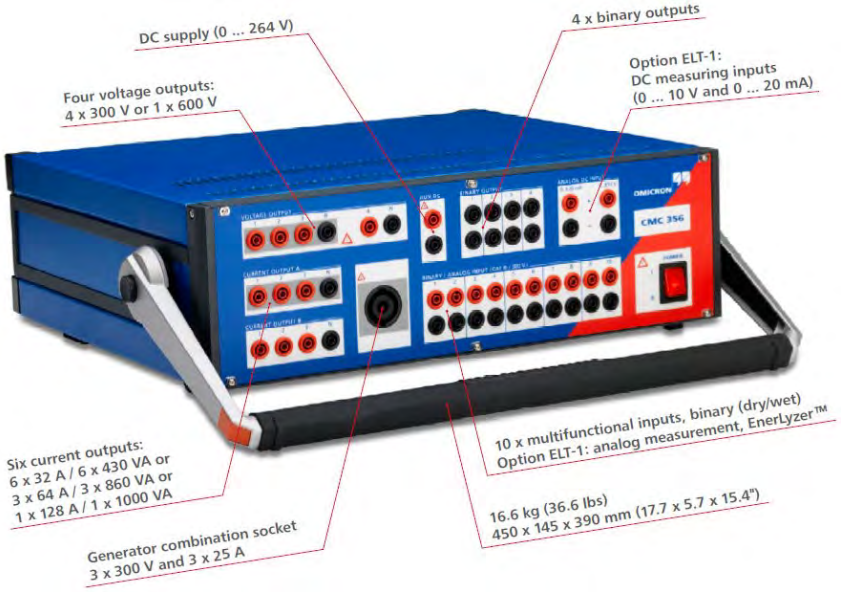


Figure A.34: Front view

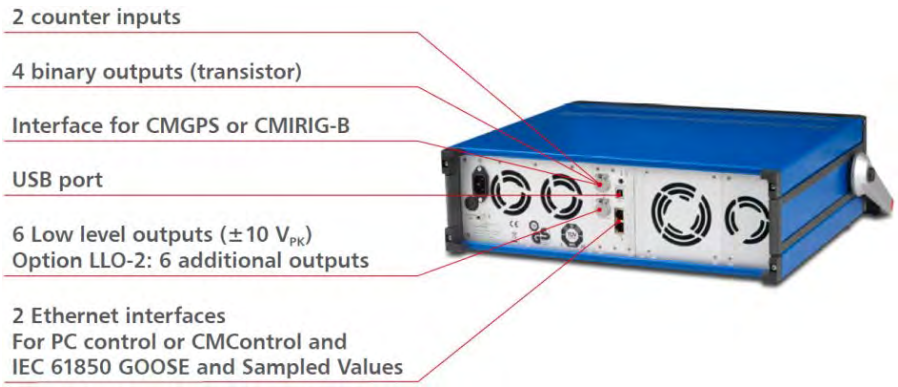


Figure A.35: Rear view

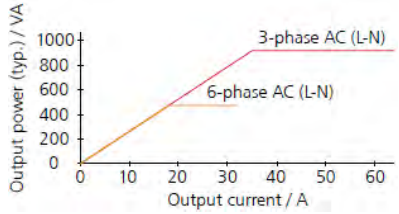
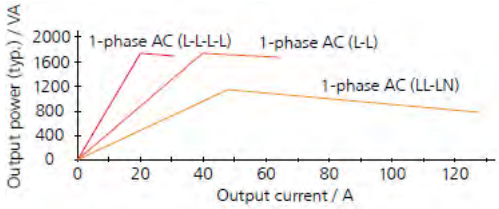
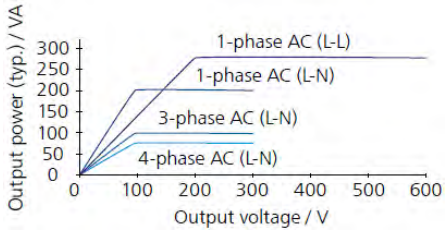
Analog test signals are generated digitally using DSP technology. This in combination with the use of additional error correction algorithms, results in accurate testing signals even at small amplitudes. The six current and four voltage output channels are continuously and independently adjustable in amplitude, phase and frequency. All outputs are short-circuit proof and are protected against external high-voltage transient signals and over-temperature.

The integrated network interface supports comprehensive testing of the IEC61850 protocol using GOOSE subscription of sampled values. Up to 12 independent channels with low-level signals are available at the back of the test set, which can be used to test relays with low-level input facilities. By utilising the EnerLyzer software option, the ten binary inputs of the CMC356 equipped with the ELT-1 hardware option alternatively work as analog measurement inputs. The unit can then be used as a multifunctional multimeter and transient recorder.

Table A.20 illustrates technical data for the CMC356.

Table A.20: Technical data

Current Generators		
Setting range	6-phase AC (L-N)	6 x 0 ... 32A
	3-phase AC (L-N)	3 x 0 ... 62A (Group A || B)
	1-phase AC (LL-LN)	1 x 0 ... 128A (Group A || B)
	DC (LL-LN)	1 x 0 ... ±180A (Group A || B)
Power	6-phase AC (L-N)	6 x 430VA typ. at 25A 6 x 250W guar. at 20A
	3-phase AC (L-N)	3 x 860VA typ. at 50A 3 x 500W guar. at 40A
	1-phase AC (LL-LN)	1 x 1000VA typ. at 80A 1 x 700W guar. at 80A
	1-phase AC (L-L)	1 x 1740VA typ. at 50A 1 x 1100W guar. at 40A
	1-phase AC (L-L-L-L)	1 x 1740VA typ. at 25A 1 x 1100W guar. at 20A
	DC (LL-LN)	1 x 1400VA typ. at ±80A 1 x 1000W guar. at ±80A

		
		
Accuracy	Error < 0.05% rd. + 0.02% rg. typ. Error < 0.15% rd. + 0.05% rg. guar.	
Distortion	< 0.05% typ., < 0.15% guar.	
Resolution	1mA	
Max. compliance voltage (L-N)(L-L)(L-L-L-L)	35Vpk / 70Vpk / 140 Vpk	
Connection banana sockets	4mm (0.16in) banana sockets (32A continuously)	
Connection combination socket	Group A only (25A continuously max.)	
Voltage Generators		
Setting range	4-phase AC (L-N)	4 x 0 . .. 300V (VL4(t) automatically calculated: VL4 = (VL1+VL2+VL3)*c or freely programmable)
	3-phase AC (L-N)	3 x 0 ... 300V
	1-phase AC (L-L)	1 x 0 ... 600V
	DC (L-N)	4 x 0 ... ±300V
Power	3-phase AC (L-N)	3 x 100VA typ. at 100 ... 300V 3 x 85VA guar. at 85 ... 300V
	4-phase AC (L-N)	4 x 75VA typ. at 100 ... 300V 4 x 50VA guar. at 85 ... 300V
	1-phase AC (L-N)	1 x 200VA typ. at 100 ... 300V 1 x 150VA guar. at 75 ... 300V
	1-phase AC (L-L)	1 x 275VA typ. at 200 ... 600V 1 x 250VA guar. at 200 ... 600V
	DC (L-N)	1 x 420W typ. at ±300V 1 x 360W guar. at ±300V
		
Accuracy	Error < 0.03% rd. + 0.01% rg. typ. at 0 ... 3000V Error < 0.08% rd. + 0.02% rg. guar. at 0 ... 300V	
Distortion	0.015% typ., < 0.05% guar.	
Ranges	150V / 300V	
Resolution	5mV / 10mV in range 150V / 300V	
Connection	4mm (0.16in) banana sockets / combination socket (1, 2, 3, N)	
Generators, general		
Frequency	Range sine signals	10 ... 1000 Hz
	Range harmonics / interharmonics	Voltage: 10 ... 3000 Hz Current: 10 ... 1000 Hz
	Range transient signals	DC ... 3.1 kHz
	Accuracy/drift	±0.5ppm / ±1ppm
	Resolution	< 5µHz
Phase	Angle range	-360° ... +360°
	Resolution	0.001°

	Error at 50/60Hz	Voltage: 0.02º typ., < 0.1º guar. Current: 0.05º typ., < 0.2º guar.
Bandwidth (-3 dB)	3.1kHz	
Low level outputs		
Number of outputs	6 (12 with option LLO-2)	
Setting range	0 ... ±10Vpk	
Max. output current	1mA	
Accuracy	Error < 0.025% typ., < 0.07% guar. at 1 ... 10Vpk	
Resolution	250µV	
Auxiliary DC supply		
Voltage ranges	0 ... 264 VDC, 0.2A / 0 ... 132 VDC, 0.4A / 0 ... 66 VDC. 0.8A	
Power	Max. 50W	
Accuracy	Error < 2% typ., <5% guar	
Binary inputs		
Number	10	
Trigger criteria	Toggling of potential-free contacts or DC voltage compared to threshold voltage	
Input characteristics	0 ... ±300 VDC threshold or potential-free if equipped with ELT-1: 0 ... ±600 VDC threshold or potential-free	
Ranges	20V / 300V If equipped with ELT-1: 100mV / 1V / 10V / 100V / 600V	
Resolution of threshold	50mV (0 ... 20V), 500mV (20V ... 3000V) ELT-1: ±2mV, ±20mV, ±200mV, ±2V, ±20V in ranges	
Sample rate	10kHz (resolution 100µs)	
Time stamping accuracy	±0.00015% of rd. ±70µs	
Max. measuring time	Infinite	
Debounce/Deglitch time	0 ... 25ms / 0 ... 25ms	
Counting function	< 3kHz at pulse width > 150µs	
Galvanic isolation	5 galvanically isolated groups (2+2+2+2+2)	
Max. input voltage	CAT IV / 150V, CAT III / 300V, transient immunity 2kV If equipped with ELT-1: CAT IV / 150V, CAT III / 300V, CAT II / 600V (850Vpk)	
Binary outputs, relays		
Type	Potential-free relay contacts, software controlled	
Number	4	
Break capacity AC	Vmax: 300 VAC / Imax: 8A / Pmax: 2000VA	
Break capacity DC	Vmax: 300 VDC / Imax: 8A / Pmax: 50W	
DC voltage measuring input		
Measuring range	0 ... ±10V	
Accuracy	Error < 0.003% rg. typ., < 0.02% rg. guar.	
Input impedance	1 MΩ	
DC current measuring input		
Measuring range	0 ... ±1mA, 0 ... ±20mA	
Accuracy	Error < 0.003% rg. typ., < 0.02% rg. guar.	
Input impedance	15Ω	
Analog AC+DC measuring inputs		
Type	AC+DC analog voltage inputs (current measurement with external current clamps or shunt resistors)	
Number	10	
Nominal input ranges (RMS values)	100mV, 1V, 10V, 100V, 600V	
Amplitude accuracy	Error < 0.06% typ., < 0.15% guar.	
Bandwidth	DC ... 10kHz	
Sampling frequency	28.44kHz, 9.48kHz, 3.16kHz	
Input impedance	500kΩ // 50pF	
Transient input buffer at 28kHz	3.5s for 10 input channels / 35s for 1 input channel	
Transient input buffer at 3kHz	31s for 10 input channels / 5 min. for 1 input channel	
Transient trigger	Threshold voltage, power quality trigger, sag, swell, harmonic, frequency, frequency change, notch	
IEC61850 GOOSE		
Simulation	Mapping of binary outputs to data attributes in published GOOSE messages. Number of virtual binary outputs: 360 Number of GOOSEs to be published: 128	
Subscription	Mapping of data attributes from subscribed GOOSE messages to binary inputs. Number of virtual binary inputs: 360 Number of GOOSEs to be subscribed: 128	

Performance	Type 1A; Class P2/3. Processing time < 1ms
VLAN support	Selectable priority and VLAN-ID
Power supply	
Nominal input voltage	100-240 VAC, 1-phase
Permissible input voltage	85 ... 264 VAC
Nominal frequency	50/60Hz
Permissible frequency range	45 ... 65Hz
Rated current	12A at 115V/10A at 230V
Connection	Standard AC socket (IEC 60320)
Miscellaneous	
Weight	16.6kg (36.6lbs)
Dimensions (W x H x D)	450 x 145 x 390 mm (17.7 x 5.7 x 15.4 in)
PC connection	Two PoE Ethernet ports: • 10/100 Mbit/s • IEEE 802.3af compliant • Port capability limited to one Class 1 (3.84W) and one C lass 2 (6.49W) powered device USB 2.0 port • Full speed (Type B connector)
Signal indication (LED)	> 42V for voltage and current outputs and AUX DC

A.2.9 KDN-U200 SMITT Relay

The KDN-U200 SMITT relay is used for external signalling. The KDN-U200 is a plug-in bistable relay with eight change-over contacts. The contacts are isolated by two coils and a mechanical rocker mechanism. The relay is reset from green to red following a fault or power impulse condition. Figure A.36 illustrates the connection and dimension diagrams of the KDN-U200.

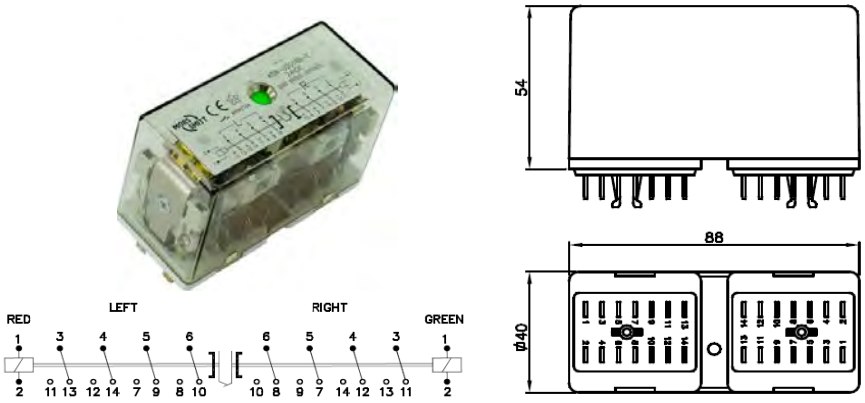


Figure A.36: KDN-U200 relay

Table A.21 summarises technical data for the KDN-U200.

Table A.21: Technical data

Contact Specifications	
Amount and type of contacts	8 C/O
Maximum make current	16A
Peak inrush current	200A (withstand > 10 x 200A at 10ms, 1min)
Maximum continuous current	10A
Maximum switching voltage	250 VDC, 440 VAC
Minimum switching voltage	12V
Minimum switching current	10mA
Maximum contact resistance	15mΩ
Maximum breaking capacity	110 VDC, 8A (L/R ≤ 15ms) 230 VAC, 10A (cos φ≥0.7)
Material	Ag standard (optional $AgSnO_2$, Au on Ag)

Contact gap	0.7mm
Contact force	> 200mN
Coil Specification	
Nominal voltage (Un)	VDC: 12 ... 220 VAC: 24 ... 380
Operating times at nominal voltage	Minimum impulse time: 50ms Bounce time N/O contacts: ≤4ms Bounce time N/C contacts: ≤8ms
Inductance L/R at U_{NOM}	Energised: 11ms Released: 8ms
Operating voltage range	70% - 125% U_{NOM}

A.2.10 C10 Miniature Circuit Breaker

The C10 MCB is intended for protection of short-circuit or overload currents. These current limiting circuit breakers are commonly used in substation networks where the single phase fault levels are less than 4.5kA. Currents less than the prospective fault current are only allowed to flow under short-circuit conditions as illustrated in Figure A.37. This presents better network protection, reduced thermal effects and limited electromagnetic effect.

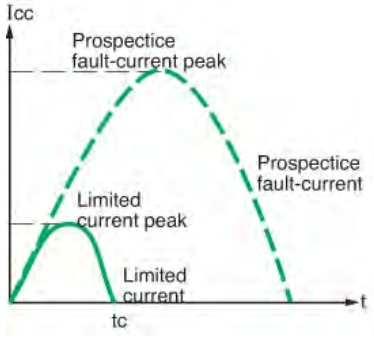


Figure A.37: Prospective current and actual limited current

Figure A.38 illustrates the basic dimensions of the C10.

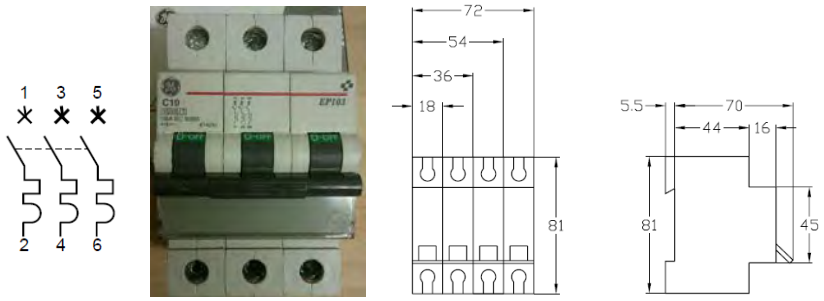


Figure A.38: C10 MCB

Table A.22 outlines common technical data.

Table A.22: Technical data

Power Circuit	
Voltage rating	240/415V AC
I^2t classification	3
Number of cycles (O-C)	20000
Braking capacity	1P (Voltage: 240/415V, breaking capacity 6000A) 2P (Voltage: 415 ... 480V, breaking capacity 6000A) 3P (Voltage: 415V, breaking capacity 6000A)

A.3 Portable IEC61850 Testing Unit Wiring & Tests

Figure A.39: Portable IEC61850 Testing Unit (Front View)

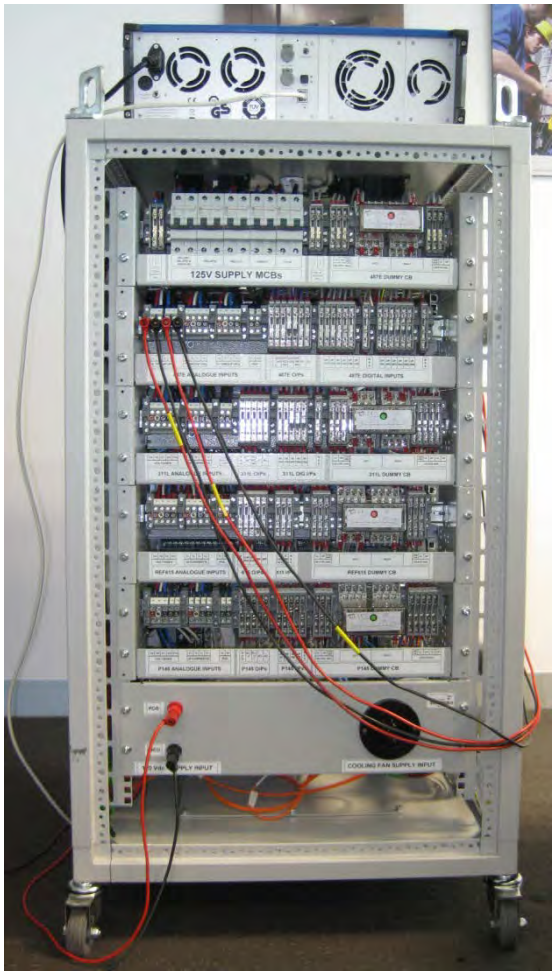


Figure A.40: Portable IEC61850 Testing Unit (Rear View)

Figure A.41: Portable IEC61850 Testing Unit (Side View)

Figure A.42: IED wiring connections

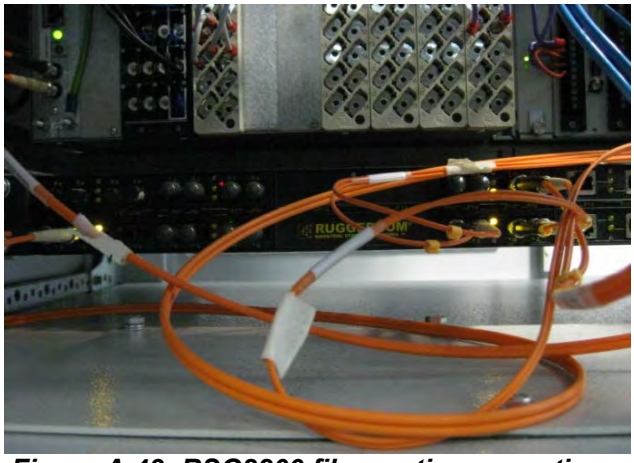


Figure A.43: RSG2200 fibre optic connections

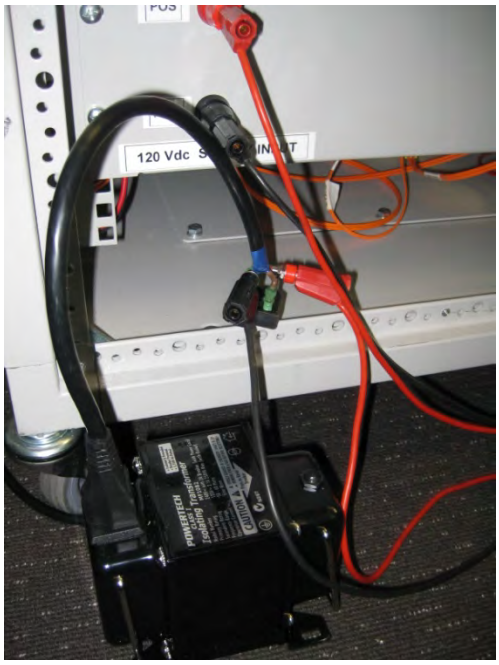


Figure A.44: DC power supply (stepdown transformer with bridge rectifier)

Figure A.45: CMC356 Ethernet cable connection

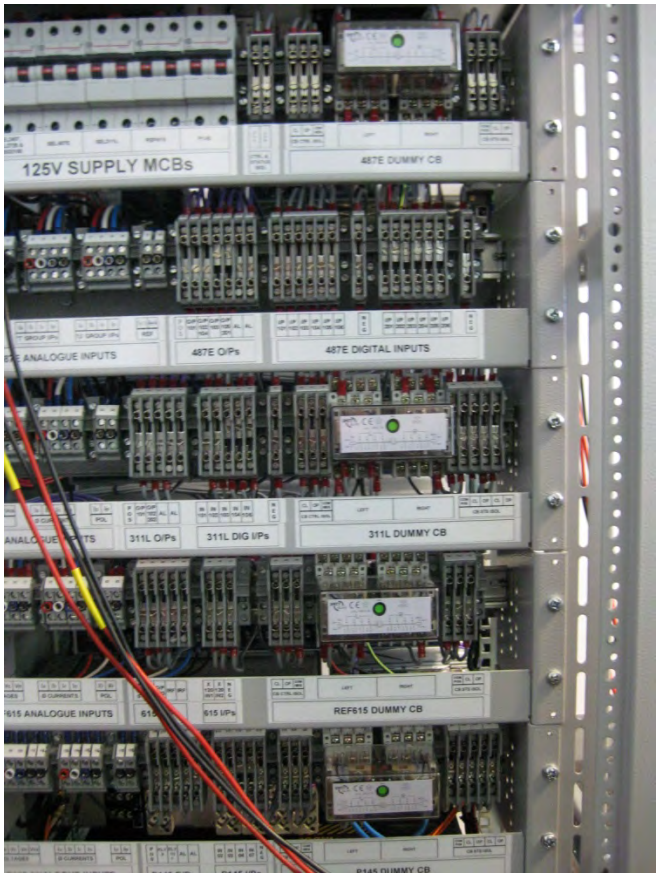


Figure A.46: Circuit breakers closed

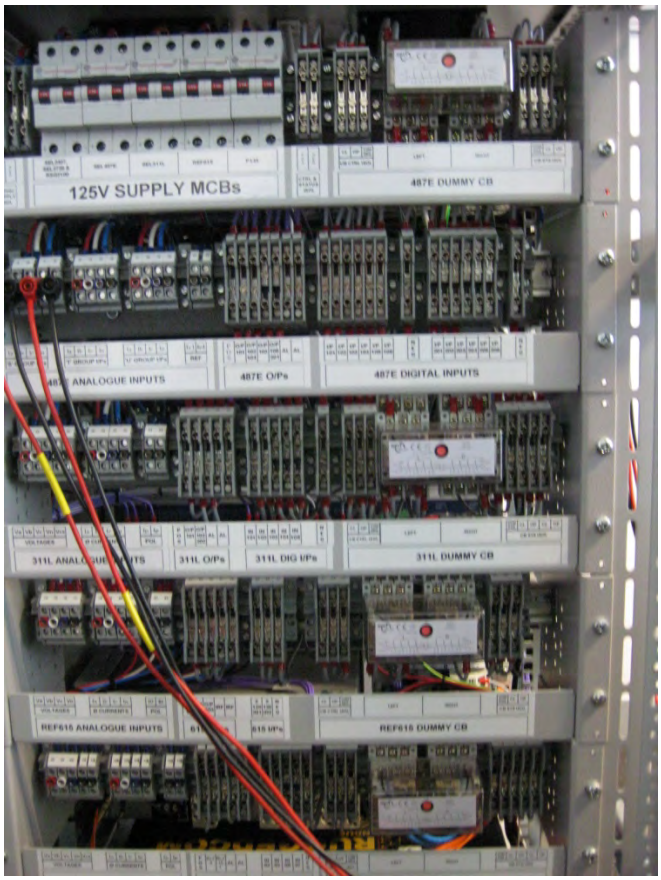


Figure A.47: Circuit breakers opened

Figure A.48: SEL-487E GOOSE messages

Figure A.49: SEL-311L GOOSE messages

Figure A.50: P145 GOOSE messages

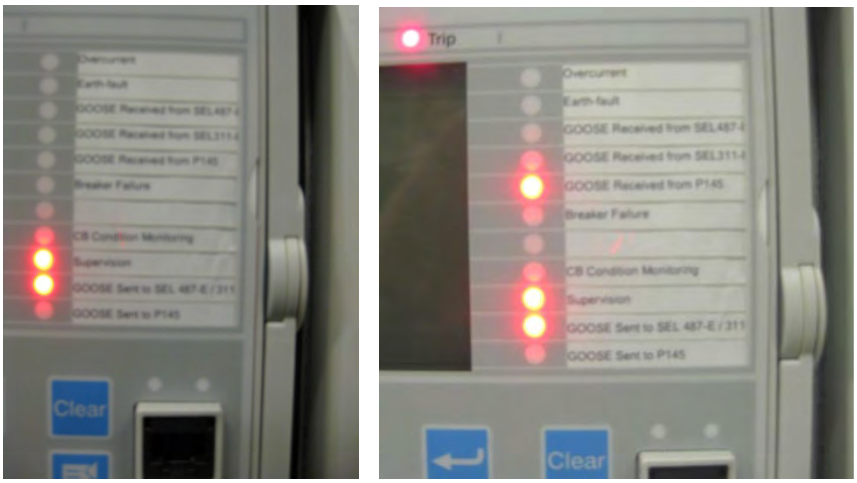


Figure A.51: REF615 GOOSE messages

Figure A.52: RSG2200 Managed Ethernet Switch Status

Figure A.52: SEL-2725 Unmanaged Ethernet Switch Status

APPENDIX B

B.1 Close-up of the top level PSL mapping for the P145

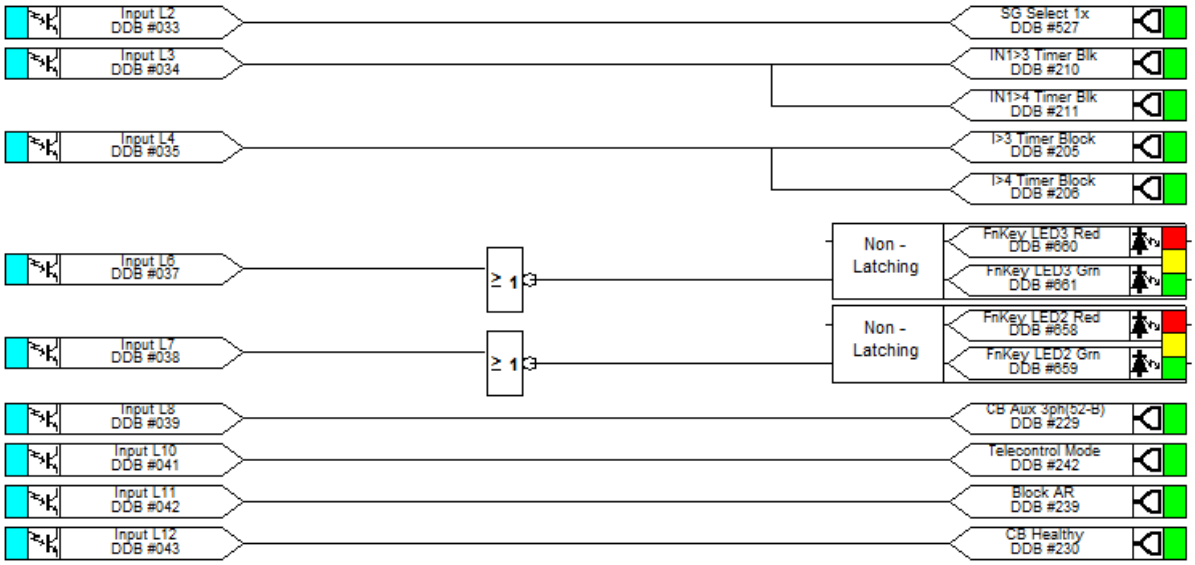


Figure B.1: Opto input mapping

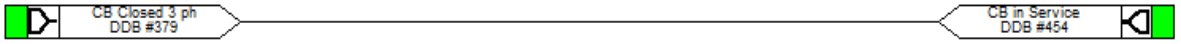


Figure B.2: Circuit breaker mapping

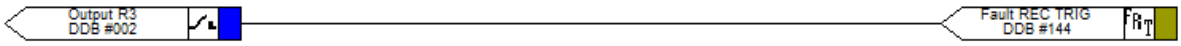


Figure B.3: Fault record trigger mapping

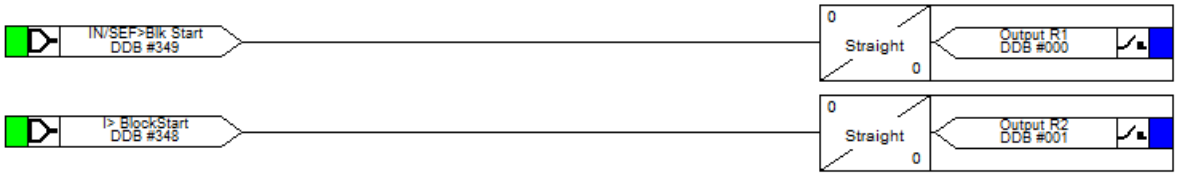


Figure B.4: Output relay mapping

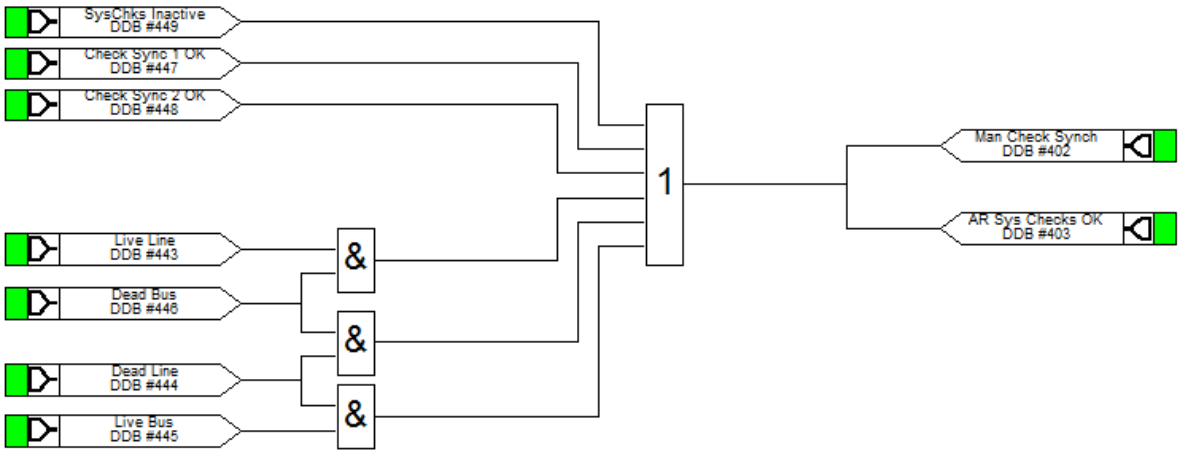
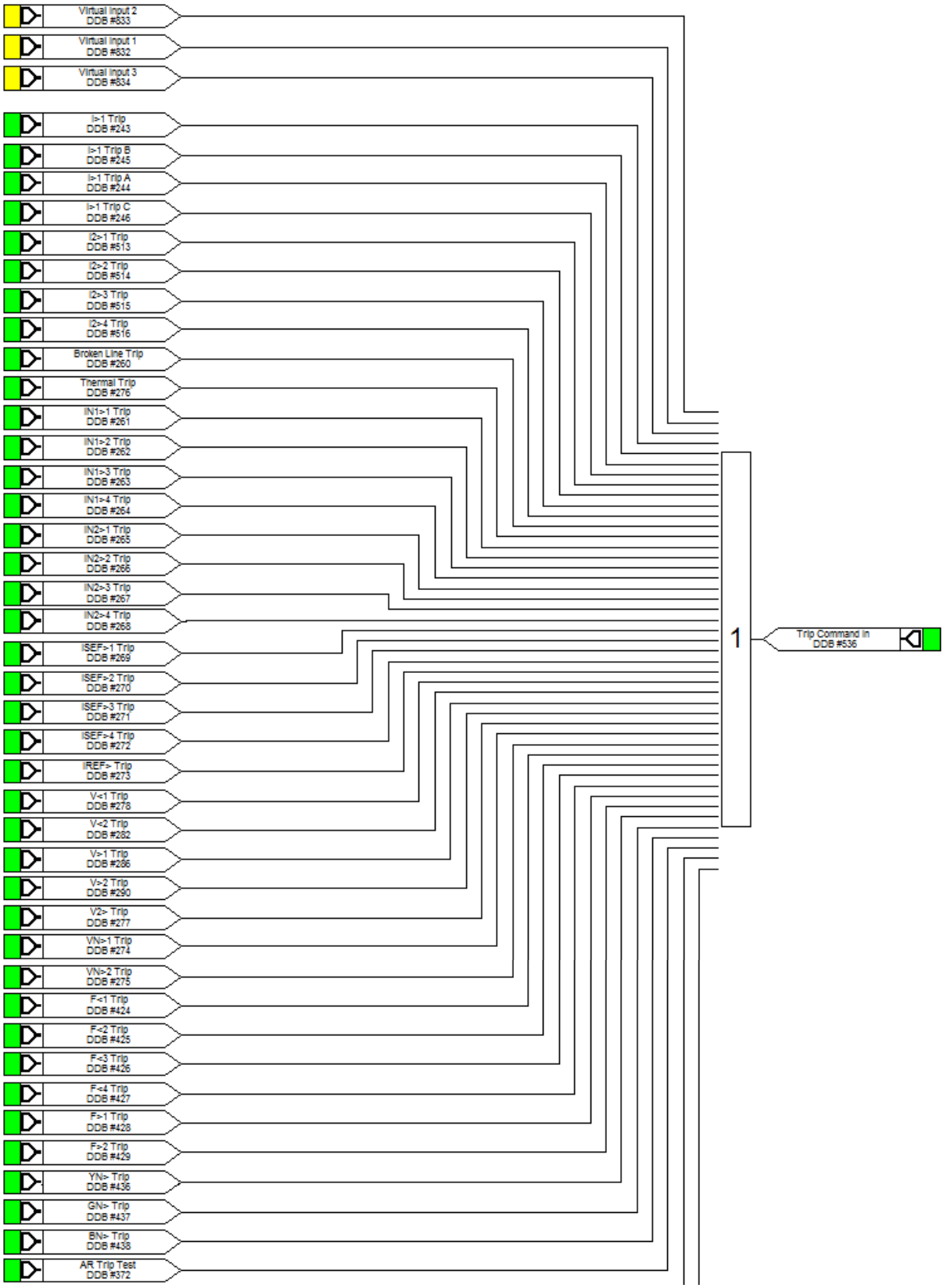
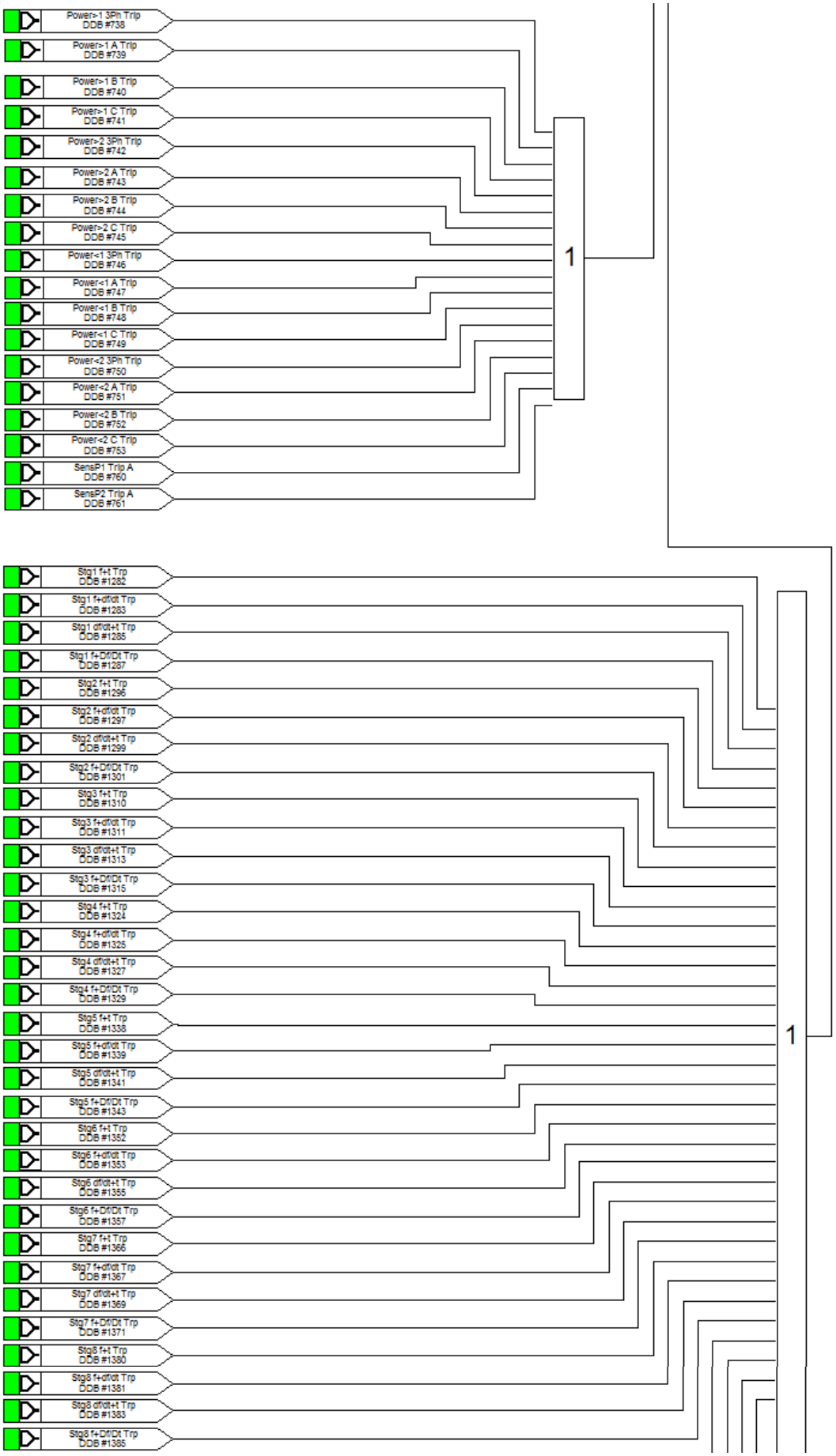


Figure B.5: Check synchronisation and voltage monitor mapping


Virtual Input 2
DDB #833
Virtual Input 1
DDB #832
Virtual Input 3
DDB #834
I>1 Trip
DDB #243
I>1 Trip B
DDB #245
I>1 Trip A
DDB #244
I>1 Trip C
DDB #246
I2>1 Trip
DDB #513
I2>2 Trip
DDB #514
I2>3 Trip
DDB #515
I2>4 Trip
DDB #516
Broken Line Trip
DDB #260
Thermal Trip
DDB #276
IN1>1 Trip
DDB #261
IN1>2 Trip
DDB #262
IN1>3 Trip
DDB #263
IN1>4 Trip
DDB #264
IN2>1 Trip
DDB #265
IN2>2 Trip
DDB #266
IN2>3 Trip
DDB #267
IN2>4 Trip
DDB #268
ISEF>1 Trip
DDB #269
ISEF>2 Trip
DDB #270
ISEF>3 Trip
DDB #271
ISEF>4 Trip
DDB #272
IREF> Trip
DDB #273
V<1 Trip
DDB #278
V<2 Trip
DDB #282
V>1 Trip
DDB #286
V>2 Trip
DDB #290
V2> Trip
DDB #277
VN>1 Trip
DDB #274
VN>2 Trip
DDB #275
F<1 Trip
DDB #424
F<2 Trip
DDB #425
F<3 Trip
DDB #426
F<4 Trip
DDB #427
F>1 Trip
DDB #428
F>2 Trip
DDB #429
YN> Trip
DDB #436
GN> Trip
DDB #437
BN> Trip
DDB #438
AR Trip Test
DDB #372
1
Trip Command In
DDB #536


Power>1 3Ph Trip
DDB #738
Power>1 A Trip
DDB #739
Power>1 B Trip
DDB #740
Power>1 C Trip
DDB #741
Power>2 3Ph Trip
DDB #742
Power>2 A Trip
DDB #743
Power>2 B Trip
DDB #744
Power>2 C Trip
DDB #745
Power<1 3Ph Trip
DDB #746
Power<1 A Trip
DDB #747
Power<1 B Trip
DDB #748
Power<1 C Trip
DDB #749
Power<2 3Ph Trip
DDB #750
Power<2 A Trip
DDB #751
Power<2 B Trip
DDB #752
Power<2 C Trip
DDB #753
SensP1 Trip A
DDB #760
SensP2 Trip A
DDB #761
1
Stg1 f+t Trp
DDB #1282
Stg1 f+df/dt Trp
DDB #1283
Stg1 df/dt+t Trp
DDB #1285
Stg1 f+Df/Dt Trp
DDB #1287
Stg2 f+t Trp
DDB #1296
Stg2 f+df/dt Trp
DDB #1297
Stg2 df/dt+t Trp
DDB #1299
Stg2 f+Df/Dt Trp
DDB #1301
Stg3 f+t Trp
DDB #1310
Stg3 f+df/dt Trp
DDB #1311
Stg3 df/dt+t Trp
DDB #1313
Stg3 f+Df/Dt Trp
DDB #1315
Stg4 f+t Trp
DDB #1324
Stg4 f+df/dt Trp
DDB #1325
Stg4 df/dt+t Trp
DDB #1327
Stg4 f+Df/Dt Trp
DDB #1329
Stg5 f+t Trp
DDB #1338
Stg5 f+df/dt Trp
DDB #1339
Stg5 df/dt+t Trp
DDB #1341
Stg5 f+Df/Dt Trp
DDB #1343
Stg6 f+t Trp
DDB #1352
Stg6 f+df/dt Trp
DDB #1353
Stg6 df/dt+t Trp
DDB #1355
Stg6 f+Df/Dt Trp
DDB #1357
Stg7 f+t Trp
DDB #1366
Stg7 f+df/dt Trp
DDB #1367
Stg7 df/dt+t Trp
DDB #1369
Stg7 f+Df/Dt Trp
DDB #1371
Stg8 f+t Trp
DDB #1380
Stg8 f+df/dt Trp
DDB #1381
Stg8 df/dt+t Trp
DDB #1383
Stg8 f+Df/Dt Trp
DDB #1385
1

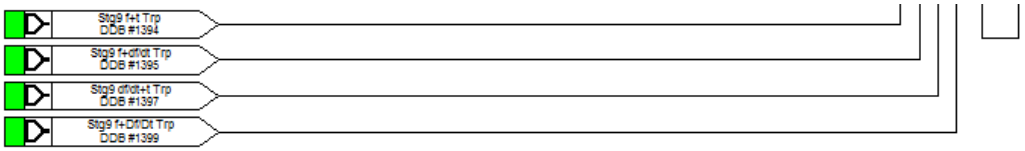


Figure B.6: Trip output mapping

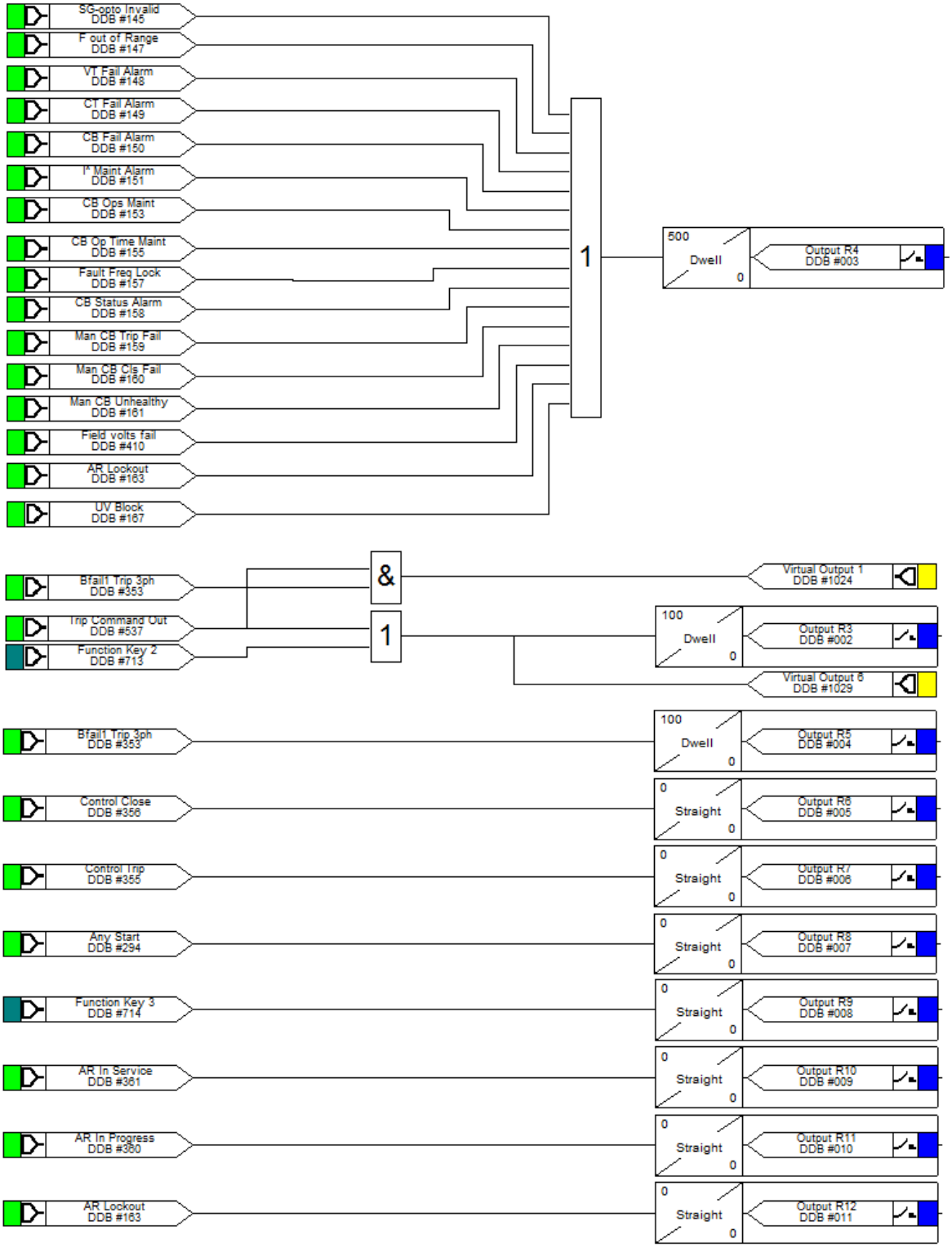


Figure B.7: Output relay mapping

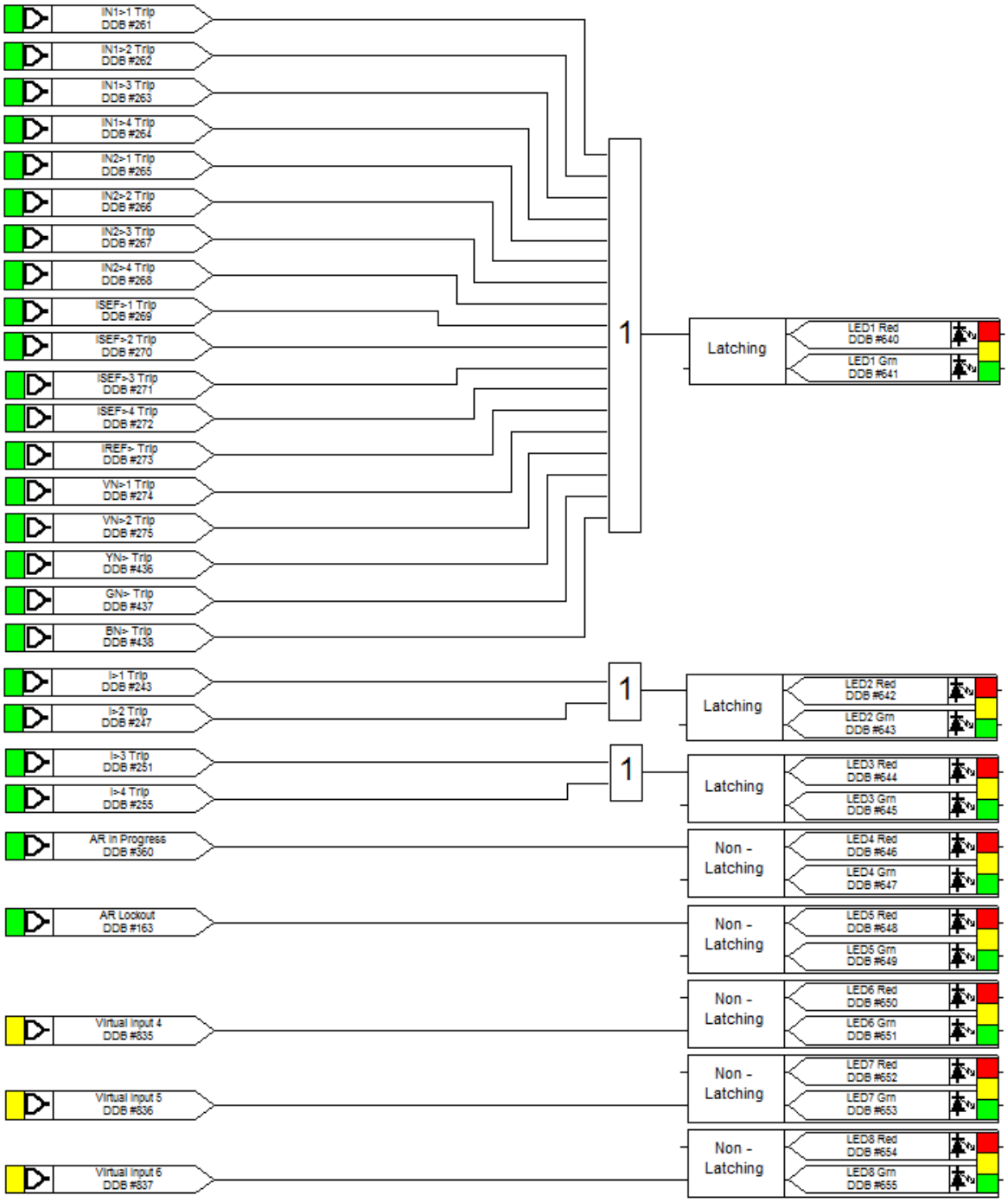
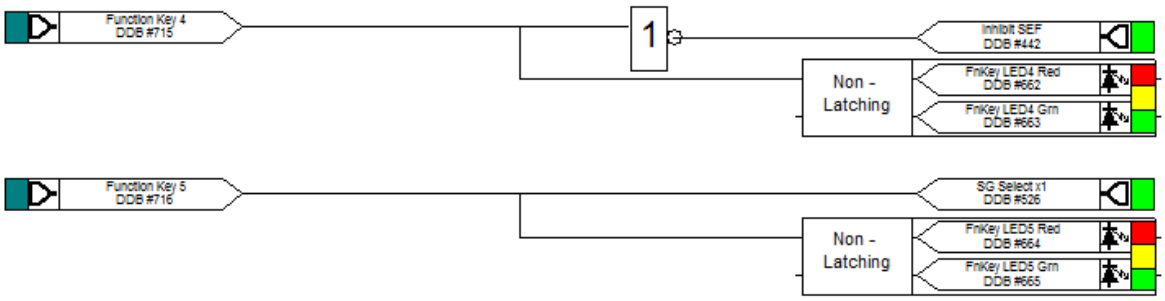


Figure B.8: LED mapping



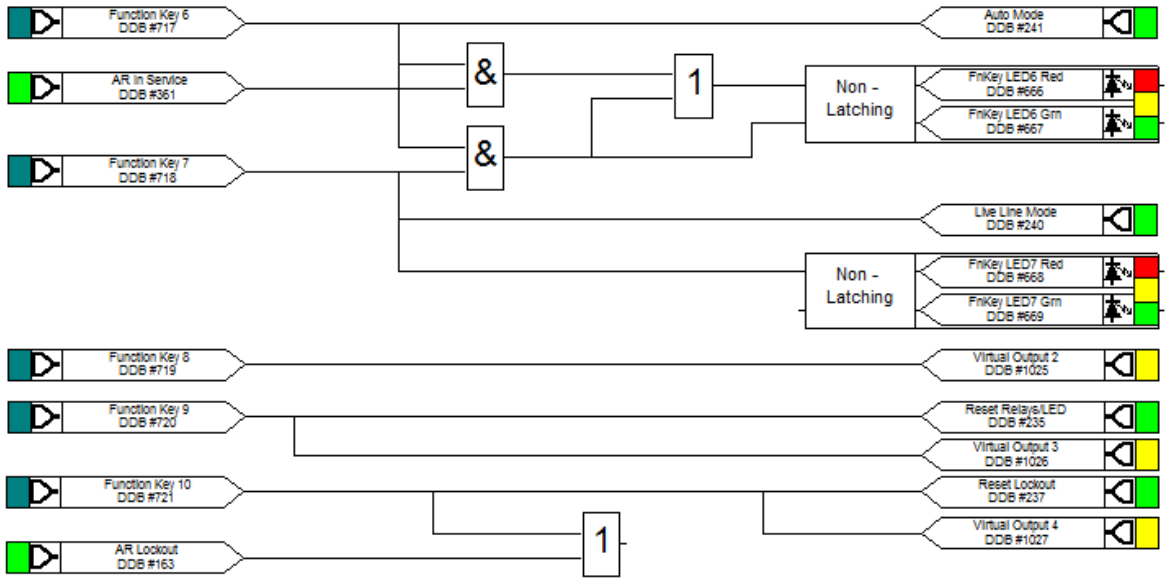


Figure B.9: Function key mapping

APPENDIX C

C.1 Unsymmetrical Faults

Most faults that occur on power systems are a result of unsymmetrical faults. Unsymmetrical faults come in single phase-to-ground, phase-to-phase or double phase-to-ground faults. Unsymmetrical faults give rise to unbalanced fault currents and phase displacements. During the occurrence of an unsymmetrical fault, the source voltage and system impedances are symmetrical within primary equipment (i.e. generators, synchronous reactors and transmission lines).

C.1.1 Single phase-to-ground fault

A single phase-to-ground fault is produced mainly from the breaking of conductors that come into contact with ground structures. Figure C.1 illustrates an fault impedance (Z_f) on phase A of the line. The conditions at the fault bus (k) are expressed as $I_{fb} = 0$, $I_{fc} = 0$ and $V_{ka} = Z_f I_{fa}$.

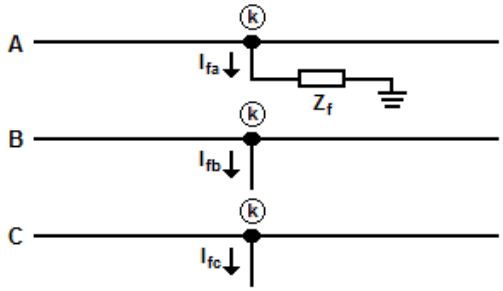


Figure C.1: Single phase-to-ground fault

With $I_{fb} = I_{fc} = 0$, the symmetrical components of the current are given by:

$$\begin{bmatrix} I_{fa}^{(0)} \\ I_{fa}^{(1)} \\ I_{fa}^{(2)} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix}\begin{bmatrix} I_{fa} \\ 0 \\ 0 \end{bmatrix}$$

where the multiplication yields

$$I_{fa}^{(0)} = I_{fa}^{(1)} = I_{fa}^{(2)} = \frac{I_{fa}}{3} \qquad \text{(C.1)}$$

Substituting $I_{fa}^{(0)}$ into $I_{fa}^{(1)}$ and $I_{fa}^{(2)}$ results in $I_{fa} = 3I_{fa}^{(0)}$. The terminal voltage of the positive, negative and zero sequence components for phase A can be found as:

$$\begin{aligned} V_{ka}^{(0)} &= -Z_{kk}^{(0)} I_{fa}^{(0)} \\ V_{ka}^{(1)} &= V_f - Z_{kk}^{(1)} I_{fa}^{(0)} \\ V_{ka}^{(2)} &= -Z_{kk}^{(2)} I_{fa}^{(0)} \end{aligned} \qquad \text{(C.2)}$$

Summing these equations produces:

$$V_{ka} = V_{ka}^{(0)} + V_{ka}^{(1)} + V_{ka}^{(2)} = V_f - \left(Z_{kk}^{(0)} + Z_{kk}^{(1)} + Z_{kk}^{(2)}\right) I_{fa}^{(0)} = 3Z_f I_{fa}^{(0)}$$

Solving for $I_{fa}^{(0)}$ and combining equation (C.1) results in the fault currents:

$$I_{fa}^{(0)} = I_{fa}^{(1)} = I_{fa}^{(2)} = \frac{V_f}{Z_{kk}^{(1)} + Z_{kk}^{(2)} + Z_{kk}^{(0)} + 3Z_f} \qquad \text{(C.3)}$$

Figure C.2 illustrates the Thevenin equivalent circuit of the positive, negative and zero sequence networks [46]. The sequence networks at bus (k) are in series with the fault impedance ($3Z_f$) and the prefault voltage source (V_f). The voltage and current across each sequence network is equal to the voltage V_{ka} and the current entering bus k.

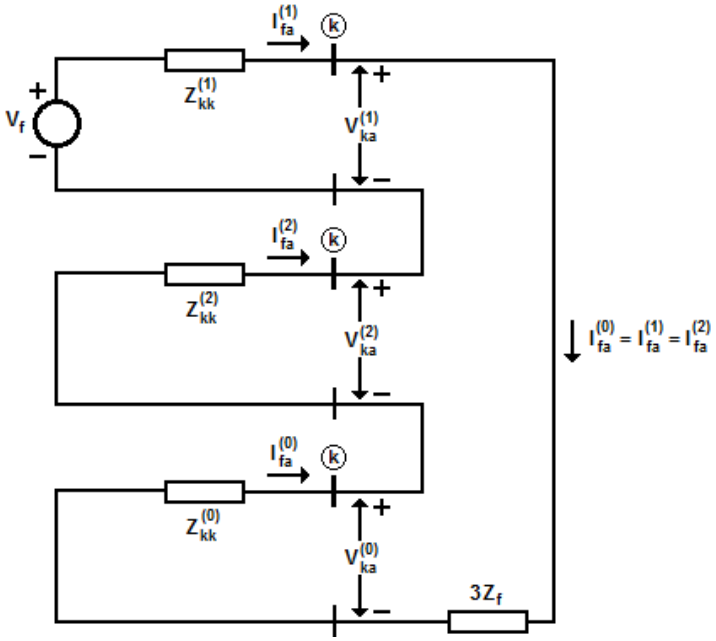


Figure C.2: Thevenin equivalent network of a single phase-to-ground fault

C.1.2 Phase-to-phase fault

A phase-to-phase fault between lines B and C is represented in Figure C.3. The conditions at fault bus (k) are expressed as $I_{fa} = 0$, $I_{fb} = -I_{fc}$, $V_{kb} - V_{kc} = I_{fb} Z_f$.

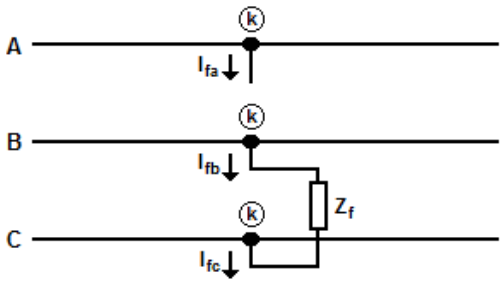


Figure C.3: Phase-to-phase fault

Since $I_{fb} = -I_{fc}$ and $I_{fa} = 0$, the symmetrical components of the current are given by:

$$\begin{bmatrix} I_{fa}^{(0)} \\ I_{fa}^{(1)} \\ I_{fa}^{(2)} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix}\begin{bmatrix} 0 \\ I_{fb} \\ -I_{fb} \end{bmatrix}$$

where the multiplication yields

$$I_{fa}^{(0)} = 0 \tag{C.4}$$

$$I_{fa}^{(1)} = -I_{fa}^{(2)} \tag{C.5}$$

The voltage at the zero sequence network is nil considering it is a dead network. To satisfy the requirement that $I_{fa}^{(1)} = -I_{fa}^{(2)}$, the Thevenin equivalent of the positive and negative sequence network is illustrated in Figure C.4 [46]. The voltage equation $V_{kb} - V_{kc} = I_{fb}Z_f$ is expanded as follows:

$$\begin{aligned} V_{kb} - V_{kc} &= \left(V_{kb}^{(1)} + V_{kb}^{(2)}\right) - \left(V_{kc}^{(1)} + V_{kc}^{(2)}\right) = \left(V_{kb}^{(1)} - V_{kc}^{(1)}\right) + \left(V_{kb}^{(2)} - V_{kc}^{(2)}\right) \\ &= \left(a^2 - a\right)V_{ka}^{(1)} + \left(a - a^2\right)V_{ka}^{(2)} = \left(a^2 - a\right)\left(V_{ka}^{(1)} - V_{ka}^{(2)}\right) \\ I_{fb}Z_f &= \left(I_{fb}^{(1)} + I_{fb}^{(2)}\right)Z_f = \left(a^2 I_{fa}^{(1)} + aI_{fa}^{(2)}\right)Z_f \end{aligned}$$

Equating both terms and setting $I_{fa}^{(2)} = -I_{fa}^{(1)}$ leads to the voltage drop:

$$\left(a^2 - a\right)\left(V_{ka}^{(1)} - V_{ka}^{(2)}\right) = \left(a^2 - a\right)I_{fa}^{(1)}Z_f$$

$$V_{ka}^{(1)} - V_{ka}^{(2)} = I_{fa}^{(1)}Z_f \tag{C.6}$$

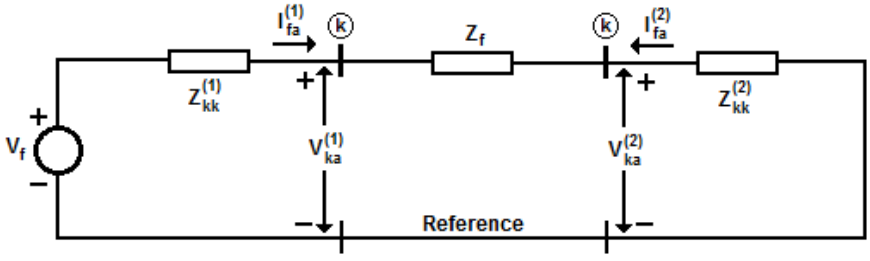


Figure C.4: Thevenin equivalent network of a phase-to-phase fault

The positive sequence current is determined by:

$$I_{fa}^{(1)} = -I_{fa}^{(2)} = \frac{V_f}{Z_{kk}^{(1)} + Z_{kk}^{(2)} + Z_f} \tag{C.7}$$

C.1.3 Double phase-to-ground fault

A double phase-to-ground fault is shown in Figure C.5 where the conditions at the fault bus are expressed as $I_{fa} = 0$ and $V_{kb} = V_{kc} = (I_{fb} + I_{fc})Z_f$.

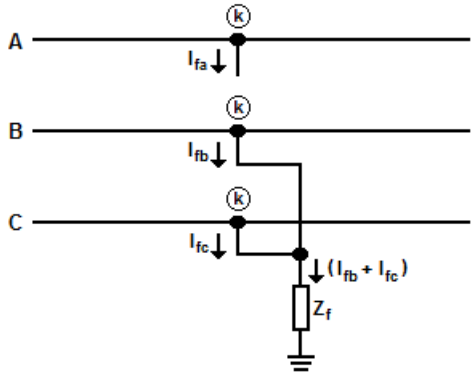


Figure C.5: Double phase-to-ground fault

The zero sequence current is $I_{fa}^{(0)} = (I_{fb} + I_{fc})/3$ where the voltage becomes:

$$V_{kb} = V_{kc} = 3Z_f I_{fa}^{(0)} \tag{C.8}$$

Substituting V_{kb} for V_{kc} in the symmetrical component yields:

$$\begin{bmatrix} V_{ka}^{(0)} \\ V_{ka}^{(1)} \\ V_{ka}^{(2)} \end{bmatrix} = \frac{1}{3}\begin{bmatrix} 1 & 1 & 1 \\ 1 & a & a^2 \\ 1 & a^2 & a \end{bmatrix}\begin{bmatrix} V_{ka} \\ V_{kb} \\ V_{kb} \end{bmatrix} \tag{C.9}$$

The second and third row of Equation (C.9) demonstrates that $V_{ka}^{(1)} = V_{ka}^{(2)}$, while the first row states $3V_{ka}^{(0)} = V_{ka} + 2V_{kb} = (V_{ka}^{(0)} + V_{ka}^{(1)} + V_{ka}^{(2)}) + 2(3Z_f I_{fa}^{(0)})$. Collecting the zero sequence terms and setting $V_{ka}^{(2)} = V_{ka}^{(1)}$ produces:

$$V_{ka}^{(1)} = V_{ka}^{(0)} = -3Z_f I_{fa}^{(0)} \tag{C.10}$$

Bringing together Equation (C.10) and declaring $V_{ka}^{(1)} = V_{ka}^{(2)}$ results in:

$$V_{ka}^{(1)} = V_{ka}^{(2)} = V_{ka}^{(0)} - 3Z_f I_{fa}^{(0)}$$

$$I_{fa}^{(0)} + I_{fa}^{(1)} + I_{fa}^{(2)} = 0 \tag{C.11}$$

These equations are satisfied when all three of the sequence networks are connected in parallel as depicted in Figure C.6. The diagram of the network connections show

that the positive sequence current $I_{fa}^{(1)}$ is determined by applying the prefault voltage V_f across the total impedance consisting of $Z_{kk}^{(1)}$ in series with the parallel combination of $Z_{kk}^{(2)}$ and $\left(Z_{kk}^{(0)} + 3Z_f\right)$ [46]. This provides:

$$I_{fa}^{(1)} = \frac{V_f}{Z_{kk}^{(1)} + \left[\frac{Z_{kk}^{(2)}\left(Z_{kk}^{(0)} + 3Z_f\right)}{Z_{kk}^{(2)} + Z_{kk}^{(0)} + 3Z_f}\right]} \tag{C.12}$$

The negative and zero sequence currents out of the system and into the fault can be determined through the process of current division:

$$I_{fa}^{(2)} = -I_{fa}^{(1)}\left[\frac{Z_{kk}^{(0)} + 3Z_f}{Z_{kk}^{(2)} + Z_{kk}^{(0)} + 3Z_f}\right] \tag{C.13}$$

$$I_{fa}^{(0)} = -I_{fa}^{(1)}\left[\frac{Z_{kk}^{(2)}}{Z_{kk}^{(2)} + Z_{kk}^{(0)} + 3Z_f}\right] \tag{C.14}$$

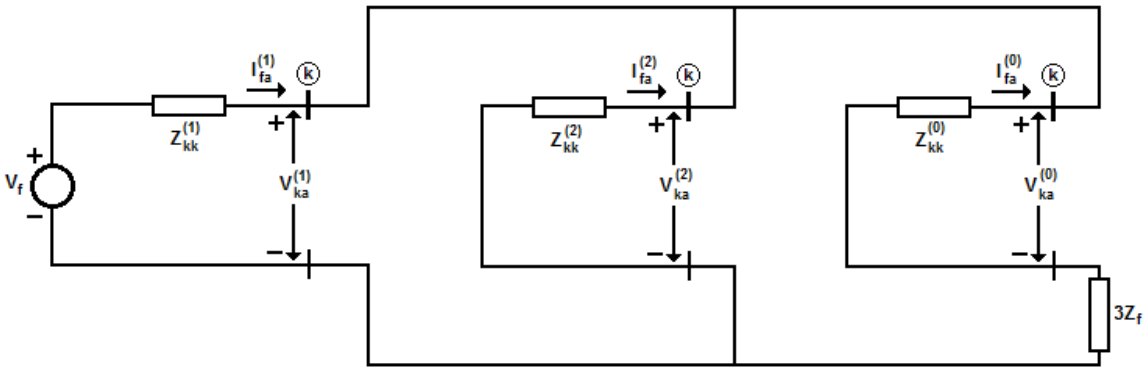


Figure C.6: Thevenin equivalent network of a double phase-to-ground fault

APPENDIX D

D.1 Relay Reach

D.1.1 Single phase-to-ground fault

From Zone	To Zone	Z nominal	Z actual	Z min	Z max	Deviation	Result
Zone 0	Zone 1	4.120 Ω	4.115 Ω	3.914 Ω	4.326 Ω	-0.1172 %	Passed
Zone 1	Zone 2	6.544 Ω	6.480 Ω	6.217 Ω	6.871 Ω	-0.9766 %	Passed
Zone 2	Zone 3	10.72 Ω	10.62 Ω	10.18 Ω	11.26 Ω	-0.9766 %	Passed
Zone 3	Zone 4	13.91 Ω	13.73 Ω	13.21 Ω	14.60 Ω	-1.289 %	Passed

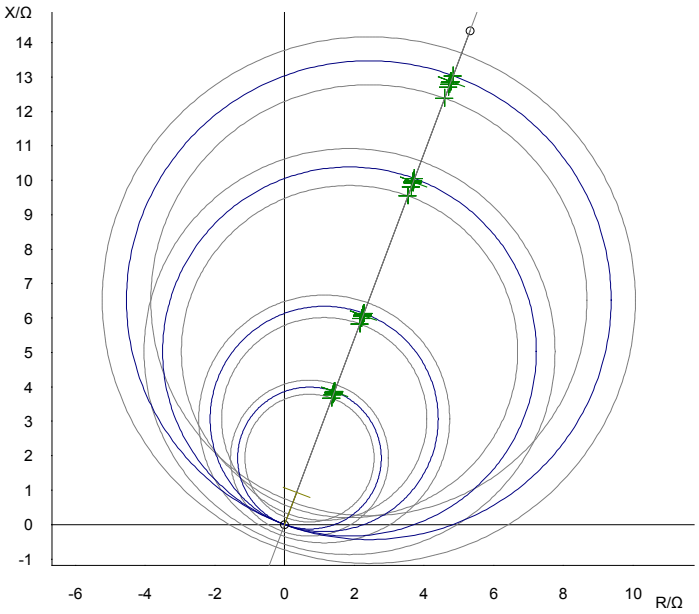


Figure D.1: SEL-311L relay reach for a single phase-to-ground fault

D.1.2 Phase-to-phase fault

From Zone	To Zone	Z nominal	Z actual	Z min	Z max	Deviation	Result
Zone 0	Zone 1	4.120 Ω	4.118 Ω	3.914 Ω	4.326 Ω	-0.03906 %	Passed
Zone 1	Zone 2	6.544 Ω	6.516 Ω	6.217 Ω	6.871 Ω	-0.4297 %	Passed
Zone 2	Zone 3	10.72 Ω	10.67 Ω	10.18 Ω	11.26 Ω	-0.4297 %	Passed
Zone 3	Zone 4	13.91 Ω	13.84 Ω	13.21 Ω	14.60 Ω	-0.5078 %	Passed

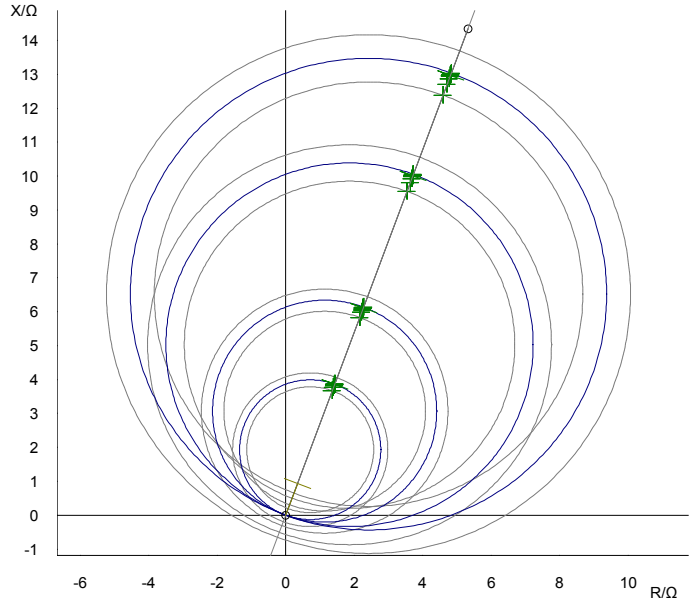


Figure D.2: SEL-311L relay reach for a phase-to-phase fault

D.1.3 Three phase fault

From Zone	To Zone	Z nominal	Z actual	Z min	Z max	Deviation	Result
Zone 0	Zone 1	4.120 Ω	4.122 Ω	3.914 Ω	4.326 Ω	0.03906 %	Passed
Zone 1	Zone 2	6.544 Ω	6.531 Ω	6.217 Ω	6.871 Ω	-0.1953 %	Passed
Zone 2	Zone 3	10.72 Ω	10.70 Ω	10.18 Ω	11.26 Ω	-0.1953 %	Passed
Zone 3	Zone 4	13.91 Ω	13.87 Ω	13.21 Ω	14.60 Ω	-0.2734 %	Passed

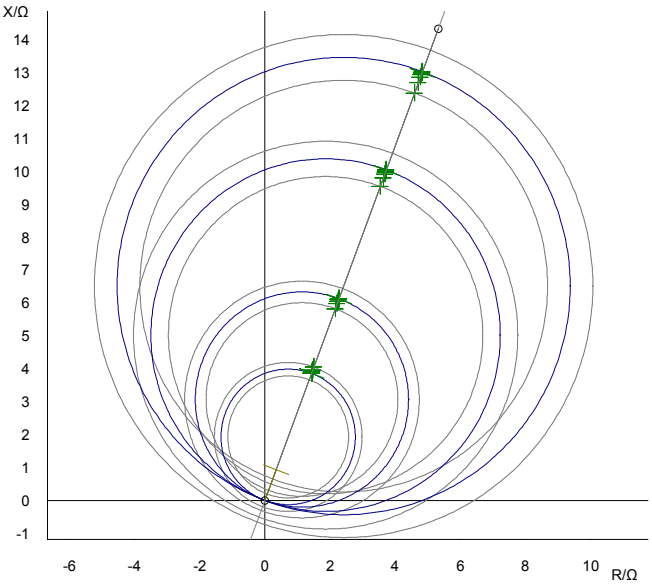


Figure D.3: SEL-311L relay reach for a three phase fault

D.2 Fault Records

D.2.1 No fault

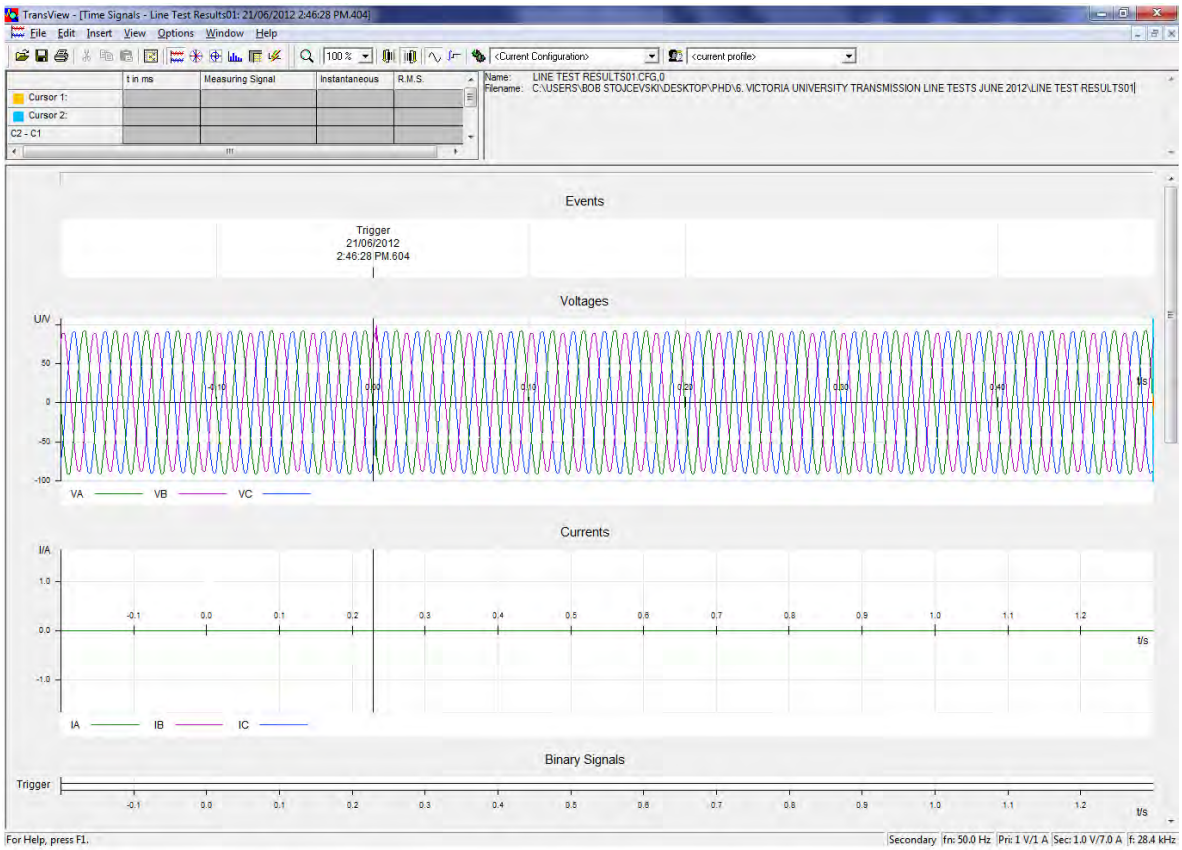


Figure D.4: Time signals

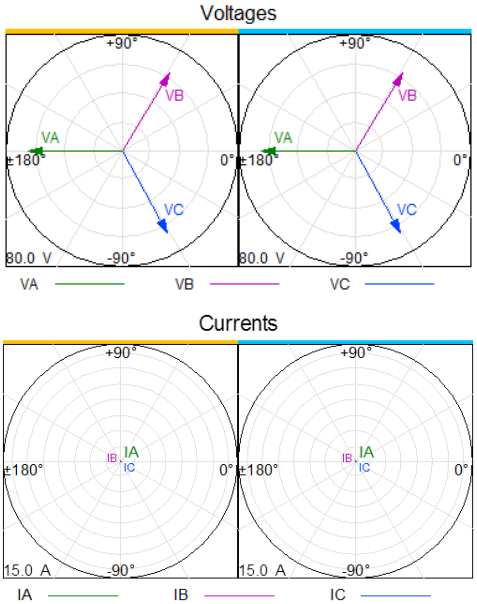


Figure D.5: Vector diagrams

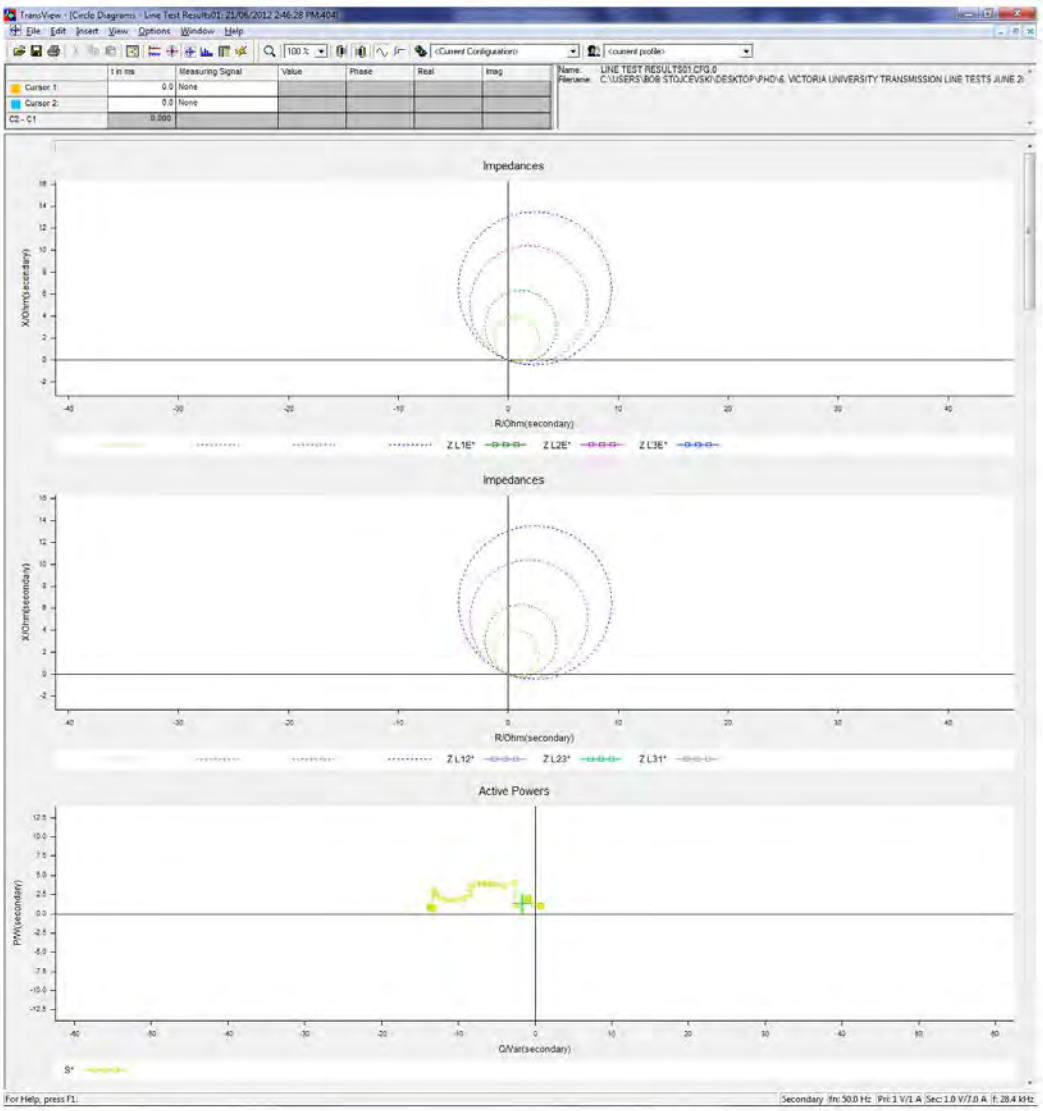


Figure D.6: Circle diagrams

D.2.2 Single phase-to-ground fault (Segment 1: 0-75km)

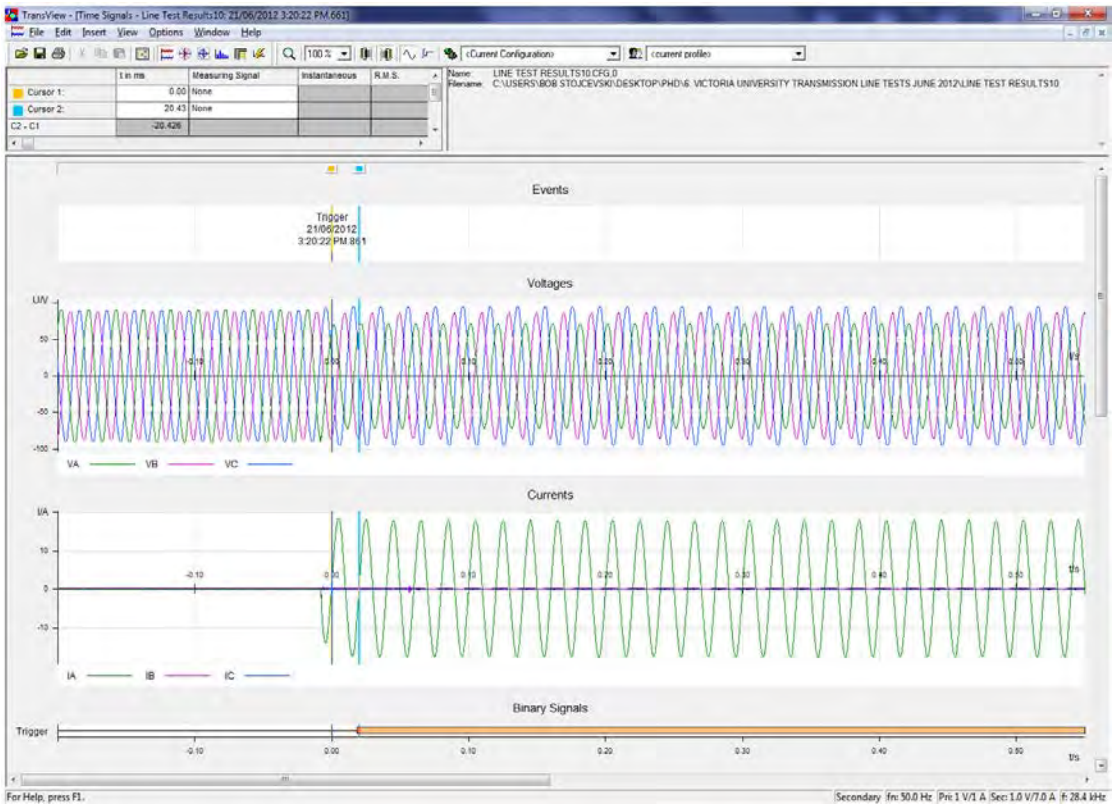
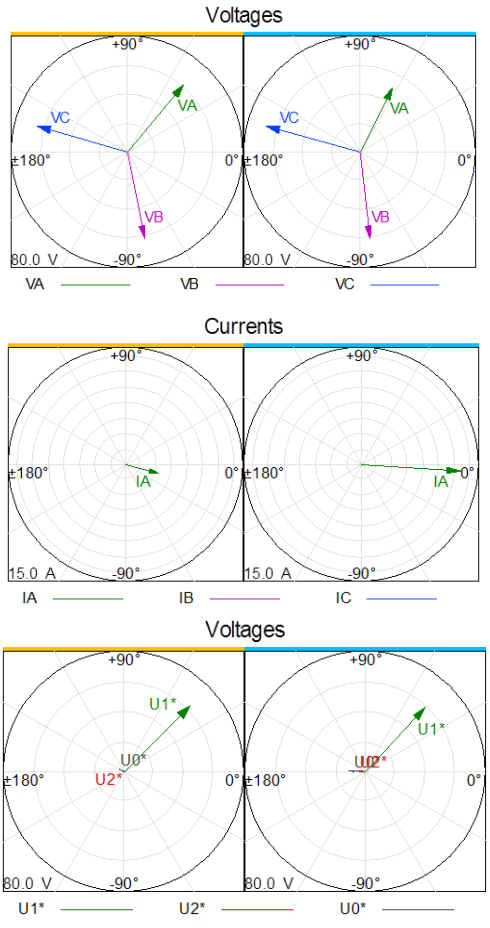


Figure D.7: Time signals



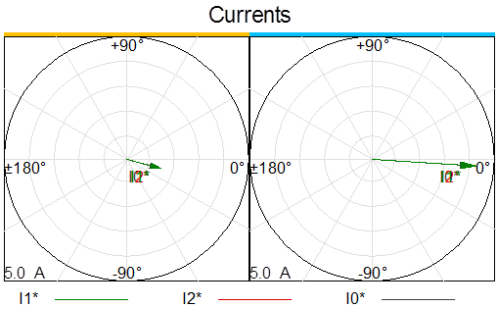


Figure D.8: Vector diagrams

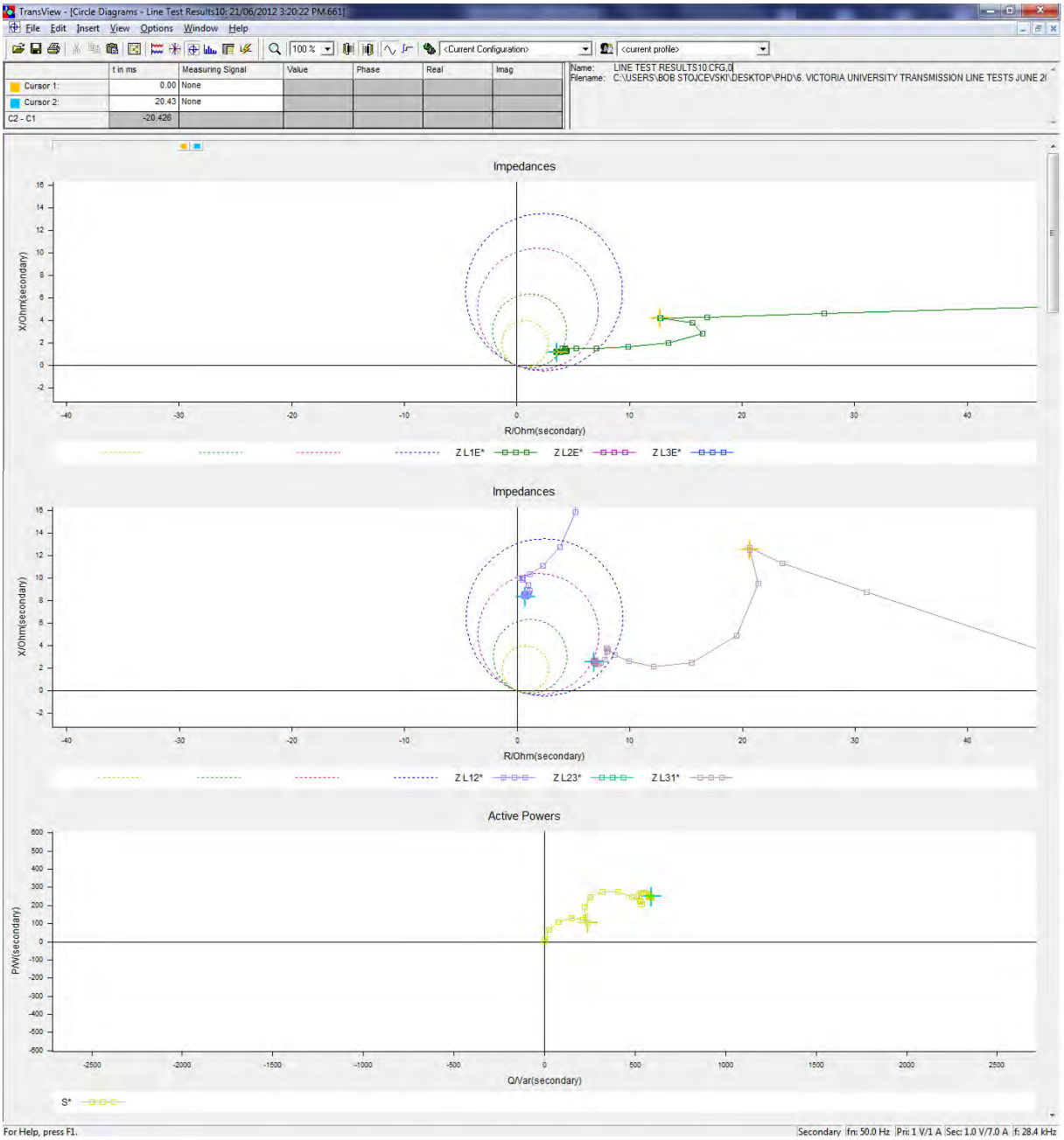
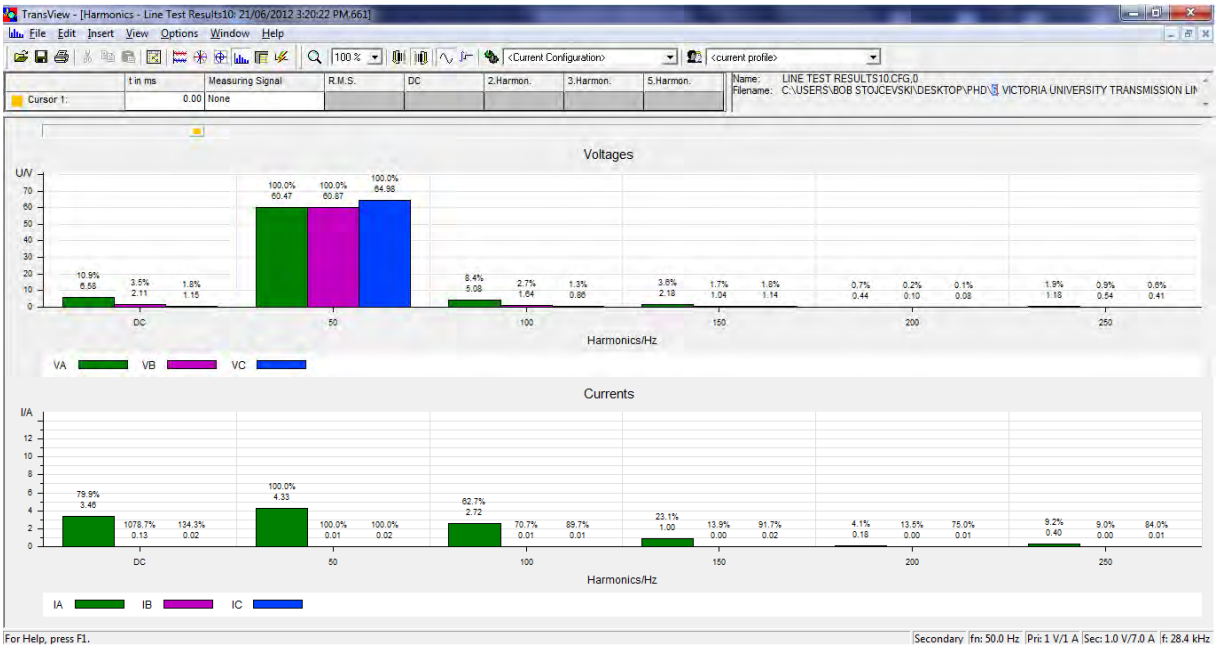


Figure D.9: Circle diagrams



Measuring Signal	Value	Phase	Extremum	DC	2.Harmon.	3.Harmon.	5.Harmon.
IA	4.32 A	-15.8°	-14.10 A	-79.9%	62.7%	23.1%	9.2%
IB	0.012 A	175.1°	0.152 A	1078.7%	70.7%	13.9%	9.0%
IC	16.6 mA	174.6°	-62.04 mA	-134.3%	89.7%	91.7%	84.0%
VA	60.4 V	50.5°	-82.36 V	10.9%	8.4%	3.6%	1.9%
VB	60.9 V	-78.6°	-87.41 V	3.5%	2.7%	1.7%	0.9%
VC	65.0 V	163.6°	94.01 V	1.8%	1.3%	1.8%	0.6%

Figure D.10: Harmonics

D.2.3 Single phase-to-ground fault (Segment 2: 75-150km)

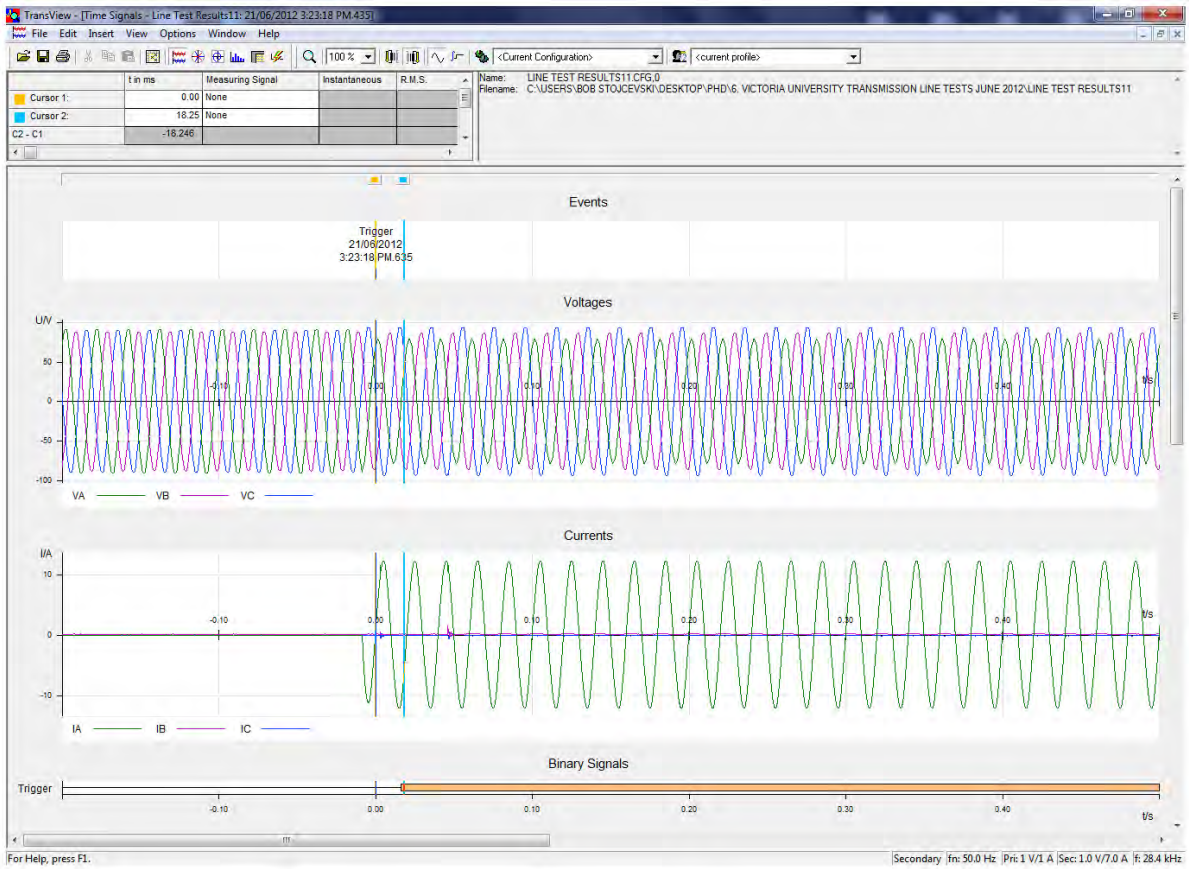


Figure D.11: Time signals

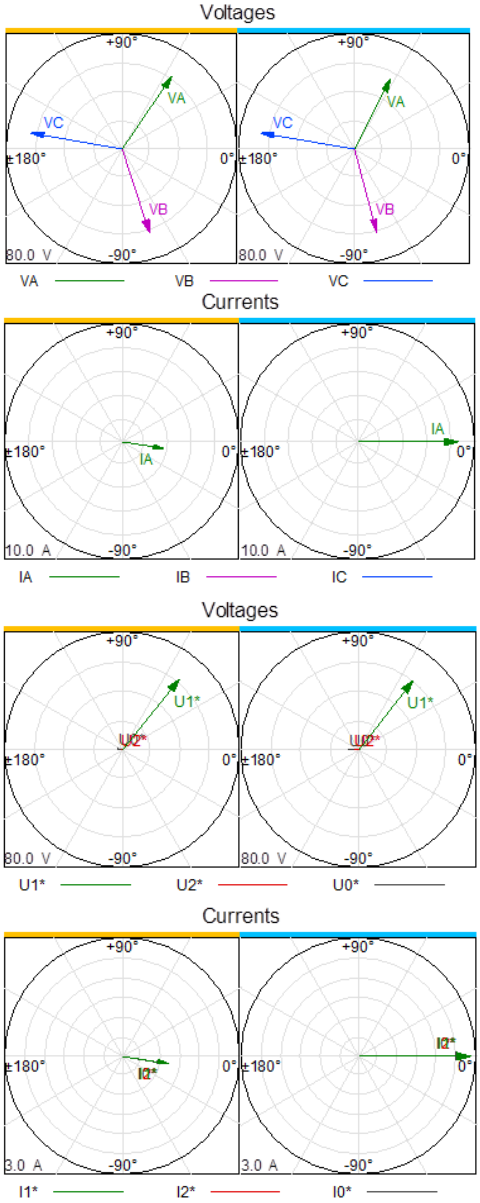
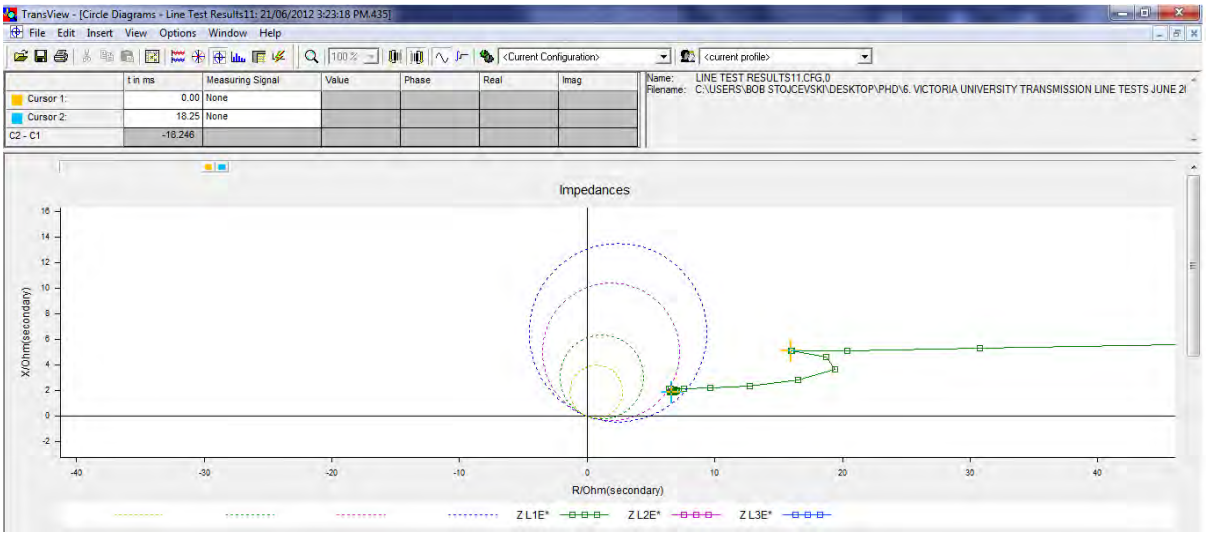


Figure D.12: Vector diagrams



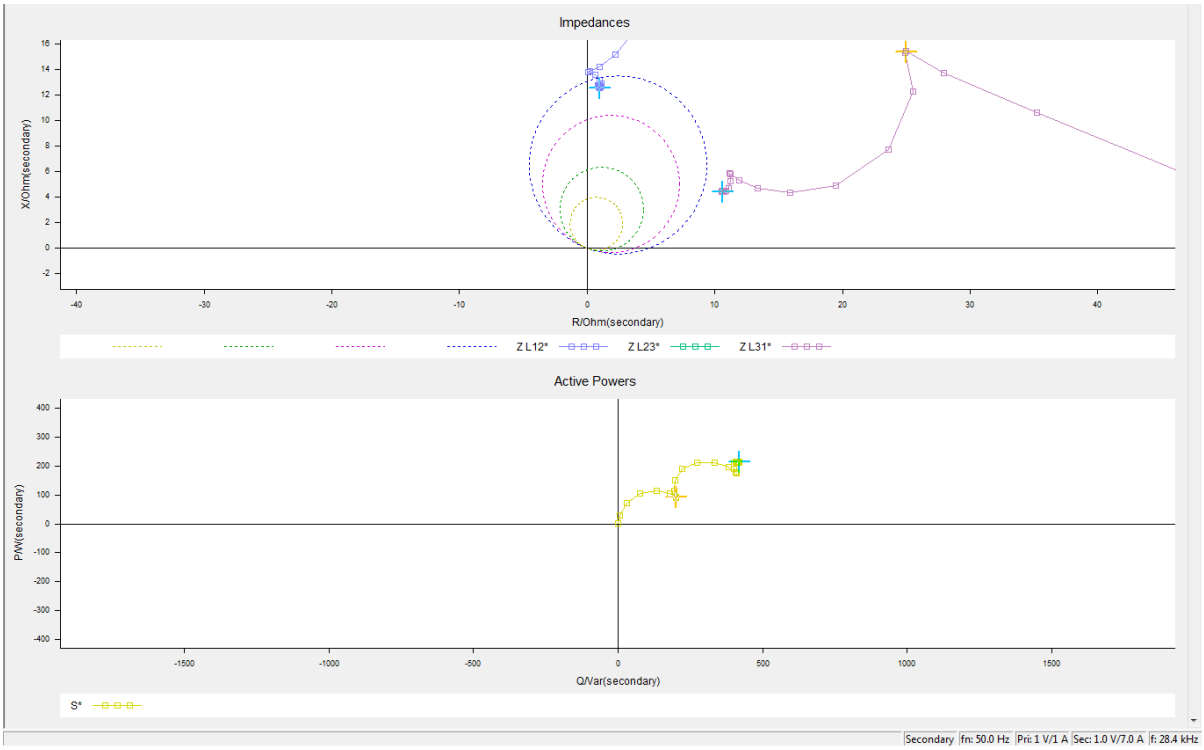
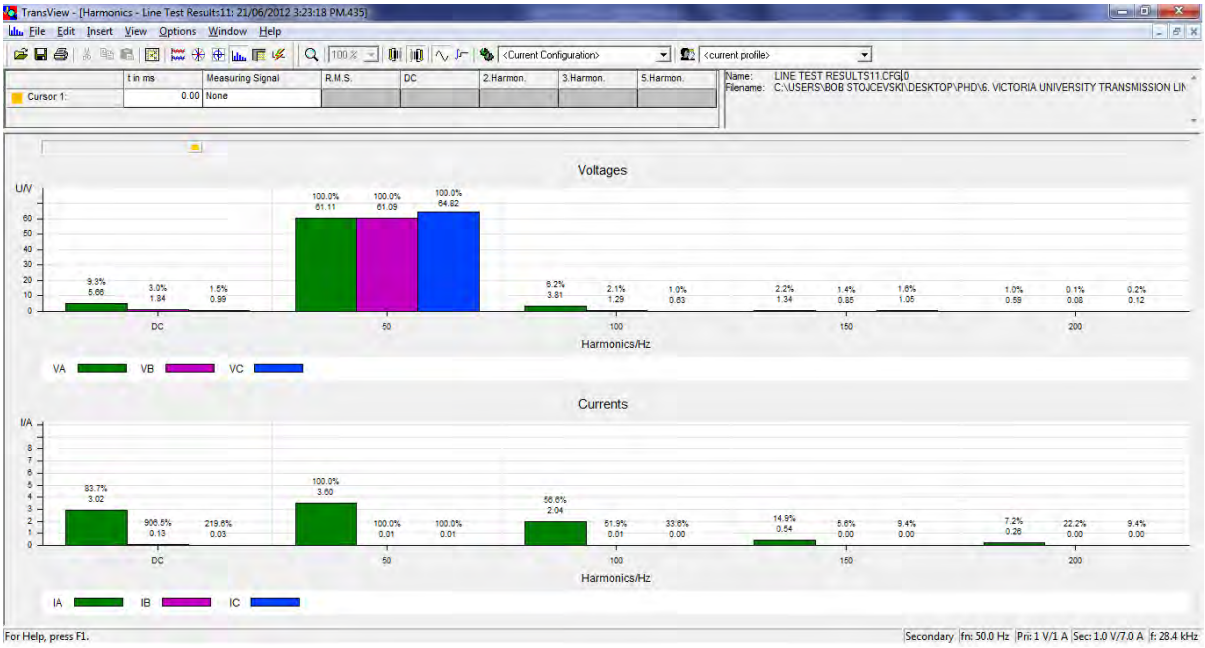


Figure D.13: Circle diagrams



Measuring Signal	Value	Phase	Extremum	DC	2.Harmon.	3.Harmon.	5.Harmon.
IA	3.59 A	-9.9°	-11.17 A	-83.7%	56.6%	14.9%	7.4%
IB	0.014 A	168.4°	0.191 A	906.5%	51.9%	5.6%	8.7%
IC	14.1 mA	140.1°	-23.95 mA	-219.6%	33.6%	9.4%	2.9%
VA	61.0 V	55.6°	-86.23 V	9.3%	6.2%	2.2%	1.5%
VB	61.1 V	-71.9°	-86.68 V	3.0%	2.1%	1.4%	0.9%
VC	64.8 V	169.8°	93.40 V	1.5%	1.0%	1.6%	0.7%

Figure D.14: Harmonics

D.2.4 Single phase-to-ground fault (Segment 3: 150-225km)

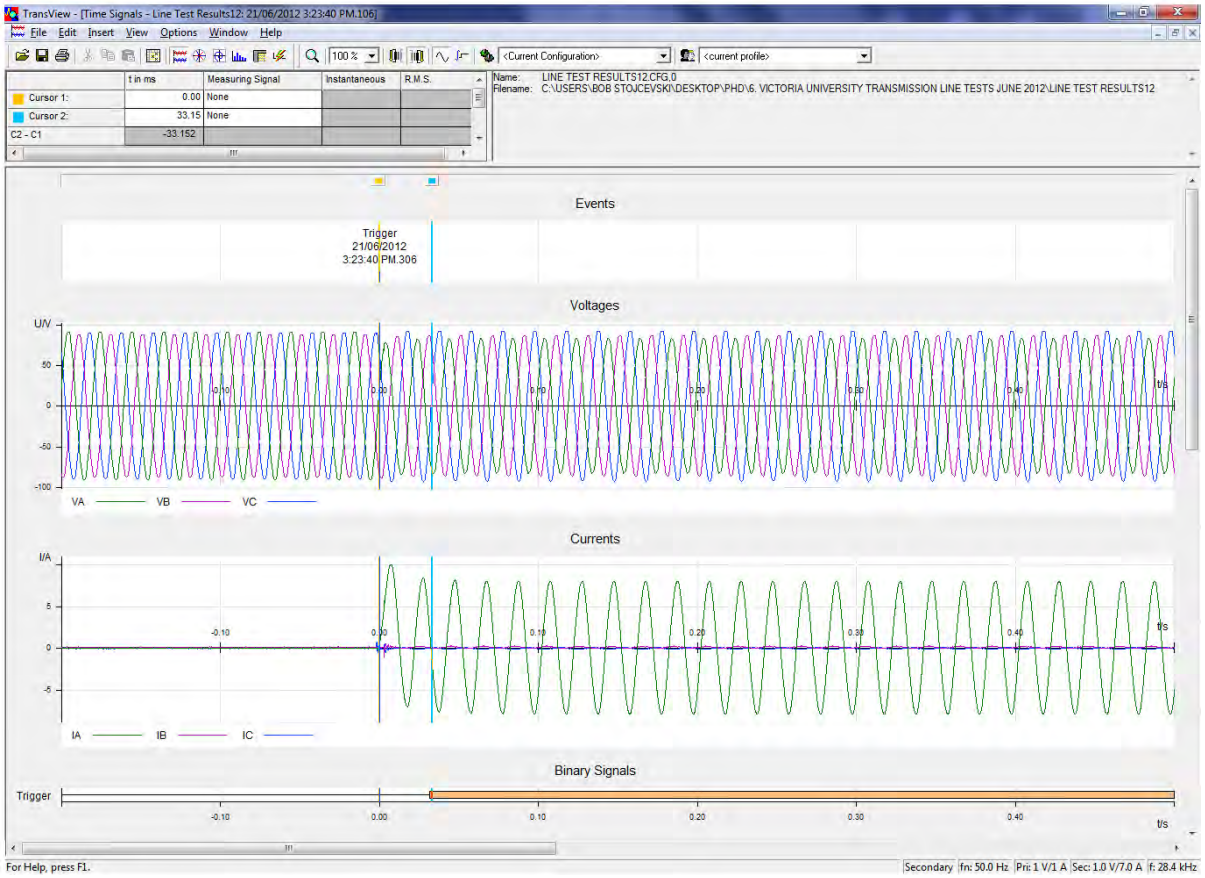
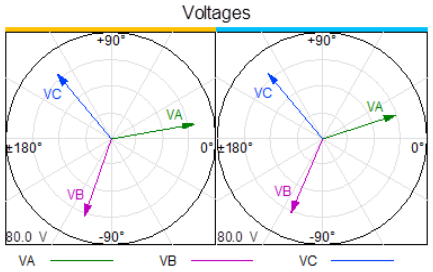
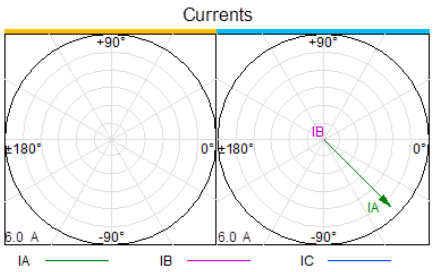
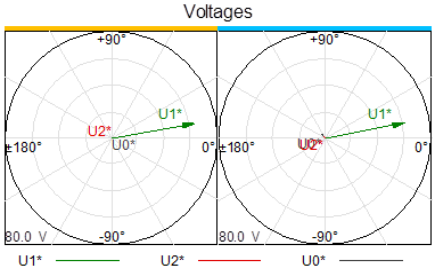


Figure D.15: Time signals







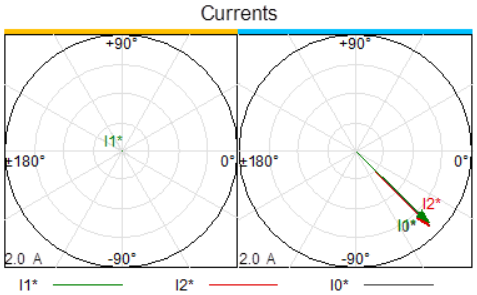


Figure D.16: Vector diagrams

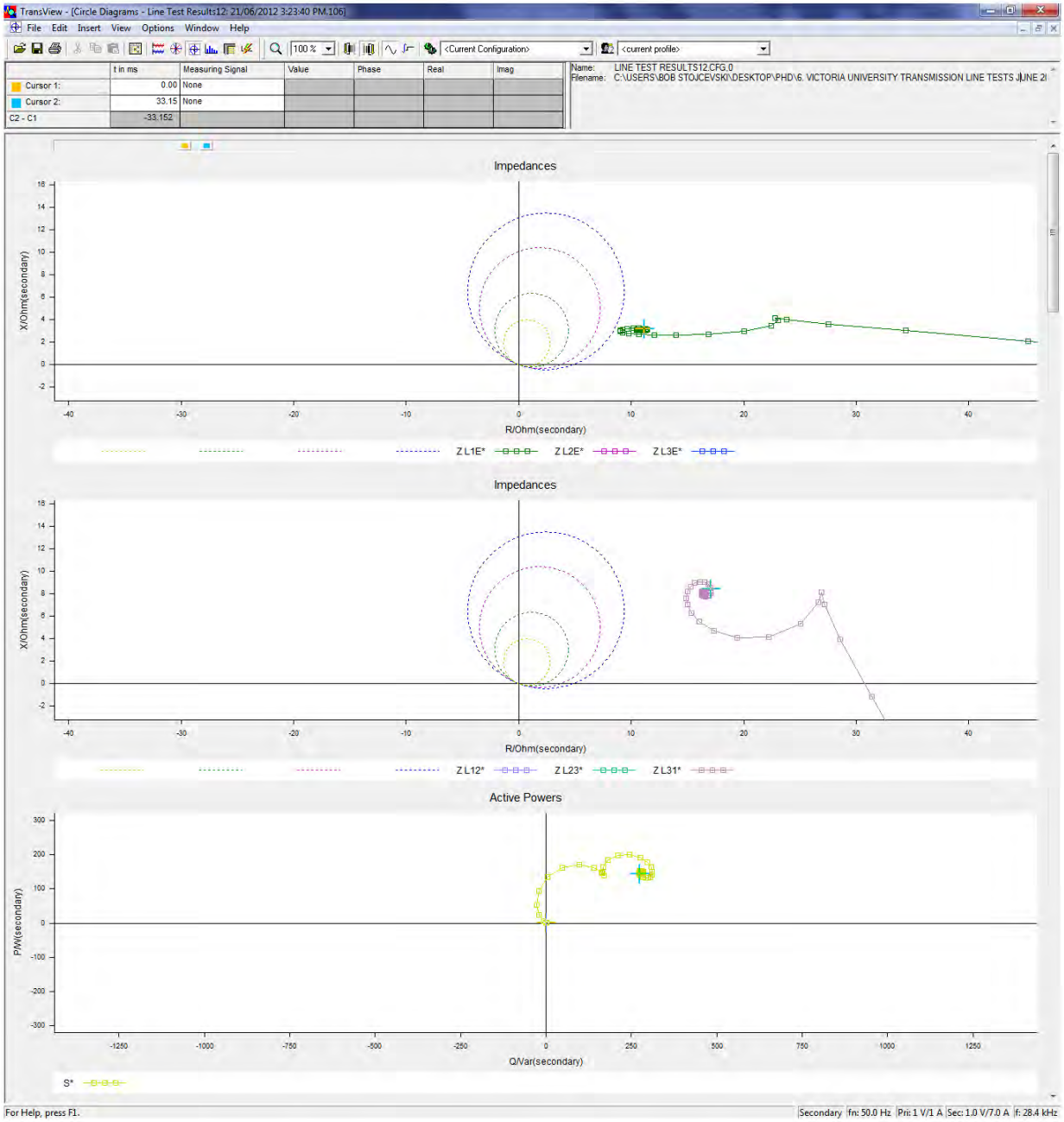
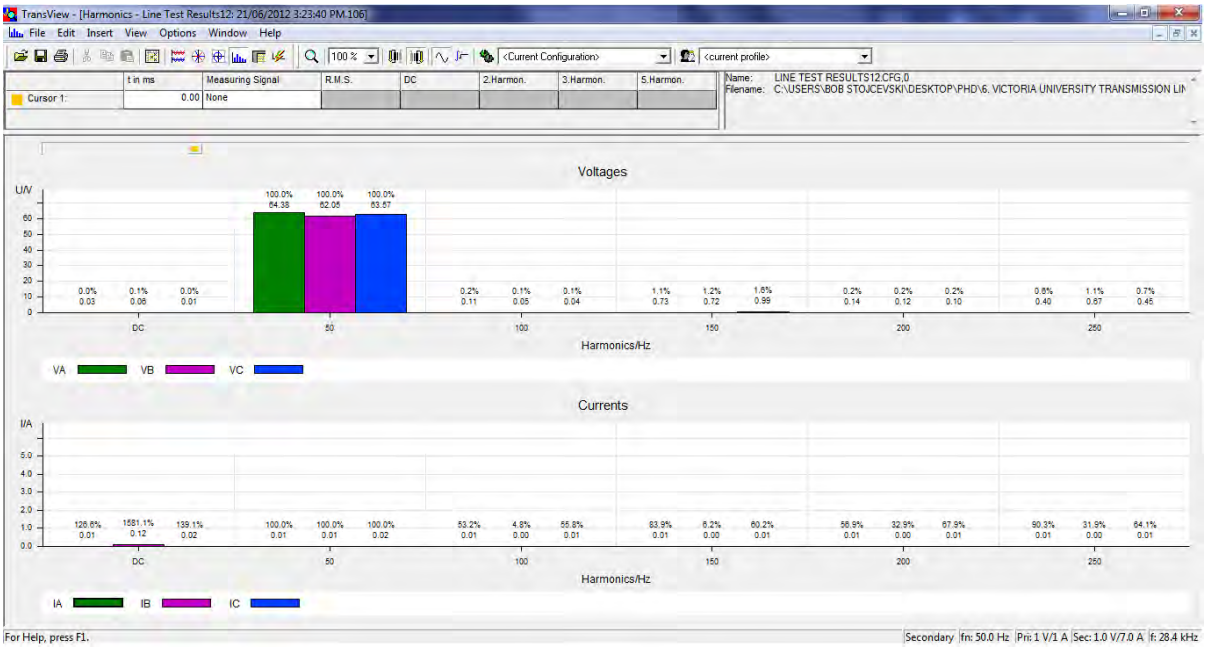


Figure D.17: Circle diagrams



Measuring Signal	Value	Phase	Extremum	DC	2.Harmon.	3.Harmon.	5.Harmon.
IA	0.012 A	15.2°	0.261 A	126.6%	53.2%	83.9%	90.3%
IB	0.0078 A	-155.7°	0.152 A	1581.1%	4.8%	6.2%	31.9%
IC	12.3 mA	105.2°	-290.7 mA	-139.1%	55.8%	60.2%	64.1%
VA	64.4 V	10.5°	-90.78 V	0.0%	0.2%	1.1%	0.6%
VB	62.1 V	-109.9°	87.66 V	0.1%	0.1%	1.2%	1.1%
VC	63.6 V	130.0°	89.29 V	-0.0%	0.1%	1.6%	0.7%

Figure D.18: Harmonics

D.2.5 Single phase-to-ground fault (Segment 4: 225-300km)

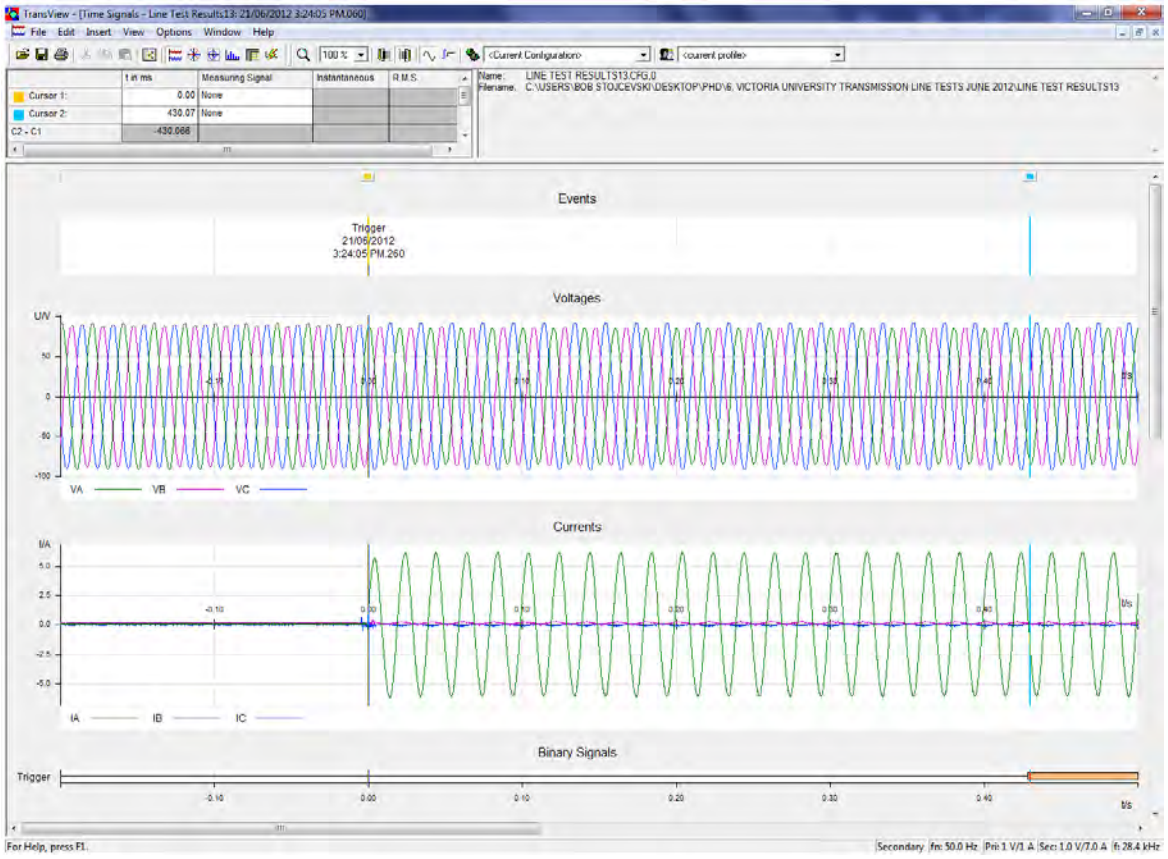


Figure D.19: Time signals

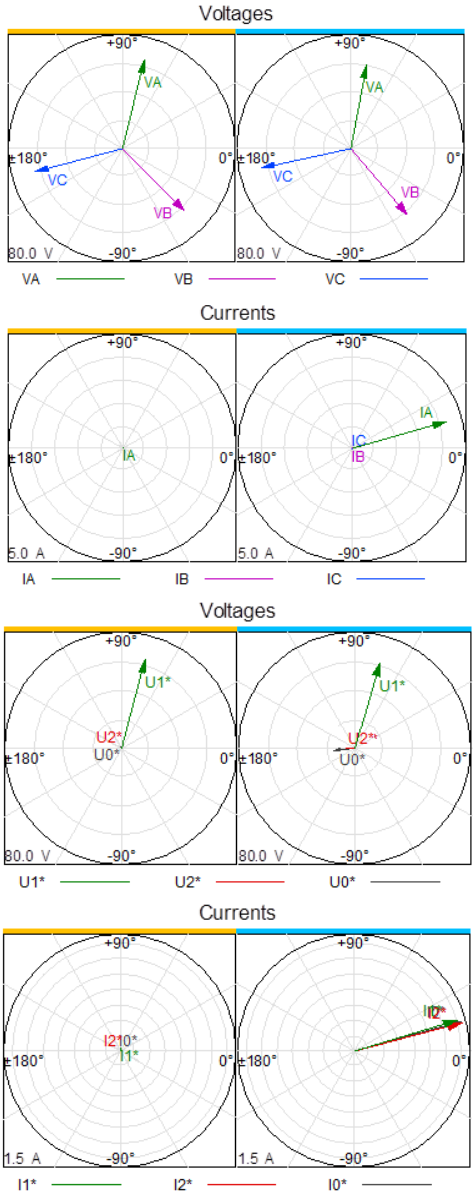
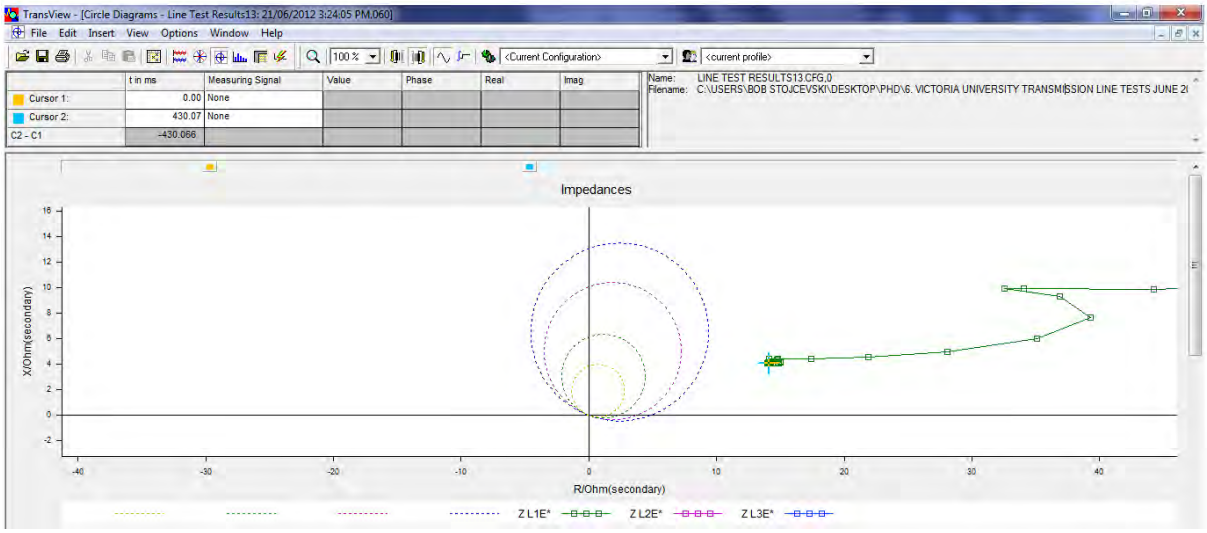


Figure D.20: Vector diagrams



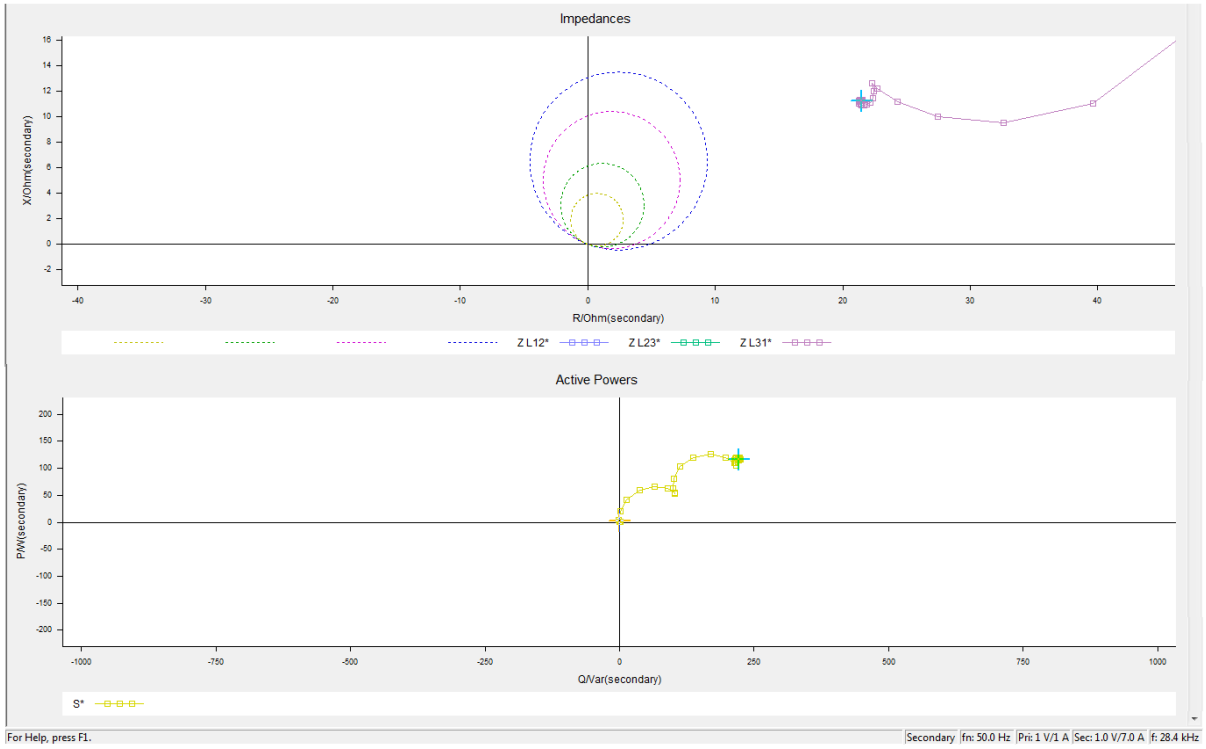
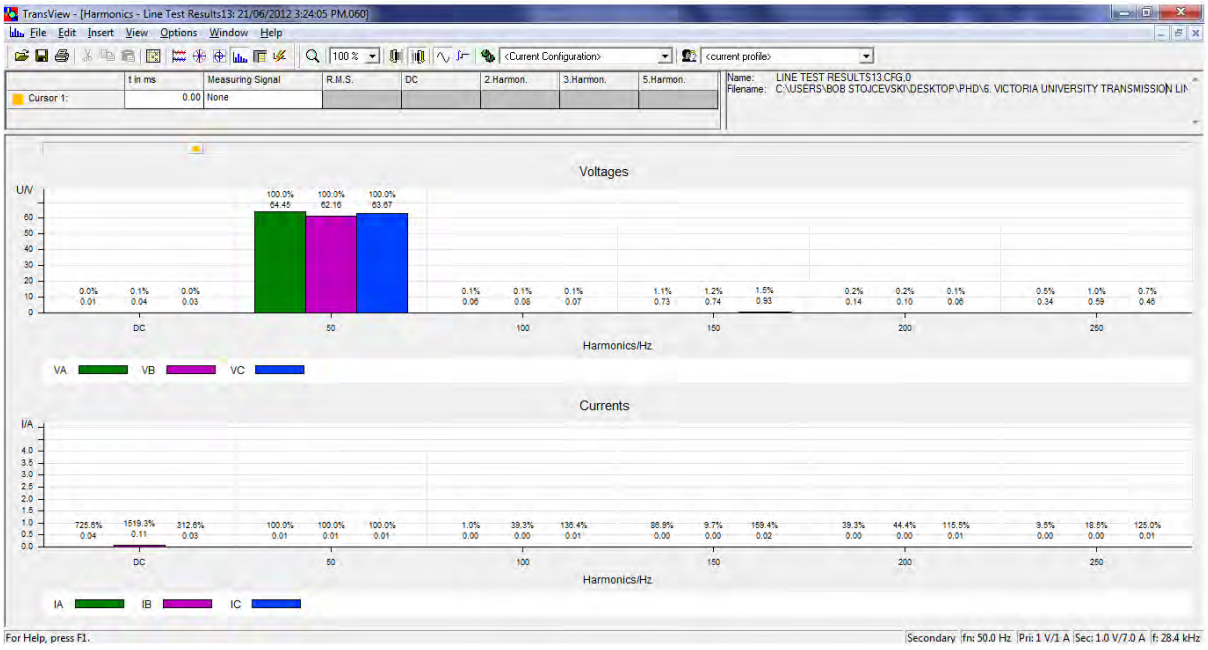


Figure D.21: Circle diagrams



Measuring Signal	Value	Phase	Extremum	DC	2.Harmon.	3.Harmon.	5.Harmon.
IA	0.029 A	64.9°	-0.0394 A	725.6%	1.0%	86.9%	9.5%
IB	7.16 mA	-51.3°	75.98 mA	1519.3%	39.3%	9.7%	18.5%
IC	13.2 mA	-144.3°	-62.05 mA	-312.6%	136.4%	159.4%	125.0%
VA	64.4 V	75.5°	85.57 V	-0.0%	0.1%	1.1%	0.5%
VB	62.2 V	-44.9°	-87.64 V	0.1%	0.1%	1.2%	1.0%
VC	63.7 V	-165.1°	-20.86 V	0.0%	0.1%	1.5%	0.7%

Figure D.22: Harmonics

D.2.6 Phase-to-phase fault (Segment 1: 0-75km)

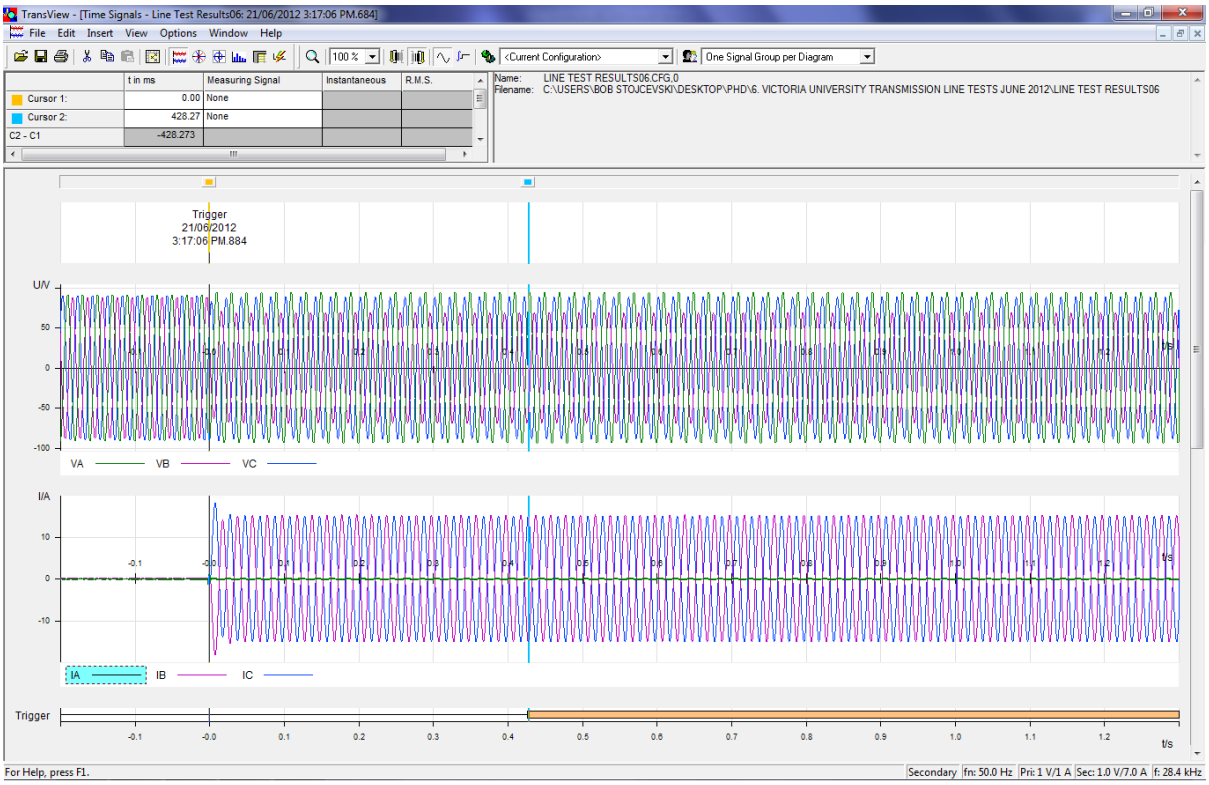
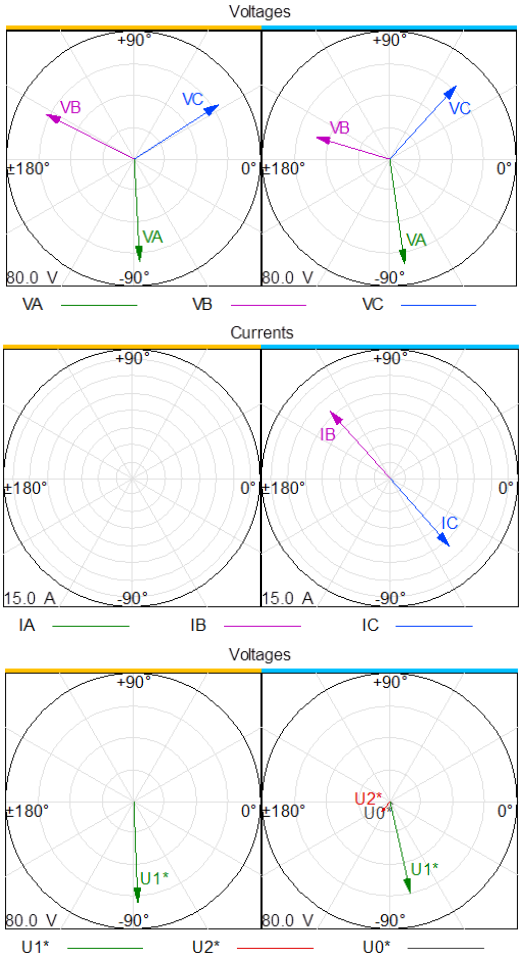


Figure D.23: Time signals



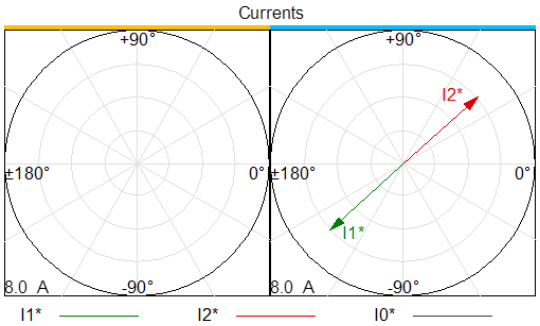


Figure D.24: Vector diagrams

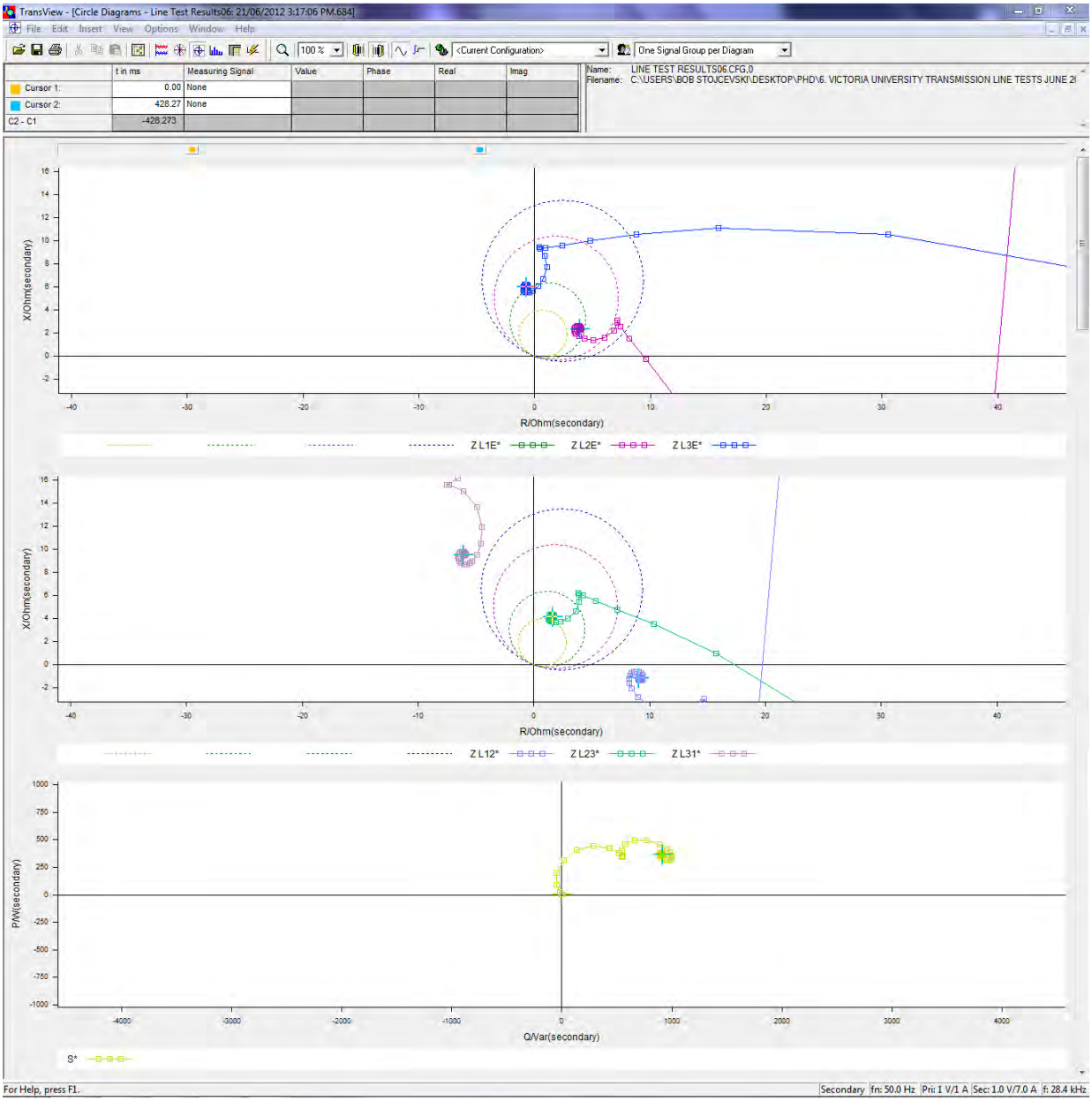
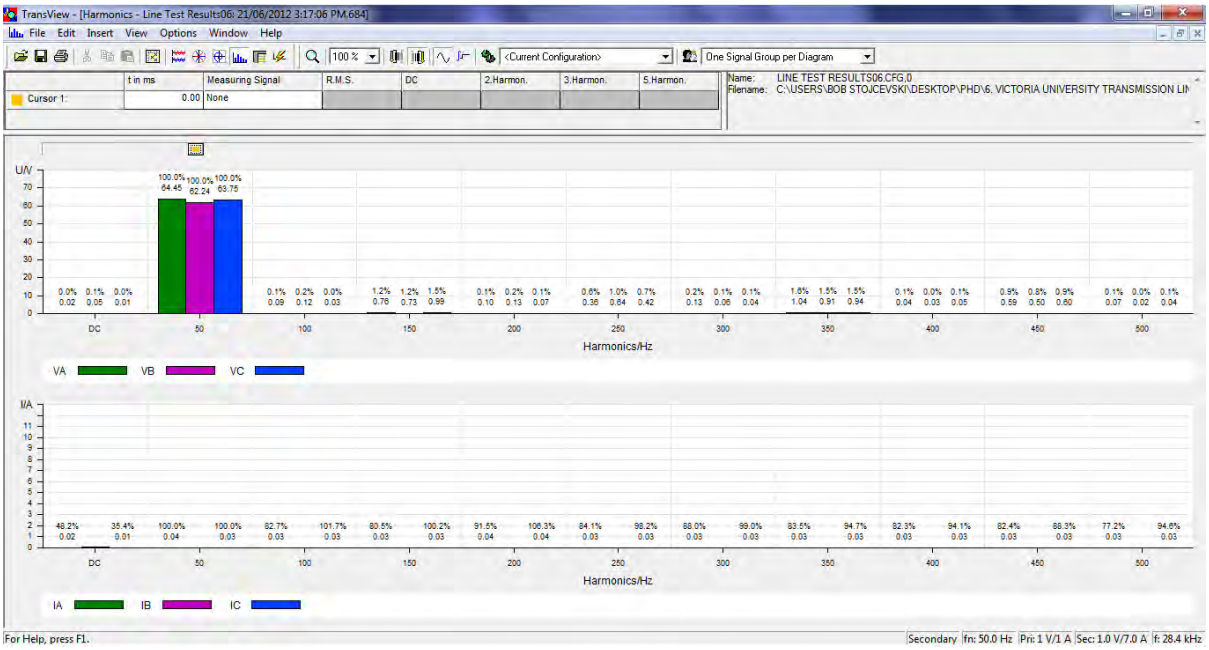


Figure D.25: Circle diagrams



Measuring Signal	Value	Phase	Extremum	DC	2.Harmon.	3.Harmon.	5.Harmon.
IA	0.018 A	-90.7°	-1.093 A	48.2%	82.7%	80.5%	84.1%
IB	0.0066 A	114.7°	0.152 A	1907.8%	40.4%	23.5%	13.0%
IC	0.013 A	71.1°	0.701 A	-35.4%	101.7%	100.2%	98.2%
VA	64.5 V	-86.7°	-89.67 V	0.0%	0.1%	1.2%	0.6%
VB	62.2 V	152.8°	87.62 V	0.1%	0.2%	1.2%	1.0%
VC	63.8 V	32.9°	31.47 V	0.0%	0.0%	1.5%	0.7%

Figure D.26: Harmonics

D.2.7 Phase-to-phase fault (Segment 2: 75-150km)

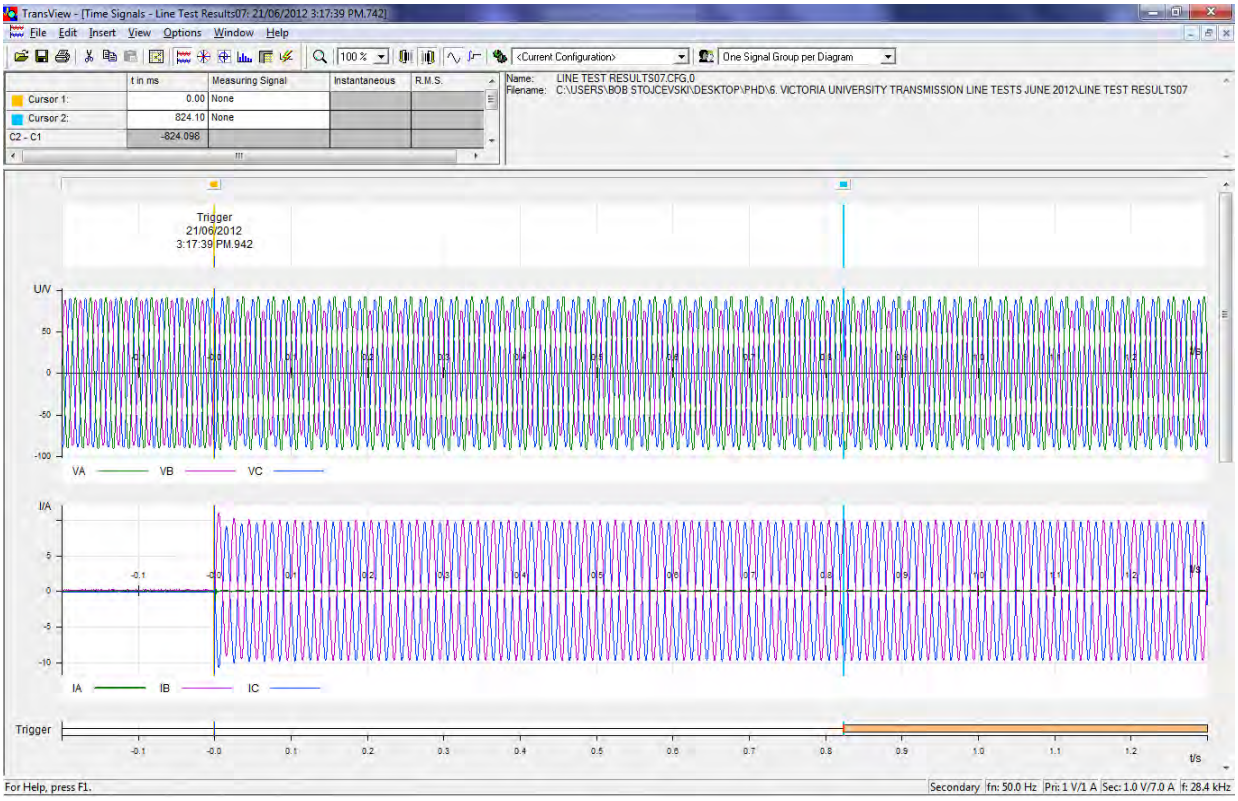


Figure D.27: Time signals

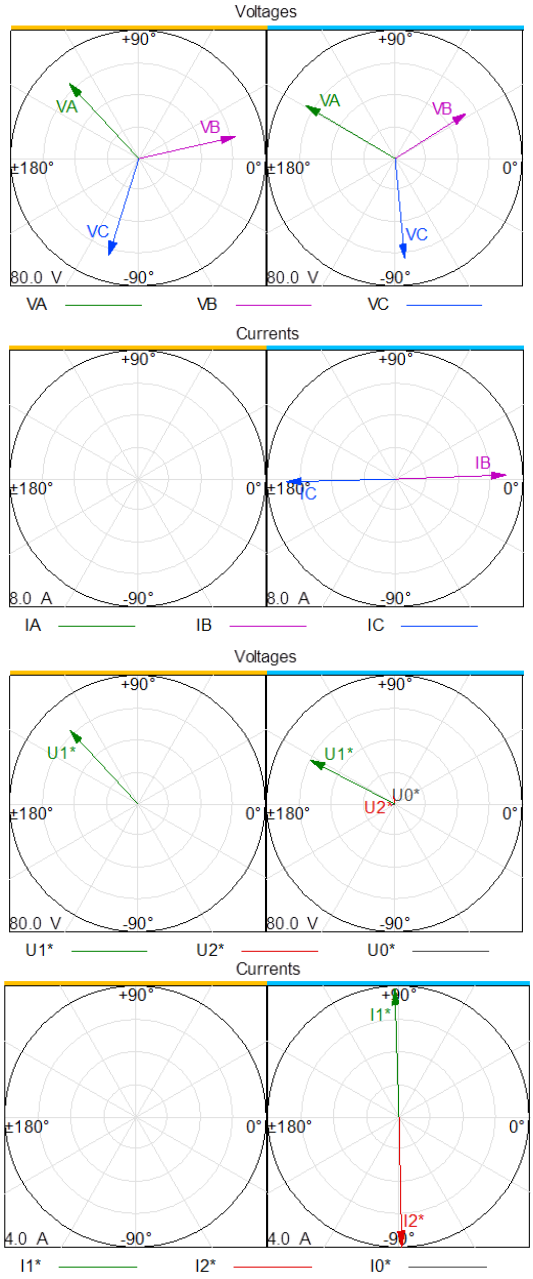
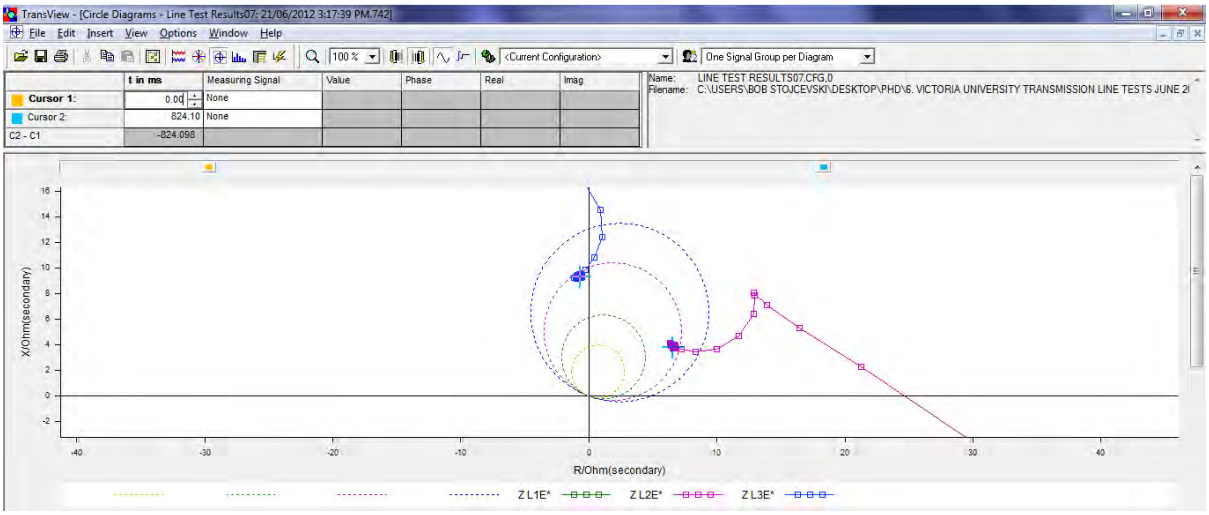


Figure D.28: Vector diagrams



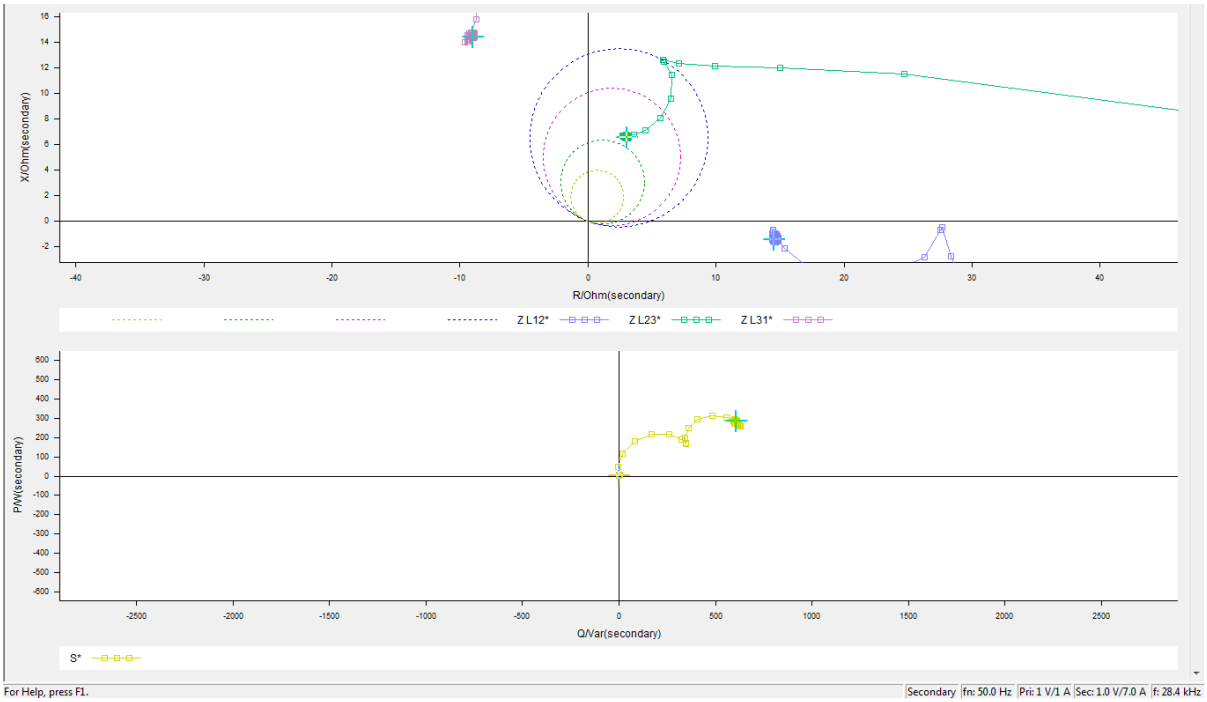
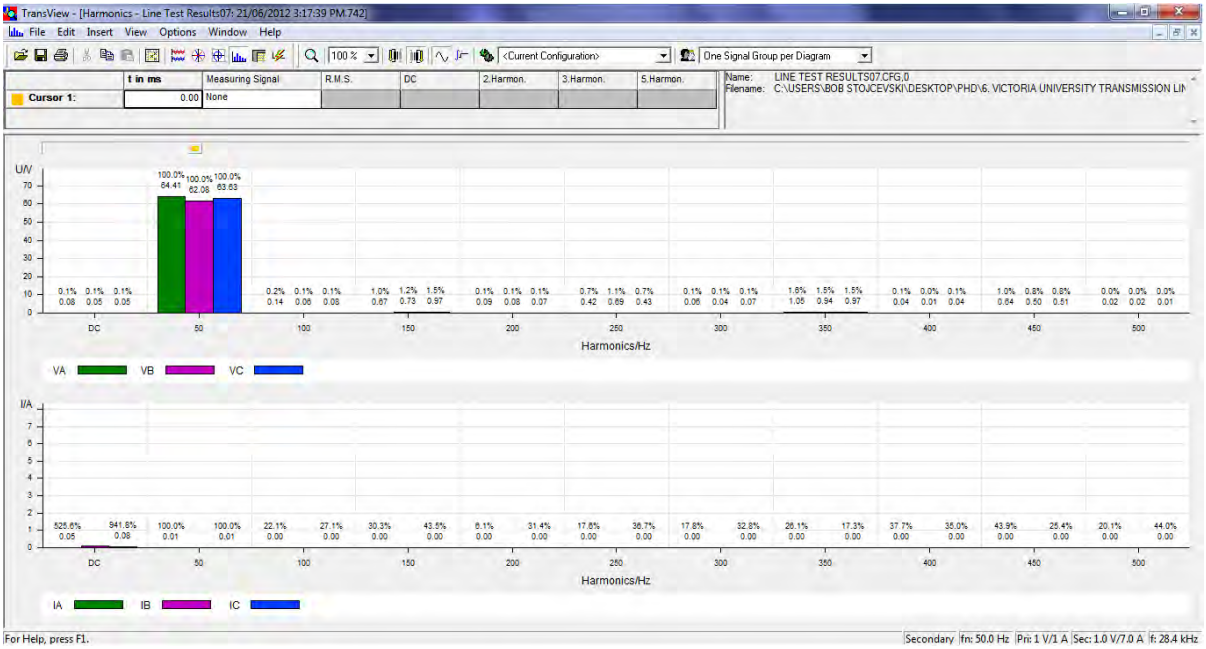


Figure D.29: Circle diagrams



Measuring Signal	Value	Phase	Extremum	DC	2.Harmon.	3.Harmon.	5.Harmon.
IA	0.029 A	91.7°	-0.190 A	525.6%	22.1%	30.3%	17.6%
IB	0.0068 A	-36.2°	0.229 A	2536.7%	60.9%	33.2%	28.9%
IC	0.027 A	-127.9°	-0.100 A	-941.8%	27.1%	43.5%	36.7%
VA	64.4 V	133.1°	60.98 V	0.1%	0.2%	1.0%	0.7%
VB	62.1 V	12.7°	-87.68 V	0.1%	0.1%	1.2%	1.1%
VC	63.6 V	-107.3°	-81.07 V	-0.1%	0.1%	1.5%	0.7%

Figure D.30: Harmonics

D.2.8 Phase-to-phase fault (Segment 3: 150-225km)

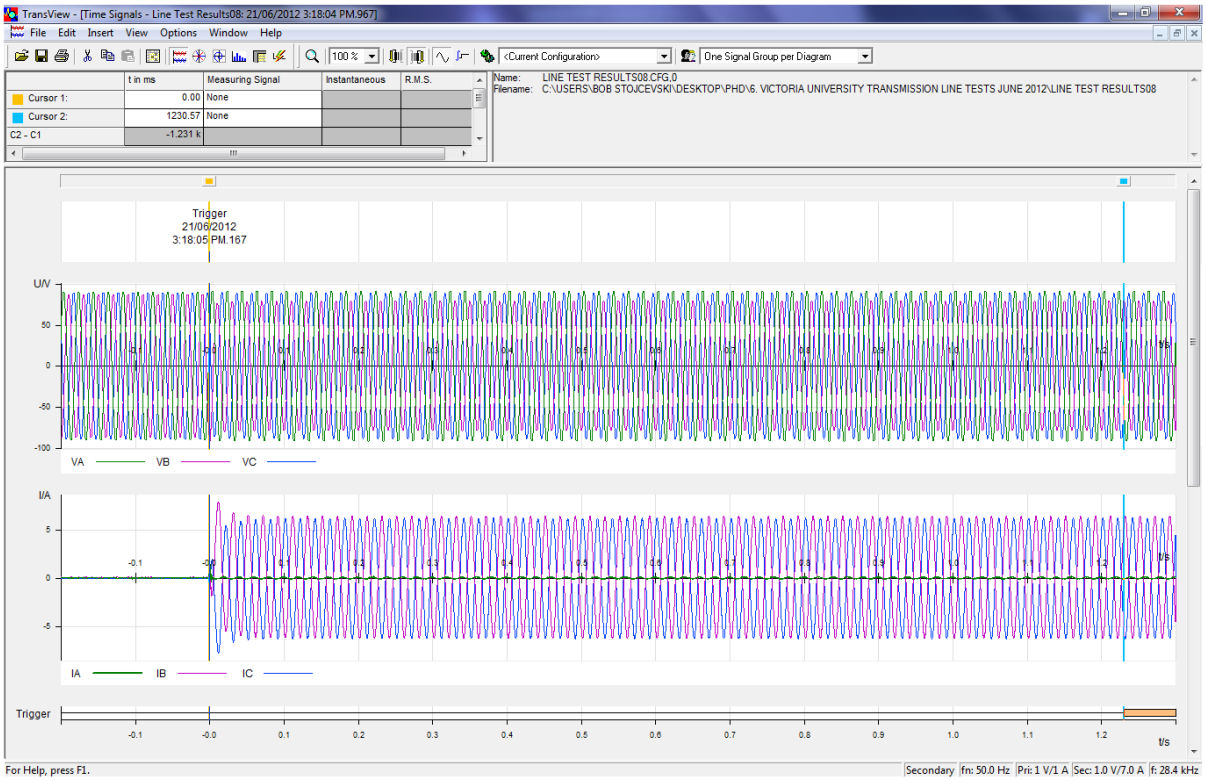
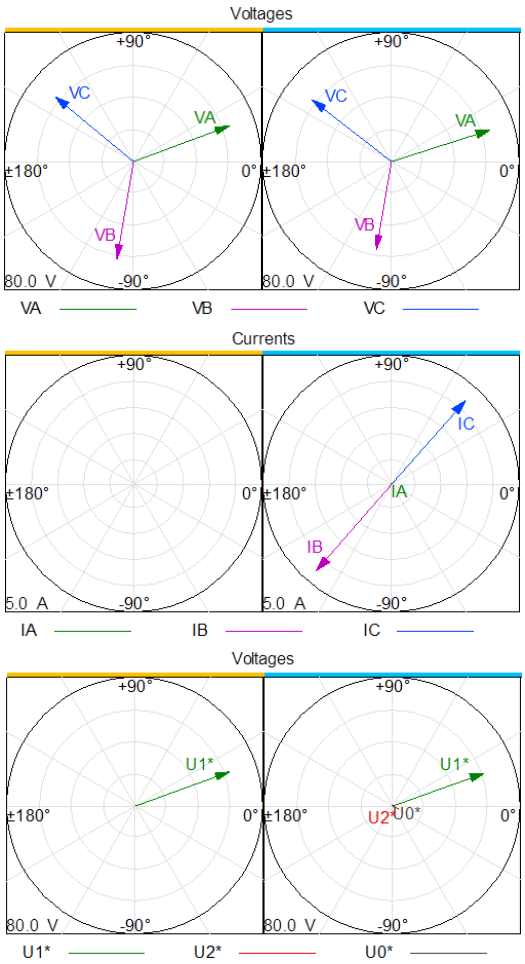


Figure D.31: Time signals



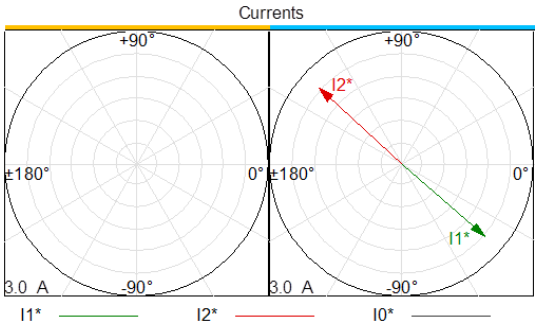


Figure D.32: Vector diagrams

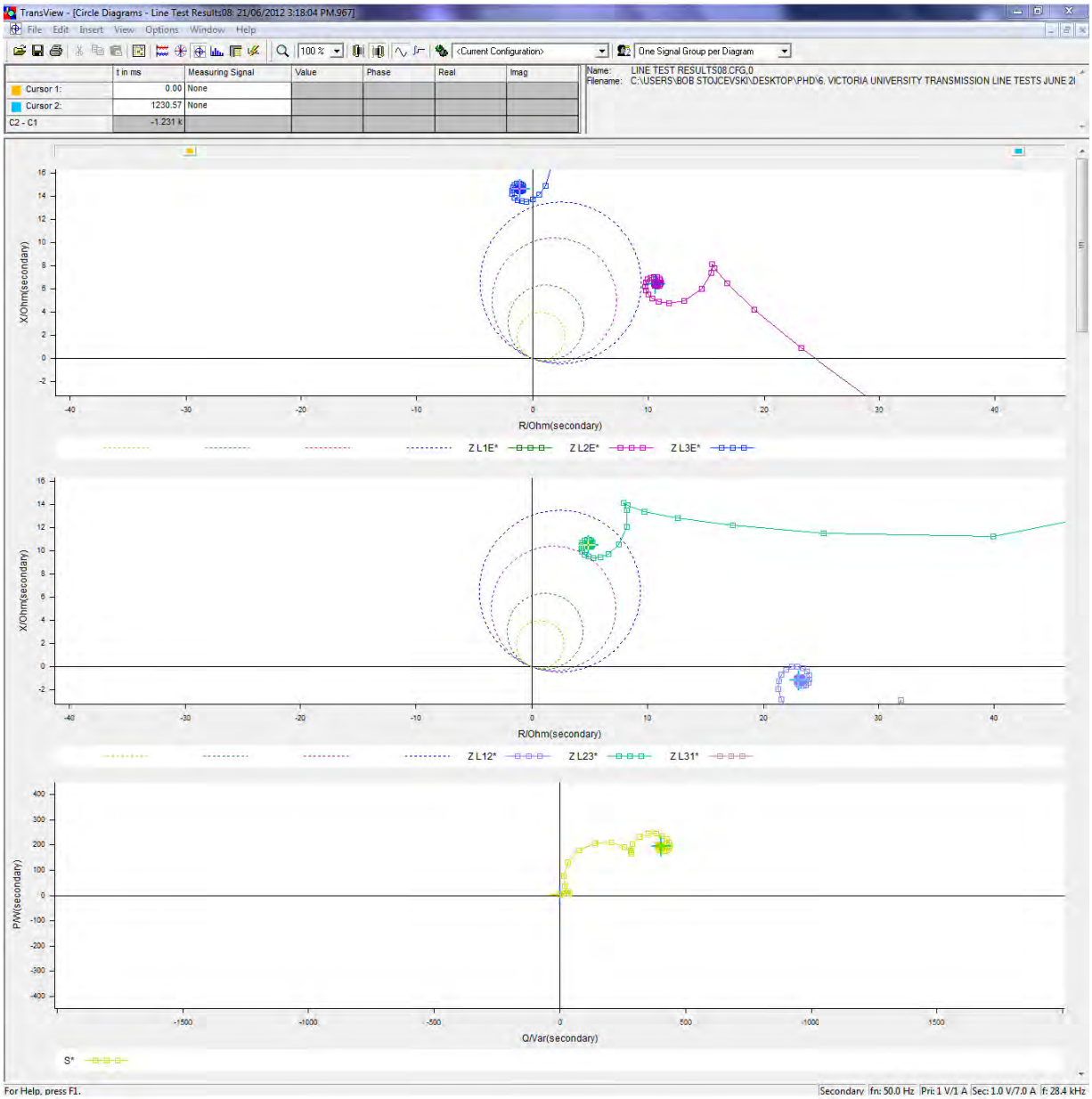
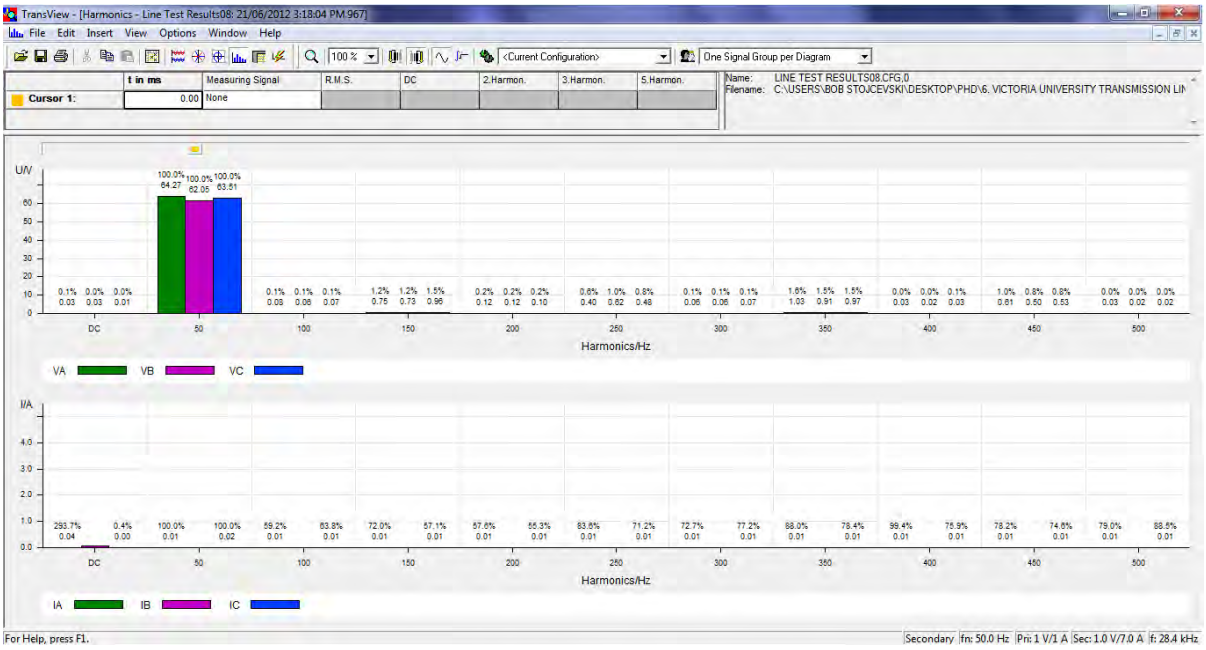


Figure D.33: Circle diagrams



Measuring Signal	Value	Phase	Extremum	DC	2.Harmon.	3.Harmon.	5.Harmon.
IA	0.010 A	-21.2°	-0.0396 A	293.7%	59.2%	72.0%	83.6%
IB	0.0063 A	-123.9°	0.0762 A	1419.0%	27.4%	27.6%	39.0%
IC	0.0089 A	130.5°	-0.329 A	0.4%	63.8%	57.1%	71.2%
VA	64.3 V	20.6°	9.113 V	0.1%	0.1%	1.2%	0.6%
VB	62.1 V	-99.8°	87.58 V	0.0%	0.1%	1.2%	1.0%
VC	63.5 V	140.2°	66.15 V	0.0%	0.1%	1.5%	0.8%

Figure D.34: Harmonics

D.2.9 Phase-to-phase fault (Segment 4: 225-300km)

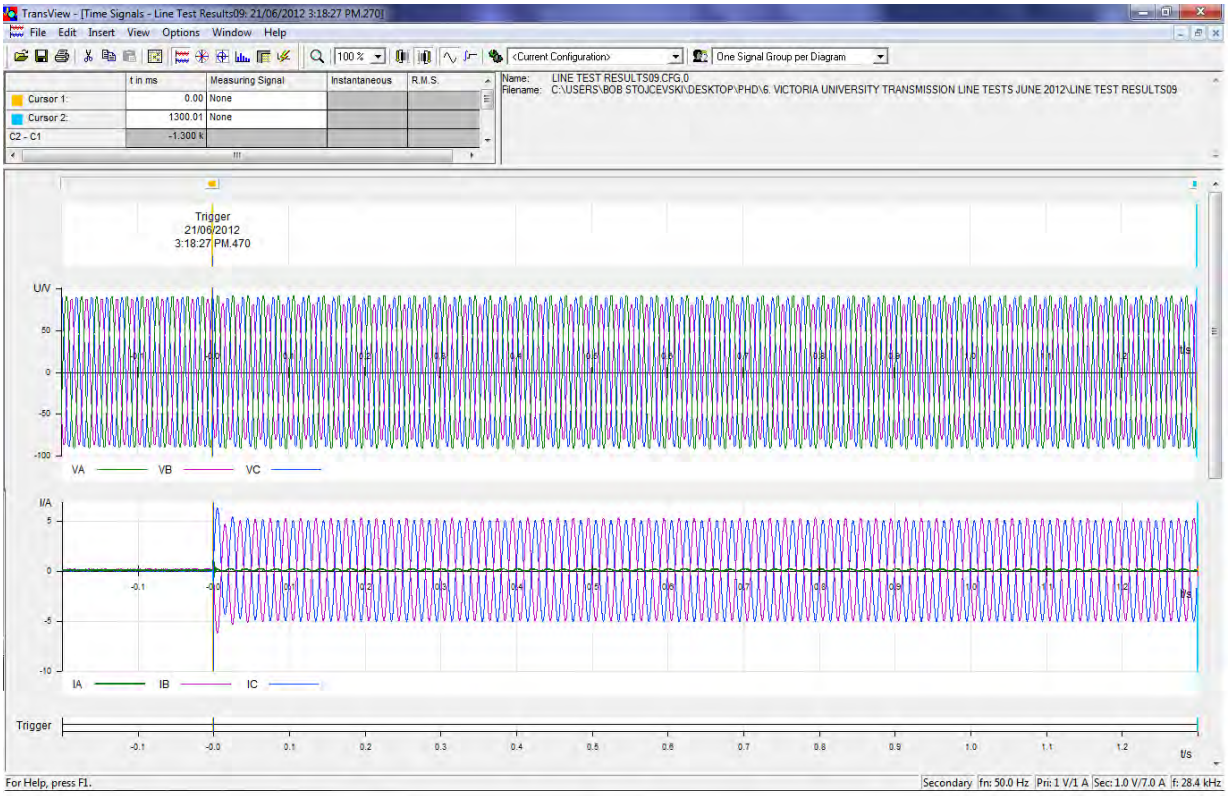


Figure D.35: Time signals

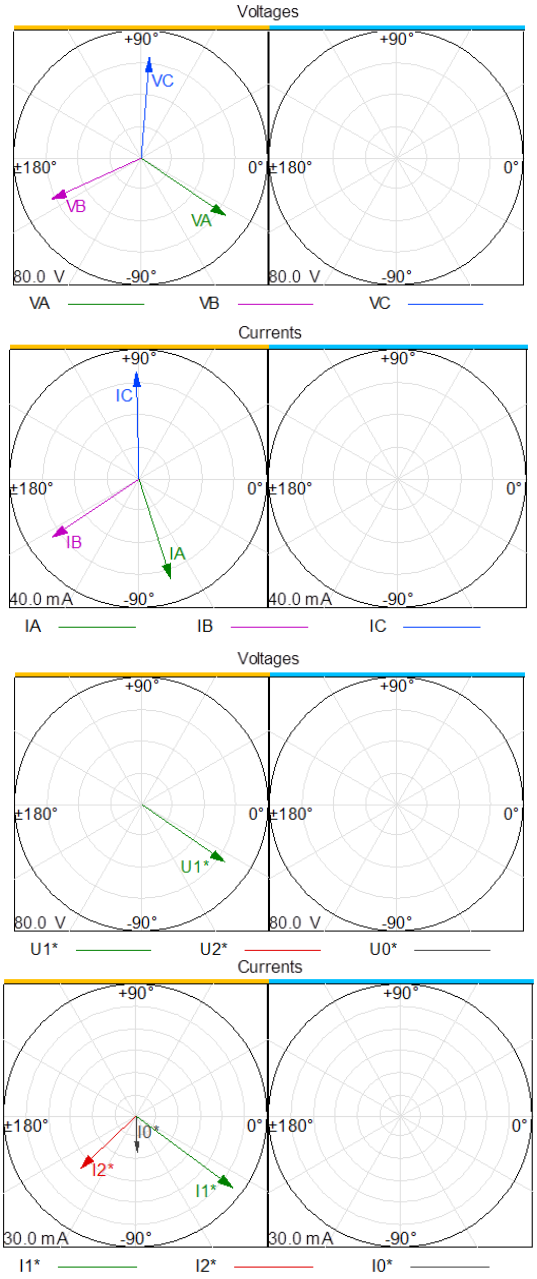
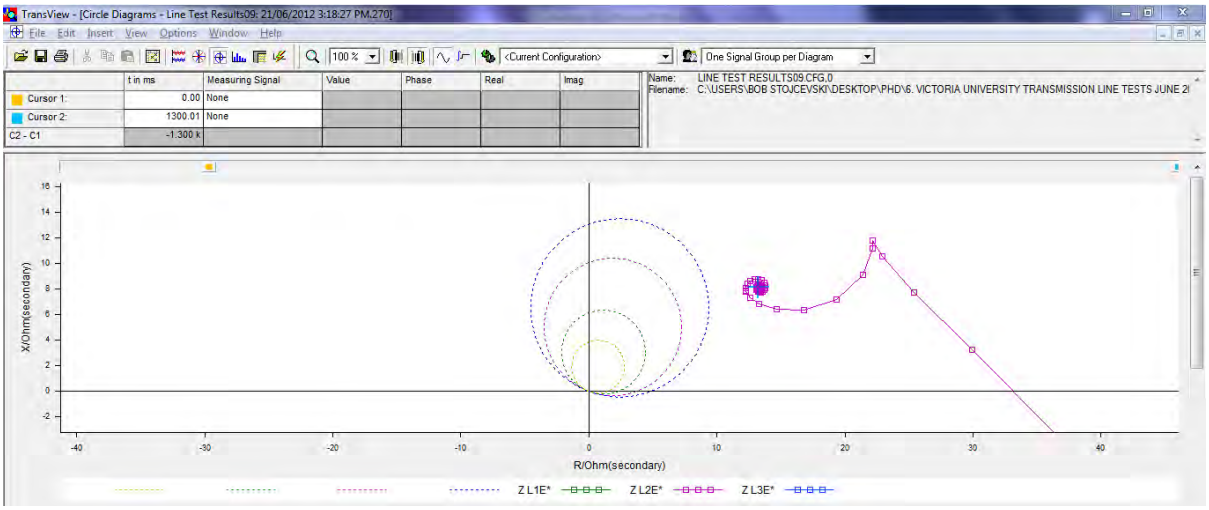


Figure D.36: Vector diagrams



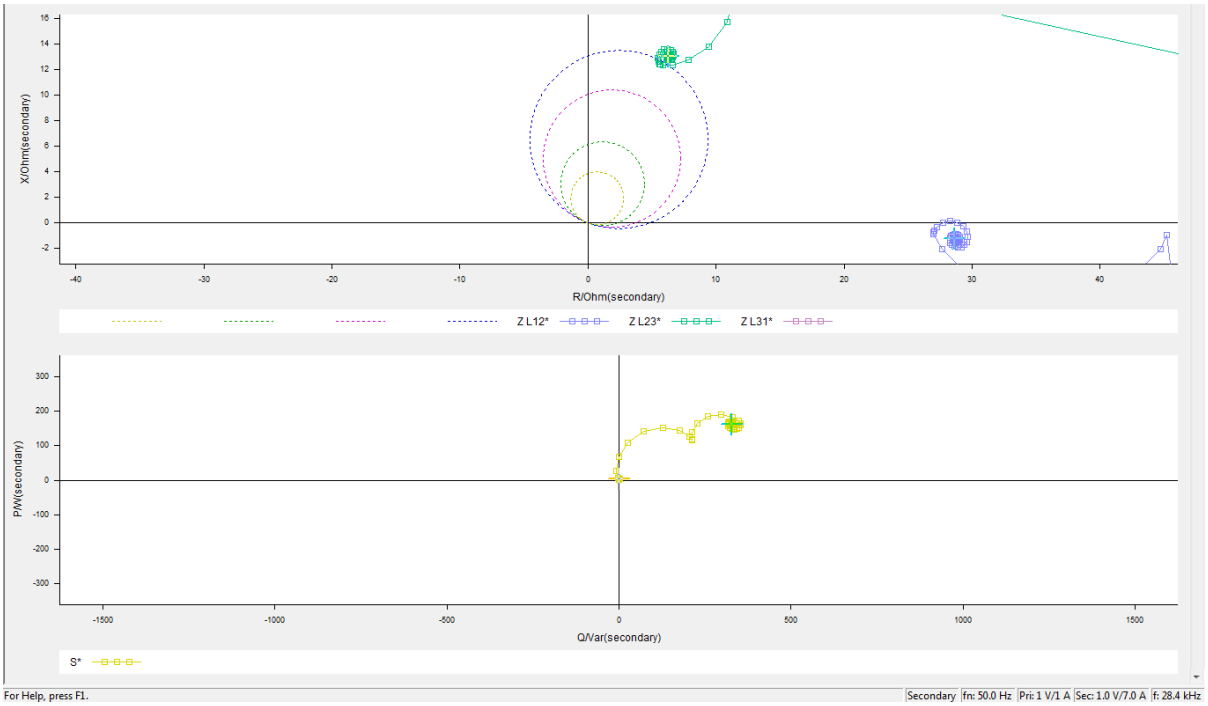
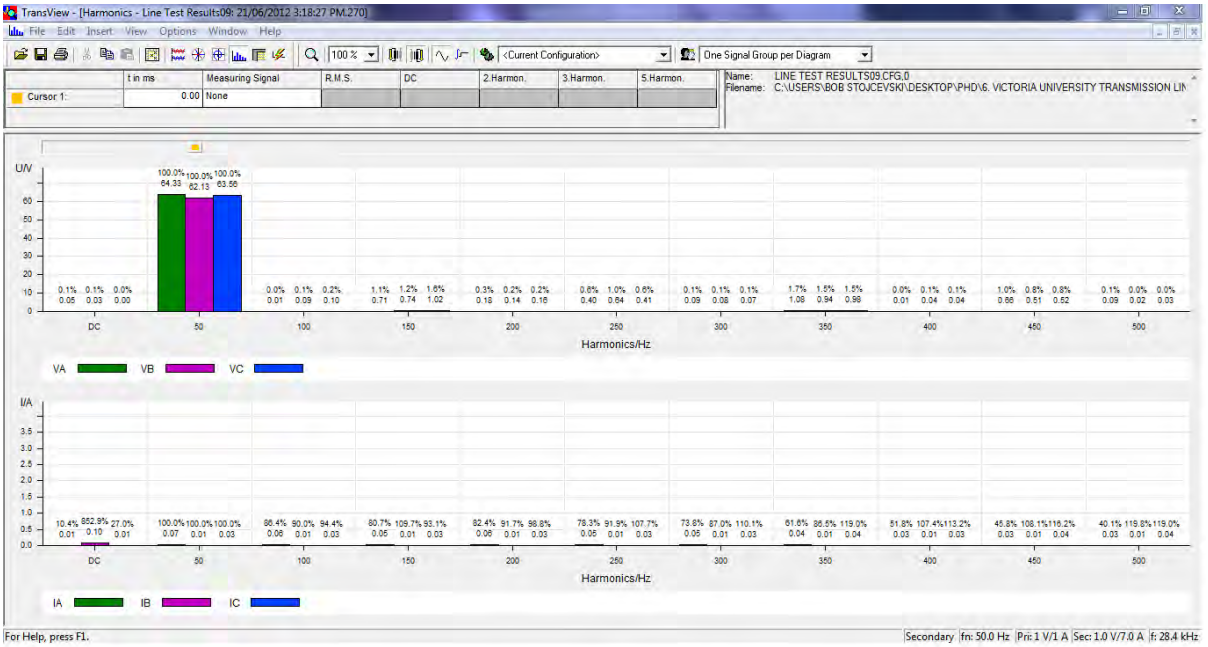


Figure D.37: Circle diagrams



Measuring Signal	Value	Phase	Extremum	DC	2.Harmon.	3.Harmon.	5.Harmon.
IA	0.032 A	-72.0°	1.051 A	10.4%	86.4%	80.7%	78.3%
IB	0.033 A	-146.5°	-3.817 A	852.9%	90.0%	109.7%	91.9%
IC	0.033 A	91.6°	-4.101 A	-27.0%	94.4%	93.1%	107.7%
VA	64.3 V	-34.6°	-39.26 V	0.1%	0.0%	1.1%	0.6%
VB	62.1 V	-155.1°	-46.91 V	0.1%	0.1%	1.2%	1.0%
VC	63.6 V	85.0°	83.39 V	-0.0%	0.2%	1.6%	0.6%

Figure D.38: Harmonics

D.2.10 Three phase fault (Segment 1: 0-75km)

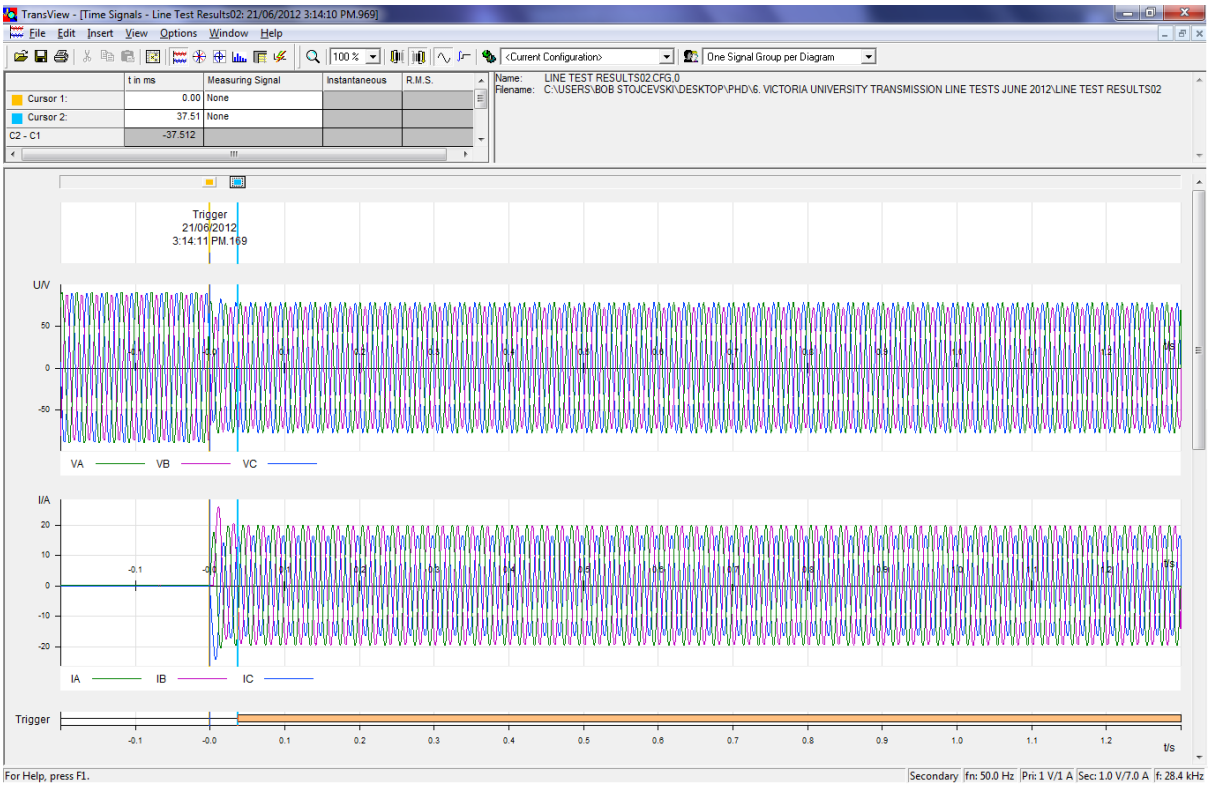
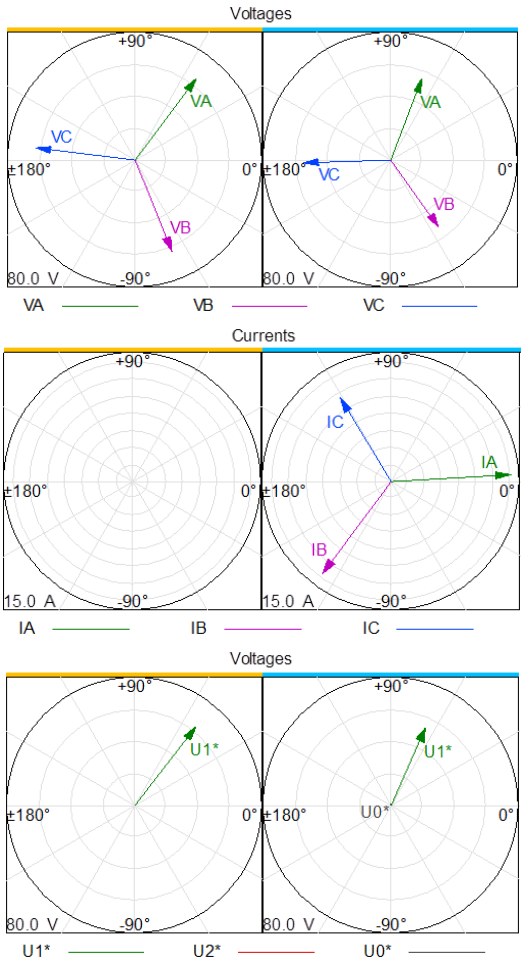


Figure D.39: Time signals



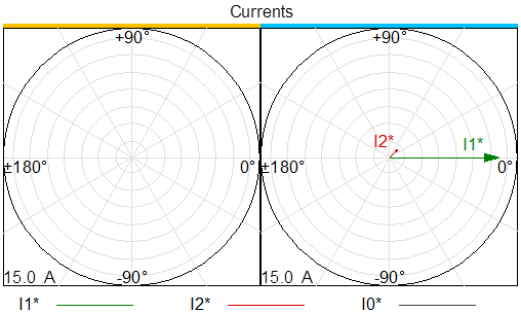


Figure D.40: Vector diagrams

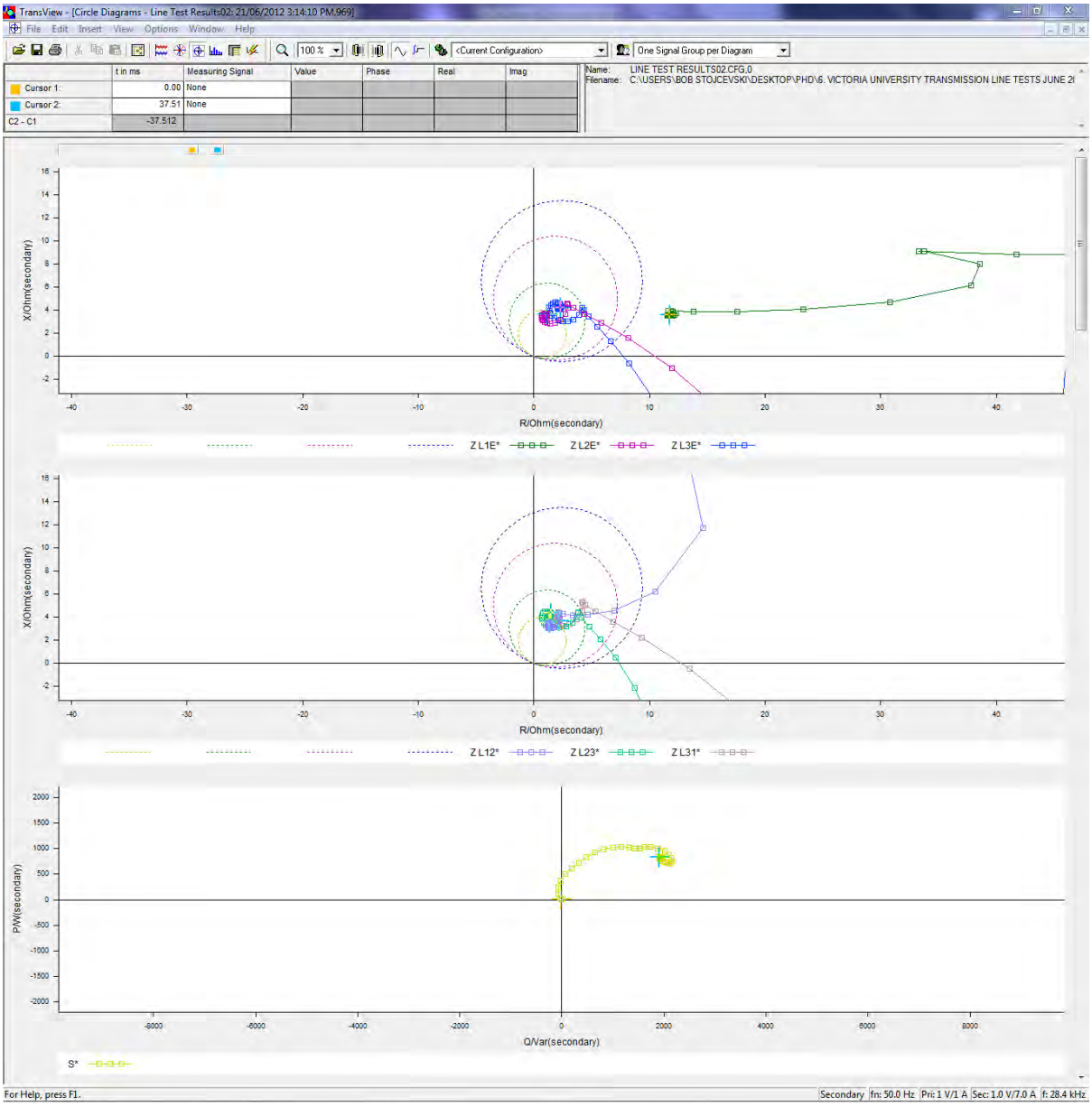
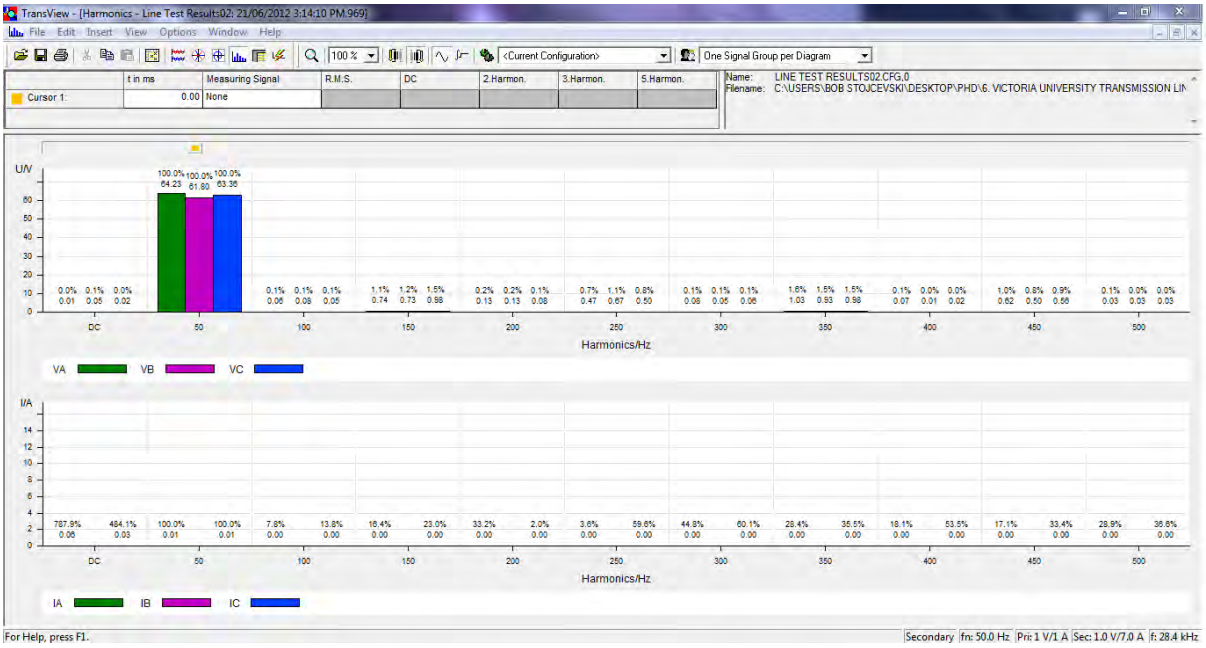


Figure D.41: Circle diagrams



Measuring Signal	Value	Phase	Extremum	DC	2.Harmon.	3.Harmon.	5.Harmon.
IA	0.036 A	55.1°	0.0356 A	787.9%	7.8%	16.4%	3.6%
IB	0.0070 A	-110.6°	0.0769 A	1456.3%	4.9%	35.8%	4.8%
IC	0.030 A	-159.6°	0.0144 A	-484.1%	13.8%	23.0%	59.6%
VA	64.2 V	52.8°	70.18 V	0.0%	0.1%	1.1%	0.7%
VB	61.8 V	-67.6°	-87.18 V	0.1%	0.1%	1.2%	1.1%
VC	63.4 V	172.4°	11.68 V	0.0%	0.1%	1.5%	0.8%

Figure D.42: Harmonics

D.2.11 Three phase fault (Segment 2: 75-150km)

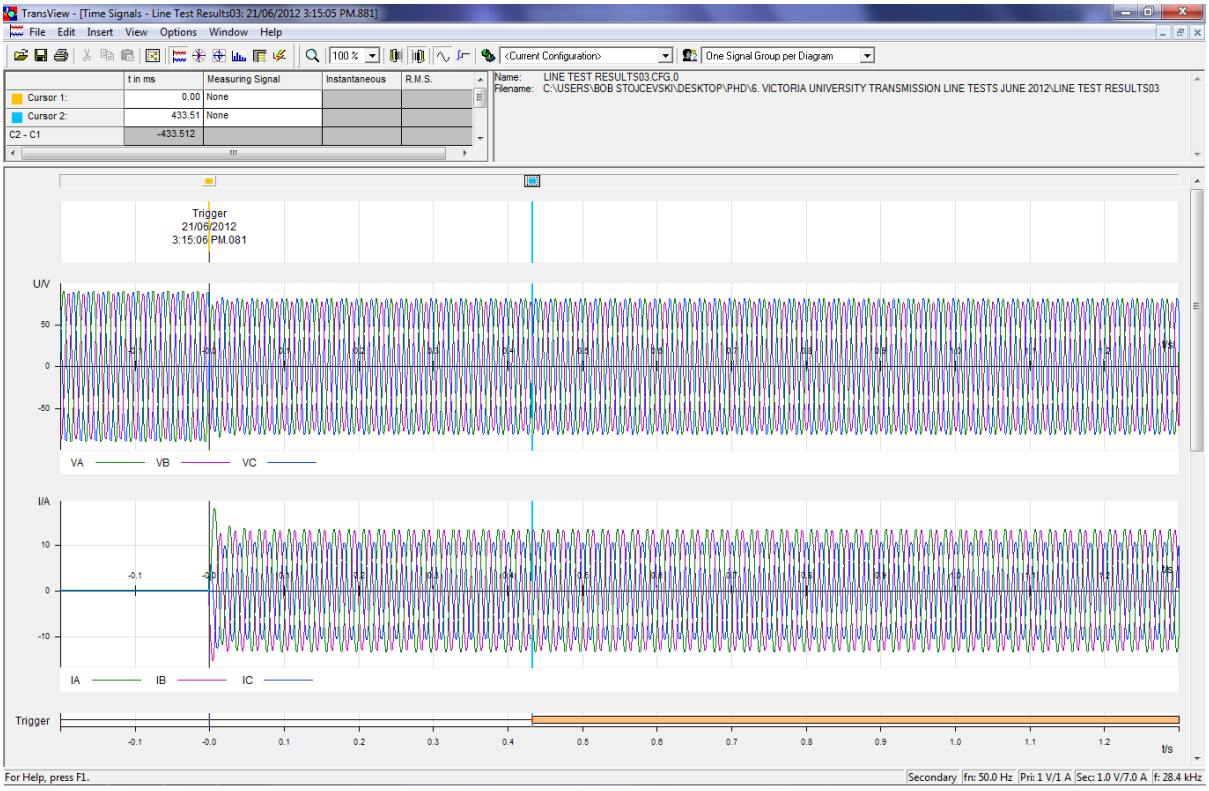


Figure D.43: Time signals

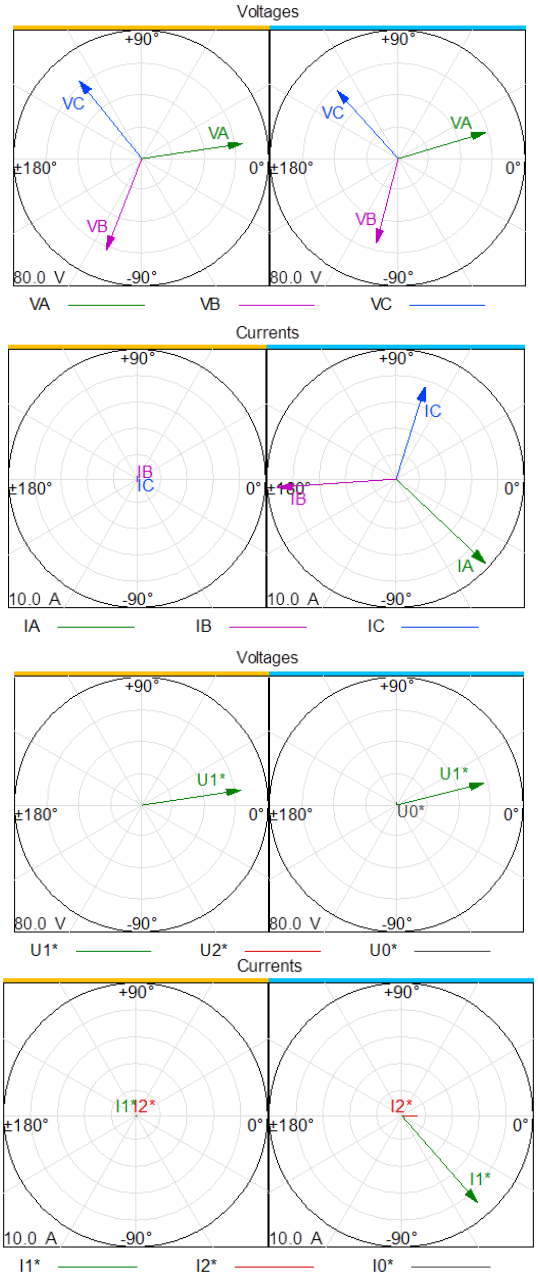
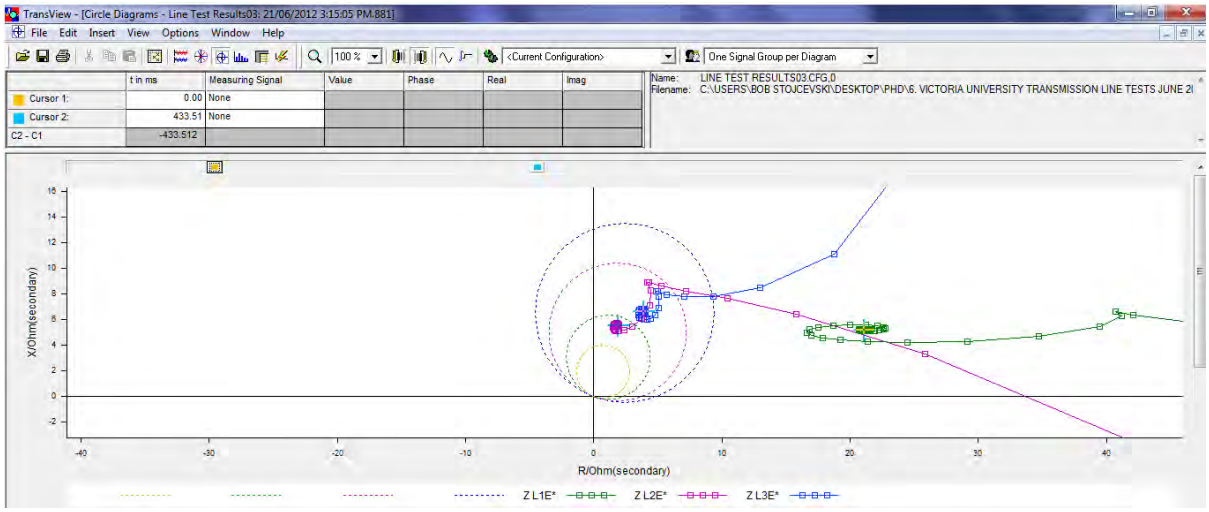


Figure D.44: Vector diagrams



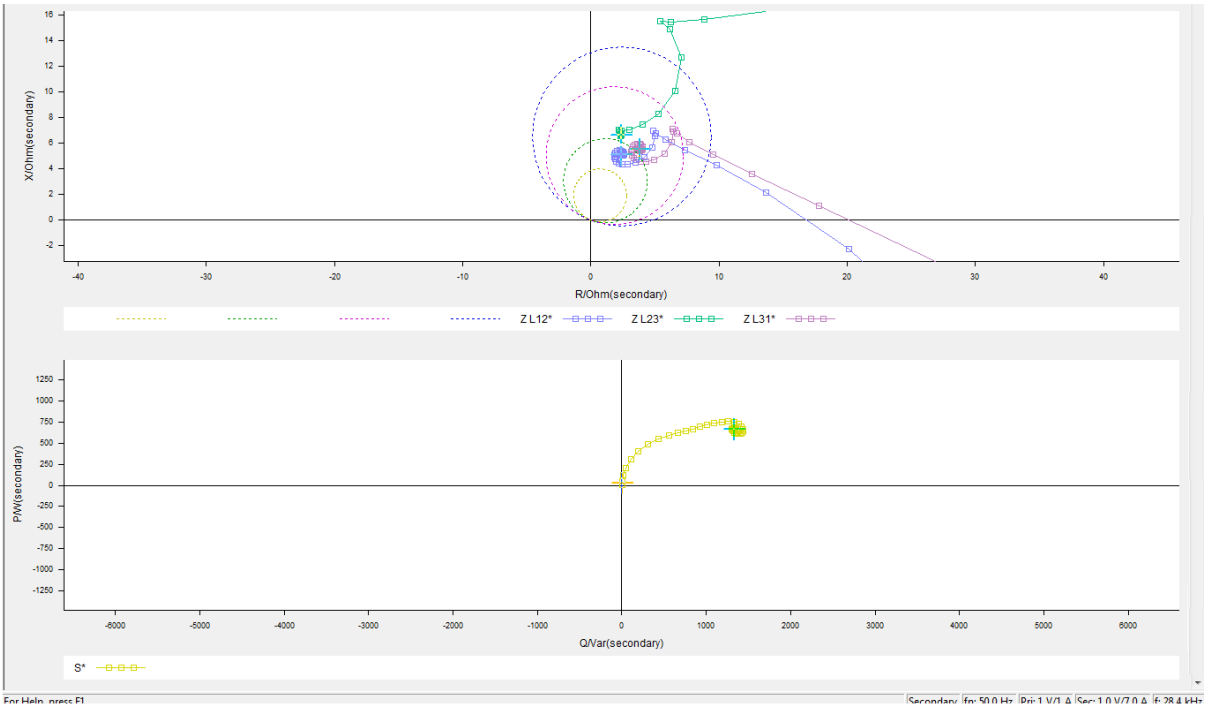
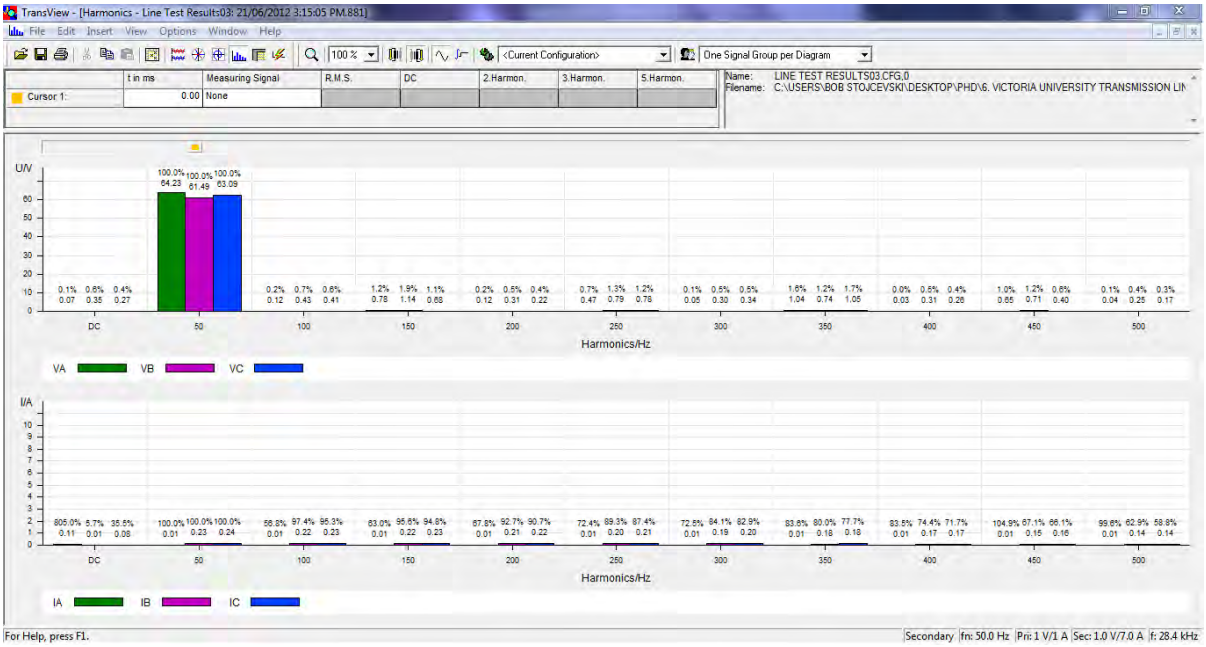


Figure D.45: Circle diagrams



Measuring Signal	Value	Phase	Extremum	DC	2.Harmon.	3.Harmon.	5.Harmon.
IA	0.022 A	8.1°	-0.0392 A	805.0%	56.8%	63.0%	72.4%
IB	0.27 A	-86.8°	-0.535 A	5.7%	97.4%	95.6%	89.3%
IC	0.26 A	97.2°	0.776 A	35.5%	95.3%	94.8%	87.4%
VA	64.2 V	9.1°	-16.16 V	0.1%	0.2%	1.2%	0.7%
VB	61.4 V	-111.5°	-64.44 V	0.6%	0.7%	1.9%	1.3%
VC	63.1 V	128.8°	81.83 V	-0.4%	0.6%	1.1%	1.2%

Figure D.46: Harmonics

D.2.12 Three phase fault (Segment 3: 150-225km)

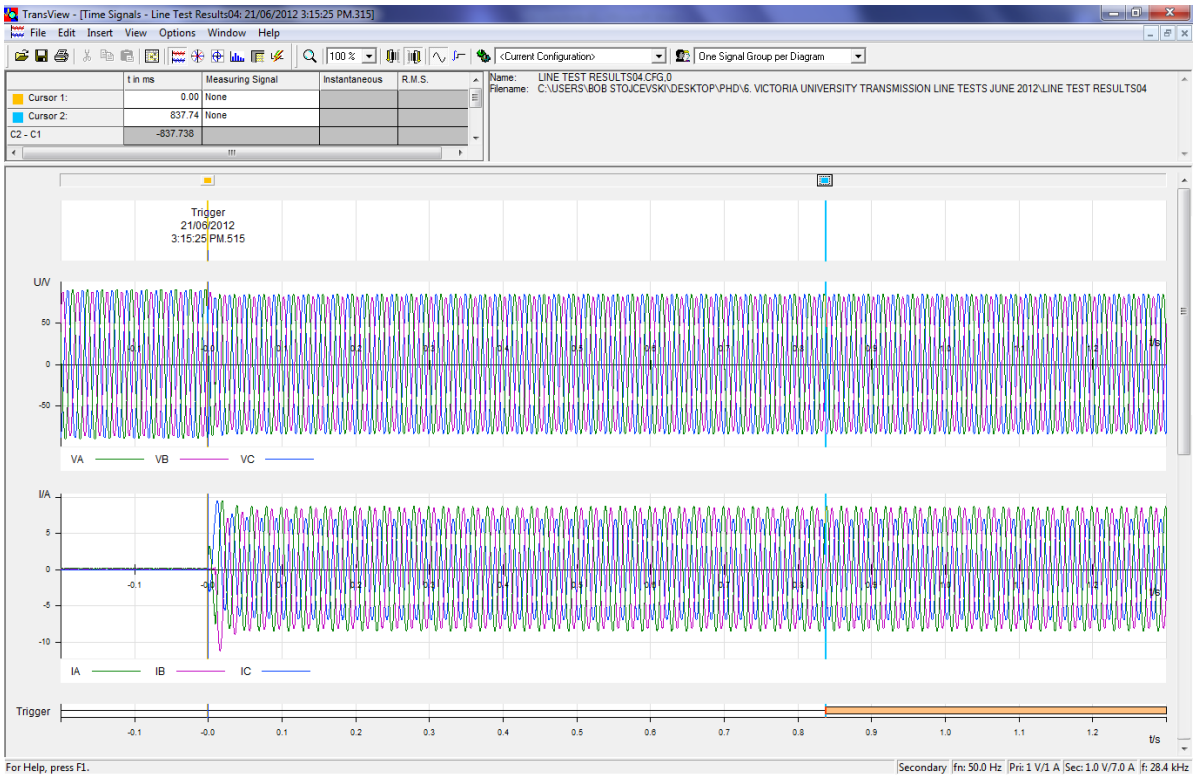
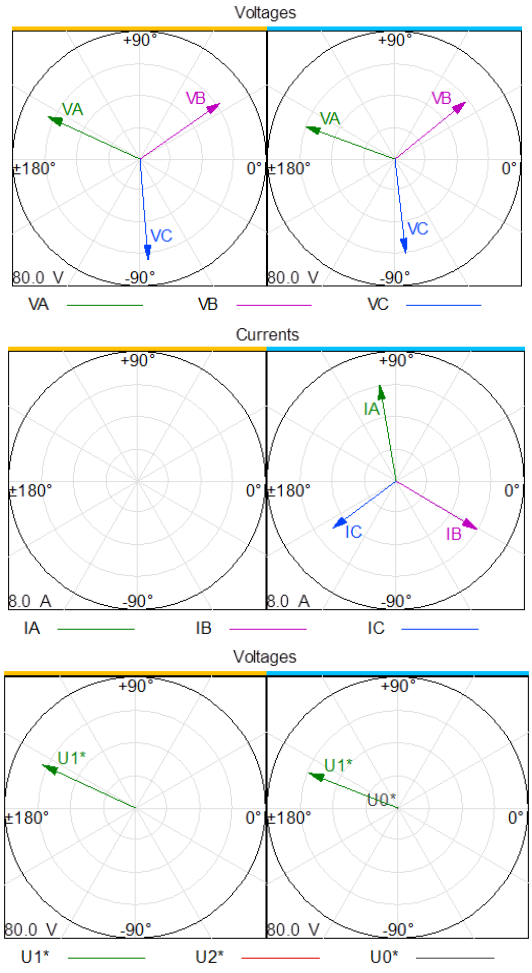


Figure D.47: Time signals



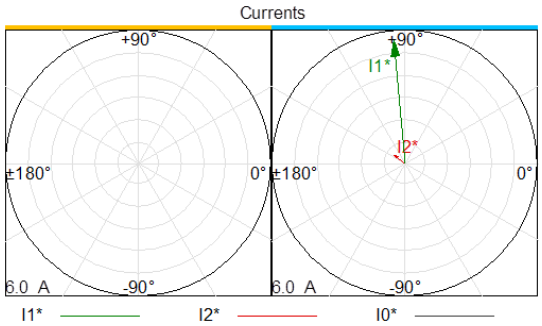


Figure D.48: Vector diagrams

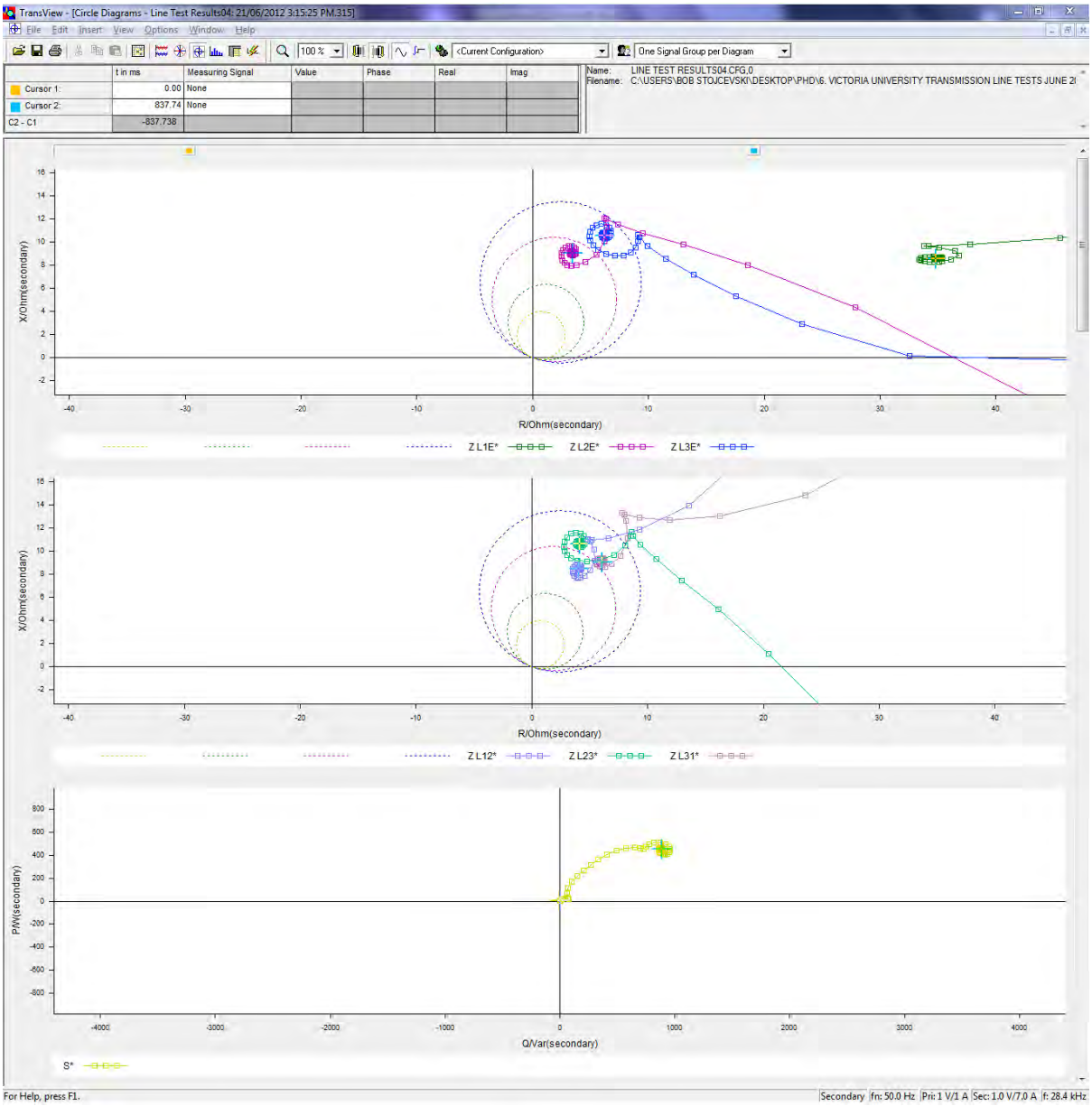
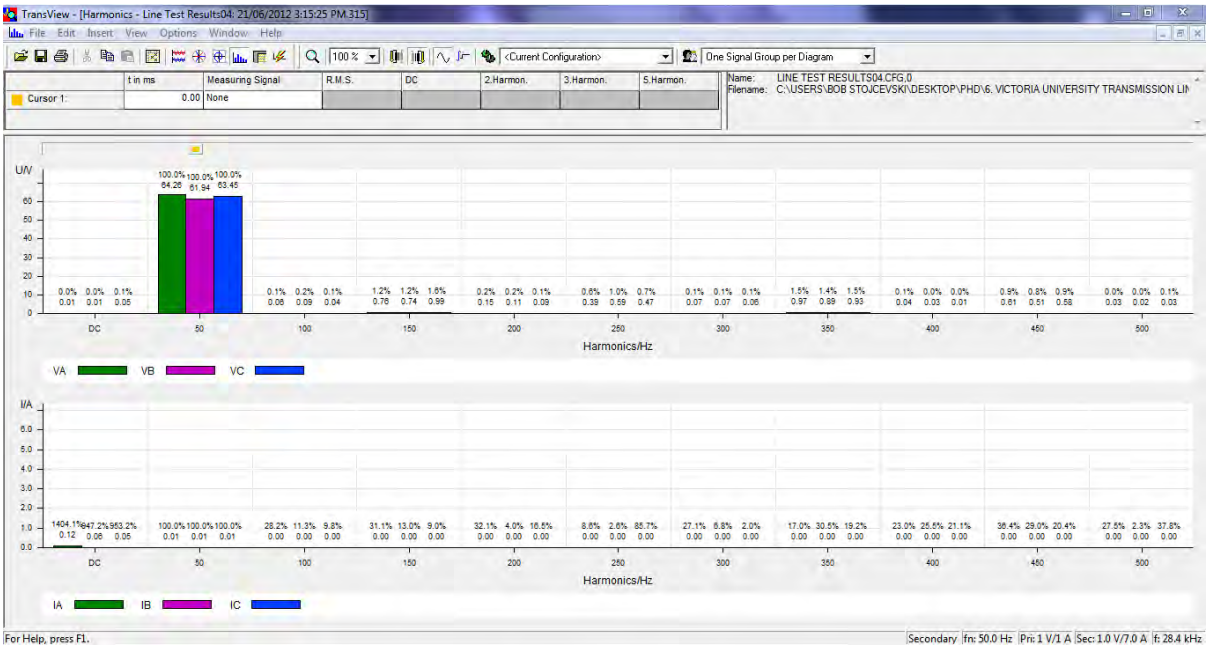


Figure D.49: Circle diagrams



Measuring Signal	Value	Phase	Extremum	DC	2.Harmon.	3.Harmon.	5.Harmon.
IA	0.028 A	108.5°	0.0734 A	1404.1%	28.2%	31.1%	8.6%
IB	0.0065 A	-4.4°	0.114 A	947.2%	11.3%	13.0%	2.6%
IC	0.027 A	-112.7°	-0.0617 A	-953.2%	9.8%	9.0%	85.7%
VA	64.3 V	155.3°	90.75 V	0.0%	0.1%	1.2%	0.6%
VB	61.9 V	34.8°	-87.30 V	0.0%	0.2%	1.2%	1.0%
VC	63.4 V	-85.2°	-84.35 V	0.1%	0.1%	1.6%	0.7%

Figure D.50: Harmonics

D.2.13 Three phase fault (Segment 4: 225-300km)

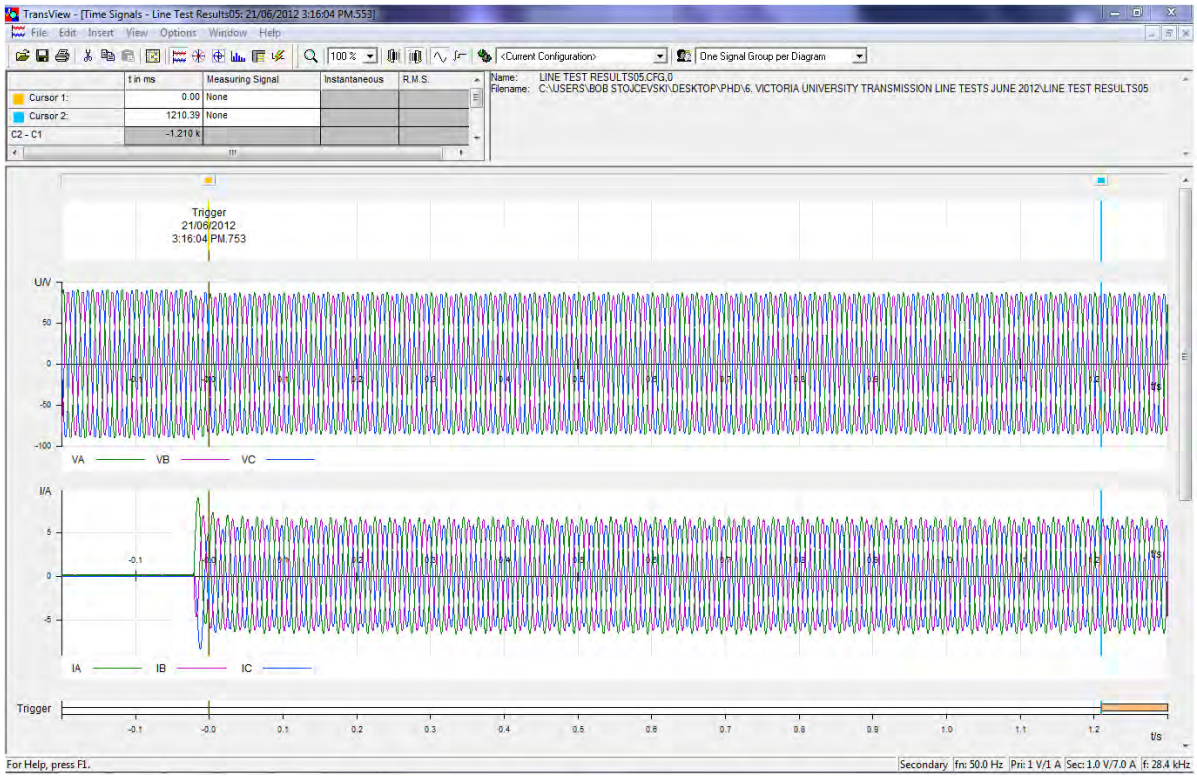


Figure D.51: Time signals

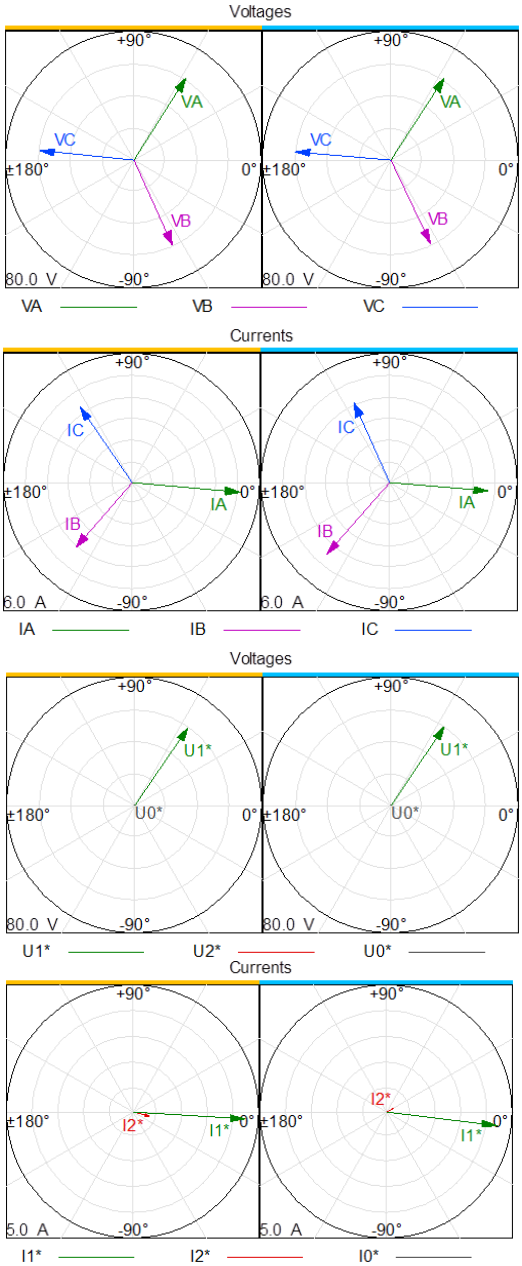
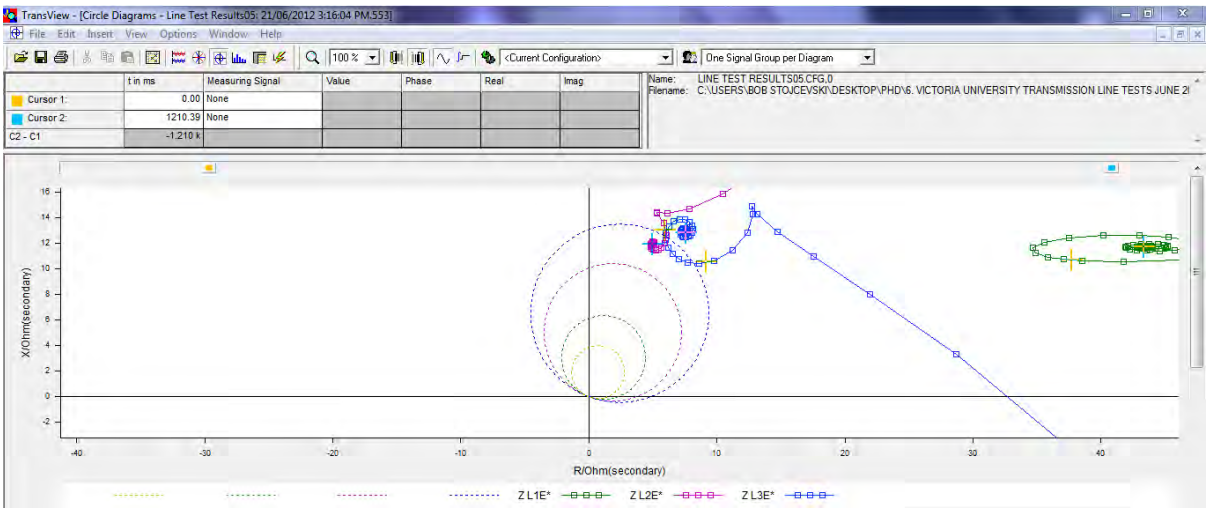


Figure D.52: Vector diagrams



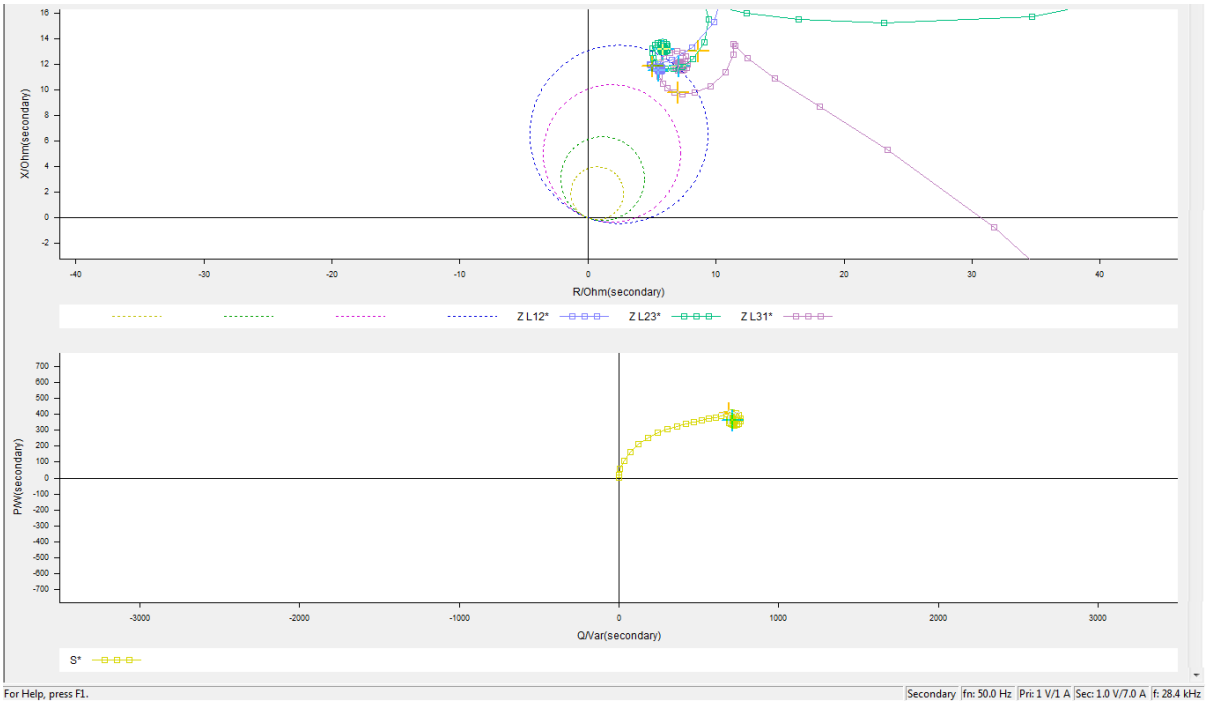
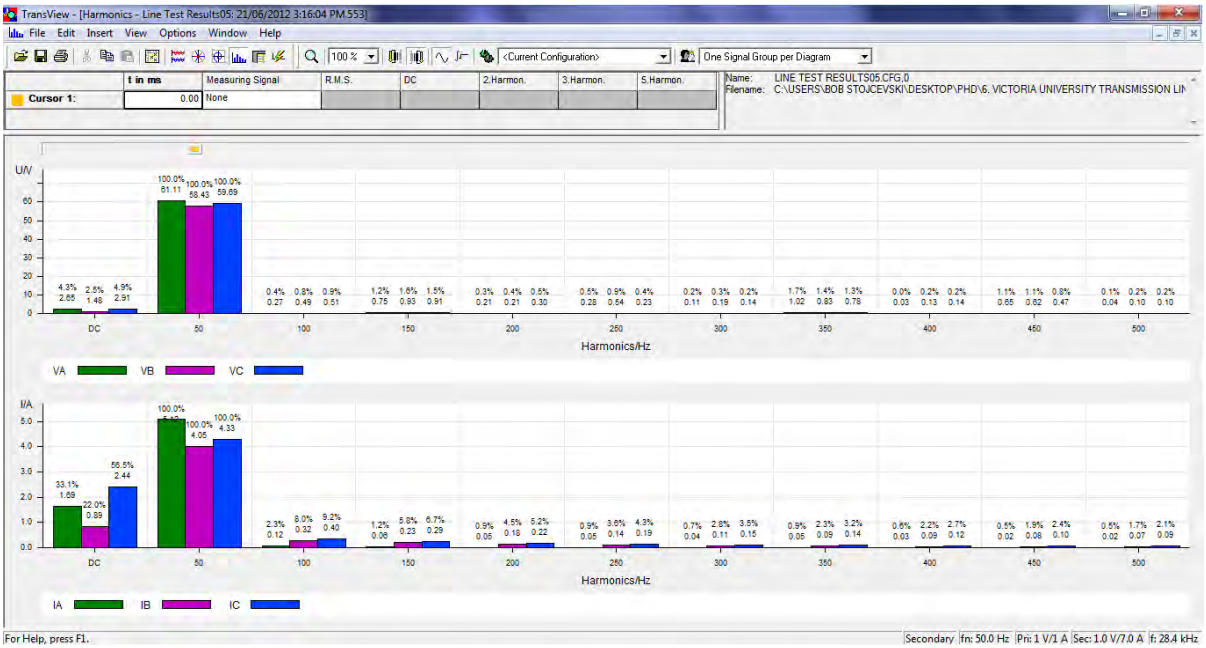


Figure D.53: Circle diagrams



Measuring Signal	Value	Phase	Extremum	DC	2.Harmon.	3.Harmon.	5.Harmon.
IA	5.12 A	-5.7°	0.412 A	33.1%	2.3%	1.2%	0.9%
IB	4.05 A	-130.9°	-3.779 A	22.0%	8.0%	5.8%	3.6%
IC	4.31 A	124.7°	4.167 A	-56.5%	9.2%	6.7%	4.3%
VA	61.1 V	57.1°	-88.53 V	-4.3%	0.4%	1.2%	0.5%
VB	58.5 V	-65.3°	-83.28 V	-2.5%	0.8%	1.6%	0.9%
VC	59.7 V	174.1°	86.55 V	4.9%	0.9%	1.5%	0.4%

Figure D.54: Harmonics