High Resolution Integrated Passive Phase Shifters for Future Wireless Communications

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To my dear husband, Andrew

Declaration

”I, Robabeh Amirkhanzadeh Antiohos, declare that the PhD thesis entitled ’High Resolution Integrated Passive Phase Shifters for Future Wireless Communications’ is no more than 100,000 words in length including quotes and exclusive of tables, figures, appendices, bibliography, references and footnotes. This thesis contains no material that has been submitted previously, in whole or in part, for the award of any other academic degree or diploma. Except where otherwise indicated, this thesis is my own work.”

Robabeh Amirkhanzadeh Antiohos

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Abstract

This thesis focuses on the implementation of high resolution phase shifter devices for adaptive cancelling applications. Cancelling is a potential replacement for filtering in wireless handsets, where the area allocated to filtering is becoming excessive due to the growing numbers of transmission frequencies. Cancelling circuits have the potential to be integrated directly in silicon as part of the radio circuit. Adaptive cancelling requires precise adjustments of the gain and phase of the reference RF signal.

Passive methods are chosen for linearity purposes, as the circuit should be capable of handling high power transmit signals. To increase the power handling, stacked FETs (Field-Effect Transistors) are employed as switches. An SOS (Silicon-on-Sapphire) process is chosen for the implementation, firstly, because it is silicon based, and therefore compatible for integration with the other Tx/Rx circuits. Secondly, it provides passive components with a high quality factor, benefiting from an insulating substrate, to obtain high speed, improved linearity and low insertion loss.

In this research, two high resolution passive phase shifters are designed and fabricated in Peregrine's 0.25 μm GC SOS process. The first design, a 9-bit phase shifter, is a capacitor loaded lumped element transmission line. Switched capacitor banks are used to obtain fine resolution. To keep the size of the chip reasonably small, a combination of ganged and individual switching is employed, which provides a nominal 9-bit resolution with only a 6-bit chip area. The device provides 360° phase shift at 1.4 GHz with an insertion loss of 12.6 dB. The measured IIP_3 (input third order intercept point) is 40±1 dBm. The chip size including pads, RF (Radio Frequency) and digital, is 5.94 mm^2.

The second design is a new topology, a combination of three different methods, which is proposed to decrease the size and insertion loss of the 9-bit phase shifter. The resolution is also increased by one bit, which can further improve the overall performance of the cancellation loop in the adaptive duplexer. An auto-transformer is used to obtain 180° phase shift; this approach decreases the size and insertion loss significantly. This stage is controlled by the MSB (Most Significant Bit) of the control word. Three fixed 45° phase shift circuits are combined to provide up to 135° phase shift under control of the next two MSBs. Finally, a two stage π section with switched capacitor banks is used to obtain a fine 0.38° resolution up to a maximum phase shift of 45° and is controlled by seven LSBs (Least Significant Bits).

The 10-bit phase shifter device has a small footprint of 3.4 mm^2 (including pads). The insertion loss is improved by 5.3 dB, in comparison with the 9-bit device. The maximum measured insertion loss in the frequency range of 1.8 GHz to 2.4 GHz is 7.3 dB. The measured IIP_3 is 55±1 dBm. It is the highest reported resolution digital passive phase shifter, and obtains the lowest insertion loss per bit of any silicon integrated passive phase shifter on the market today.

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Last but not least, my deepest gratitude and love goes to my dear husband, Andrew, for all his support and care through years of hard work and night shifts during tape-outs.

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Abbreviations

3G	3rd Generation
4G	4th Generation
3GPP	3rd Generation Partnership Project
ACLR	Adjacent Channel Leakage Ratio
ACS	Adjacent Channel Selectivity
ADC	Analog-to-Digital Converter
ADS	Advance Design System
BAW	Bulk Acoustic Wave
BP	Band Pass
BPF	Band Pass Filter
BST	Barium Strontium Titanate
BW	Band Width
CDMA	Code Division Multiple Access
CMOS	Complementary Metal-Oxide-Semiconductor
DAC	Digital-to-Analog Converter
DL	Down-link
DR	Dynamic Range
DSP	Digital Signal Processing
DUT	Device Under Test
ESD	Electrostatic Discharge
EVM	Error Vector Magnitude
FDD	Frequency Division Duplex
FET	Field-Effect Transistor
FFCS	Feed-Forward noise Cancellation System

FOM	Figure Of Merit
GaAs	Gallium Arsenide
GSG	Ground-Signal-Ground
GSM	Global System for Mobile communications
HD-FDD	Half-duplex FDD
HP	High Pass
IC	Integrated Circuit
IL	Insertion Loass
IM	Intermodulation
IMD	Intermodulation Distortion
ITU	International Telecommunication Union
LMS	Least Mean Square
LNA	Low Noise Amplifier
LP	Low Pass
LTE	Long Term Evolution
LSB	Least Significant Bit
MESFET	Metal-Semiconductor Field Effect Transistor
MIM	Metal-Insulator-Metal
MMIC	Monolithic Microwave Integrated Circuit
MSB	Most Significant Bit
MSE	Mean Square Error
NF	Noise Floor
OOB	Out-Of-Band
PA	Power Amplifier
PIVA	Phase Invertible Variable Attenuator
PSD	Power Spectral Density
QAF	Quadrature All-pass Filter
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase-Shift Keying
RB	Resource Block
RF	Radio Frequency

RFFE	Radio Frequency Front End
RMS	Root Mean Square
RTPS	Reflective Type Phase Shifter
SAW	Surface Acoustic Wave
SEM	Spectrum Emission Mask
SiGe	Silicon Germanium
SNR	Signal-to-Noise Ratio
SOI	Silicon-on-Insulator
SOS	Silicon-on-Sapphire
SP9T	Single-pole nine-through
TDD	Time Division Duplexing
TD-SCDMA	Time Division Synchronous Code Division Multiple Access
TFBAR	Thin-Film Bulk Acoustic Wave
UL	Up-link
UMTS	Universal Mobile Telecommunication System
VGA	Variable Gain Amplifier
WiFi	Wireless Fidelity

Symbols

$\hat{}$	Quantised quantity
A	Amplitude of input signal
A_{1dB}	Amplitude of input signal at 1-dB compression point
$A_{In,IP3}$	Amplitude of input signal at IP_3
C_{OFF}	OFF-Capacitance
C_{ON}	ON-Capacitance
e^2	Error signal power
E	Cost function
f_d	Duplexing offset
f_{Rx}	Receive frequency
f_{TDD}	Frequency in TDD system
f_{Tx}	Transmit frequency
F_r	Receiver noise figure
F_t	Transmitter noise figure
g	Gain through the main signal path
G	Amplifier gain
h	Complex gain
h_i	Gain/phase cancellation coefficient
I	Additional isolation
IP_3	Third order intercept point
IIP_3	Input third order intercept point
k_B	Boltzmann constant
k	Coupling coefficient

OIP_3	Output third order intercept point
P_{1dB}	1-dB compression point
$P_{out,1dB}$	Output 1-dB compression point
P_{Noise}	Thermal noise
Q	Quality factor
Q_{ON}	Quality factor in ON state
r	Amplitude of complex gain
R_v	Varactor loss
S	Transmit signal
S'	Signal through the cancellation loop
t_{Rx}	Receive time
t_{Tx}	Transmit time
T	Room temperature
V_0	Amplitude of signal with 0° phase offset
V_{90}	Amplitude of signal with 90° phase offset
$x(t)$	Input signal
X	Reactance of the load
$y(t)$	Output signal
Z	Impedance
Z_C	Characteristic impedance
α_i	i^{th} order non-linearity constant
Γ	Reflection coefficient
θ	Phase of complex gain
τ_1	Delay
ϕ	Phase shift
ω	angular frequency

Chapter 1

Introduction

LTE (Long Term Evolution) is a wireless communications standard of high speed data for handsets and any data terminals. The LTE system is an update to the UMTS (Universal Mobile Telecommunication System) technology, which completes the technology progress continuing from GSM (Global System for Mobile communications) to UMTS by providing the services beyond the voice calls and with significantly faster data rates. The 3GPP (3rd Generation Partnership Project) organisation is the dominant standard developer for the LTE, which was established in December 1998 [1]. The main aim of 3GPP was to provide globally applicable technical specifications and reports for the 3rd generation (3G) mobile system, based on developed networks and their supported technologies.

Various LTE frequency bands are allocated to be used around the world. Using different frequency bands means that the frequency dependant components of the handsets differ based on the targeted market. As the number of allocated bands continue to

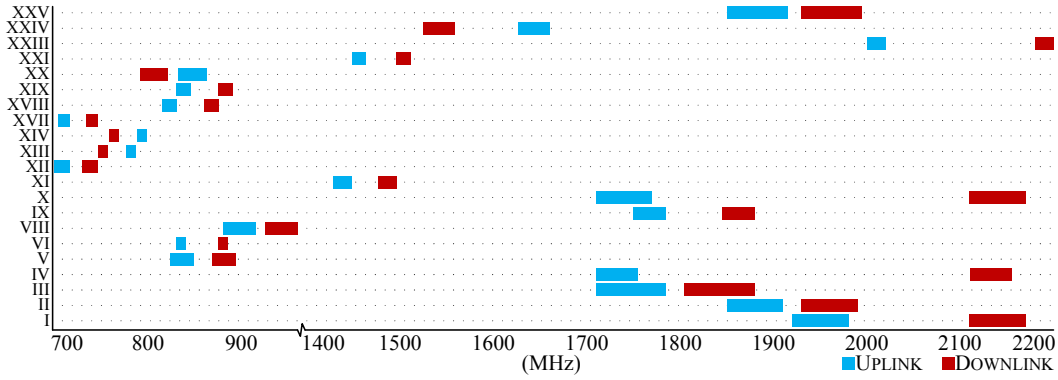

FIGURE 1.1: LTE frequency bands showing uplink and downlink frequency allocation.

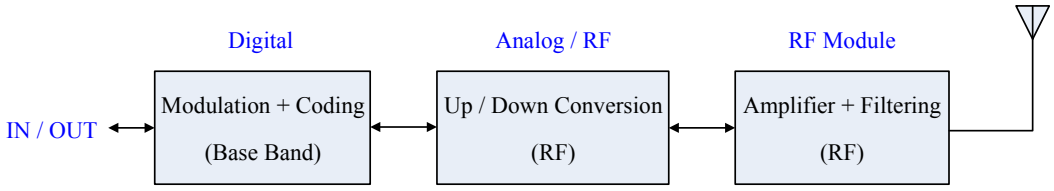

FIGURE 1.2: The basic building blocks of a traditional mobile handset.

rise, handset designers are required to include switching elements in handset Radio Frequency Front Ends (RFFEs) to provide multi-band devices, when roaming in different regions of the world. A selection of 25 bands and their frequency allocation is shown in Fig. 1.1 as per ITU (International Telecommunication Union). Any given country will use a subset of these bands (≈ 3-8 bands). Considering mobile telephony is becoming the biggest consumer electronics product in the world, the availability of low-cost terminals with long battery life and less complexity is a significant consideration for competitive deployment of LTE.

1.1 Transceiver Architecture

The basic functional building blocks of a traditional mobile handset is shown in Fig. 1.2. From the left there is a baseband circuit, responsible for modulation and coding the

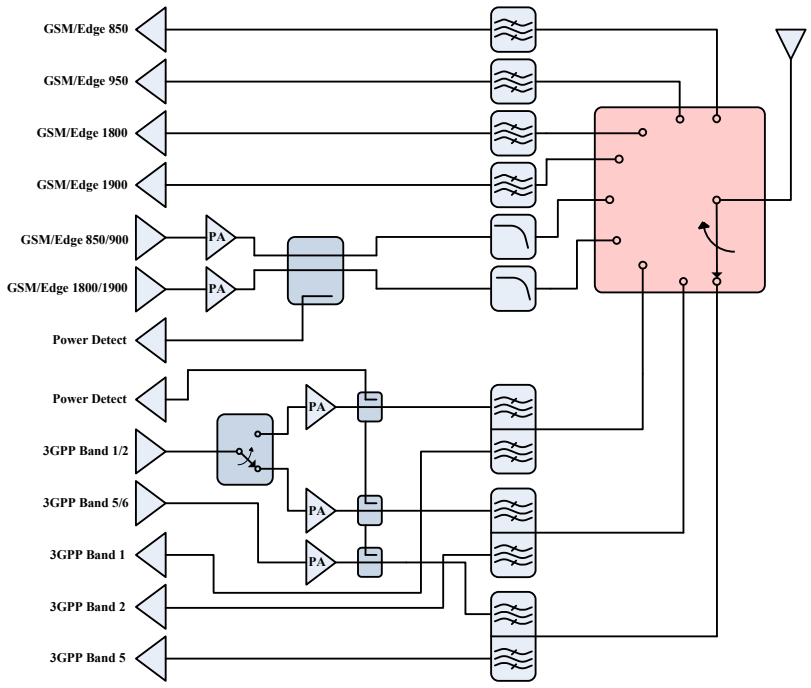

FIGURE 1.3: An RF switch, SP9T (single-pole nine-throw).

input data into two analog in-phase and quadrature signals. These signal pass into the RF circuit which does the up-conversion to radio frequency. The circuit has a separate RF input and output for each frequency band. Finally the RF module consists of power amplifiers (PAs), filters, duplexers and a switch that connects the appropriate signals to the antenna. A more detailed structure of the RF module is shown in Fig. 1.3.

PIN diodes were widely used for switching purposes in GSM-only handsets, due to their high performance and low cost. However, since the evolution of multi-band systems, PIN diodes no longer meet system requirements. This created a technology gap, which is filled by IC-based switching devices that are manufactured using UltraCMOS or GaAs technologies. Fig. 1.3 shows an RF switch, SP9T (single-pole nine-throw), which provides multi-band functionality for the radio frequency front ends in smart phones. The switch simply routes all the PAs and their associated filters to the antenna.

Peregrine Semiconductor's UltraCMOS technology, benefiting from a low-loss and

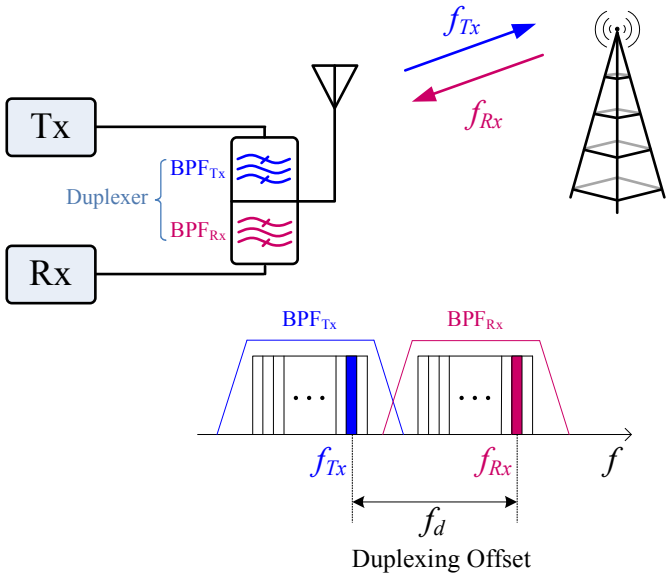

FIGURE 1.4: A traditional duplexer; block diagram and frequency response.

low-parasitics of its sapphire substrate, is the first CMOS technology to provide a solution for switching in the RFFE. The UltraCMOS SP9T device (manufactured in 0.5 μm process) has a smaller foot print in comparison with the GaAs competitor (34% smaller) and better linearity performance without requiring external matching components. Peregrine's latest SP10T and SP8T devices support 4G LTE insertion loss and linearity requirements and offer flexible switching arrangements.

One of the key frequency dependant components in a handset is the duplexer. Fig. 1.4 shows a block diagram of a traditional duplexer. A duplexer is a three port device which enables the system to use a common antenna for concurrent transmission and reception on two separate frequencies (f_{Tx} and f_{Rx}), while providing the required isolation between the two. The isolation is performed by two band pass filters placed in the transmitting and receiving paths (BPF_{Tx} and BPF_{Rx}), and operating at the transmit and receive frequencies, respectively.

Traditional duplexers use fixed frequency filters for each band of operation. These

filters are bulky and costly devices, and their insertion loss forces the transmitter to have a higher output power than would normally be expected, which greatly reduces the 'talk-time' in handsets. The uplink and downlink frequency allocations for each band is shown in Fig. 1.1.

Traditional duplexing filters are available in different technologies, such as lumped element (LC), cavity, ceramic, surface acoustic wave (SAW), bulk acoustic wave (BAW), and thin-film bulk acoustic resonator (FBAR or TFBAR) devices. Recent developments in the fabrication of BAW devices have demonstrated them to be linear and low noise components. As mentioned earlier, a duplexer filter is needed for each frequency band, therefore, a large number of duplexing filters are required in the multi-band devices (Fig. 1.5a). Replacing the fixed frequency filters with tunable devices can reduce the size and cost of the handsets significantly. However, designing the tunable duplexing filters with an ability to cover the extended frequency range in the LTE system is almost impossible.

Adaptive duplexing has been recently proposed as a solution to this problem [2, 3]. Fig. 1.5b shows the adaptive duplexer concept, which involves a low isolation device combined with an adaptive cancellation loop. This architecture can be employed to eliminate the need for multiple duplexers or to reduce their requirements for the multi-band implementation. The cancellation loop has a delay element and adjustable gain/phase devices. The latter must give precision adjustments, to reach the necessary cancellation requirement, yet it must also be capable of handling the large Tx signal without generating distortion. The phase adjustment component is the topic of this thesis.

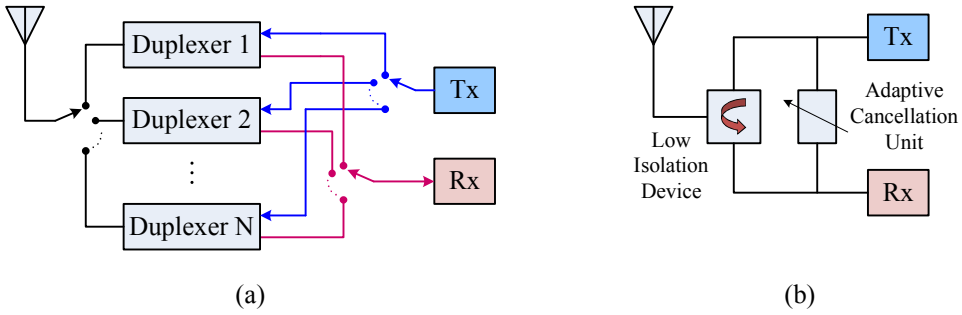

FIGURE 1.5: The multi-band RFFE a) using number of duplexers b) using an adaptive duplexer.

1.2 Research Objectives

This research has been targeted to implement a phase shifter device for adaptive duplexing applications, with a particular focus on implementation in a silicon based technology, suitable for inclusion on the existing transmitter/receiver (Tx/Rx) chip. The research objectives are:

- To study the adaptive duplexer and obtain the design requirements for a phase shifter device employed in the cancellation loop.
- To develop an appropriate phase shifting architecture with small chip area and low distortion.
- To choose the suitable process technology for implementing the phase shifter.
- To design, implement and measure the fabricated phase shifter device.

1.3 Research Contributions

The design requirements for a phase shifter device in the cancellation loop of an adaptive duplexer are obtained. To achieve an additional isolation of 35 dB through the cancellation loop a phase resolution of better than 1.15° (≈ 9-bit) is required. Two digital passive phase shifters, with 9- and 10-bit resolutions, are designed based on the delay type structure, and implemented in Peregrine Silicon-On-Sapphire (SOS) 0.25 μ m GC process. Both devices have the highest reported resolution and linearity to date.

The 9-bit device employs a novel control method to achieve high resolution while maintaining the size as small as a 6-bit device. The measured resolution of >8.1-bit is obtained, which provides more than 30 dB isolation, with an IIP_3 > +39 dBm. The 10-bit device benefits from a novel combination of an auto-transformer, a tunable delay line, and switched fixed phase stages. This results in a decreased insertion loss of 0.76 dB/bit and chip area of 3.4 mm^2. The phase resolution of > 9-bit provides at least 35 dB cancellation, with an IIP_3 of 55± 1 dBm.

The research has led to the following contributions:

- R. Amirkhanzadeh, H. Sjöland, J.-M. Redouté, D. Nobbe, and M. Faulkner, "High Resolution Passive Phase Shifters for Adaptive Duplexing Applications in SOS Process", Microwave Theory and Techniques, IEEE Transactions on, vol. 62, no. 8, pp. 1678–1685, Aug. 2014.

- R. Amirkhanzadeh, H. Sjöland, J.-M. Redouté, D. Nobbe, and M. Faulkner, ”L-Band 180° Passive Phase Shifter Employing Auto-Transformer in an SOS Process”, in Proc. of IEEE International Symposium on Circuits and Systems (ISCAS), Melbourne, Australia, Jun. 2014, pp. 333–336.

- R. Eslampanah, L. Linton, S. Ahmed, R. Amirkhanzadeh, M. Pourakbar, J.-M. Redouté, and M. Faulkner, ”Active Duplexing for Software Defined Radio”, in Proc. of IEEE International Symposium on Circuits and Systems (ISCAS), Melbourne, Australia, Jun. 2014, pp. 185–188 (*nominated among top 10 best student paperss*).

- R. Amirkhanzadeh, M. Pourakbar, J.-M. Redouté, M. Faulkner, ”Design considerations for switched passive circuits on silicon-on-sapphire (SOS) process technology”, 17th Asia and South Pacific Design Automation Conference, Jan. 2012.

- M. Pourakbar, R. Amirkhanzadeh, M. Tormanen, J.-M. Redouté, M. Faulkner, ”High Power and High Performance RF SOS FET Switches”, GigaHertz Symposium, Stockholm, Sweden, Feb. 2012.

- R. Amirkhanzadeh, H. Sjöland, A. Tikka, and M. Faulkner, ”Comparative analysis of switching performance of transistors in SOS process for RF applications,” in Proc. IEEE Asia Pacific Circuits Syst., Dec 2010, pp. 1111-1114.

1.4 Thesis Outline

This thesis is organised in eight chapters. A brief description of each chapter is outlined below:

- Chapter 2 reviews the background information on the RF aspects of the LTE system. Some basic concepts, such as duplexing and intermodulation distortion are also discussed.

- Chapter 3 discusses the adaptive duplexing applications, which includes division free duplexing and frequency division duplexing.

- Chapter 4 provides a review of the adaptive duplexing concept. A calculation of the design requirements for implementation of the gain and phase adjuster components in the cancellation loop of the adaptive duplexer is also presented in this chapter.

- Chapter 5 reviews the different methods of realising integrated phase shifters. The review includes implementation of active and passive phase shifters. The chapter concludes by choosing an appropriate method of implementing the phase shifter, based on the design requirements for the adaptive duplexer application.

- Chapter 6 discusses the Silicon-on-Sapphire (SOS) process technology and provides basic information about the passive and active devices, which are available in this process.

- Chapter 7 discusses the design steps of a 9-bit passive phase shifter. The experimental procedure and the measurement results of the device are provided in this chapter.

- The improvement to the 9-bit phase shifter design, which results in a higher resolution with a smaller foot print (10-bit phase shifter) are provided in Chapter 8. The measurement results conclude this chapter.

- Finally, a summary of the measured results for both the 9-bit and 10-bit devices are provided in Chapter 9. A comparison with state-of-the-art published work and commercial products, and potential future work are also provided.

Chapter 2

Background Information

In this chapter, the fundamental design requirements of a traditional wireless handset are presented. Particular emphasis is placed on the radio frequency subsystem that is responsible for transmission and reception. Some basic concepts of nonlinearity in an RFFE (RF Front End) are presented in Section 2.1. In Section 2.2, the duplexing modes and the duplexer as the key component of a full duplex scheme are discussed. The supported duplexing modes and the assigned frequency bands in LTE are provided in Section 2.3. The RF requirements of the transmitter and the receiver, as well as the duplexing requirements in LTE are discussed in Section 2.4, Section 2.5, and Section 2.6, respectively. Finally a summary is provided in Section 2.7.

2.1 Nonlinearity

Analog and RF circuits can be considered as a linear system under small signal conditions. However, large signals can cause nonlinear operation, which is not predictable

from a small signal model. A discussion of some of the nonlinear phenomena found in RFFEs are provided in this section [4].

The input/output characteristic of a memoryless nonlinear system can be approximated by:

$$y(t) \approx \alpha_1 x(t) + \alpha_2 x^2(t) + \alpha_3 x^3(t) \tag{2.1}$$

where, $x(t)$ is the input signal and $y(t)$ is the output signal. In the case of a small input signal ($x(t) \ll 1$), α_1 is the small signal gain, as the terms $x^2(t)$ and $x^3(t)$ are negligible. The nonlinearity effects are mainly caused by signal compression and modeled by the third-order term in Eq. 2.1. The second-order (even-order) effects are caused by waveform asymetry and can degrade some specific types of receiver architectures (such as direct-conversion receivers).

2.1.1 Harmonic Distortion

If the input of a nonlinear system is a sinusoidal signal, the output normally exhibits the harmonics of the input frequency. Using Eq. 2.1, if $x(t) = Acos\omega t$, then:

$$\begin{aligned} y(t) &= \alpha_1 Acos\omega t + \alpha_2 A^2 cos^2\omega t + \alpha_3 A^3 cos^3\omega t \\ &= \alpha_1 Acos\omega t + \frac{\alpha_2 A^2}{2}(1 + cos2\omega t) + \frac{\alpha_3 A^3}{4}(3cos\omega t + cos3\omega t) \\ &= \frac{\alpha_2 A^2}{2} + \left(\alpha_1 A + \frac{3\alpha_3 A^3}{4}\right) cos\omega t + \frac{\alpha_2 A^2}{2} cos2\omega t + \frac{\alpha_3 A^3}{4} cos3\omega t \end{aligned} \tag{2.2}$$

The first term in the Eq. 2.2 is a dc term, which is caused by the second-order nonlinearity. The second term is the fundamental, and the third and forth terms are the second and

third harmonics, respectively. Two observations can be made from the above equation. Firstly, the even-order harmonics are generated by α_j with even j. These harmonics can be eliminated if the system has odd symmetry, i.e. a fully differential system. Secondly, the amplitude of the *nth* harmonic is proportional to A^n. Harmonic distortion is not important in many RF circuits, as they usually have narrow-band filters, which can suppress the distortions.

2.1.2 Gain Compression

Gain of a nonlinear system with an input of $Acos\omega t$ is equal to $\alpha_1 + \frac{3}{4}\alpha_3 A^2$, for the fundamental frequency (Eq. 2.2), which is proportional to A. However, the sign of α_1 and α_3 is more important in this equation. Considering the polynomial expression of a nonlinear system by Eq. 2.1, if $\alpha_1\alpha_3 > 0$, the term $\alpha_1 x(t) + \alpha_3 x^3(t)$ dominates the second-order term ($\alpha_2 x^2(t)$) for a large input signal, despite the sign of α_2. This results in an *expansive* characteristic. In contrast, if $\alpha_1\alpha_3 < 0$, the third-order term decreases the gain and compresses the characteristic; referred to as *compressive* behaviour. Most RF circuits fall into the compressive category, therefore, we further discuss this type.

2.1.2.1 1-dB Compression Point (P_{1dB})

The effect of gain compression in a nonlinear system is measured by *1-dB compression point*. This is defined as the input signal level that results in a 1 dB reduction in the ideal value of the gain. Practically, the compression is expressed in terms of power quantities, defined as P_{1dB}.

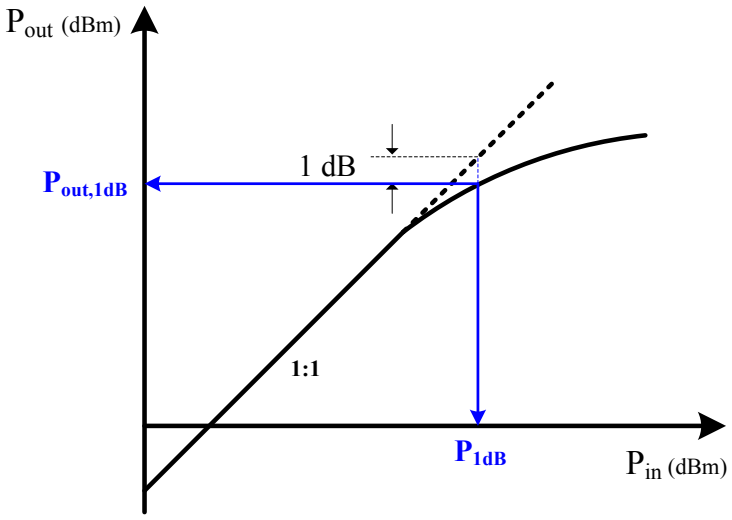

FIGURE 2.1: 1 dB compression point.

To calculate the 1-dB compression point, the compressed gain, $\alpha_1 + \frac{3}{4}\alpha_3 A_{1dB}^2$, is equated to 1 dB less than the ideal gain, α_1 :

$$20\,log\left|\alpha_1 + \frac{3}{4}\,\alpha_3\,A_{1dB}^2\right| = 20\,log\,|\alpha_1| - 1\,dB \tag{2.3}$$

where, A_{1dB} is the input signal level, in which the compression occurs. Therefore :

$$A_{1dB} = \sqrt{0.145\left|\frac{\alpha_1}{\alpha_3}\right|}. \tag{2.4}$$

Thus,

$$P_{1dB} = 10\,log\left(0.145\left|\frac{\alpha_1}{\alpha_3}\right|\right). \tag{2.5}$$

By increasing the input power beyond the 1-dB compression point, the RF circuit eventually saturates, and the output power remains constant. Fig. 2.1 demonstrates the compression concept. The output 1-dB compression power, denoted as $P_{out,1dB}$, can also be calculated as:

$$P_{out,1dB} = 20\,log\,\alpha_1 + P_{1dB} - 1\,dB\,. \tag{2.6}$$

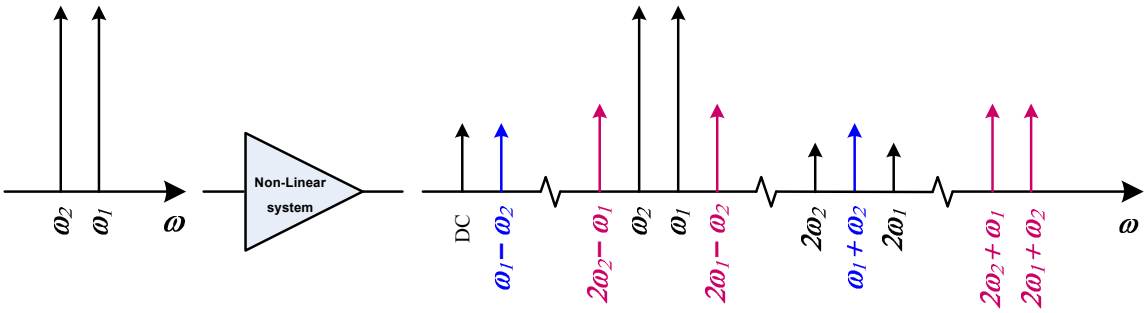

FIGURE 2.2: Intermodulation products in a two-tone test.

Gain compression can adversely affect the RFFE receiver. The problem takes place when a strong jamming signal coincides with the received signal. Despite the frequency difference between the two signals, the jammer causes the receiver to saturate, as in the time domain the small received signal is superimposed on the large interferer. This phenomenon is called *desensitisation* and reduces the signal-to-noise ratio (SNR) of the receiver.

2.1.3 Intermodulation

In characterising the harmonic distortion performance of a nonlinear system, it is assumed that the system experiences a single signal. However, this is not a practical measure for a multi-band system that involves different frequencies. When two interfering signals mix through a nonlinear system, the output contains components that are not the harmonics of the input frequencies. These components are defined as *intermodulation (IM)* products, which are generated by the multiplication of the two input frequencies. To investigate this effect, it is assumed that the input signal in Eq. 2.1 is

$x(t) = A_1 cos\omega_1 t + A_2 cos\omega_2 t$. Thus,

$$y(t) = \alpha_1(A_1 cos\omega_1 t + A_2 cos\omega_2 t) + \alpha_2(A_1 cos\omega_1 t + A_2 cos\omega_2 t)^2 + \alpha_3(A_1 cos\omega_1 t + A_2 cos\omega_2 t)^3. \quad (2.7)$$

Expanding the equation, we can categorize the components as:

$$\begin{aligned} \omega_1 &: \quad \left(\alpha_1 A_1 + \frac{3}{4}\alpha_3 A_1^3 + \frac{3}{2}\alpha_3 A_1 A_2^2\right) cos\omega_1 t \\ \omega_2 &: \quad \left(\alpha_1 A_2 + \frac{3}{4}\alpha_3 A_2^3 + \frac{3}{2}\alpha_3 A_2 A_1^2\right) cos\omega_2 t \end{aligned} \quad (2.8)$$

ω_1 and ω_2 are the fundamental components.

$$\omega_1 \pm \omega_2 : \quad \alpha_2 A_1 A_2 \, [cos(\omega_1 + \omega_2)t + cos(\omega_1 - \omega_2)t \,] \quad (2.9)$$

$\omega_1 \pm \omega_2$ are the second-order IM products.

$$\begin{aligned} 2\omega_1 \pm \omega_2 &: \frac{3}{4}\alpha_3 A_1^2 A_2 \, [\, cos(2\omega_1 + \omega_2)t + cos(2\omega_1 - \omega_2)t \,] \\ 2\omega_2 \pm \omega_1 &: \frac{3}{4}\alpha_3 A_1 A_2^2 \, [\, cos(2\omega_2 + \omega_1)t + cos(2\omega_2 - \omega_1)t \,] \end{aligned} \quad (2.10)$$

$2\omega_1 \pm \omega_2$ and $2\omega_2 \pm \omega_1$ are the third-order IM products. Among these four terms, the third-order IM products with the frequencies at $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ are of particular interest. If ω_1 and ω_2 have small separation, then $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ appear in the vicinity of ω_1 and ω_2. The problem arises when one of these third-order IM products falls into the desired channel and corrupts the signal. Fig. 2.2 illustrates the intermodulation products in a two-tone test.

2.1.3.1 Third Order Intercept Point (IP_3)

The IM performance of a nonlinear system is defined as *third order intercept point (IP_3)*. IP_3 is commonly measured using a two-tone test, where the amplitude of both tones are equal. Therefore, the input of the nonlinear system is $x(t) = A\,(cos\omega_1 t + cos\omega_2 t)$. Considering Eq. 2.8 and Eq. 2.10, the fundamental and third-order IM components of the output are:

$$y(t) = \left(\alpha_1 + \frac{9}{4}\alpha_3 A^2\right) A\,[\,cos\omega_1 t + cos\omega_2 t\,] + \frac{3}{4}\alpha_3 A^3\,[\,cos(2\omega_1 - \omega_2)t + cos(2\omega_2 - \omega_1)t\,] + ... \tag{2.11}$$

Assuming $\alpha_1 \gg \frac{9}{4}\alpha_3 A^2$, it can be seen that by increasing A, the amplitude of the fundamental increases in proportion to A, but that of the third-order IM products increase in proportion to A^3. If A continues to rise, the amplitude of the third-order IM products at the output becomes equal to the amplitude of the fundamental. The point at which this phenomenon occurs is the IP_3. The input and corresponding output levels at this point are called the *input third order intercept point (IIP_3)* and *output third order intercept point (OIP_3)*, respectively. This is demonstrated in Fig. 2.3.

At the IP_3 point, we have:

$$\left|\,\alpha_1 A_{In,IP_3}\,\right| = \left|\frac{3}{4}\alpha_3 A^3_{In,IP_3}\right|, \tag{2.12}$$

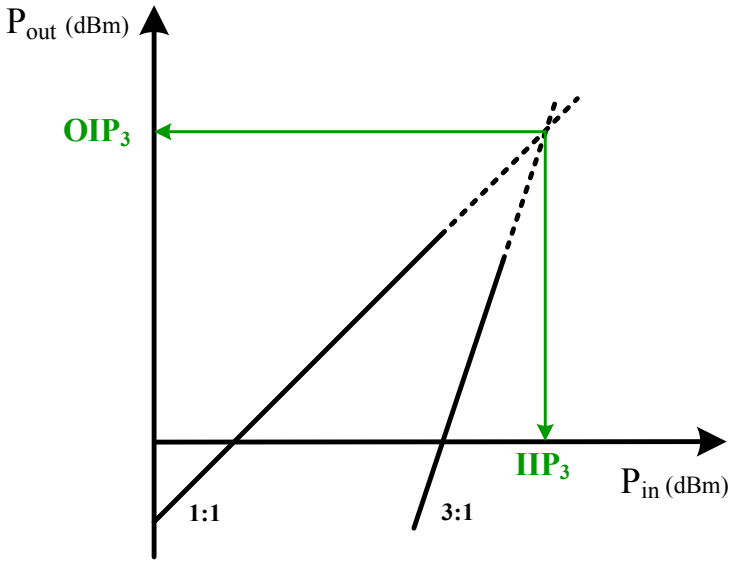

FIGURE 2.3: Third order intercept point.

where, A_{In,IP_3} is the amplitude of the input and is calculated as:

$$A_{In,IP_3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|}. \tag{2.13}$$

Then the power representation of the IIP_3 is:

$$IIP_3 = 10\,log\left(\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|\right), \tag{2.14}$$

and OIP_3 is:

$$OIP_3 = 20\,log\,|\alpha_1| + IIP_3, \tag{2.15}$$

Considering Eq. 2.14 and Eq. 2.5, we have :

$$IIP_3 - P_{1dB} = 10\,log\left(\frac{4/3}{0.145}\right) \approx 9.6\,dB \tag{2.16}$$

The above relationship is an approximation, as the nonlinear system discussed here is

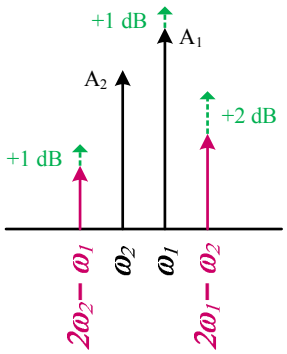

FIGURE 2.4: Intermodulation products with unequal jamming signals.

considered a third order system. The IP_3 is a theoretical concept, and in practice it can never be measured directly, since the amplifier would be significantly overloaded by the time that it reached the IP_3 point.

When the jamming signals, A_1 and A_2 are not equal, then the two IM products are also not equal. The larger IM product is closest to the larger jamming signal, A_1 in this case (Fig. 2.4). Considering Eq. 2.10, a 1 dB increase in A_1 (@ ω_1) leads to a 2 dB increase in $IM_{A_1^2 A_2}$ (@ $2\omega_1 - \omega_2$), and a 1 dB increase in $IM_{A_1 A_2^2}$ (@ $2\omega_2 - \omega_1$).

2.2 Duplexing

In order to have bidirectional communication, it is necessary to have a duplex scheme. This is possible by transmission over a link in each direction at the same time (full-duplex) or at different time slots (half-duplex). In this section, the duplexing schemes and duplexer circuit are discussed.

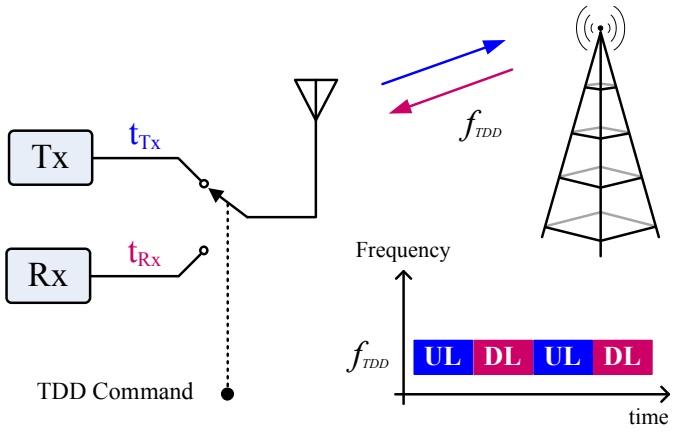

FIGURE 2.5: Time division duplexing.

2.2.1 Time Division Duplex (TDD)

In a half-duplex system, the required separation between the up-link (UL) and the down-link (DL) is provided by using the different time slots. The system is called Time Division Duplex if the same carrier frequency is used for transmission in both directions. Fig. 2.5 shows the operational concept of a TDD system. The transmission is generally fast enough to be transparent to the user.

The antenna is alternatively connected to the transmit (Tx) and receive (Rx) paths by an RF switch, which usually has an insertion loss of less than 1 dB. Regardless of the high transmit power, there is no leakage from the transmitter to the receiver, as the transmitter is simply turned off while receiving signals. However, the strong signals from the neighbouring transmitters that fall in the receive band can desensitize the receiver.

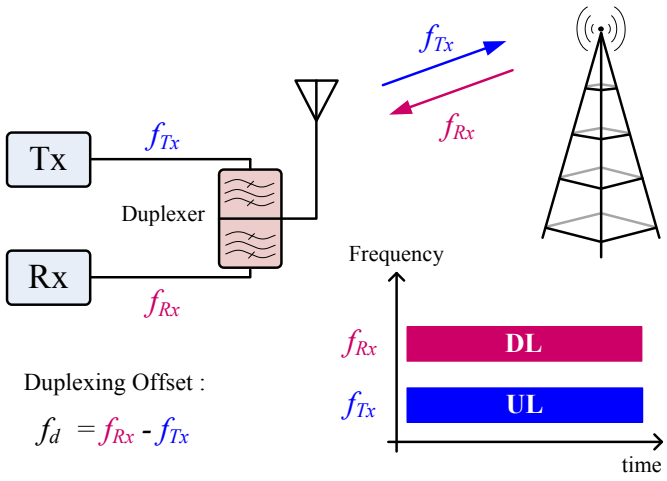

FIGURE 2.6: Frequency division duplexing.

2.2.2 Frequency Division Duplex (FDD)

In a full-duplex system, different carrier frequencies are employed for UL and DL transmissions. This is refereed to as Frequency Division Duplex, and is shown in Fig. 2.6. A pair of frequencies, f_{Rx} and f_{Tx} , with a fixed frequency offset defined as the duplexing offset, f_d, are used to define a radio channel in the system. At the user end, where the transmitter and receiver share a common antenna, duplexing filters are required to obtain sufficient isolation between the Tx and Rx paths. However, base stations can operate separate antennas for the Tx and Rx paths to achieve the required isolation.

The loss associated with the duplexing filters is around 3 dB, which is much higher than the RF switch used in the TDD system. From the transmitter point of view, a 3 dB loss means that only 50% of the power reaches the antenna. On the other hand, in the Rx path, this increases the noise figure by 3 dB.

2.2.3 Half Duplex FDD (HD-FDD)

In a TDD system, different carrier frequencies may be used for UL and DL. In this case the system is called Half-Duplex FDD. HD-FDD can be considered as a hybrid combination of FDD and TDD systems. If the users are scheduled at exclusive time slots, the transmission resources can be occupied fully, without the need for the simultaneous transmission and reception at each user-end. Therefore, the base-station is required to be full-duplex, as per Fig. 2.6, while the user terminals are half-duplex, as per Fig. 2.5. The benefit being that expensive duplexing filters are not required for the user terminals. GSM is an example of such a system.

2.2.4 Duplexer

The duplexer is a key component in a full duplex system. It is a filtering device, which isolates the transmitter and the receiver, where there is a common antenna shared between them (Fig. 1.4). It consists of two band-pass filters (BPFs), one in the Tx band and the other in Rx band.

The BPF in the Rx path (denoted as BPF_{Rx} in Fig. 1.4) attenuates the transmitter leakage in the Rx path to avoid the receiver desensitisation by the strong Tx signal, as shown in Fig. 2.7.

The BPF in the Tx path (denoted as BPF_{Tx} in Fig. 1.4) decreases the transmitter's noise level at the Rx frequency and stops it from leaking to the receiver. This is illustrated in Fig. 2.8.

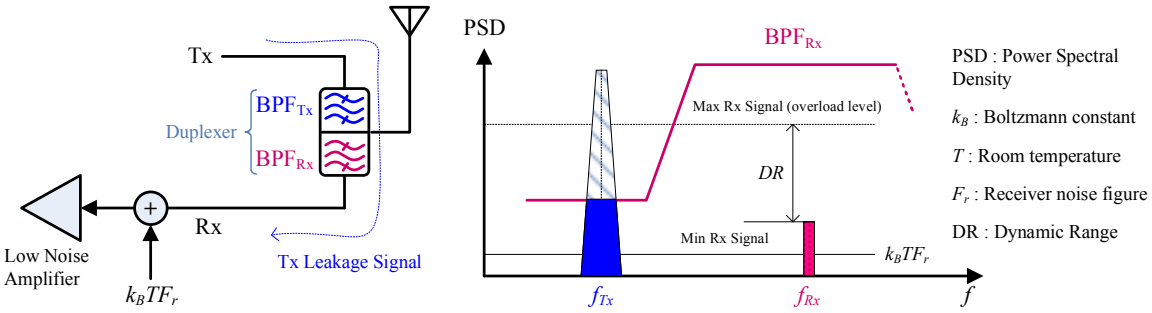

FIGURE 2.7: Receiver desensitisation due to overload by Tx signal unless attenuated by BPF_{Rx}.

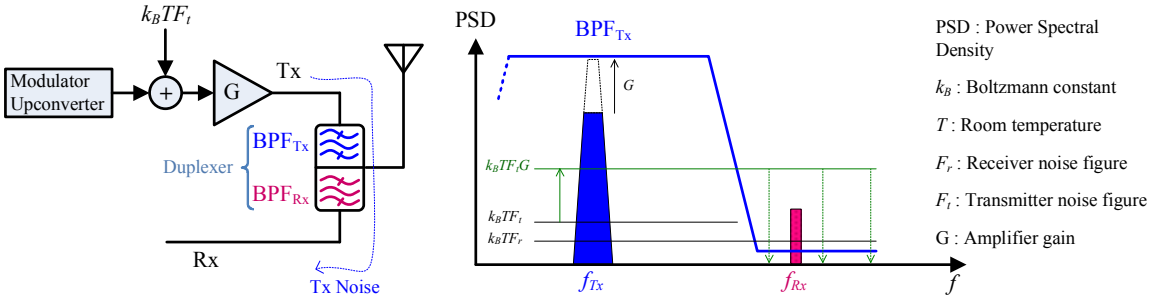

FIGURE 2.8: Transmitter noise in the Rx band is attenuated by BPF_{Tx}.

2.3 LTE Duplex Modes and Frequency Bands

2.3.1 Duplex Modes

Fig. 2.9 shows a diagram of three duplex modes supported by LTE. LTE TDD was developed to support the evolution of TD-SCDMA (Time-Division Synchronous Code Division Multiple Access) for the Chinese market. However, the design of the mobile handsets can be simplified without the need for multi-band duplexers if they take the advantage of HD-FDD and TDD systems.

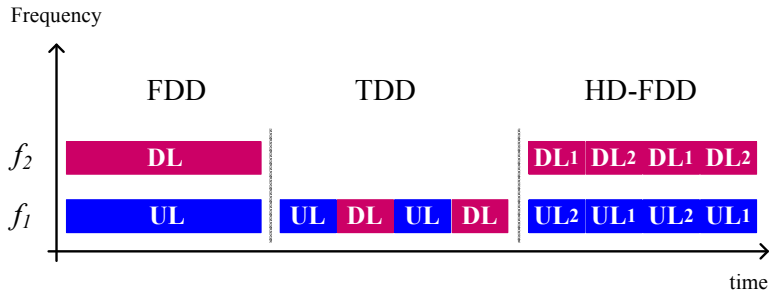

FIGURE 2.9: FDD, TDD and HD-FDD duplex modes.

TABLE 2.1: FDD

Band No.	Uplink (MHz)	Downlink (MHz)	Width of Band (MHz)	Duplex Offset (MHz)	Band Gap (MHz)
1	1920-1980	2110-2170	60	190	130
2	1850-1910	1930-1990	60	80	20
3	1710-1785	1805-1880	75	95	20
4	1710-1755	2110-2155	45	400	355
5	824-849	869-894	25	45	20
6	830-840	875-885	10	35	25
7	2500-2570	2620-2690	70	120	50
8	880-915	925-960	35	45	10
9	1749.9-1784.9	1844.9-1879.9	35	95	60
10	1710-1770	2110-2170	60	400	340
11	1427.9-1452.9	1475.9-1500.9	20	48	28
12	698-716	728-746	18	30	12
13	777-787	746-756	10	-31	41
14	788-798	758-768	10	-30	40
15	1900-1920	2600-2620	20	700	680
16	2010-2025	2585-2600	15	575	560
17	704-716	734-746	12	30	18
18	815-830	860-875	15	45	30
19	830-845	875-890	15	45	30
20	832-862	791-821	30	-41	71
21	1447.9-1462.9	1495.5-1510.9	15	48	33
22	3410-3500	3510-3600	90	100	10
23	2000-2020	2180-2200	20	180	160
24	1625.5-1660.5	1525-1559	34	-101.5	135.5
25	1850-1915	1930-1995	65	80	15
26	814-849	859-894	30/40		10
27	807-824	852-869	17	45	28
28	703-748	758-803	45	55	10
29	n/a	717-728	11		
30	2305-2315	2350-2360	10	45	35
31	452.5-457.5	462.5-467.5	5	10	5

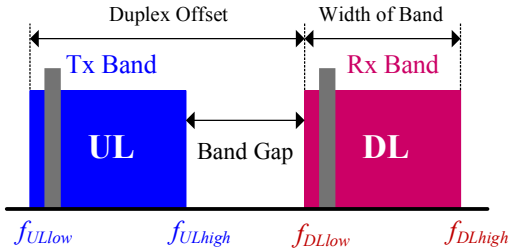

FIGURE 2.10: Frequency band definition in LTE

TABLE 2.2: TDD

Band No.	Allocation (MHz)	Width of Band (MHz)
33	1900-1920	20
34	2010-2025	15
35	1850-1910	60
36	1930-1990	60
37	1910-1930	20
38	2570-2620	50
39	1880-1920	40
40	2300-2400	100
41	2496-2690	194
42	3400-3600	200
43	3600-3800	200
44	703-803	100

2.3.2 Frequency Bands

A wide range of different frequency bands are allocated for FDD and TDD operations in LTE. Fig. 2.10 presents the definition used in frequency bands specifications in LTE. In each band, we have :

$$\begin{aligned} Width-of-Band &= f_{ULhigh} - f_{ULlow} = f_{DLhigh} - f_{DLlow} \\ Band-Gap &= f_{DLlow} - f_{ULhigh} \\ Duplex-Offset &= f_{DLlow} - f_{ULlow}\,. \end{aligned}$$

The details of the frequency bands for FDD and TDD are given in Table 2.1 and Tabel 2.2, respectively.

2.4 LTE Transmitter RF Requirements

The design requirements of a transmitter to satisfy the LTE RF performance specifications are discussed in this section. There are two types of requirements to be met: the parameters related to the power level and quality of the transmitted signal, and the parameters dependant on the unwanted emissions.

2.4.1 Intended Transmission

The intended transmission is confined to the channel band width (BW) and has some key specifications.

- Transmit Output Power :

  In LTE, the maximum transmitted power is defined as 23 dBm, measured at the antenna. The handheld device is required to satisfy this measure within a range of ±2 dB.

- Signal Quality : Error Vector Magnitude (EVM)

  The EVM is the main measure of the transmitted signal's quality, which is specified as the magnitude difference between a theoretical signal and the real transmitted signal. The EVM is usually the result of the RF imperfection of practical realisation.

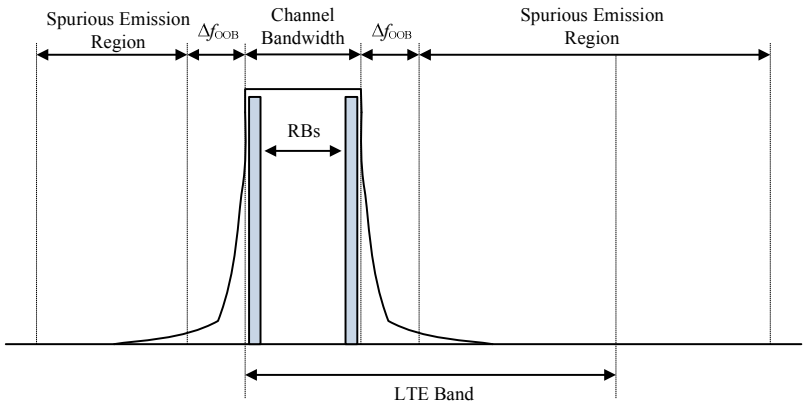

FIGURE 2.11: Transmitter spectrum in LTE [7].

The required EVM in LTE depends on the type of modulation. For Example, it is required to be less than 17.5% for QPSK (Quadrature Phase-Shift Keying), and less than 12.5% for 16QAM (Quadrature Amplitude Modulation) [5, 6].

2.4.2 Unwanted Emission

The transmitted signal's power outside the channel should be zero, however this is the ideal case. There are two categories of unwanted emissions, which are specified in LTE; Out-Of-Band (OOB) emissions and spurious emissions. Fig. 2.11 shows the transmitter spectrum. It can be seen that the OOB emissions are the emissions closer to the channel, while the spurious ones can be at any other frequency.

- Out-Of-Band Emissions:

  These type of emissions are often a result of the modulation process due to non-linearity in the PAs. Therefore, reducing the power level of the transmitted signal will decrease the OOB emissions. OOB emissions are defined using Spectrum Emission Masks (SEMs) and Adjacent Channel Leakage Ratio (ACLR) measures. SEM depends on the BW of the transmitted signal, as per Fig. 2.12.

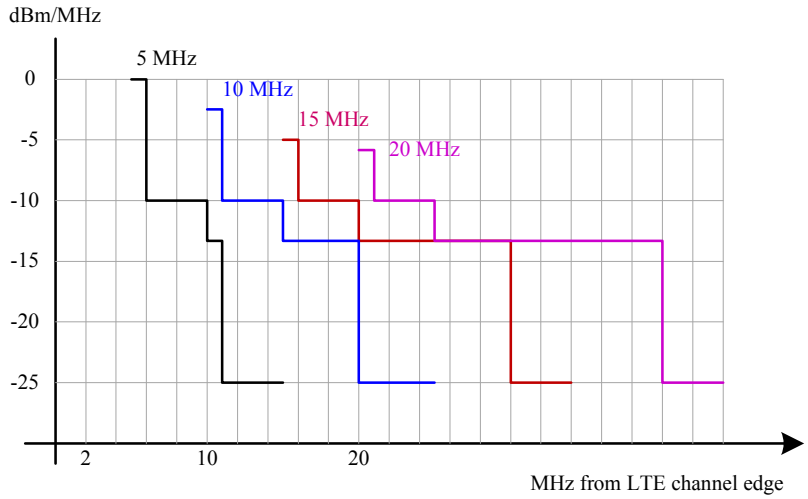

FIGURE 2.12: Spectrum Emission Mask for a user-end transmitter for different channel bandwidths [7].

ACLR measures the effect of OOB emissions on the neighbouring channels, and is defined as the ratio of the mean power at the centre of the assigned channel to the mean power at the centre of an adjacent channel. The powers are measured after filtering. For an adjacent LTE channel with 20 MHz BW, the ACLR of a wireless terminal is required to be > 30 dB.

- Spurious Emissions:

  These unwanted emissions occur well outside the channel, so the power of the transmitted signal might not affect them. Spurious emissions are caused by any non-ideal effects and consist of intermodulation products and harmonic emissions. The required limits of the spurious emissions in LTE depend on the frequency range, with a maximum level of -30 dBm/MHz over 1 GHz. The LTE receive band has even tougher requirements.

- Emissions in the Rx Band:

In LTE, to test a receiver in a full-duplex FDD operation mode, the transmitter is also required to be operating. From the receiver point of view, not only the fundamental component of the transmitted signal acts as a jammer (having high signal power in the transmit band), but also the OOB emissions of the transmitter can fall into the receive band.

The maximum permitted spurious emissions from a handheld device in LTE is -47 dBm/1 MHz (-107 dBm/Hz). Considering the maximum transmit power of a mobile device in LTE, being +23 dBm (measured at the antenna), the requirement for the spurious emissions is -130 dBc/Hz. However, this requirement for UMTS is more robust, being -149.8 dBc/Hz.

2.5 LTE Receiver RF Requirements

The receiver requirements in LTE are mainly based on UMTS requirements, since all transceivers are backward compatible, and UMTS often has the tighter specifications.

2.5.1 General Requirements

For testing purposes, a number of key assumptions are considered. The receiver is assumed to have two antenna ports, and an integrated antenna with 0 dBi gain (compared with the hypothetical isotropic antenna). It is assumed that the energy is distributed uniformly in all directions.

2.5.2 Transmit Signal Leakage

To measure a receiver's performance, the transmitter operates at its full power. In order to allow not more than 0.5 dB degradation in the receiver's sensitivity, the transmitter's noise is required to be 9 dB less than the Noise Floor (NF) at the antenna (NF = -174 dBm/Hz, NF-9 dB = -183 dBm/Hz). The duplexing filter provides the necessary isolation to meet this requirement. Typical duplexers can provide around 50 to 55 dB isolation. We assume similar transmitter performance requirements for this work. In particular, any spirous signals generated by the adaptive duplexing process, must meet the -183 dBm/Hz specifications.

2.5.3 Selectivity and Blocking Specifications

A receiver's ability to acquire a wanted signal, while interfering signals exist in adjacent channels and beyond, is measured by selectivity and blocking tests. The requirements for a 5 MHz BW signal are shown in Fig. 2.13. In general, the ability to reject these signals increases with frequency offset from the receive channel.

- Adjacent Channel Selectivity (ACS):

  Measured in dBc, is the jamming signals strength above the received signal level. ACS is defined by the receiver filtering.

- Blocking:

  Measured in dBm, is the strength of jamming signals that the receiver must accommodate. Blockers are normally attenuated by filtering, but can also generate

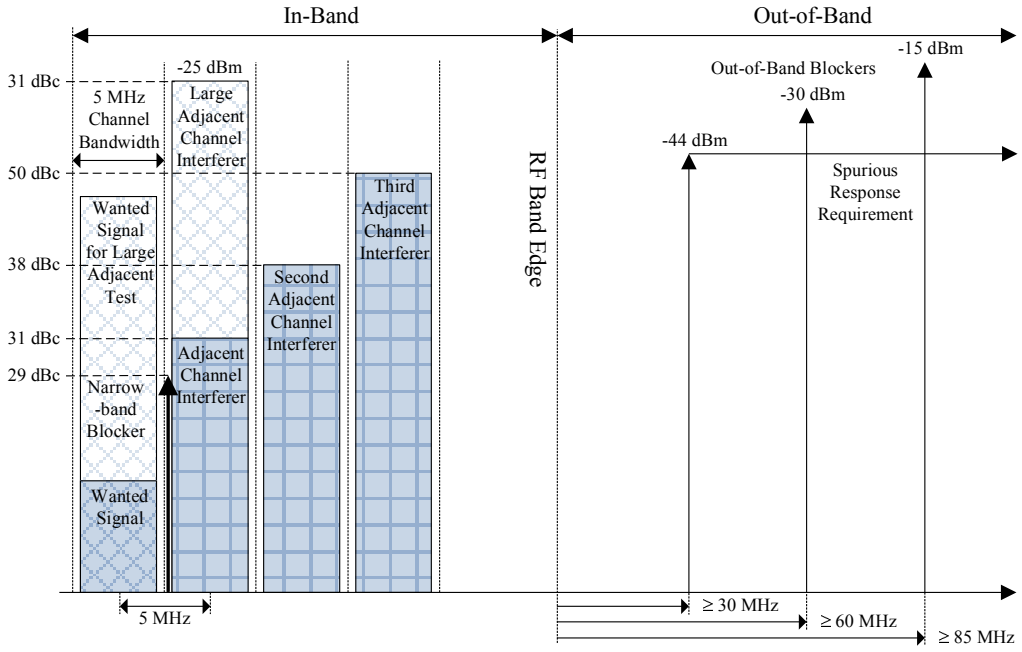

FIGURE 2.13: Selectivity and blocking requirements for a 5 MHz user end in LTE [7].

intermodulation products that are in-band and can not be removed by filtering. In this thesis, the intermodulation performance of the phase shifter is designed to meet the receiver's blocking requirements.

2.5.4 Intermodulation Requirements

A non-linear system, in the presence of two or more signals, generates intermodulation products, which can appear in the desired frequency band. The signals can be in-band or out-of-band. In-band interfering tones cause more critical problems, since there is no attenuation provided by the RF filter. This concept has been discussed in Section 2.1.

LTE intermodulation performance is defined by a wideband interferer and a narrow-band (single tone) interferer each with a power of -46 dBm. The wideband interferer has the same bandwidth as the desired signal or 5 MHz, whichever is the smaller. The single tone is placed mid-way between the desired and interference signals. In order

to have a constant IMD requirement for different bandwidths, the desired signal level is considered to be around -94 dBm despite its bandwidth. The standard method to evaluate the receiver's IMD performance is to determine the third-order-intercept point (IP_3).

2.6 LTE Duplexing Requirements (*Typical Example*)

Fig. 2.14 shows a block diagram of the transceiver, which demonstrates the transmitter leakage in the receiver. A typical duplexer provides ≈ 50 dB isolation between the transmitter and the receiver, with a 2 dB loss from the transmitter to the antenna and the antenna to the receiver. The maximum transmit power at the output of the PA is +25 dBm, therefore, the transmitter leakage at the input of the Low Noise Amplifier (LNA) is equal to -25 dBm.

As discussed in Section 2.5.2, to stop transmitter leakage from desensitising the receiver, the transmitter's noise level at the receive band should be 9 dB less than the NF. This implies a maximum permitted transmitter noise level at the receive band of -183 dBm/Hz. Considering the isolation provided by the duplexer, the noise level of the transmitter at the receive band is set to -133 dBm/Hz (as per Fig. 2.14).

There is a trade off between the duplexer requirement and the transmitter/receiver requirement. By providing higher isolation through the duplexer, the transmitter's noise requirement can be relaxed. Similarly, designing a transmitter with low noise level can ease up the duplexer specifications.

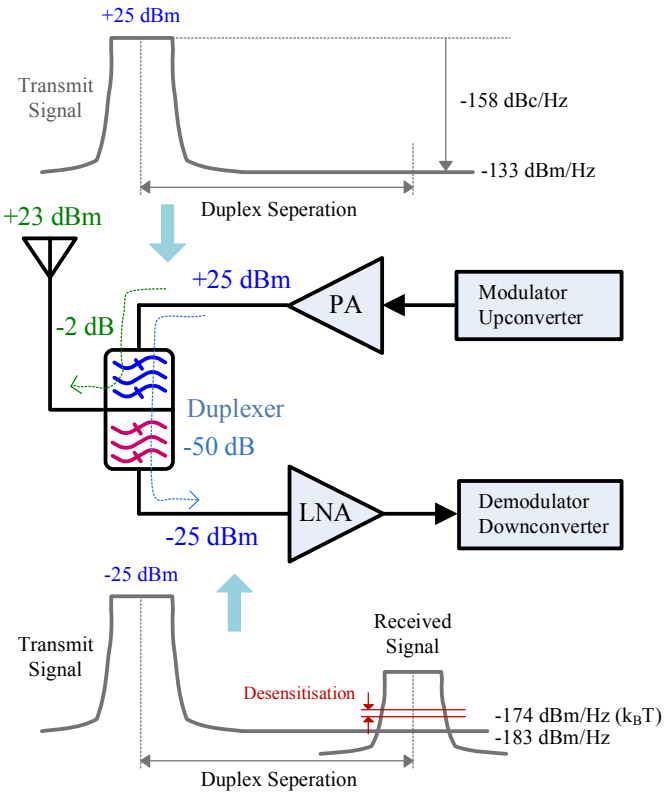

FIGURE 2.14: Tx leakage in the receiver in LTE [7].

The transmitter's leakage in the receiver can coincide with a blocker, which may result in IM3 products. If the blocker appear mid-way between the Tx and Rx bands, then the IM3 products will fall into the Rx band. The duplexing offset in Band 1 is 190 MHz, therefore a blocker at 95 MHz offset will cause IMD. Today's radio receivers can meet blocker requirements if the Tx leakage signal is below -25 dBm (Fig. 2.14), implying 50 dB od duplexer isolation. An adaptive duplexer must meet or exceed this specification.

2.7 Summary

In this chapter some fundamental concepts such as 1 dB compression point (P_{1dB}) and third order intercept point (IP_3) in RFFEs are presented. The importance of a duplexer

circuit in an FDD system and its operation is also discussed. LTE RF requirements for the transmitter and the receiver along with the duplexing constraints are provided. We discussed the significance of adaptive duplexing in the multi-band system in Chapter 1. Next chapter provides a review on applications of adaptive duplexing.

Chapter 3

A Review on Adaptive Duplexing

There are two applications for adaptive duplexing; Division Free Duplexing (often known as Full Duplexing) and Frequency Division Duplexing (FDD). The former uses the same channel for both transmission and reception, to double the spectrum efficiency. The latter is more traditional and targeted at filter replacement in existing systems. Both schemes have similar analog structures that require gain/phase adjusters as control elements.

3.1 Division Free Duplexing

A division free duplex method is proposed in [8] [9]. To provide full duplex operation, it is required to have around 110-130 dB isolation between the Tx and Rx paths, depending on the level of transmitted power. Fig. 3.1 shows the block diagram of this method. The self-interference cancellation is obtained by employing a combination of the following three techniques; (a) antenna placement, (b) analog RF cancellation, and

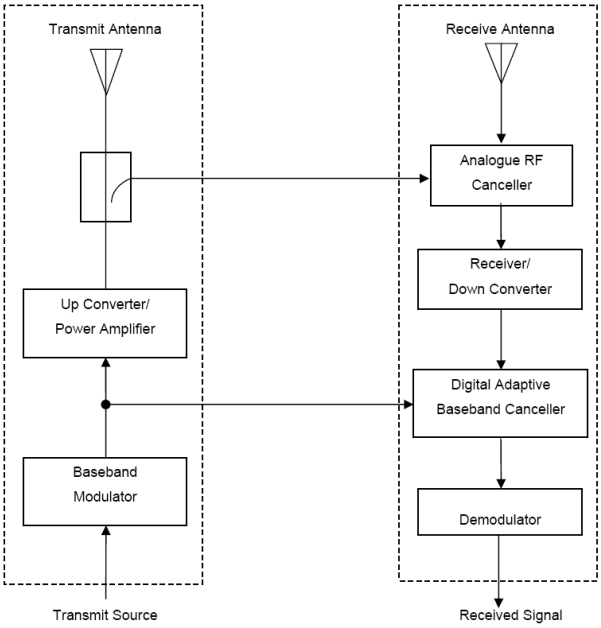

FIGURE 3.1: Block diagram of full duplex RF communication system [8].

(c) digital adaptive filtering. In [9] a total of 72 dB isolation is achieved; 27 dB by employing dual antennas and 45dB from the analog RF cancellation. The analog cancellation, which is usually performed before the LNA circuit, must be high enough to stop the interference signal desensitizing the LNA.

Recent research [10–13] use the same method, but with slightly different techniques for the cancellation. In [10] a balun cancellation method is employed for cancellation at RF, as shown in Fig. 3.2. The inverted signal through the balun is adjusted precisely in phase and amplitude using variable attenuators and delay lines. This approach provides wideband cancellation (40 dB for a 100 MHz signal), but requires high resolution gain/phase adjusters.

A full duplex system, presented in [11], provides 110 dB of self-interference signal cancellation for WiFi applications. This is achieved by obtaining 15 dB from a circulator, 45 dB from analog cancellation circuit, and 50 dB from the digital cancellation unit,

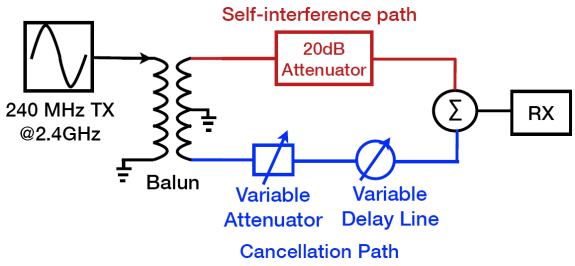

FIGURE 3.2: Balun cancellation method used in [10].

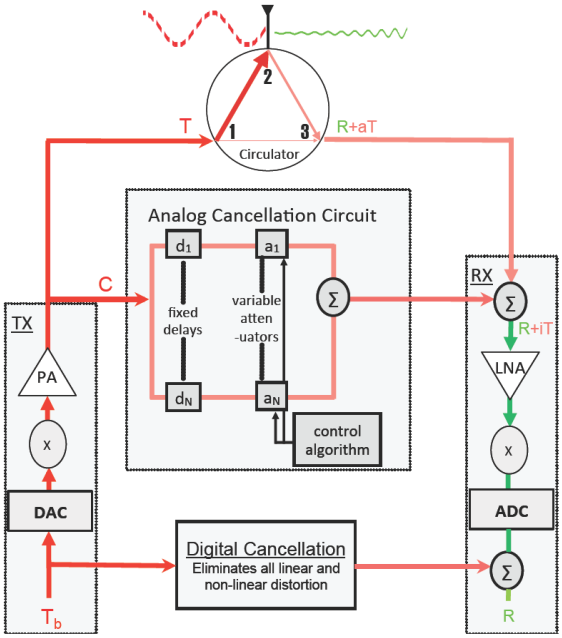

FIGURE 3.3: Full duplex configuration used in [11].

as shown in Fig. 3.3. A copy of the transmitted signal goes through the analog cancellation circuit to reconstruct the self-interference signal. This signal is then subtracted from the received signal to eliminate the self-interference signal.

The analog cancellation unit employs sixteen lines, with different but fixed delays and adjustable gains, to creat a copy of the self-interference signal. The delay lines are wires with different length, which occupy a large area in the implementation of the circuit. An Adjustable delay line (RF phase shifter) is a potential solution for this problem.

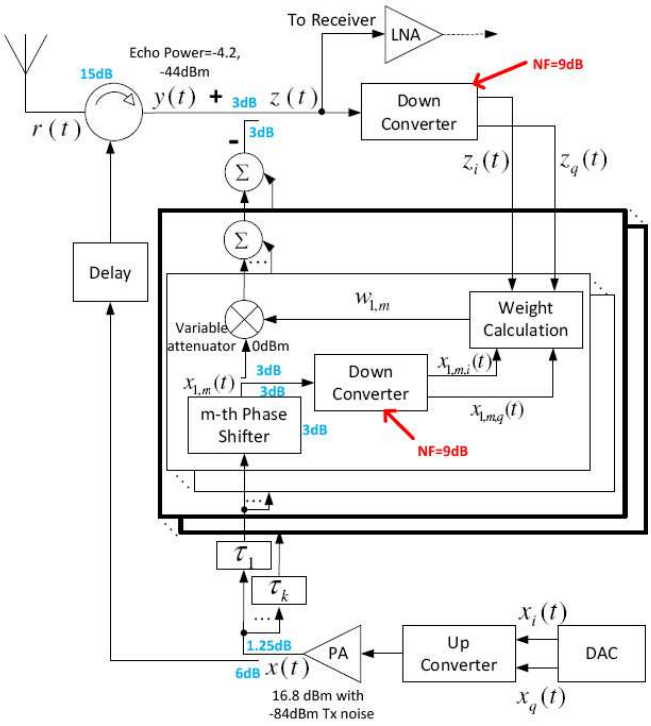

FIGURE 3.4: Full duplex configuration used in [12].

A fully analog cancellation technique is proposed in [12], as shown in Fig. 3.4. In this method, an initial isolation of 15 dB is obtained by using a circulator. Then, adaptive analog cancellation is employed to provide the rest of the required isolation. Similar to [11], a multi-tap configuration with different delays is used to create a copy of the self-interference signal. The level of achieved cancellation depends on the number of taps and the delay differences between them, regardless of the frequency. Once again, a high resolution RF phase adjuster is required.

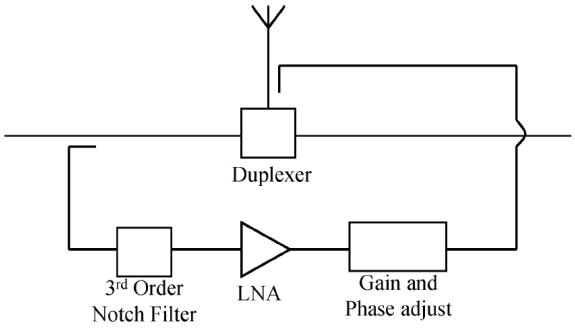

FIGURE 3.5: System topology for the adaptive duplexer presented by OSullivan [15].

3.2 Self-Interference Cancellation for Frequency Division Duplexing

FDD systems occupy two different spectra, for transmission and reception. Several methods have been proposed to cancel Tx leakage in the Rx path. Most of the techniques are not integrated solutions and use different technologies for implementation of the whole system. Therefore, it is currently not feasible to integrate the system on one single chip. McGeenhan et al. in [14] present an adaptive active cancellation technique, which cancels the Tx leakage in the Rx path by sampling the Tx signal and adjusting the gain and the phase of the sampled signal. The adjusted signal is then subtracted from the Rx signal. However achievable isolation between Tx and Rx has not been reported, in addition, cancellation of the Tx noise falling in the Rx band has not been considered. In some cases the Tx noise can mask the received signal entirely.

Tx noise cancellation has been discussed in [16] and [17]. Cancellation of Tx noise is possible by using a noise cancellation loop (feedforward method) in the Tx path or by employing different filters (Rx-BPF or Tx-BPF), such as found in a traditional duplexing filter. Whereas this method is not adaptive, to make it feasible for multi-band

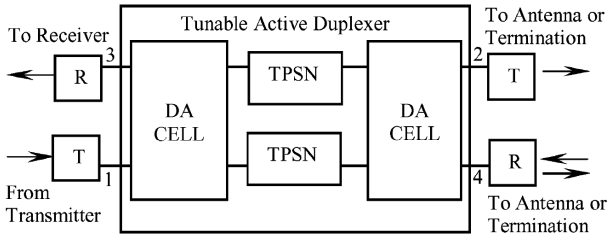

FIGURE 3.6: Tx/Rx module schematic [20].

applications, multiple switched filters are required, as is common in today's cellphones. The proposed configuration can be changed to an adaptive structure. In [18], cancellation is performed by using an auxiliary Tx, which can not be a cost-efficient solution, and does nothing to reduce the Tx noise falling in the Rx band.

The feedforward technique has been employed again by OSullivan et al. in [15] to improve the performance of a SAW duplexer by decreasing the noise levels in the received band. The system topology is shown in Fig. 3.5. The isolation enhancement was about 20dB over a 2MHz bandwidth. They used barium strontium titanate (BST) to implement the required phase shifter, which is an expensive technology and not compatible with CMOS [19].

An electronically tunable active duplexer has been presented in [20]. The block diagram of the proposed technique, which is based on the bi-directional distributed amplifier architecture [21], is shown in Fig. 3.6 as a Tx/Rx module. The module can be implemented as a monolithic microwave integrated circuit (MMIC). The only problem with MMIC is cost.

A frequency agile RF feedforward noise cancellation system (FFCS) was developed and presented in [22] by Roussel et al. As discussed earlier, feedforward cancellation is a viable solution to realize an adaptive duplexer [23], [24]. The behavior of FFCS

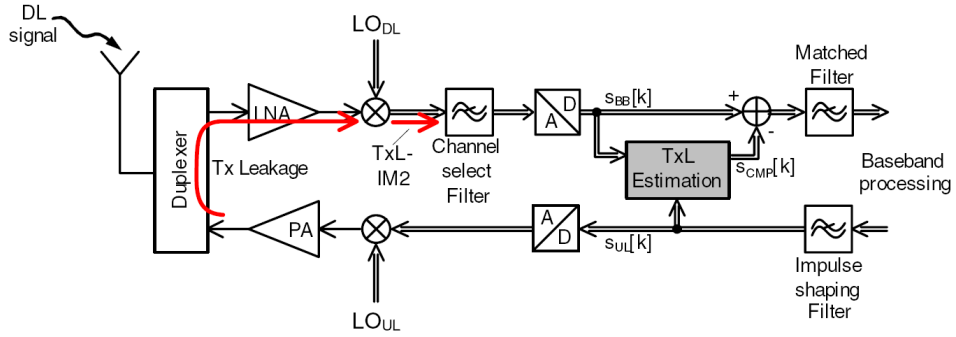

FIGURE 3.7: Block diagram of a FDD transceiver in a terminal, employing the direct conversion principle and compensating the Tx Leakage impact [25].

is as a tunable notch filter which is located at the output of the power amplifier (PA). Achieved isolation was 50dB over a bandwidth of 4.5MHz. Implementation of this architecture was based on off-the-shelf components that operate in the 800MHz CDMA (code division multiple access) band.

Another research study has been performed by Frotzscher et al. [25], which used a stochastic gradient least mean square (LMS) algorithm for further cancellation of Tx leakage in the digital domain. A block diagram of this architecture is shown in Fig. 3.7. This technique is for enhancement of duplexer isolation and it is not aimed to replace the fixed frequency duplexer with a multi-band and multi-mode duplexer.

The most relevant work to the aim of this research, which has been presented by Aparin et al. [26], is an analog integrated LMS adaptive filter. The cancellation process is applied after the low noise amplifier, as shown in Fig. 3.8. However, this structure is also for improving the duplexer performance and does not eliminate the need for a duplexer. The main advantages of this work are the reduced area and eventually cost of the CDMA Rx, and the low Rx gain degradation.

Kannangara et al. [3] [2] [27] proposes a new adaptive duplexer architecture, which

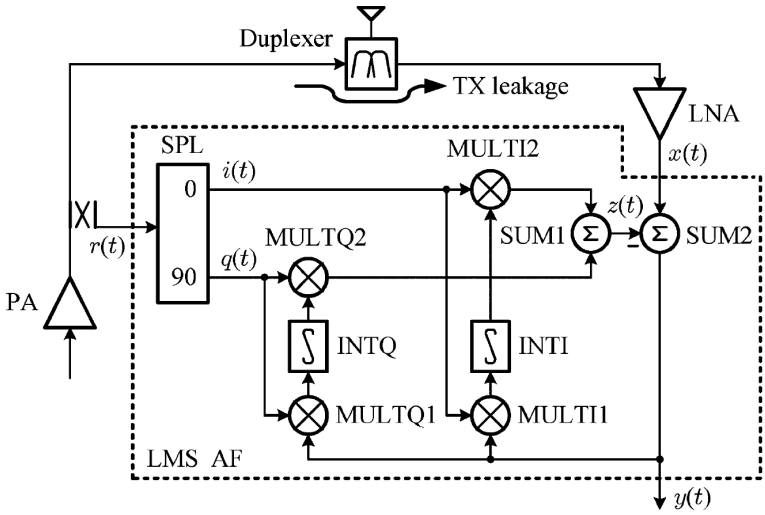

FIGURE 3.8: LMS adaptive filter architecture used in [26].

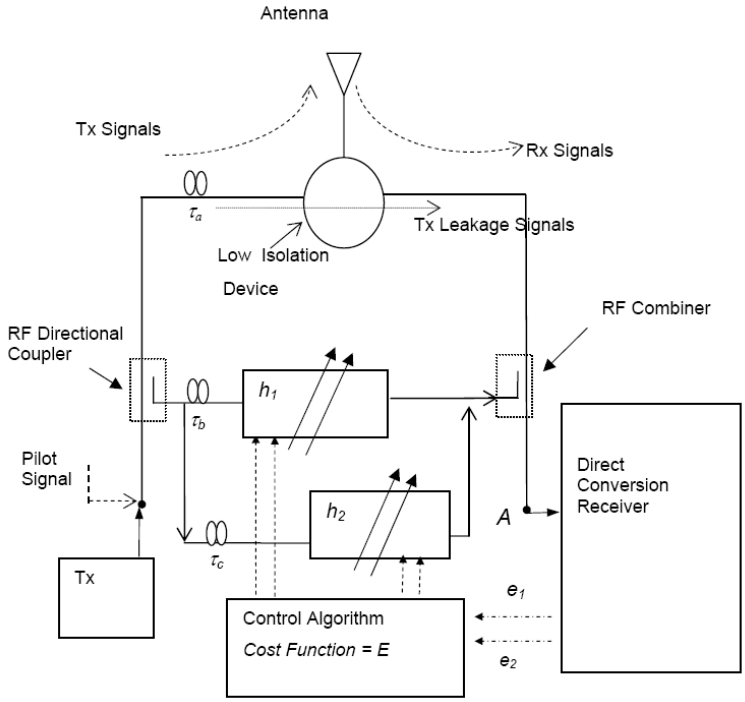

FIGURE 3.9: Double loop cancellation configuration presented by Kannangara [3].

is based on a two step isolation procedures. Initial isolation is achieved by a low isolation passive device such as wide-band circulator which gives about 20 dB isolation. Directional couplers, low selectivity stripe-line filters, and separate antennas are other alternatives for the circulator that are not of interest due to the fact that they are not compact devices. The low isolation implies significant Tx leakage and noise in the Rx

path, so further isolation is still necessary. An active double-loop cancellation technique is employed to obtain the required isolation by creating one null at the Tx frequency (to reduce the Tx leakage signal), and another null at the Rx frequency (to reduce the noise).

The system configuration is shown in Fig. 3.9. the gain/phase cancellation coefficients, h_1 and h_2 are adjusted by a DSP control algorithem, which reduces a cost function:

$$E = e_1 + Ke_2 \tag{3.1}$$

where e_1 is a measure of the residue transmit signal, and e_2 is a measure of the transmit noise falling in the receive band. The constant K controls the balance between the residual signals, e_1 and e_2. This technique provides 66 dB total isolation between the Tx signal and the Rx signal and 37dB total Tx noise cancellation at the Rx band; enough for most application.

The proposed solution for this project is the combination of previous works. Kannangaras [3] proposed architecture is the most suitable cancellation technique, which can be integrated using circuit design techniques presented by Aparin [26]. The major research goals are implementation of the delay lines and gain/phase adjusters with the required dynamic range and fidelity.

3.3 Summary

Adaptive duplexing applications, such as division free duplexing and frequency division duplexing, are discussed in this chapter. Both applications require high resolution

gain/phase adjuster elements in the RF cancellation unit.

The frequency division duplexing application is the focus of this research. The next chapter discusses the requirements of the gain/phase control elements for this application.

Chapter 4

Cancelling Requirements for Adaptive Duplexing

Implementing tunable RF duplexing filters with an ability to cover the required frequency range in LTE is almost impossible. Therefore, multiple switched duplexing filters are required to provide isolation between the receiver and the transmitter in the FDD multi-band radio implementations. Adaptive duplexing has been proposed to address this problem, as discussed in Chapter 1. This method eliminates the need for multiple switched duplexers.

In this chapter, an overview of the adaptive duplexing is provided in Section 4.1. The design requirements for implementing the gain/phase adjuster circuits are discussed in Section 4.2, and finally a summary is given in Section 4.3.

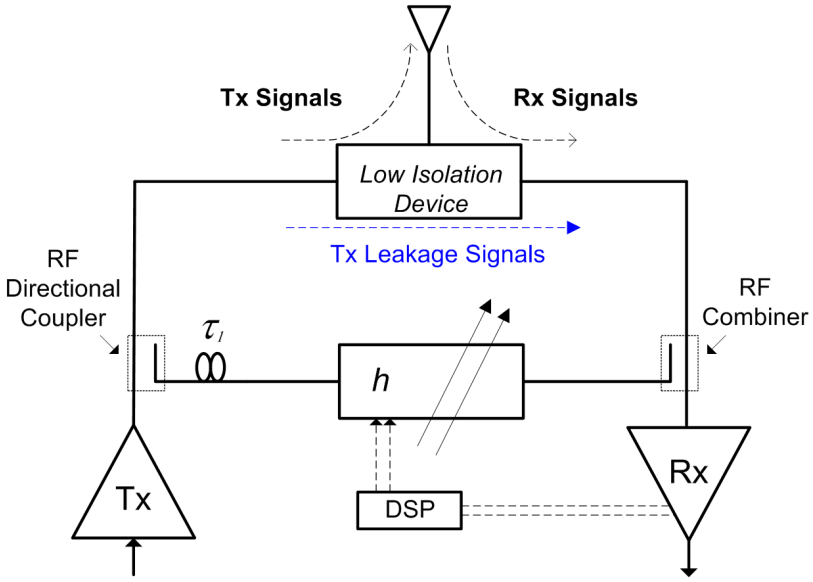

FIGURE 4.1: Adaptive duplexer architecture.

4.1 Adaptive Duplexer Architecture

The architecture of the adaptive duplexer is shown in Fig. 4.1. The isolation is a two step procedure; a low isolation device provides initial isolation, which is further improved by a cancellation loop. The feed-forward path of the cancellation loop consists of time delays and adjustable gain and phase devices. A sample of the transmitted signal can then be appropriately scaled to cancel the residue leakage signal from the low isolation device. A DSP (Digital Signal Processing) algorithm controls the gain and phase adjusters to minimize the residue leakage signal as monitored by the receiver circuitry. The design requirements of the gain and phase adjuster block are discussed in the next section.

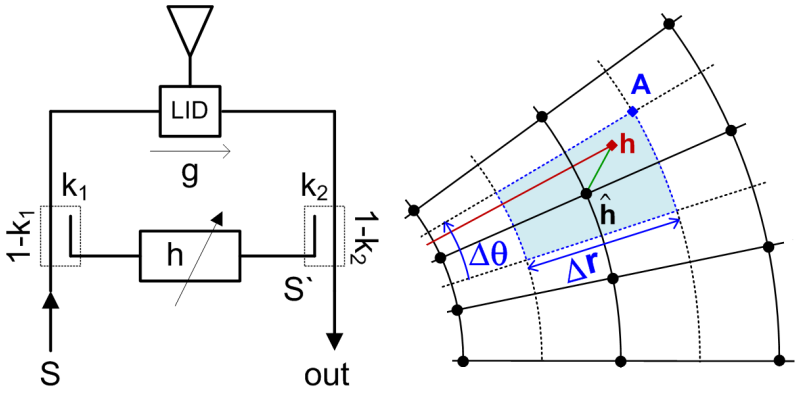

FIGURE 4.2: Simplified configuration of the adaptive duplexer architecture.

4.2 Design Requirements

4.2.1 Resolution

Duplexing filters in handsets typically provide 55 dB of isolation. If an initial isolation of 20-30 dB can be achieved by a low isolation device (using for example devices such as circulators, directional couplers, filters and dual antennas), then the cancellation loop is required to provide an additional isolation of about 25-35 dB to stop the Tx signal from desensitizing the receiver circuit. The requirements for the gain and phase adjuster can be calculated considering Fig. 4.2, which shows the simplified configuration of the adaptive duplexing diagram along with the representation of the signal in the polar coordinates with the nearest quantisation point marked as a black dot.

It is assumed that delays through the main signal path and the cancellation loop are identical. To achieve an ideal cancellation it is required to have :

$$S\,g - S' = 0, \tag{4.1}$$

while S is the transmitter signal, g is the gain through the main signal path (including the low isolation device and power losses through the couplers of $(1 - k_1)$ and $(1 - k_2)$ respectively), and S' is the signal through the cancellation loop. The RF coupler and combiner have coupling coefficient of k_1 and k_2, respectively, while h is the vector gain. Then:

$$S' = k_1\, k_2\, h\, S. \tag{4.2}$$

Considering Eq. 4.1 and Eq. 4.2 results in $g = k_1\, k_2\, h$ for ideal cancellation. But in practice, there is an error signal due to the quantisation of the vector adjuster, $\hat{h}$, where$\hat{}$ represents the quantised quantity. The error signal power is:

$$e^2 = |S\ (g - k_1\, k_2\, \hat{h})|^{\,2}. \tag{4.3}$$

Letting $\hat{h} = h - dh$, we can re-witre e^2 as:

$$e^2 = |S\ (k_1\, k_2\, dh)|^{\,2}, \tag{4.4}$$

from which the *additional* isolation, I, provided by the cancelling loop is given by

$$I^{\,-1} = \frac{e^2}{|g\, S|^2} = |\frac{dh}{h}|^{\,2} \tag{4.5}$$

Since $h = r\, e^{j\,\theta}$, and $\hat{h} = \hat{r}\, e^{j\,\hat{\theta}}$ then

$$dh^2 = (r - \hat{r})^2 + r^2\, (\theta - \hat{\theta})^2 \tag{4.6}$$

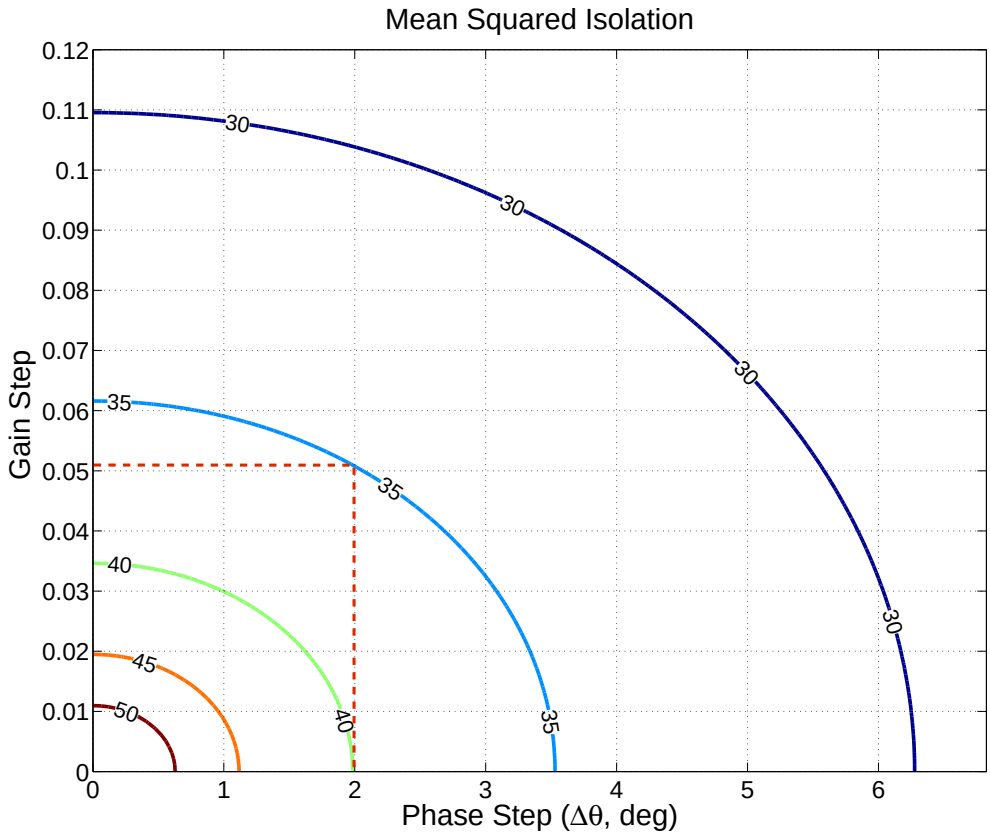

FIGURE 4.3: Isolation(dB) versus gain and phase step size for MSE requirements.

We can calculate the mean squared error of dh,

$$\begin{aligned}
\overline{dh}^2 &= \int_{\Delta\theta}\int_{\Delta r} \frac{((r-\hat{r})^2 + r^2(\theta-\hat{\theta})^2)dr(rd\theta)}{\Delta r(r\Delta\theta)} \\
&= \frac{1}{\Delta r\Delta\theta}\left(\int_{\Delta\theta}\int_{\Delta r}(r-\hat{r})^2 drd\theta + \int_{\Delta\theta}\int_{\Delta r} r^2(\theta-\hat{\theta})^2 drd\theta\right) \\
&= \frac{1}{12}\left(\hat{r}^2\ \Delta\theta^2\ +\ \frac{1}{12}\Delta r^2\right)
\end{aligned} \tag{4.7}$$

Then:

$$\overline{I}^{-1} = |\frac{\overline{dh}}{\hat{h}}|^2 = \frac{1}{12}\left(\Delta\theta^2\ +\ \frac{\Delta r^2}{\hat{r}^2}\right) \tag{4.8}$$

Where $\Delta r/\hat{r}$ and $\Delta\theta$ are the gain and phase step sizes, respectively. Using Eq. 4.8, the achievable isolation levels with the respective phase and gain steps can be presented as

shown in Fig. 4.3.

The above isolation measure is an averaged quantity. Therefore some individual measures can have poor isolation and cause significant interference to the received signal. Provided these interference bursts are averaged with the periods of low interference then the mean isolation (Eq. 4.8) is the appropriate measure. The channel coding schemes of modern wireless systems do just this [28, 29]. Bits having large error contributions are corrected by bits with low error contributions. We conclude therefore that provided there are a number of coefficient updates within the period of one code-word and the updates are sufficiently busy then the average measure is appropriate. From Fig. 4.3, to achieve 35 dB isolation, a $\Delta r/\hat{r}$ of 0.051 and $\Delta\theta$ of 2° are required, which means at least 5-bit and 8-bit resolutions for the gain and the phase adjusters, respectively.

In some circumstances, however, the above conditions might not apply. For example, when the coefficient updates are slow or the coefficients values are very stable. Such a scenario might be found in a base station environment, where antenna impedances do not vary. In these circumstances a worst case analysis might be more appropriate, since the maximum error condition could occur over a longer time period.

To calculate the maximum error we consider the case where the desired coefficient value lies on the decision boundary of both phase and magnitude (marked A in Fig. 4.2). The error in the quantized signal is

$$dh^2_{max} = (\hat{r}\,\frac{\Delta\theta}{2})^2 + (\frac{\Delta r}{2})^2\,, \tag{4.9}$$

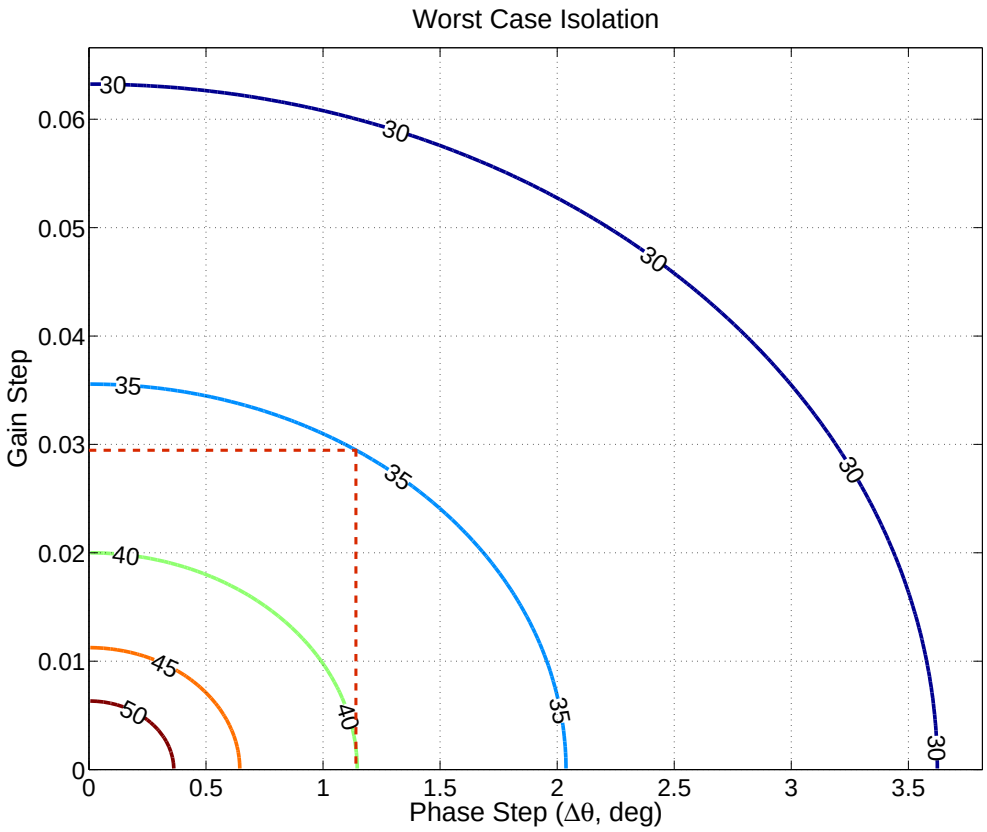

FIGURE 4.4: Isolation(dB) versus gain and phase step size for worst case requirements.

then

$$I^{-1} = \frac{1}{4}\left(\Delta\theta^2 + (\frac{\Delta r}{\hat{r}})^2\right). \tag{4.10}$$

The obtained isolation regarding the gain and phase step sizes are plotted in Fig. 4.4 using Eq. 4.10. For example, to achieve 35 dB isolation, a $\Delta r/\hat{r}$ of 0.029 and $\Delta\theta$ of 1.15° are required, which implies that at least 6-bit and 9-bit resolutions for the gain and phase adjuster components, respectively. It should be noted that the control loops require fine phase adjustment (small step size), but have no requirement for absolute phase accuracy.

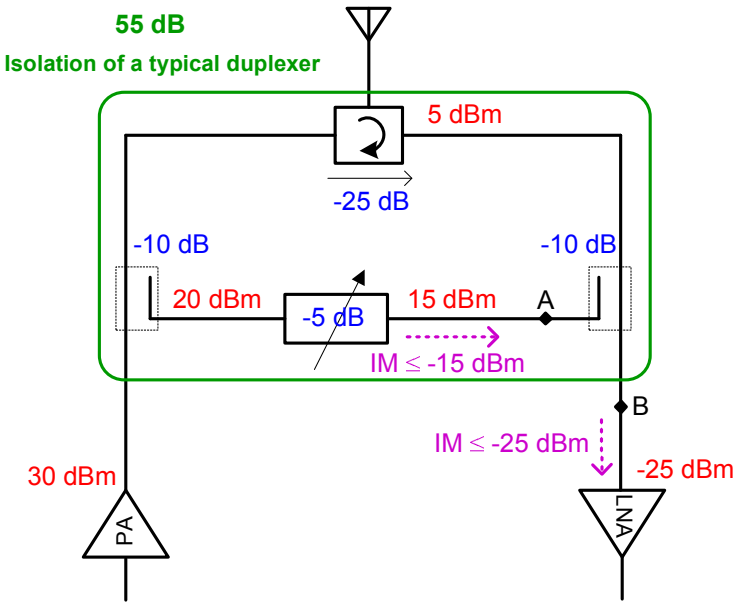

FIGURE 4.5: Block diagram of adaptive duplexer with signal levels.

4.2.2 Signal Handling

There are two criteria for large signal handling of the cancelling loop. Firstly, any intermodulation product should not be larger than the residual signal after the canceller (to stop overloading the receiver). Secondly, the higher order intermodulation products that have the potential of falling in the Rx band (with 190 MHz separation) should be below the noise floor.

To investigate this requirement, we consider the block diagram of the adaptive duplexer shown in Fig. 4.5. The aim is to achieve similar performance as a typical duplexer with 55 dB isolation. A circulator can provide 25 dB of isolation. Therefore, the transmitter's leakage in the receive path is equal to 5 dBm (=30 dBm - 25 dB) with a transmitted signal power of 30 dBm. The transmitted signal is coupled to the cancellation loop through a 10 dB coupler. The gain/phase adjuster has an insertion loss of 5 dB. The signal is then fed to the receive path using another 10 dB coupler.

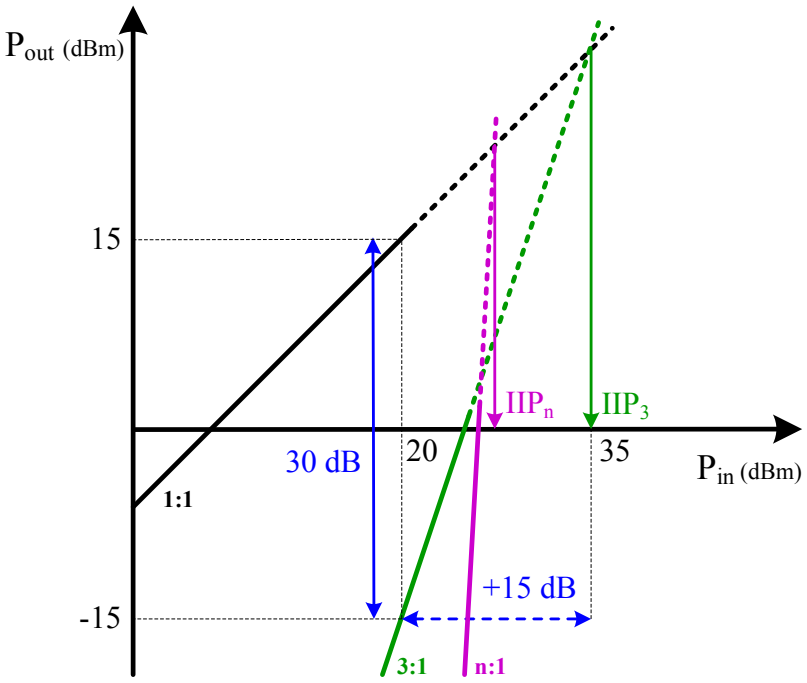

FIGURE 4.6: IP_3 requirements of the canceller.

To obtain the performance of a 55 dB duplexer, any IM products at the LNA (position B, Fig. 4.5) should be less than -25 dBm (= 30 -55). This implies that the IM products of the cancellation loop (position A, Fig. 4.5) should be less than -15 dBm (= -25 + 10). The signal level at the output of the canceller (position A, Fig. 4.5) is 15 dBm (= 30 - 10 - 5). We consider this measure to calculate the IP_3 requirement of the canceller using the plot shown in Fig. 4.6. The necessary separation between the signal and the third intermodulation product is 30 dB (= 15 -(-15)). This means an IIP_3 of at least 35 dBm is needed for the canceller.

The higher intermodulation products, which might fall into the Rx band, are required to be below the noise floor. The thermal noise in dBm can be calculated as:

$$P_{Noise\,(dBm)} = 10\,log_{10}(\frac{k_B T \Delta f}{1\,mW}), \tag{4.11}$$

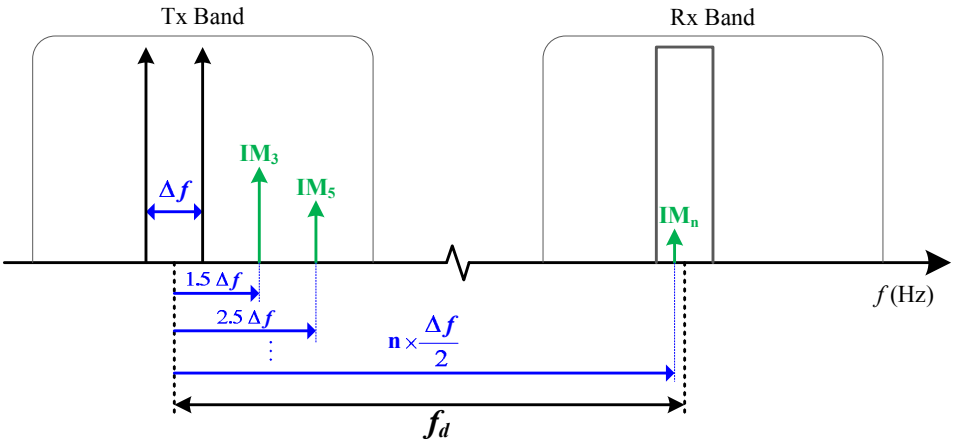

FIGURE 4.7: *IM* requirements of the canceller.

where, k_B is the *Boltzmann's constant* in joules per kelvin, T is the temperature in kelvin, and Δf is the channel bandwidth. In LTE, the transmission bandwidth is 18 MHz [7], then the thermal noise can be calculated (using Eq. 4.11) as -101.5 dBm. This implies that the intermodulation products of the canceller (position A, Fig. 4.5), which fall into the Rx band, must be below -91.5 dBm (= -101.5 + 10).

We use two-tones to model the worst case LTE scenario, with two active resource blocks (RBs) at each end of the channel. First, we calculate the order of the IM product falling into the Rx band for LTE Bands 1 and 2, with the duplexing offsets of $f_{d1} = 190$ MHz and $f_{d2} = 80$ MHz, respectively (Fig. 4.7).

$$IM_{order} = n = 2 \times \frac{f_d}{\Delta f} \tag{4.12}$$

Therefore, IM_{21} and IM_9 will fall into the Rx band for LTE Band 1 and 2, respectively. We use the plot shown in Fig. 4.6 to calculate IP_{21} and IP_9 by considering the required isolation between the fundamental output and the nth order IM product, which is 106.5 dB (= 15 - (-101.5)). This gives an IIP_{21} of 25.5 dBm and IIP_9 of 33.5 dBm.

Higher order IP data for modelling purposes are not generally available from device manufacturers. Hence, testing the prototype is the only means of ascertaining the IM interferences falling into the RX band.

4.3 Summary

The adaptive duplexing principles are discussed in this chapter. The cancelling loop requires precise gain and phase adjustments. We show theoretically that a phase resolution of better than 1.02°, or approximately 9-bit, is needed for 32 dB loop isolation using a worst-case assumption. This drops to 7-bit resolution if the gain-phase updates are sufficiently busy to allow a MSE assumption.. The large signal handling is also a necessity for the cancellation loop, with a minimum IIP_3 of 35 dBm.

As stated earlier, the phase shifter device is the topic of this thesis. Thus, a literature review on the implementation of phase shifter is provided in the next chapter.

Chapter 5

Literature Review on Phase Shifters

Phase shifters are one of the key building blocks in RF signal processing systems. They are used in smart antennas for beam steering, and amplifier linearisation schemes where they form part of a gain/phase adjuster in a distortion cancelling loop. There are several design parameters to be considered, such as phase control range, phase resolution, insertion loss, noise, bandwidth, large signal handling, and chip size. This makes the design and optimisation of integrated phase shifters a challenging task. Active and passive phase shifters are widely used for different applications. Active phase shifters provide gain, while introducing more non-linearity to the system [30–35]. Passive approaches can have better large signal performance, but exhibit insertion loss [36, 37]. Varactor devices are often used when precise phase shifts are required, but varactors generate distortion when the signal levels are high [38, 39]. To overcome the large signal handling problem, switched phase shifters have been developed [40–44]. These circuits switch passive elements into and out of the phase shifting circuit. To date the highest reported resolution is 6 bits (5.625°), which is adequate for beam forming applications. However,

nulling applications such as antenna null steering and interference cancellation often require greater resolution. In adaptive duplexing, the phase adjusting component of the gain-phase adjuster device requires much higher fidelity to obtain cancellation values over 40 dB, as discussed in Chapter 4. In addition to the high resolution requirements, large signal handling of the elements is a necessity for this application.

In this chapter, a review on active phase shifters is provided in Section 5.1. Passive phase shifters are discussed in Section 5.2 and a summary is given in Section 5.3.

5.1 Active Phase Shifters

Active phase shifters are suitable for applications which deal with small signals. In this section, a few active phase shifters are discussed.

5.1.1 Active Vector Modulator

Vector modulators are one of the most common active phase shifters. They are widely used in applications such as adaptive antenna, beamforming, and phased array systems [45–50], which do not require high resolution and high dynamic range.

A vector modulator configuration is shown in Fig. 5.1. This structure provides 90° phase shift. Initially, the input signal is divided by two signals with 0° and 90° phase offset. A variable gain amplifier (VGA) in each path then scales the amplitude, and finally a combiner adds the signals to achieve the desired phase shift. The phase range between 0° and 90° can be obtained by scaling the signals appropriately. The relation

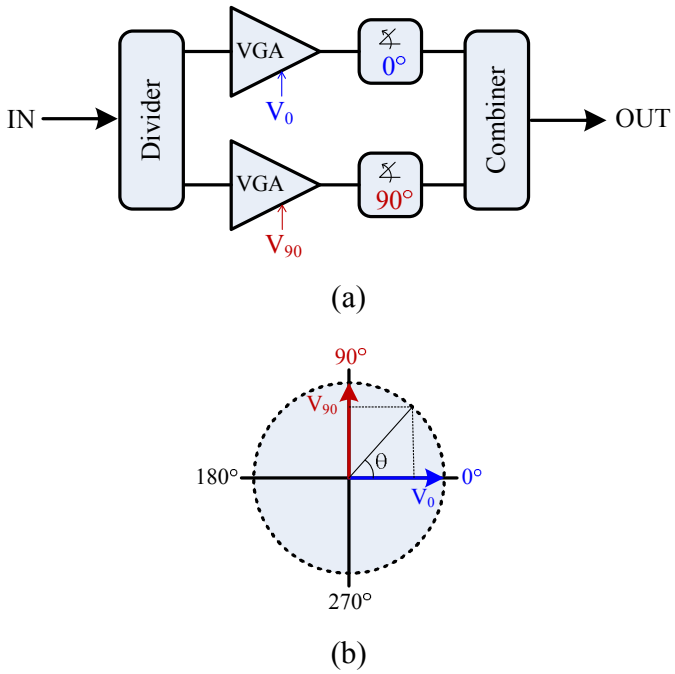

FIGURE 5.1: Vector modulator with two paths [51].

between the obtained phase, θ, and the signal amplitudes can be calculated from Fig. 5.1 as:

$$\theta = tan^{-1}\left(\frac{V_0}{V_{90}}\right), \tag{5.1}$$

where V_0 and V_{90} are the amplitude of the signals with 0° and 90° phase offsets, respectively.

To cover 360° phase range more signal paths are required, this being typically four signal paths each with 90° phase offset. The configuration of such a system is shown in Fig. 5.2. To obtain the desired phase, only two of the paths are used at the same time, therefore, VGAs can be switched to the right paths (path selection in Fig. 5.2), resulting in a reduced number of VGAs to two [30, 31].

It is also possible to implement the full 360° range vector modulator phase shifter employing three paths, each with 120° phase offset. Fig. 5.3 shows the circuit schematic

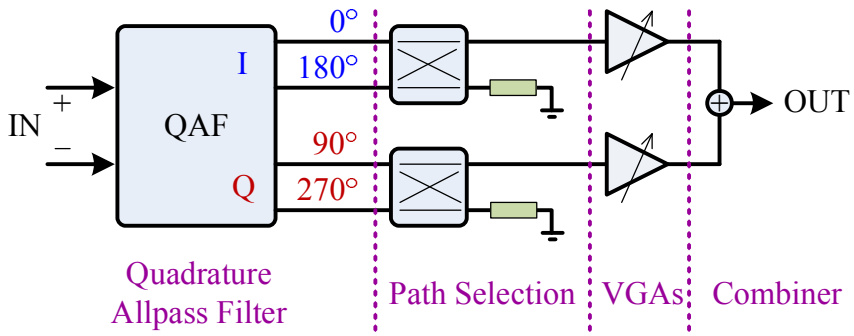

FIGURE 5.2: Vector modulator with four paths to cover 360° [30, 31].

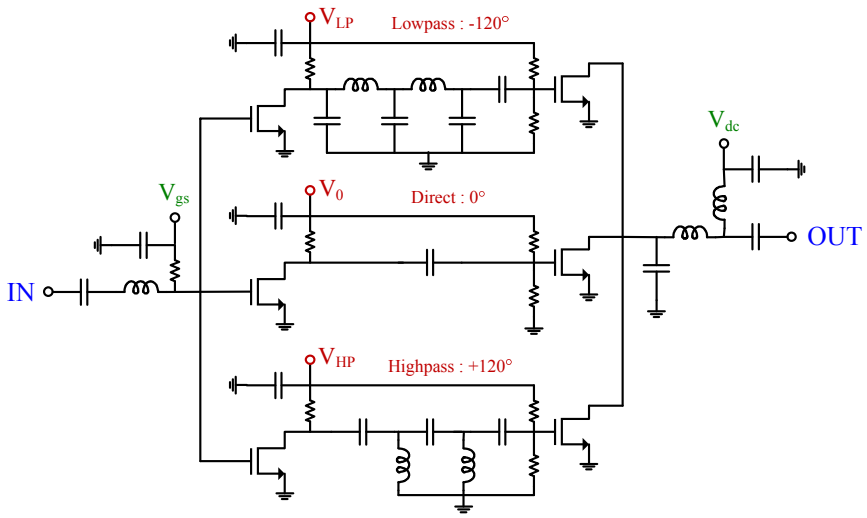

FIGURE 5.3: Vector modulator with three paths to cover 360° [32].

of the topology proposed in [32]. Three control voltages are required to achieve adjustable phase control. The number of control voltages can be reduced to one by combining the attenuators/amplifiers in each path, and therefore combining the control voltages [33].

Vector modulators, and active phase shifters in general, can provide gain and also some gain adjustments. As can be seen, their structure is simple and straight forward without requiring any special components. However, using active devices introduces distortion and non-linearity, which degrades the large signal performance.

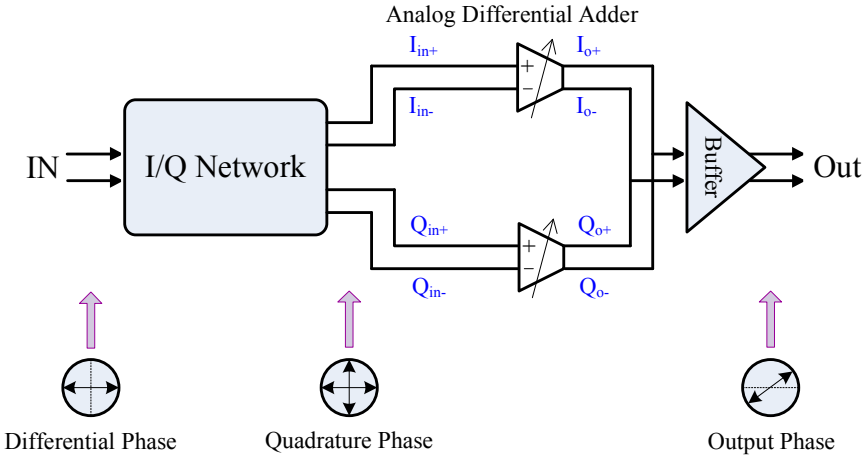

FIGURE 5.4: Active vector sum reported in [35].

5.1.2 Active Vector Sum

A differential active vector-sum phase shifter is reported in [35], achieving a wide bandwidth and low RMS phase error. The block diagram of the phase shifter is shown in Fig. 5.4. An I/Q network, consisting of three all pass filters, generates quadrature phased I- and Q-vector signals [34]. An analog adder circuitry, consisting of two Gilbert-cell type VGAs, then interpolates the signals to obtain the full 360° phase coverage. The chip is fabricated using 0.18 μm CMOS technology, which occupies an area of 0.87×0.75 mm^2. The measured RMS phase error over the frequency band of 2.3 - 4.8 GHz is less than 1.4°. However, using the active components in the VGAs degrades the large signal performance of the phase shifter, with a reported P_{1dB} of 1.8 ±1.2 dBm.

5.2 Passive Phase Shifters

Passive phase shifters provide a better large signal performance, therefore they are a better choice for adaptive duplexing application. Different methods of implementing passive phase shifters are discussed in this section.

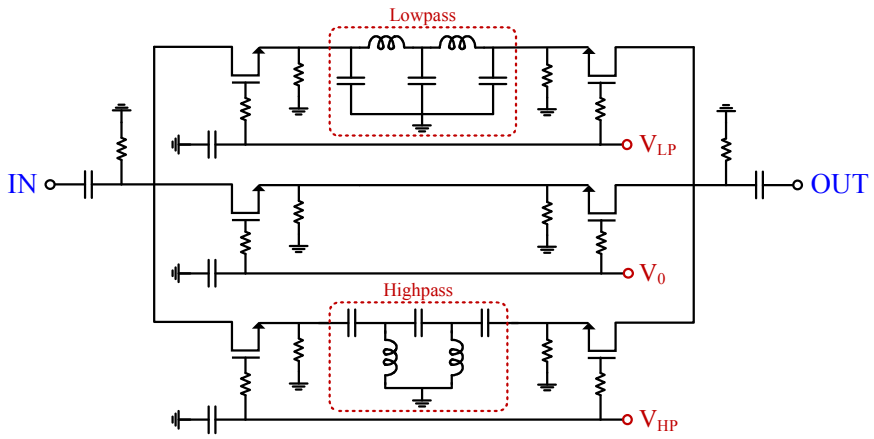

FIGURE 5.5: Passive vector modulator reported in [36].

5.2.1 Passive Vector Modulator

Vector modulators are generally active implementations, however, Ellinger et. al presented a passive vector modulator [36], implemented in the Triquint TQTRx GaAs MESFET process. The configuration is shown in Fig. 5.5. There are three control voltages, V_{LP}, V_{HP}, and V_0. By changing the control voltages within a range of 0 V to -3 V, the amplitude of the signal in each signal path changes, and therefore, a full 360° is achieved at 5.2 GHz. The measured insertion loss is 9 dB, with a P_{1dB} of 16.5 dBm.

5.2.2 Passive Vector Sum

A passive vector-sum based phase shifter is implemented in 0.18 μm 1P6M (1 Poly, 6 Metal) CMOS technology at K-band [37]. The circuit configuration is shown in Fig. 5.6. The main building block of the proposed structure is a directional coupler. First, a 3 dB directional coupler is used to divide the signal to two paths (I and Q). Then, in each path a 3 dB directional coupler with reflective loads are employed to realise the phase invertible variable attenuators (PIVA). The reflective loads are NMOS transistors with

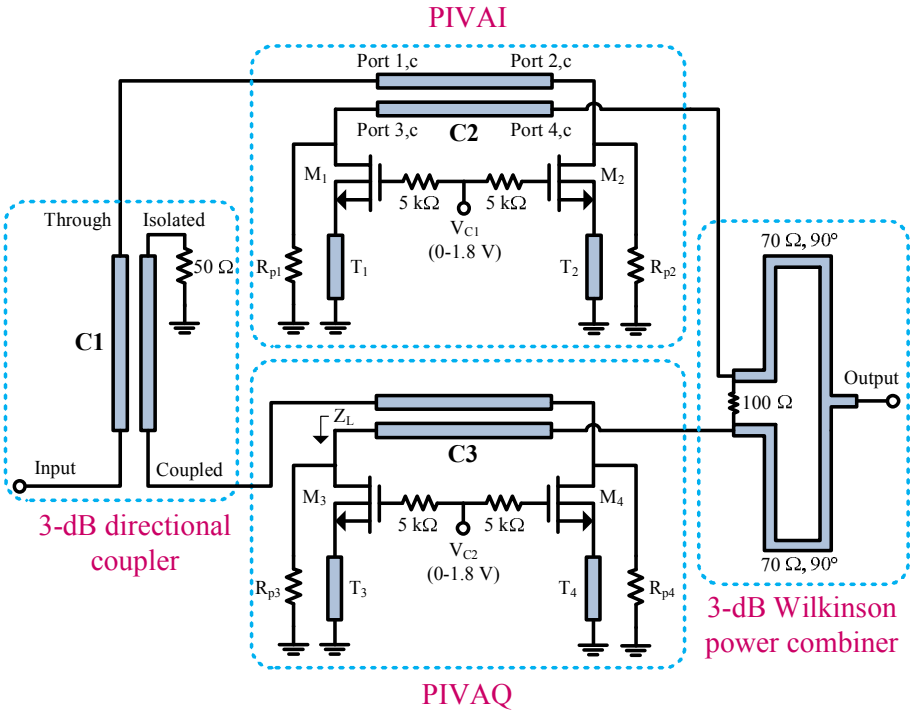

FIGURE 5.6: Passive vector sum reported in [37].

variable gate voltages. By changing the gate voltage, the drain-source impedance of the transistor changes. Therefore, the reflection coefficient, Γ, presented by Eq. 5.2 changes, resulting in a variable phase shift:

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{5.2}$$

where Z_0 is the coupler's impedance and Z_L is the impedance of the reflection load (impedance seen from the drain of the transistor). Two control voltages are required to adjust the gain/attenuation in the PIVAs, varying between 0 V and 1.8 V, which provide 292.5° of relative phase shift. The measured P_{1dB} and IIP_3 are 12 and 28 dBm, respectively, for the obtained relative phase shift. The device has a group-delay deviation of 6.3 ps at a frequency band of 22 - 26 GHz.

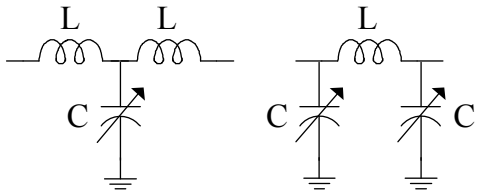

FIGURE 5.7: Building blocks of a varactor loaded transmission line.

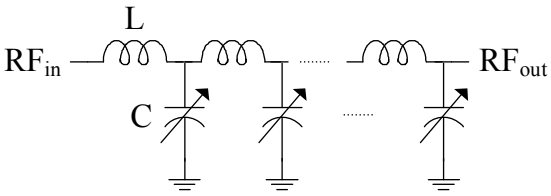

FIGURE 5.8: Varactor loaded transmission line.

5.2.3 Varactor Loaded Transmission Lines

Transmission lines with different lengths are widely used for phase shifting purposes. A lumped element equivalent of a transmission line with variable elements can be employed to obtain a variable phase shift. Low-pass or high-pass structures with T or Π configurations can be used as the main building blocks, as shown in Fig. 5.7. The variable capacitance can be easily achieved by employing varactors. However, to tune the inductance values active inductors are required, which consume high dc power, and introduce more non-linearity and complexity to the system [52]. Therefore, transmission line based phase shifters are mainly consisting of varactor loaded types with fixed inductors. Fig. 5.8 shows the circuit configuration of a varactor loaded transmission line. Multiple π sections are cascaded to increase the obtained phase shift.

Three Π sections are employed to achieve 90° phase shift (30°/section) at 4 - 6 GHz frequency band with an insertion loss of 1.2 ±0.5 dB [53]. To achieve 360° phase shift at this frequency band, twelve Π sections are required. However, the obtained phase shift per section can be degraded due to parasitics and process variations. Therefore,

to guarantee a 360° phase shift, usually a few extra sections are considered. On the other hand, by using more sections with less phase shift per section, the circuit can operate below the cut-off frequency and result in less insertion loss [38, 39]. Sixteen Π sections are used in [38] to achieve 360° phase shift. The device is implemented in 0.6 μm GaAs MESFET process, achieving 410° phase shift with 6 dB insertion loss at the center frequency of 5.5 GHz.

Varactor loaded transmission lines provide high fidelity consuming no dc power. However, the non-linear nature of the varactors limits the large signal performance of this type of phase shifter, with the highest P_{1dB} reported to be 12 dBm in [38]. Furthermore, at lower frequencies the large size is a major drawback.

5.2.4 Reflective Type

Fig. 5.9 shows the schematic of a reflective type phase shifter using a quadrature hybrid [54, 55]. The input signal is divided to two ports, which are terminated with variable reflective loads, i.e. purely reactive loads. The reflected signals from the reactive loads are phase shifted and combined at the output port. The total phase shift at the output port can be calculated as:

$$\theta = -\left(\frac{\pi}{2} + 2\,tan^{-1}\left(\frac{X}{Z_0}\right)\right), \tag{5.3}$$

where X is the reactance of the load and Z_0 is the characteristic impedance of the hybrid circuit.

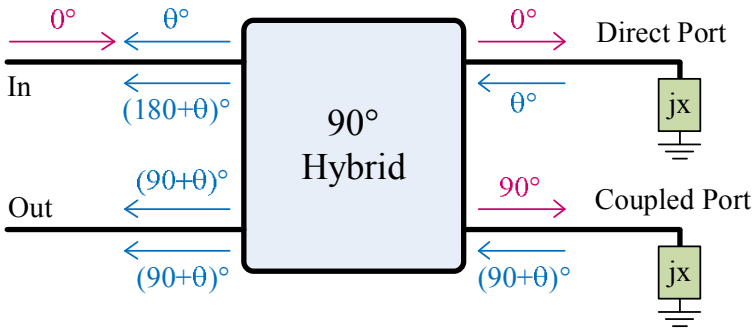

FIGURE 5.9: A reflective type phase shifter (RTPS) using quadrature hybrid.

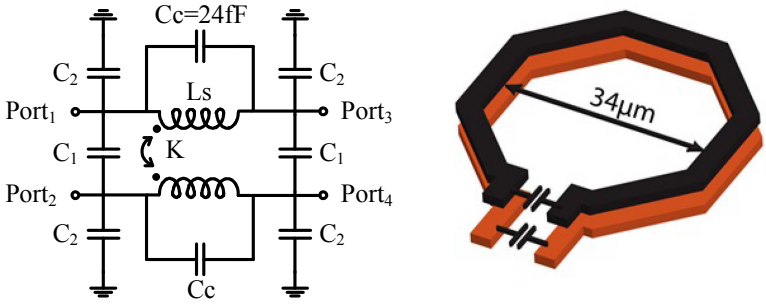

FIGURE 5.10: Balun-based quadrature hybrid employed in [54, 55].

Tabesh et. al presented two reflective type passive phase shifters in 65 nm CMOS process for phased array applications at 60 GHz [54]. In both circuits, a balun-based quadrature hybrid is used, which decreases the chip size significantly. The circuit configuration and also the conceptual layout of the balun-based circuit is shown in Fig. 5.10. The obtained phase shift from the quadrature topology is limited to the tunning range of the variable capacitor, typically ≈ 40° - 60°. Multiple hybrid circuits can be cascaded to achieve higher phase shift. Three stages are cascaded in [55] to achieve 180° phase shift (as shown in Fig. 5.11). The insertion loss and phase shift of the circuit is calculated as:

$$IL = n(2IL_{Hybrid} + \sqrt{\frac{1 + [(R_v - Z_0)C_v\omega]^2}{1 + [(R_v + Z_0)C_v\omega]^2}}) \tag{5.4}$$

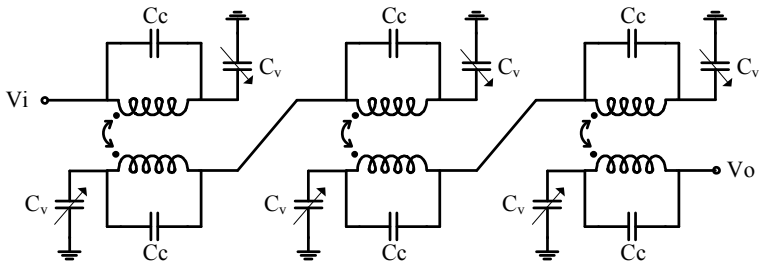

FIGURE 5.11: Cascaded RTPS [55].

$$\phi = n(-\frac{\pi}{2} - tan^{-1}(\frac{1}{(R_v - Z_0)C_v\omega}) + tan^{-1}(\frac{1}{(R_v + Z_0)C_v\omega})) \tag{5.5}$$

where n is the number of cascaded stages, and R_v is the loss of the varactor. The fabricated device has a very small area of 0.03 mm^2 and an insertion loss of 8.3 dB to cover only 180°.

5.2.5 Switched Networks

In switched networks based phase shifters, the signal is switched between two networks, where one network is the phase shifting circuit and the other one is the phase reference circuit. Therefore, a phase shift with minimum variation over a frequency range can be achieved. The traditional high-pass/low-pass (HP/LP) structures are usually used to implement the higher bits of 180° and 90°. To realise the lower bits of 45°, 22.5° and 11.25° switching between LP and BP (band-pass) networks are commonly employed. Using the same circuit to achieve smaller phase shift requires very large inductors and very small capacitors. However, this is not viable, as the large parasitics of a large inductance makes the realisation of the small capacitance impractical.

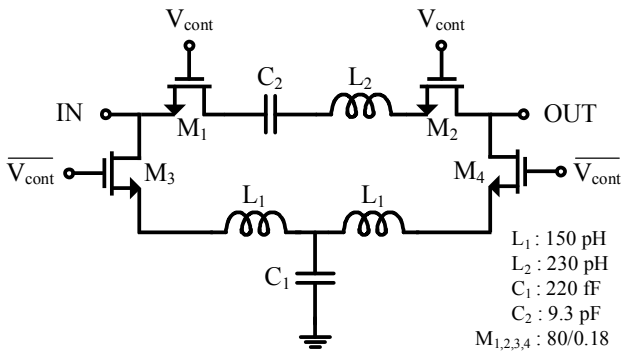

FIGURE 5.12: Circuit configuration to realise 5.625° phase shift [44].

The phase shifter reported in [44] is a 6-bit device in S-band, implemented in a standard CMOS process. They proposed a new configuration for realising the LSB (5.625°), as shown in Fig. 5.12. This circuit provides a small phase shift by switching between a BP and LP network. The component values are reasonable at the frequency band of interest. The 6-bit phase shifter is realised by cascading the switched networks in an order to minimise the insertion loss. However, the simulated insertion loss is still large (13 dB, which is normal for CMOS devices) and requires compensation. Therefore, an amplifier is employed, decreasing the overall insertion loss to 2.5±1.5 dB, even though this means degrading the large signal performance of the device (P_{1dB} of 12/2 dBm Tx/Rx).

To decrease the size of the switched networks in the lower frequency bands, i.e. C-, L-, and S-band, all-pass networks are employed. In [56], a new all pass network base phase shifting circuit is proposed, which is used to implement 90°, 45°, and 22.55° phase shift blocks, in order to maintain the small size. The LSB (11.25°) circuit is implemented using the matched embedded FET phase shifting circuit proposed in [57], where the parasitics of the switches become part of the phase shifting circuit. Two 5-bit phase shifters in S- and C-band are fabricated in 0.5 μm pHEMT technology with

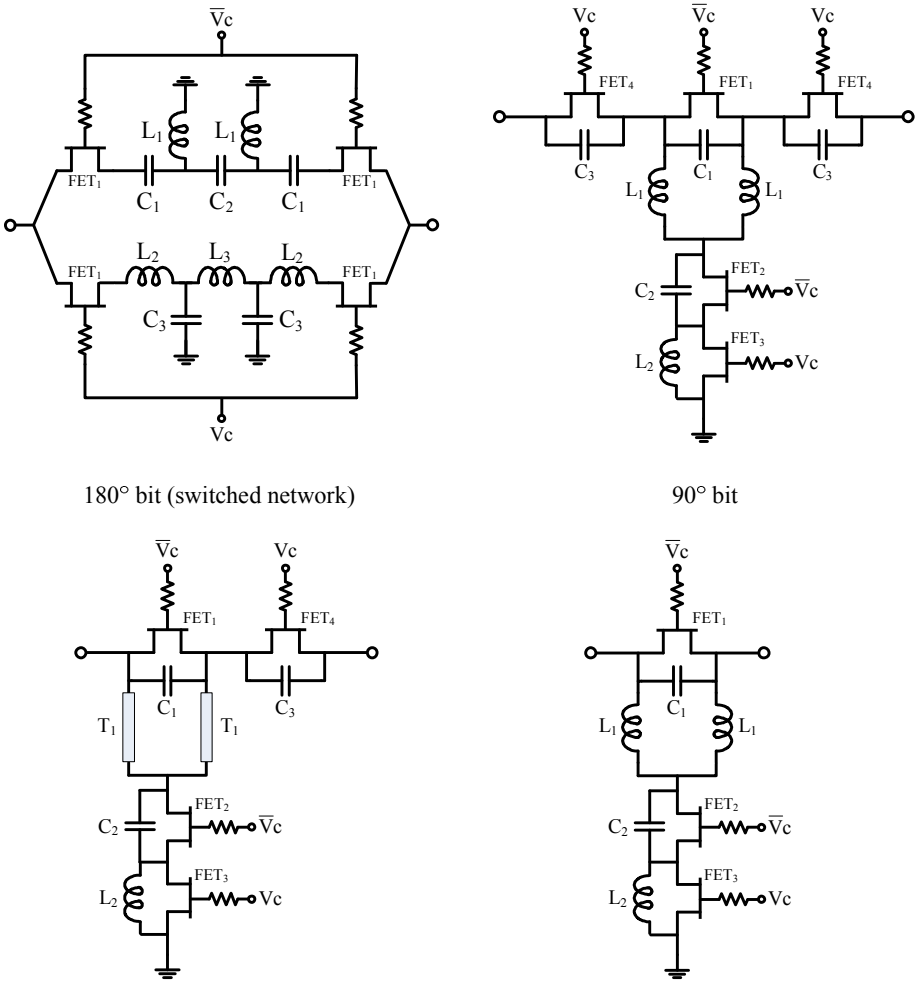

FIGURE 5.13: Circuit configuration for 4-bit L-band phase shifter [42].

high Q inductors. The S-band device occupies an area of 1.63 mm^2 and exhibits an insertion loss of 6.1±0.6 dB. The chip size for the C-band phase shifter is 1.37 mm^2, with a maximum insertion loss of 6.5 dB.

In [42], two 4-bit L- and S-band phase shifters in 0.4 μm MSAG MESFET technology are reported. They employed a commonly used HP/LP topology to implement the 180 ° phase shift, and modified embedded FET configurations for realising the 90°, 45°, and 22.55° phase shift circuits. The circuit is shown in Fig. 5.13. Both phase shifters occupy an area of 2.6 mm^2, with a maximum insertion loss of 4.7 dB for S-band and 4.2

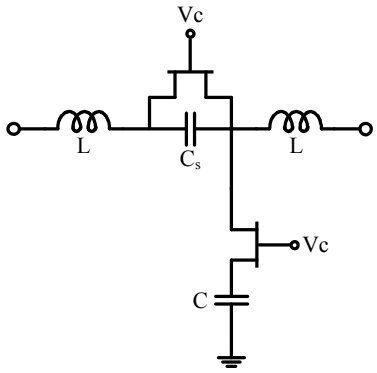

FIGURE 5.14: Circuit configuration to implement 22.5° and 11.25° [43].

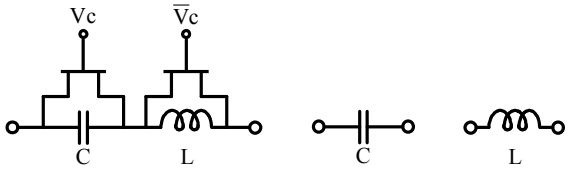

FIGURE 5.15: Circuit configuration to implement 5.625° [43].

dB for L-band devices.

A small size L-band 6-bit phase shifter is implemented in 0.5 μm GaAs pHEMT [43]. The circuit configuration for each bit is considered based on an optimum topology to achieve low insertion loss and minimum phase error. A HP/LP circuit is designed to achieve 180° phase shift at the frequency band of interest (L-band). Modified all-pass network structures used in [56] and [42] are employed to obtain the 45° and 90° phase shifts. A circuit shown in Fig. 5.14 is used to implement 22.5° and 11.25°. The phase shifting state is a bandpass circuit, and the phase reference state is a low-pass network. This topology requires less switches on the signal path, which results in a smaller insertion loss. The LSB (5.625°) circuit is simply realised by switching between a capacitive reactance and an inductive reactance (as shown in Fig. 5.15). This circuit benefits from a small size and small insertion loss. The measured insertion loss is less than 4.6 dB for the frequency band of 1.4 - 2.4 GHz.

5.3 Summary

By studying the different methods of implementing phase shifters and their performance, it can be concluded that a switched passive approach is the best candidate for circuit realisation. Most of the passive approaches, which have better large signal performance, are implemented in GaAs pHEMT technology, which is a non silicon technology and also expensive. An SiGe process is silicon based, however, has poor passive components with poor isolation. For technology choice, it is desirable to employ a silicon based process for compatibility with the other Tx/Rx circuits. In addition, high quality factor components are required to achieve better performance. An SOS process with an insulating substrate is a good choice; silicon based with good passive components.

The next chapter discusses the history of developing an SOS process and the features of Peregrine UltraCMOS® process.

Chapter 6

Silicon-On-Sapphire Process

Silicon-on-Sapphire (SOS) is a type of Silicon-on-Insulator (SOI) technology for integrated circuit manufacturing. Bulk CMOS (Complementary Metal-Oxide-Semiconductor) is the traditional circuit manufacturing technology, where the circuit is fabricated on the silicon surface. SOS technology uses a thin layer of silicon on sapphire as the substrate. The insulating substrate helps to reduce the parasitic capacitance which results in high speed, improved linearity, and low power consumption. These features of SOS circuits makes them a good candidate for radio frequency (RF) circuit design [58].

The increasing demand for single chip wireless transceivers is resulting in intensive research concentrated on CMOS technology. Low power consumption, simple packaging, and low overall cost of the system can be obtained using this technology. However, several additional advantages of SOS process makes it more attractive for RF applications as compared to bulk CMOS. SOS also gains advantage from the process refinements which have been developed for bulk silicon. This includes high manufacturing

yields, low power operation, and high levels of integration [59].

In this chapter, a brief history of SOS fabrication is presented in Section 6.1. Peregrine UltraCMOS process features are provided in Section 6.2, and a summary is included in Section 6.3.

6.1 SOS Fabrication Process

The insulating material used in SOS is synthetic sapphire (Al_3O_2). The sapphire wafers are large crystals which are grown in controlled condition to obtain a very high degree of purity. Then they are cut an angle of approximately 60°. There are two methods to make the SOS wafers.

First method, called Ultra-Thin Silicon-on-Sapphire (UTSi®), is to epitaxially grow a thin layer of silicon on sapphire substrate. For this method, the sapphire wafers are required to be finished carefully after cut to be able to receive the silicon layer. The UTSi® films were first developed by California Institute of Technology and Hewlett-Packard in 1978. Currently, Peregrine Semiconductor Corporation (founded in 1990) is the only company which has accomplished a commercially feasible product portfolio, using their patented SOS UltraCMOS® technology [59, 60]. The second method, which gives superior performance, is called bonded SOS technology and is formed by wafer-bonding processes, commercialized in 2010.

Both processes are used by Peregrine company, although they only offer the UTSi® process for the external customers. The work in this thesis used the UTSi® process.

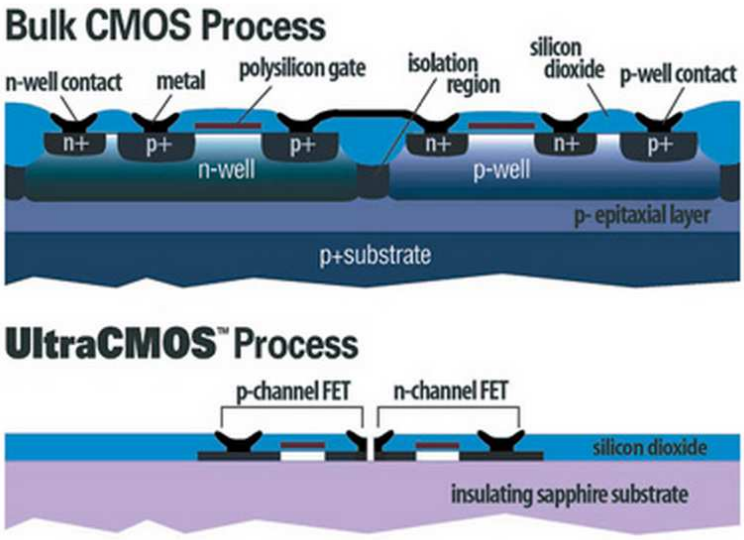

FIGURE 6.1: Ultra CMOS vs Bulk CMOS [60].

6.2 Peregrine UltraCMOS® Process

A single chip of the Peregrine's UltraCMOS® process can accommodate variety of circuits such as high performance RF, high voltage analog, optical, as well as the more traditional digital, analog and mixed signal. This is possible by taking advantage of combining standard CMOS and an insulating substrate. The cross-sections of the UltraCMOS® process in comparison with a bulk CMOS process are shown in Fig. 6.1. It is clear that to build an NMOS or PMOS transistor in a traditional bulk CMOS process, a large number of layers are required.

UltraCMOS® technology's available process options are summarised in Table 6.1, with each option optimised for a specific application. There are three metal layers available, where the top metal layer has thicker metallisation ($\approx 3\ \mu m$) in FC, GC and PC processes. This layer is used to build high quality factor inductors. Also metal-insulator-metal (MIM) capacitors are made between the thick metal layer and the second

TABLE 6.1: Technology Options of UltraCMOS® SOS Process [60]

Features Summary	Units	Process Variants					
		FA	FC	GA	GC	PA	PC
Generation		0.5 μm		0.25 μm / 0.35 μm		0.25 μm	
Release Status		Production		Production		Qualification	
Application		Com/Auto/Mil		Com/Auto/Mil		Com/Auto/Mil	
Supply Voltage	V	3.0/3.3		2.5/3.3		2.5/3.3	
Transistor Vts		3n/3p	3n/3p	3n/3p	3n/3p	3n/3p	3n/3p
Resistors		2n/1p/1polycide		2n		2n	
Interconnect Layers		3	3*	3	3*	3	3*
MIM Caps		No	Yes	No	Yes	No	Yes
Inductors		No	Yes	No	Yes	No	Yes
f_t (IN Device)	GHz	15		30		30	
f_{max}	GHz	45		90		90	

* Last layer interconnect is a thick metal layer for High Q Inductor construction

TABLE 6.2: Transistors type descriptions for FC [61] and GC [62] Processes

		Threshold Voltage (V)	Application
FC	RN	0.67	Digital and low leakage
	NL	0.13	High-performance digital and RF
	IN	-0.20	High-performance digital and RF
GC	RN	0.43	Digital and low leakage
	HN	0.70	Digital and low leakage
	IN	0.08	High-performance digital and RF

metal layer. The key features of the FC and GC processes are similar, except for smaller gate lengths in the GC process, enabling operation in higher frequency bands.

6.2.1 Switching Performance of NMOS Transistors

There are three N-channel and three P-channel transistors with different threshold voltages available in UltraCMOS® process for applications such as RF, high performance digital and low leakage applications. The specifications are shown in Table 6.2.

One of the first tasks of this research was to investigate the RF switching performance of the NMOS transistors in the FC and GC processes [63]. Fig. 6.2 shows the test circuit,

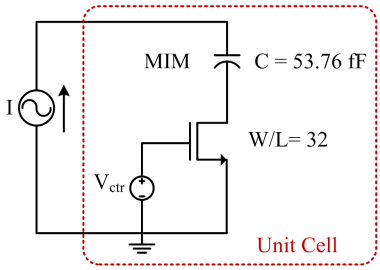

FIGURE 6.2: Test circuit

consisting of an MIM capacitor and an NMOS switch. This is a unit capacitor cell which will be used in the switched capacitor banks. The smallest available MIM capacitor in the design kit is 53.76 fF, and is used as the unit capacitor. The switching performance of the different NMOS transistors are evaluated in the test circuit using Cadence software and the Peregrine company's PDK library. Negative voltages are required to turn-OFF the NL and IN transistors, since they have a near zero threshold voltage.

The quality factor in the ON state ($Q_{ON} = \frac{Im(Z_{ON})}{Re(Z_{ON})}$), and the ratio of the ON-capacitance to the OFF-capacitance ($\frac{C_{ON}}{C_{OFF}} = \frac{Im(Z_{OFF})}{Im(Z_{ON})}$) are measured. Simulation results are summarised in Tabel 6.3. The results indicate that IN transistors in both FC and GC processes have the highest Q_{ON} and $\frac{C_{ON}}{C_{OFF}}$. The higher the Q_{ON}, the smaller the insertion loss, and the higher the $\frac{C_{ON}}{C_{OFF}}$, the higher the tuning ratio of the capacitor bank. Therefore, IN transistors are the most suitable and have the smallest $R_{ON}\times C_{OFF}$ figure of merit (FOM).

6.3 Summary

A significant improvement in performance of key RF building blocks (RF switches, low noise amplifier, mixer, power amplifier) has been shown in [64], [65] in comparison

TABLE 6.3: Q_{ON}, $\frac{C_{ON}}{C_{OFF}}$ and $R_{ON} \times C_{OFF}$ of the test circuit for NMOS transistors @ 2GHz

		W μm	L μm	Q_{ON}	$\frac{C_{ON}}{C_{OFF}}$	$R_{ON} \times C_{OFF}$ $10^{-12}s$
FC	RN	25.6	0.8	7.42	11.8	0.91
	NL	16	0.5	8.03	17.9	0.55
	IN	**16**	**0.5**	**8.99**	**17.9**	**0.49**
GC	RN	8	0.25	5.78	17.3	0.79
	HN	8	0.25	4.8	17.73	0.93
	IN	**8**	**0.25**	**7**	**17.56**	**0.65**

to the bulk silicon. The results are also comparable with Si bipolar and GaAs based circuits. On-chip inductors are one of the key passive components in RF circuits. As a result of the insulating substrate, SOS provides high performance inductors, which eliminates the need for novel and additional processing [66].

In this work we chose the GC process because of its higher operating frequency, and we used IN transistors for the better RF switching performance. A 9-bit phase shifter using the above process is described in the next chapter.

Chapter 7

9-bit Passive Phase Shifter

A high resolution and high dynamic range phase adjuster device is one of the main building blocks of the cancellation loop in the adaptive duplexing architecture. In this chapter, the design and implementation of a passive digital phase shifter is presented. It uses a capacitor loaded lumped element transmission line fabricated in a silicon-on-sapphire (SOS) process. Switched capacitor banks employing a combination of ganged and individual switching achieve a nominal 9-bit phase resolution with only a 6-bit chip area. Stacked FET transistors enabled increased power handling of the switches. A 360° phase range was measured at 1.4 GHz with a maximum insertion loss of 12.6 dB. The measured IIP_3 was better than +39 dBm.

Design requirements are presented in Section 7.1. Details of the circuit design and the challenges involved in decreasing the size and increasing the power handling and resolution are discussed in Section 7.2. Section 7.3 presents the experimental results and their comparison with the post-layout simulation results.

7.1 Design Requirements

Recalling the adaptive duplexing discussion presented in Chapter 4, the required resolution for the phase adjuster device can be calculated to obtain a desired isolation. Duplexing filters in handsets typically provide 55 dB of isolation. If an initial isolation of 25 dB can be achieved by a low isolation device (using, for example, devices such as circulators, directional couplers, filters and dual antennas), then the cancellation loop is required to provide an additional isolation of about 30 dB to stop the Tx signal from desensitizing the receiver circuit.

The contours of the worst case isolation are plotted in Fig. 7.1 versus $\Delta\theta$ and Δr. It is observed that to obtain 30 dB isolation, a $\Delta\theta$ of 3° is required. This implies that at least 7-bit resolution is needed when covering the 360° phase range.

To keep the chip area within the manufacturers limit ($< 3 \times 3$ mm^2), the frequency of operation has been limited to 1.7 GHz to 2.2 GHz. This covers a number of popular LTE bands (Fig. 1.1). Note the lower bands, 0.7 GHz to 1.5 GHz, would require larger inductors.

7.2 Circuit Design

In the adaptive cancellation technique it is important to have similar delays through the cancellation loop path as per the main signal path to achieve sufficient cancellation bandwidth. This factor is considered in the design of the phase shifter and a delay type phase shifter architecture is thus chosen, since some or all of the compensation delay,

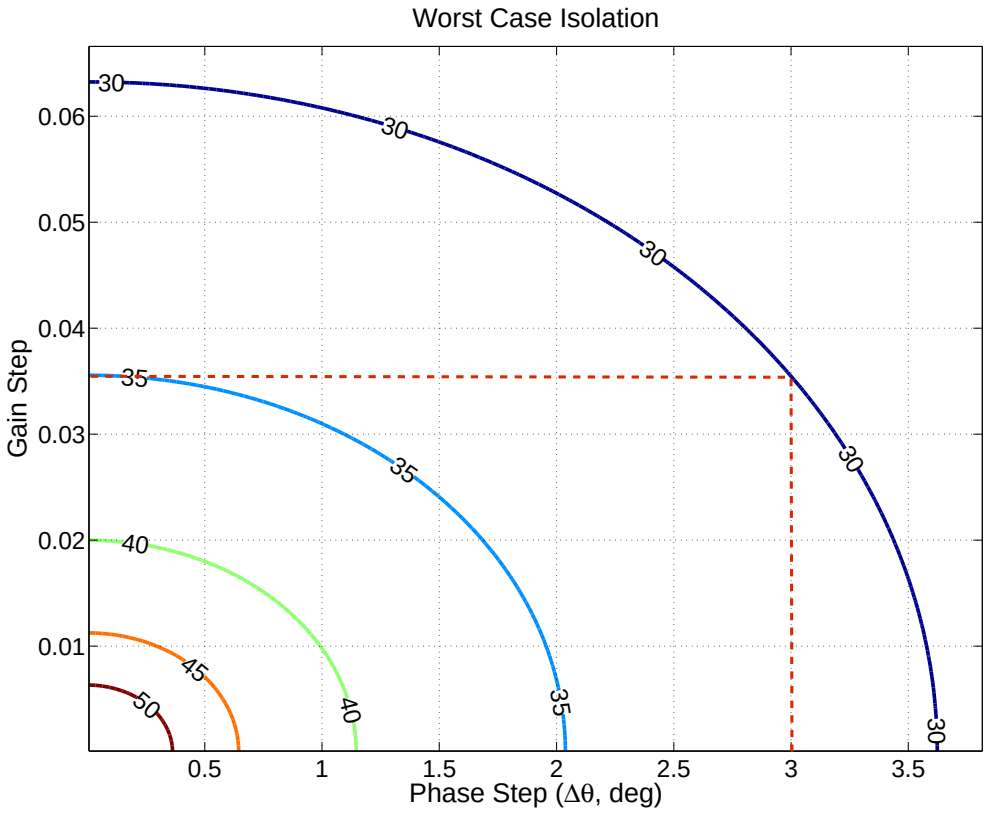

FIGURE 7.1: Worst case isolation (dB) gain and phase step size.

τ_1, can be included in the phase shifting circuit. In this section the design procedure for different parts of the phase shifter device, including the RF circuit, digital control block, and ESD protection circuit is presented.

7.2.1 RF Circuit Design

The design is based on a transmission line using lumped elements, with the main building block being a low-pass π circuit. By tuning the capacitors, phase control is achieved, and to attain a wider phase shift range, multiple π circuits are cascaded, as shown in Fig. 7.2. A downside of the topology is that not all the phase shift in the π circuit is controllable. The minimum phase shift is limited by parasitic capacitance effects. This

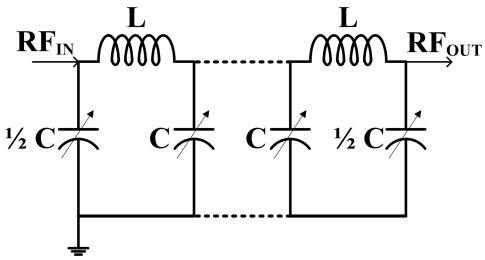

FIGURE 7.2: Lumped element transmission line topology.

forces the use of more stages (e.g. fourteen as per [39] and sixteen as per [38]) or operation closer to the cut-off frequency to get the same tuning range. Both solutions result in higher insertion loss (IL), but we choose the latter because of the lower operating frequency and size considerations.

In a lossless infinite transmission line the characteristic impedance, Z_C, and the phase shift per section, $\phi(\omega)$, can be simplified to [67]:

$$Z_C \approx \sqrt{\frac{L}{C}}\,, \tag{7.1}$$

$$\phi(\omega) \approx \omega\sqrt{LC} \quad => \quad \Delta\phi(\omega) = \omega\sqrt{L}\,(\sqrt{C_{Max}} - \sqrt{C_{Min}}), \tag{7.2}$$

where C_{Max} and C_{Min} are the maximum and minimum capacitance of the capacitor bank in each stage, respectively. The tuning range, $\frac{C_{Max}}{C_{Min}}$, is determined by the ratio of $\frac{C_{ON}}{C_{OFF}}$ in the capacitor array, which in this design is $\frac{C_{ON}}{C_{OFF}} = 6.8$. It is a trade off between the tuning range and ON state quality factor, Q_{ON}. The differential phase change that results from a differential change in the capacitance can be derived as

$$\frac{\delta\phi}{\delta C}(\omega) = \frac{1}{2}\omega\sqrt{\frac{L}{C}}. \tag{7.3}$$

Eq. 7.3 indicates that the relationship between the phase change and the capacitor

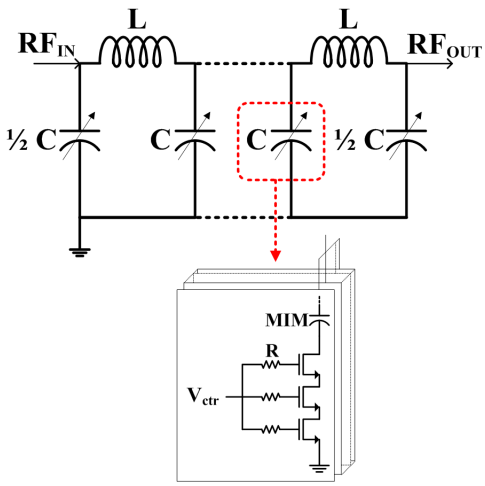

FIGURE 7.3: Schematic of the 9-bit phase shifter.

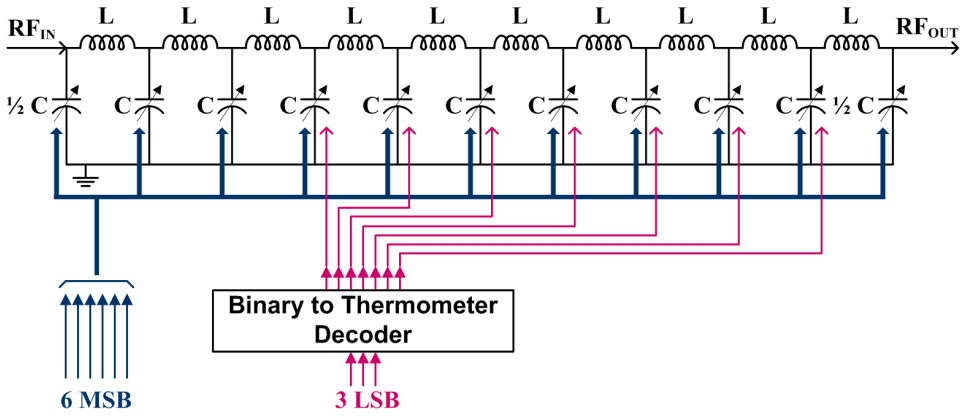

FIGURE 7.4: Proposed control method.

change is nonlinear. Switching a unit capacitor cell near the C_{Min} state will result in a $\sqrt{\frac{C_{ON}}{C_{OFF}}} = \sqrt{6.8} = 2.6$ times larger phase change than at the C_{Max} state, which means 1.4-bits difference in the resolution. Note also the increase in phase shift with frequency. Both these factors will affect the achievable resolution (in bits) of the phase shifter. To obtain sufficient resolution despite this nonlinear behaviour, the phase shifter is designed with 2 additional bits, i.e. a total of 9-bits.

The conventional method to tune the capacitors is to control all the capacitors in the network simultaneously, as it is employed in varactor loaded transmission line phase shifters [38],[39]. Varactors generate distortion when signal levels are high. In order to

provide large signal handling with low distortion, we employ switched capacitor arrays instead of varactors (as shown in Fig. 7.2), which also provides digital tunability. This enables direct control from the DSP unit and eliminates the need for a DAC (Digital to Analog Converter). Ten stages are cascaded to achieve more than 360° phase coverage (36°/stage) at 1.7 GHz also using the worst case process corners.

To achieve 9-bit resolution, $2^9 - 1 = 511$ unit capacitor cells (of size C_{uc}) are required for each capacitor array. The switch dominates the size of the unit capacitor cell(Fig. 7.4). The capacitor array becomes too big even if the minimum size MIM (Metal-Insulator-Metal) capacitor is chosen from the design kit library. A new control method is therefore proposed to achieve high resolution while keeping the capacitor array small, as shown in Fig. 7.4. The required capacitor array only uses $2^6 - 1 = 63$ unit cells organised in binary weighted groups (C_{uc}, $2C_{uc}$, $4C_{uc}$,..., $32C_{uc}$) and arranged in a semi common-centroid pattern (7×9). The layout of the capacitor array and the unit capacitor cell are shown in Fig. 7.5. All the stages are controlled simultaneously by the 6-MSBs (Most Significant Bits). To increase the resolution we take one cell from the MSB group for individual switching. These individual cells from seven of the stages are controlled by a 3-bit binary-to-thermometer decoder representing the 3-LSBs (Least Significant Bit) of the 9-bit control word (as shown in Fig. 7.4). This enables the array size to be decreased to 63 unit cells from 511 with the penalty of a slight reduction in the control range. The reduction is caused by the MSB switching a group of 31 cells instead of 32 cells. Note, the change from 01111 to 10000 now becomes 01111 to 10001 to compensate for the missing cell.

The unit capacitor cell consists of a MIM capacitor and three stacked FET transistors

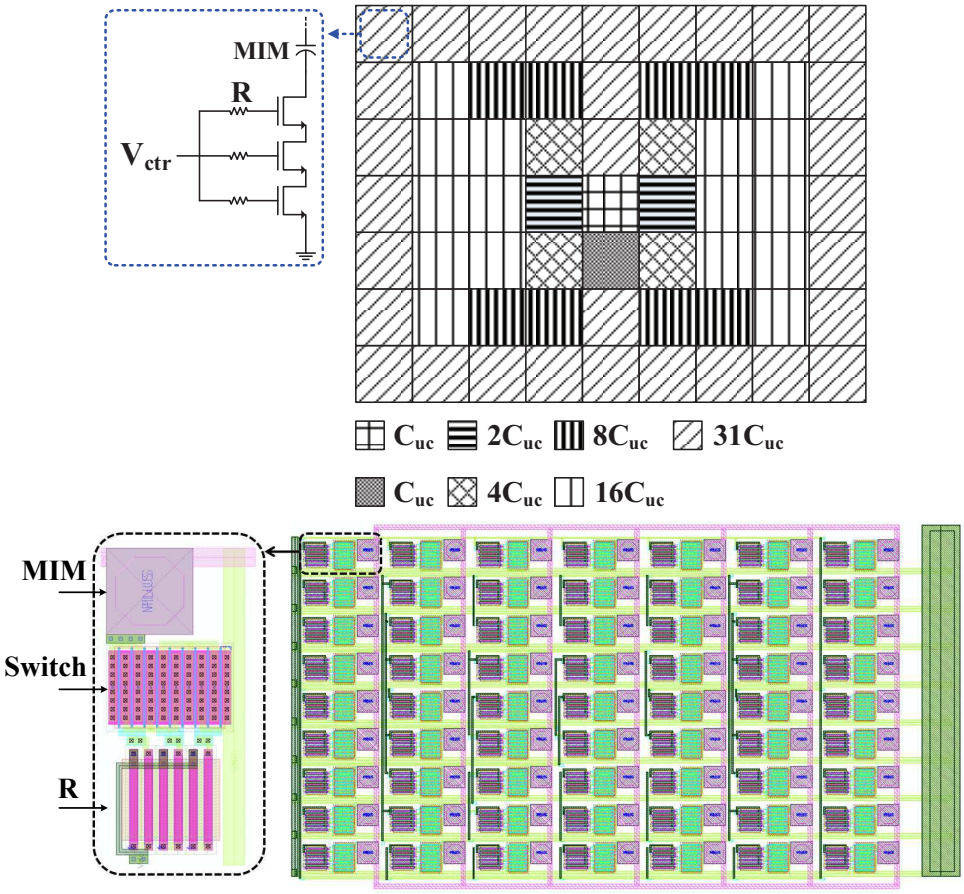

FIGURE 7.5: Layout of the unit capacitor cell, and the capacitor array.

acting as a switch. Stacking is necessary to meet the voltage handling requirements. A minimum size MIM capacitor is chosen as the unit capacitor, $C_{ON} = 66\,fF$ to keep the array size small. Zero threshold MOS transistors are used as switches since they have better distortion performance [63]. The control voltage (V_{ctr}) is 2 V to switch the transistors ON and -1.5 V to turn them OFF. The switch size determines the ON state quality factor and the OFF state capacitance, where C_{OFF} is dominated by the leakage capacitance through the switch. Post-layout simulations are conducted to optimise the size of the switch. A switch size of $W = 45\,\mu m$ and $L = 0.25\,\mu m$ results in a $Q_{ON} = 8$,

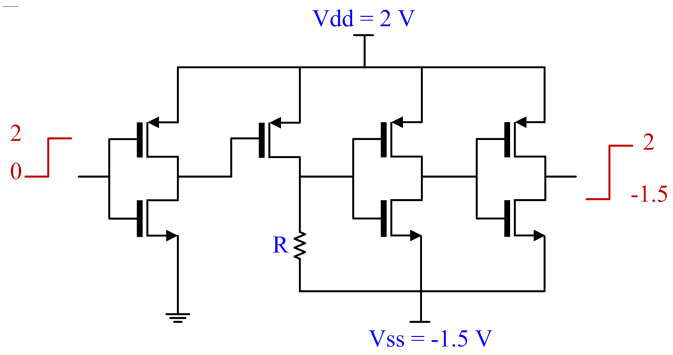

FIGURE 7.6: Level shifter circuit using thick oxide transistors.

and $\frac{C_{ON}}{C_{OFF}} = 6.8$ at 2 GHz, which are calculated as:

$$Q_{ON} = \frac{Im(Z_{ON})}{Re(Z_{ON})} \qquad \frac{C_{ON}}{C_{OFF}} = \frac{Im(Z_{OFF})}{Im(Z_{ON})} \tag{7.4}$$

The inductors are all nominally 2.3 nH and are chosen from the Peregrine library, which results in an average value of 50 Ω characteristic impedance.

7.2.2 Digital Control Block

As mentioned earlier, a 3-bit binary-to-thermometer decoder is used to provide the control lines for individual switching. Digital input lines are fed to the circuit from a DSP unit with the signal levels of 0 V and 2 V. A level shifting circuit, therefore, is integrated with the decoder circuit to provide required signal levels (-1.5 V and 2 V) to control the switches. Fig. 7.6 shows the schematic for the level shifter circuit. Thick oxide transistors are used in this circuit, as they have a higher breakdown voltage (3.5 V).

7.2.3 ESD Circuit

Two sets of digital input PADs are placed on the test chip. The required ESD circuit for each set depends on the voltage levels of the lines. One set is for the normal digital inputs to the circuit, which are fed from a DSP unit, with levels of 0 V and 2 V. A parallel combination of a clamp (gate-grounded NMOS) and a gated diode is used as the ESD protection cell (Fig. 7.7(a)). A break-down in the clamp clips the positive peaks, while the diode shunts the current during the negative peaks.

The second set is for the digital inputs of -1.5 V and 2 V. Two ESD cells are used in series with opposite polarity (Fig. 7.7 (b)) to provide ESD protection with no interference to the circuit's normal performance. The ESD current paths in both positive and negative peaks are shown in the schematic. PADs with the latter protection were available to monitor and potentially overwrite the digital circuitry to directly activate the switches for test purposes.

PAD based ESD protection is used as it simplifies the layout, when there are limited metal layers available. Circuit layout techniques are employed to provide shortest current paths form PADs to the GND, while keeping the ohmic resistance as low as possible.

7.3 Experiments

Fig. 7.8 shows the final layout of the 9-bit passive phase shifter, including the digital control circuit. The north and south pads are RF GSG (Ground-Signal-Ground) input

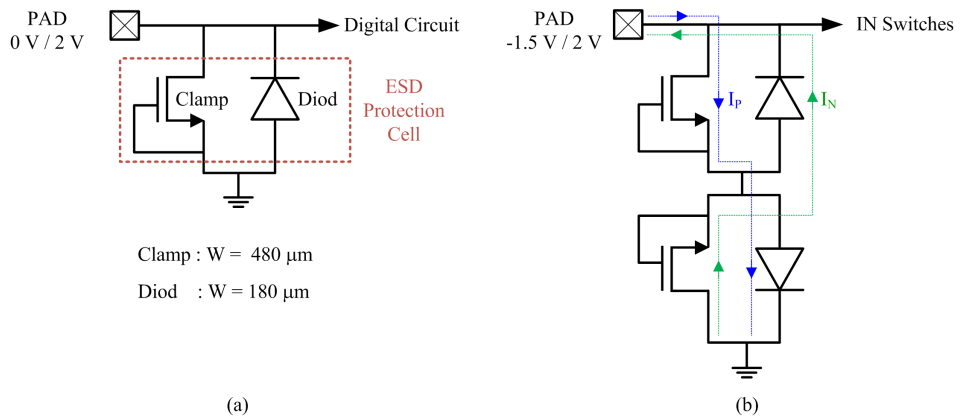

FIGURE 7.7: ESD circuit for control lines with (a) 0/2 V and (b) -1.5/2 V levels.

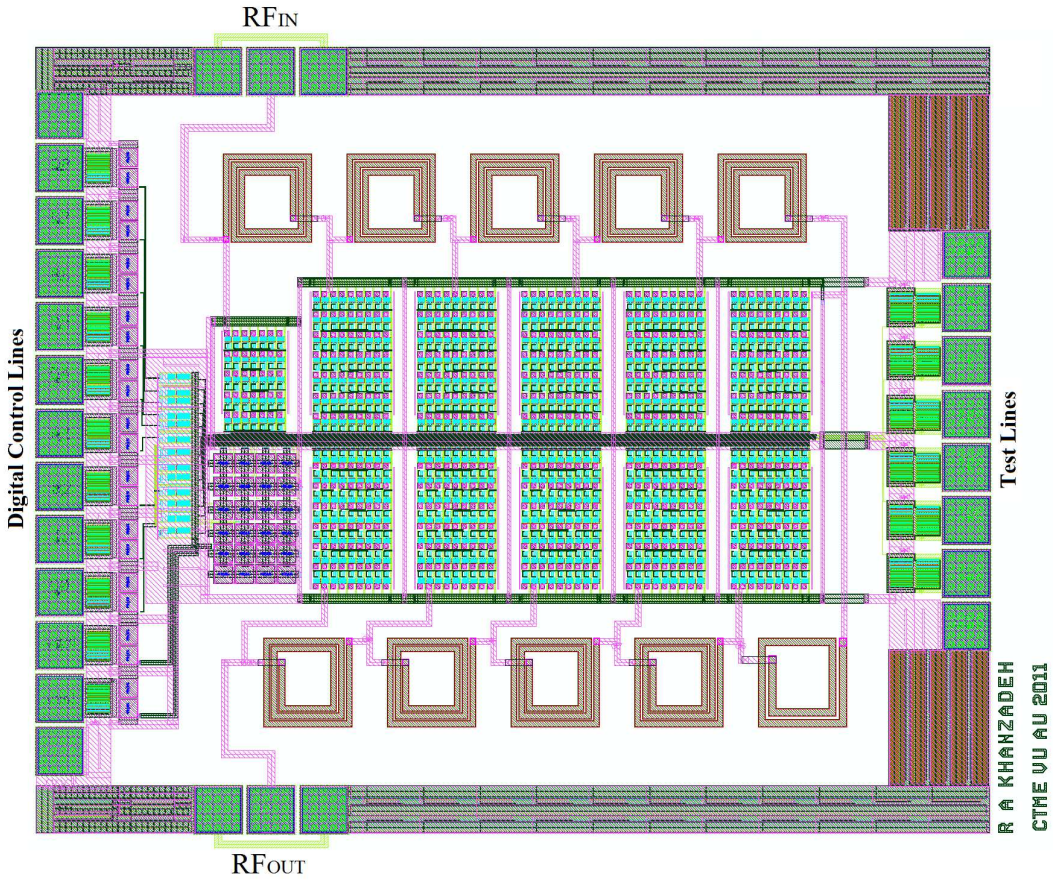

FIGURE 7.8: Final layout.

and output pads, and the west pads are the digital control lines along with the supply voltages. The 9-bit phase shifter was fabricated in the Peregrine 0.25 µm UltraCMOS GC SOS process.

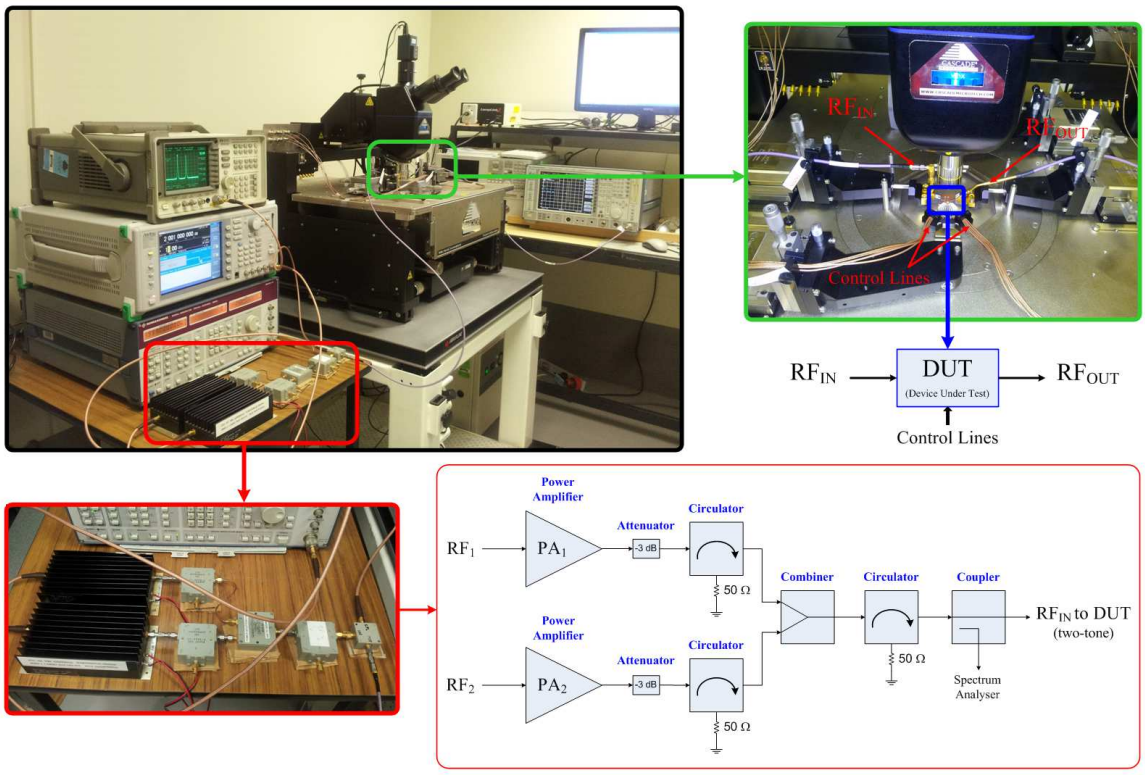

FIGURE 7.9: Probe table and two-tone test experimental set-up.

7.3.1 Measurement Set-up

A CASCADE MICROTECH probe station was used to evaluate the performance. Agilent Network Analyser (N5230A) is used to conduct the S-Parameter measurements, while a two-tone test was used for distortion analysis. Fig. 7.9 shows the measurement set-up along with the circuit diagram for the two-tone generation. A coupler is used to check the integrity of the input two-tone signal.

7.3.2 Measurement Results

The microphotograph of the chip is shown in Fig. 7.10. The chip size including pads is 5.94 mm^2. The measured total phase control range , $\Delta\phi(\omega)$, is 360° at 1.4 GHz and increases with frequency as shown in Table 7.1. The IL also increases with frequency,

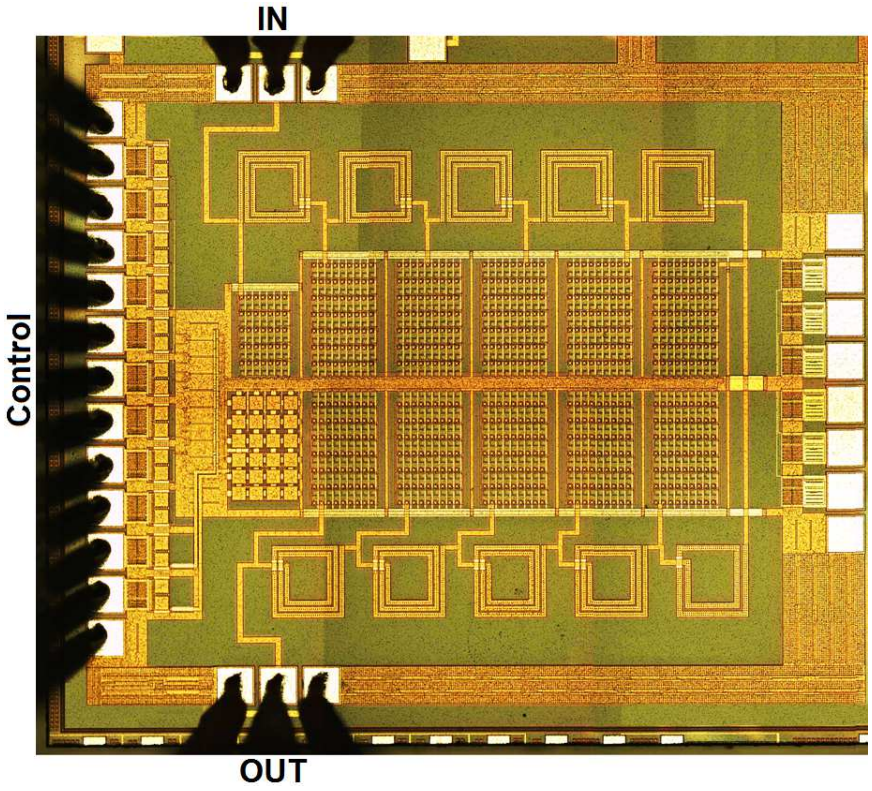

FIGURE 7.10: Chip photo of the 9-bit phase shifter.

from about 12.6 dB at 1.4 GHz to 16.6 dB at 2 GHz. The worst case insertion loss occurs at the maximum phase shift, when all the capacitors are switched in, however, only a control range of 360° is required and the IL is thus specified at that point (Table 7.1, column 2). The IL will drop below 6 dB when all capacitors are switched out, and it is therefore given as 9.3±3.3 dB. The return loss on the input and output ports is better than 10 dB over the frequency range.

At large phase shifts the impedance of the transmission line drops below 50 ohm and this causes the circulating currents to increase and the cut-off frequency to reduce.

TABLE 7.1: Measured IL, total phase shift and effective number of bits

Frequency GHz	IL for 360° dB	$\Delta\phi(\omega)$ deg	B Effective (bits)		
			@0°	@360°	Average
1.4	12.6	360°	8.1	9.5	9
1.7	13.7	444°	7.8	9.2	8.7
2	16.6	552°	7.5	8.9	8.4

The system becomes more sensitive to the finite ON-resistance (R_{ON}) of the switches which increases the IL. Unfortunately increasing the transistor width also increases the parasitic capacitance and so reduces the tunning range. The traditional solution is to use transistors with a lower $R_{ON} \times C_{OFF}$ figure of merit, and some devices have recently been reported [68]. Moving away from the common centroid structure of unit cells might also be advantageous, since switching cells of larger capacitance will reduce the amount of interconnect wiring and related fringing parasitics.

Given the measured total phase control range for the frequency of operation, $\Delta\phi(\omega)$, it is possible to use Eq. 7.2 and Eq. 7.3 to calculate the phase step size, and so obtain the effective resolution, B-bits, shown in Table 7.1. The highest average resolution of 9-bits is obtained at 1.4 GHz, when the full control range is exactly 360°; even so the resolution varies between 8.14-bits to 9.5-bits as the output phase changes between 0° to 360°. Therefore the rule of thumb is that the worst case resolution is one bit less than the nominal value. At higher frequencies the resolution is degraded because only part of the capacitor adjustment range is needed to cover the 360° span.

Fig. 7.11 presents a polar plot of the output signal at 1.7 GHz over the whole phase control range. It can be seen that more than 360° phase control is achieved. As mentioned earlier, obtaining more than 360° phase shift decreases the effective resolution. On the other hand, it has a positive effect on the control mechanism. For example, when the control algorithm is searching for the optimum phase setting in the vicinity of the 0° to 360° boundary, there will be considerable capacitor switching, which will result in many switching transients and large gain variations. The latter must be compensated by

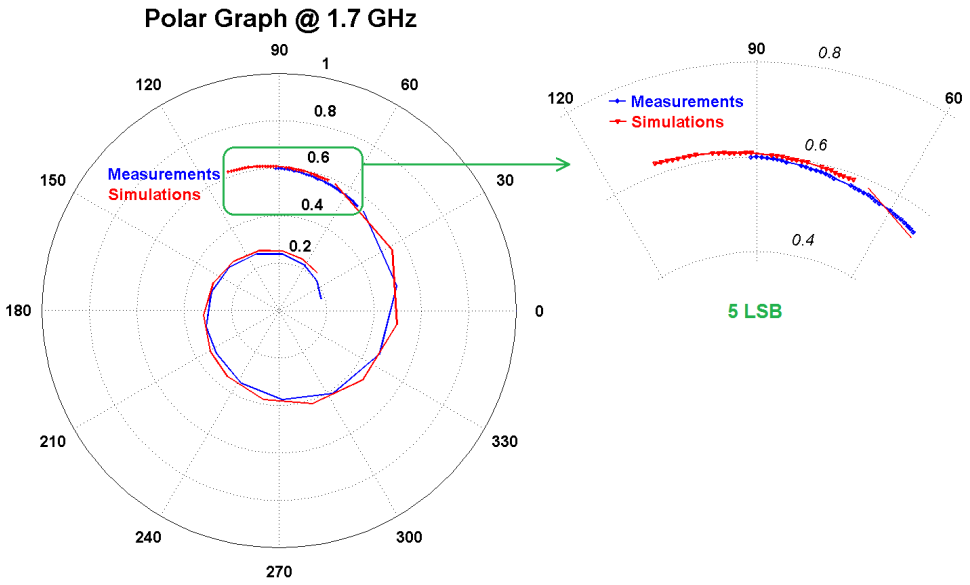

FIGURE 7.11: Phase and IL over 9-bit (5LSB and 4MSB separately); simulation and measurement.

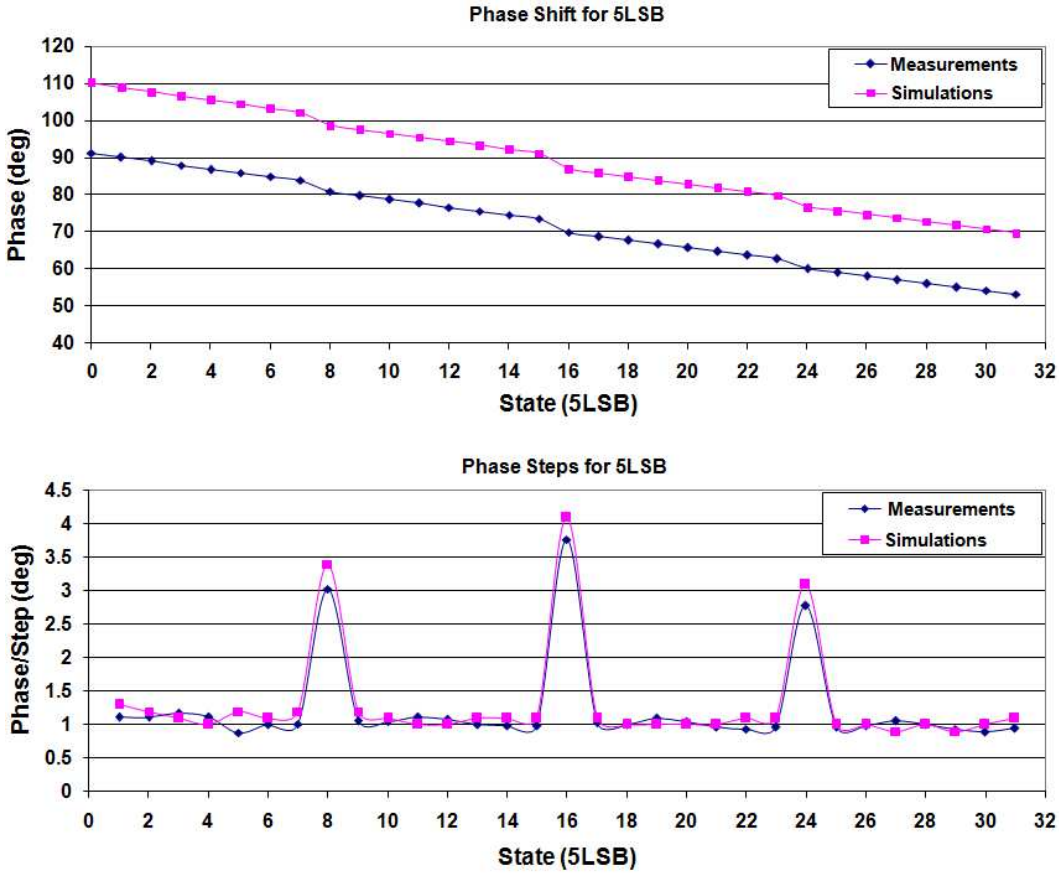

FIGURE 7.12: Phase variation over 5LSB; simulation and measurement.

a gain adjuster block. By providing more than 360° throughout the phase control range, it is possible to find a zone where there is no need for abrupt phase wrap-arounds.

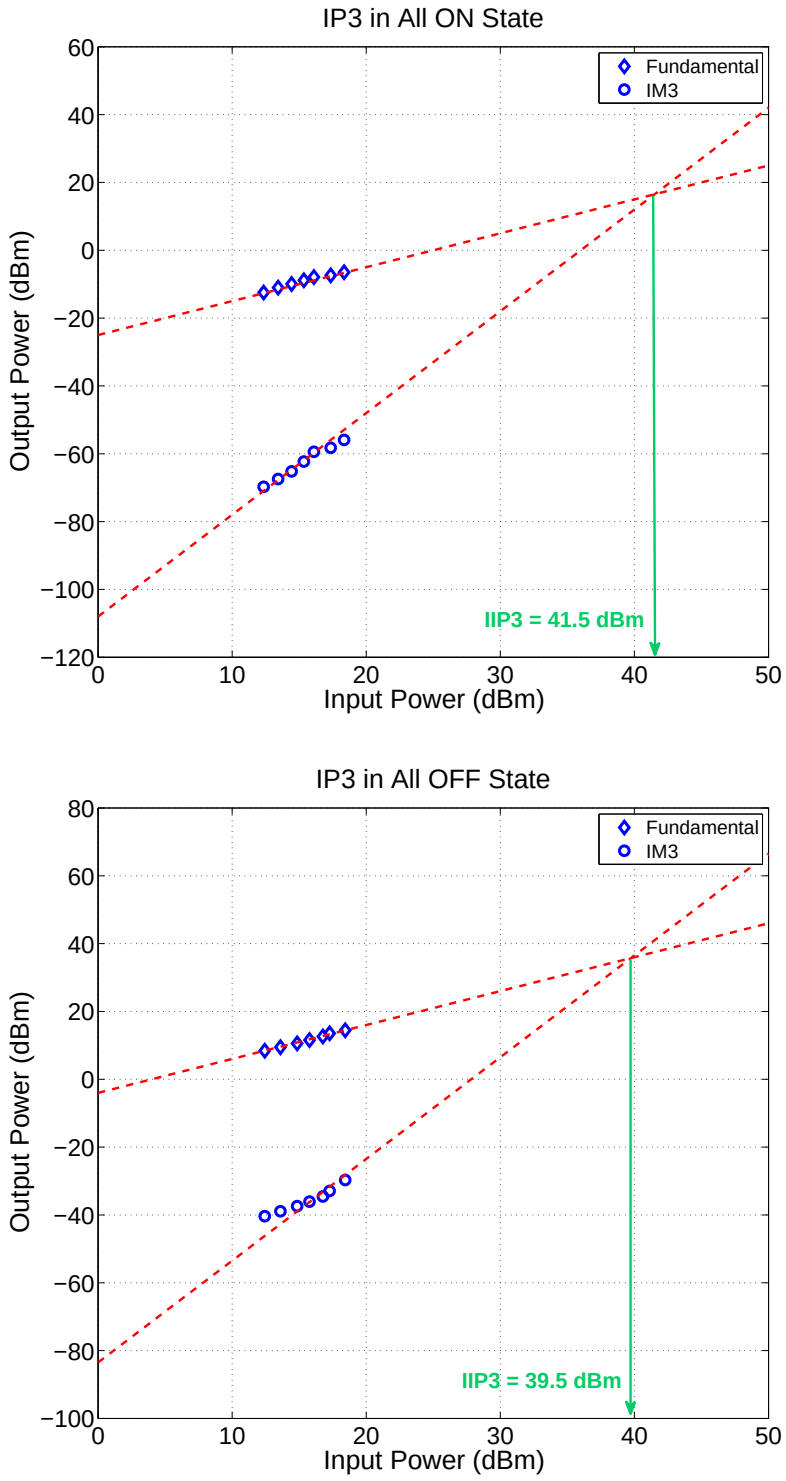

FIGURE 7.13: Measured IIP_3; all ON (maximum phase shift) and all OFF (minimum phase shift) states

The measured and simulated phase shifts that occur when the 5LSBs are adjusted, are shown in Fig. 7.12. The total phase shift is around 40° and there is a 20° fixed offset

phase (caused by process variations). However the important measure is the phase shift per step, which has excellent agreement. The peaks that occur whenever the 4th LSB changes state are caused by a design oversight. The individually switched cells should have approximately 25% extra capacitance, since the number of stages is 10 instead of 8 as was used in the initial design. The extra stages were added to compensate for process variations. The excellent agreement between the measured and simulated results indicates, however, that the peaks are correctable and this will be implemented in the next iteration.

A two-tone measurement was performed to evaluate the nonlinear behaviour of the chip (Fig. 7.9). An IIP_3 of 40 dBm±1dB was measured at the input. The higher value occurred when all the capacitors were activated to give maximum phase shift (All ON state) and the lower value occurred at minimum phase shift (All OFF state). The IIP_3 results (Fig. 7.13) satisfy the power handling requirements of the adaptive duplexer, discussed in Subsection 4.2.2.

7.4 Summary

In this chapter, the design methodology and measurement results of a nominal 9-bit passive phase shifter are discussed. A lumped element transmission line with switched capacitors is employed to achieve a combination of both high phase resolution (> 8.1-bit) and high linearity (IIP_3 > +39 dBm), but at the expense of increased insertion loss. This compares with 6-bit resolution and IIP_3 of 28 dBm for the best silicon based devices to date [37, 44]. The new control method enables 9-bit resolution with only a

6-bit chip area, however the chip size is still large (5.94 mm^2). The phase resolution is enough to meet 30 dB isolation requirement for the cancelling loop.

The measured bandwidth is from 1.4 GHz to 2 GHz, which is limited by the achieved phase shift in the lower end and insertion loss in the higher end.

In the next chapter, a 10-bit passive phase shifter is presented. The new design uses different phase shifter configurations to provide low insertion loss, high resolution and high linearity with a smaller foot print.

Chapter 8

10-bit Passive Phase Shifter

To reduce the size and insertion loss of the previous 9-bit phase shifter design, a new topology is proposed. The resolution is also increased by one bit to improve the isolation performance of the cancelling loop, which can either improve the overall performance of the adaptive duplexer or reduce the low isolation device requirements (Fig. 4.1).

Details of the circuit design and the challenges involved in decreasing the size and increasing the power handling and resolution are discussed in Section 8.1. Section 8.2 presents the experimental results and comparison with the post-layout simulation results. Section 8.3 summarises the chapter.

8.1 Circuit Design

The previous phase shifter used 10 π sections, each with a loss of 1.26 dB in the worst case condition with all capacitors switched in. The philosophy behind the new design is

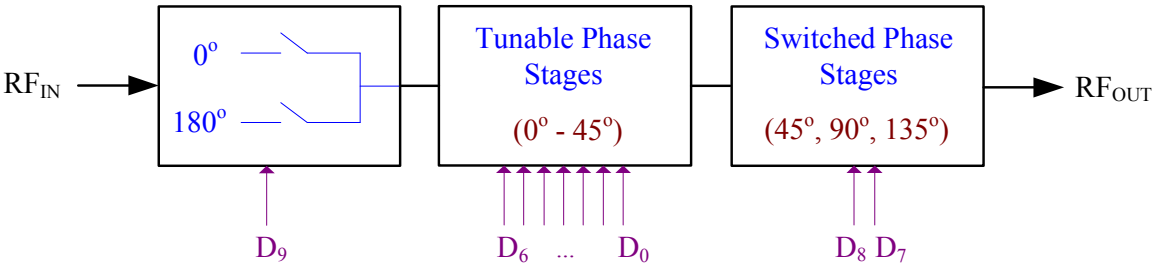

FIGURE 8.1: Block diagram of the proposed 10-bit phase shifter.

to reduce the number of π sections and also to reduce the loss per section by operating them further away from their cut-off frequency.

Three different phase shifter structures are combined to provide 10-bit phase control with low insertion loss and small chip area (Fig. 8.1). An auto-transformer is used to obtain 180° phase shift, which is controlled by the MSB of the phase control word. The auto-transformer can replace five sections (half of the transmission line) in the previous design. A tunable 45° phase shifter section then provides the fine resolution controlled by the 7-LSBs. Finally, three fixed 45° phase shift circuits are combined to provide 135° phase shift with 45° phase steps. This section is controlled by the next two MSBs. The design of each block is presented in detail in this section.

8.1.1 180° Phase Shift Block

The conventional way of implementing a 180° phase shift is using a high-pass/low-pass (HP/LP) configuration [43],[44]. A block diagram of the HP/LP network is shown in Fig. 8.2. Typically, a two stage (two inductors) high-pass filter provides a 90° phase lead, while a phase lag of 90° is achieved by a two stage (two inductors) low-pass filter. However, the phase shift that is obtained from each section maybe different. In [44], a single stage high-pass filter is used for the benefit of a smaller size (as only

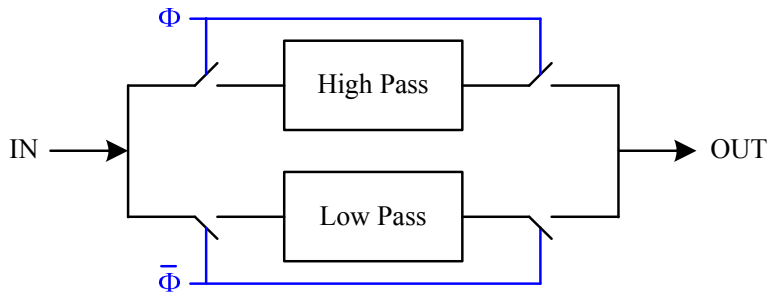

FIGURE 8.2: Block diagram of a high-pass low-pass network.

one inductor is employed), which provides +70° phase shift. Therefore the two stage low-pass circuit must provide -110° phase shift, which requires both circuits to operate closer to the cut-off frequency.

In this work, we propose an auto-transformer as an alternate solution for achieving 180° phase shift, by switching between primary and secondary terminals. The auto-transformer indeed reduces the number of inductors to just one (albeit with slightly increased area). The IL caused by the non-ideal coupling coefficient and finite Q (quality factor) of the transformer is also typically less than the IL of five sections of the previous 9-bit phase shifter. This approach decreases the size of the phase shifter significantly while maintaining a comparable insertion loss to the traditional HP/LP solution. The modeling and analysis of the auto-transformer using ADS (Advance Design System) Momentum is presented in this section. The proposed 180° phase shifter topology is presented and also compared with the traditional HP/LP network.

8.1.1.1 Auto-Transformer

On-chip transformers are typically categorised as planar or stacked structures, depending on the use of lateral or vertical coupling. Planar transformers usually have a small-to-medium coupling coefficient, k, with a medium-to-high quality factor, Q, while occupying a large area. The self-resonance frequency of the planar structure is also high. On the other hand, stacked structures provide a high coupling coefficient, benefiting from both lateral and vertical coupling, with a small size. However, the quality factor is reduced due to the use of thinner metal layers lower in the stack. The self-resonance frequency is also reduced because of higher inter-winding capacitive coupling [69–71].

In this work, a high coupling coefficient at lower frequencies is desirable, therefore a stacked configuration is chosen. The drawback of this structure is the low quality factor, which can be partially improved by employing an octagonal shape. There are three metal layers available in the SOS 0.25 μm GC process. The top metal layer, which is the thickest layer, is used as the primary winding. The second metal layer forms the secondary winding, and the first metal layer is used for bridging. Fig. 8.3 shows the 3D layout and the equivalent circuit of two different approaches. Both use the same layers for the primary and secondary, but with a slight difference in the winding connections, which is more easily understood from the circuit model.

The connection of the windings determines how the parasitic capacitance effects the self-resonance frequency of the network. In both cases the capacitance between the

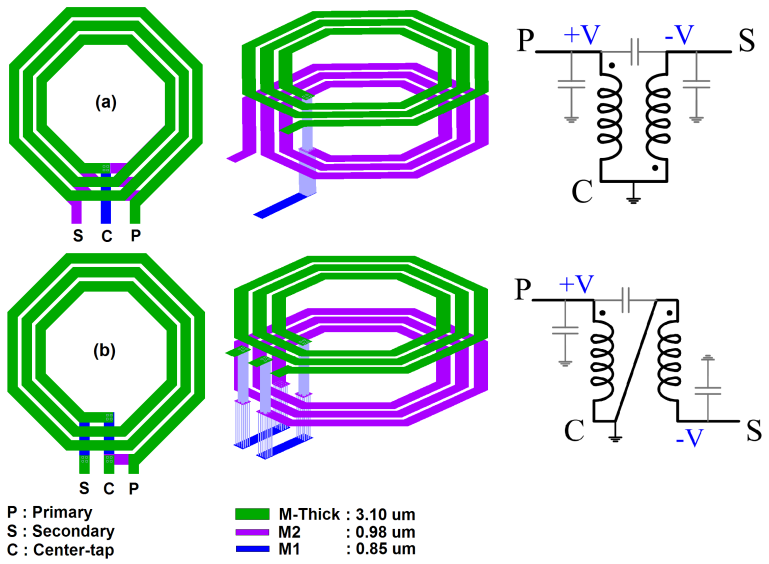

FIGURE 8.3: The top view, conceptual 3D layout, and the equivalent circuit of the two different layout for the auto-transformer.

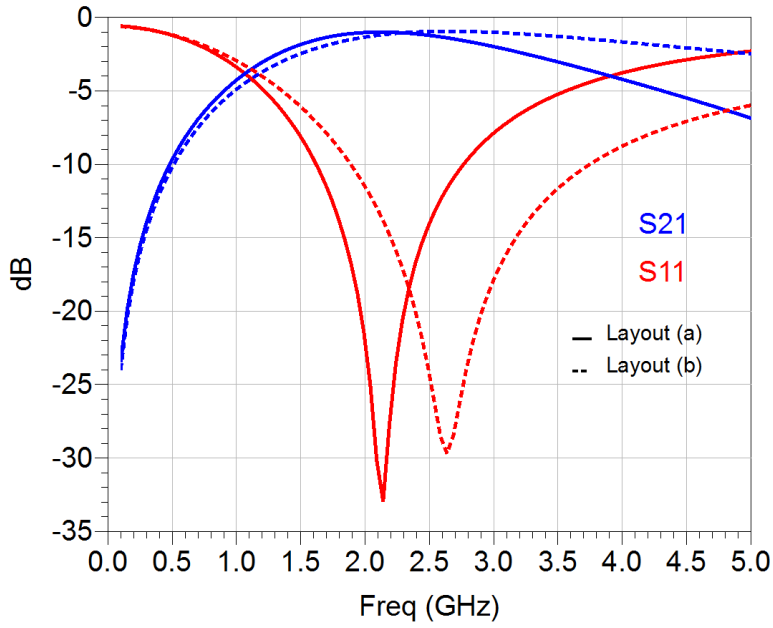

FIGURE 8.4: EM simulation results of layout (a) and (b).

windings M2 and M-thick is the same, but the energy transferred is different. We therefore calculate the energy stored in the parasitic capacitance for both circuits. The distributed capacitance per unit distance of the coil is C_l farads/m and the voltage linearly increases along the coil of length L from 0 to +V Volts (or -V for the secondary). In the top circuit (Fig. 8.3 (a)) the voltage difference between the two coils linearly changes

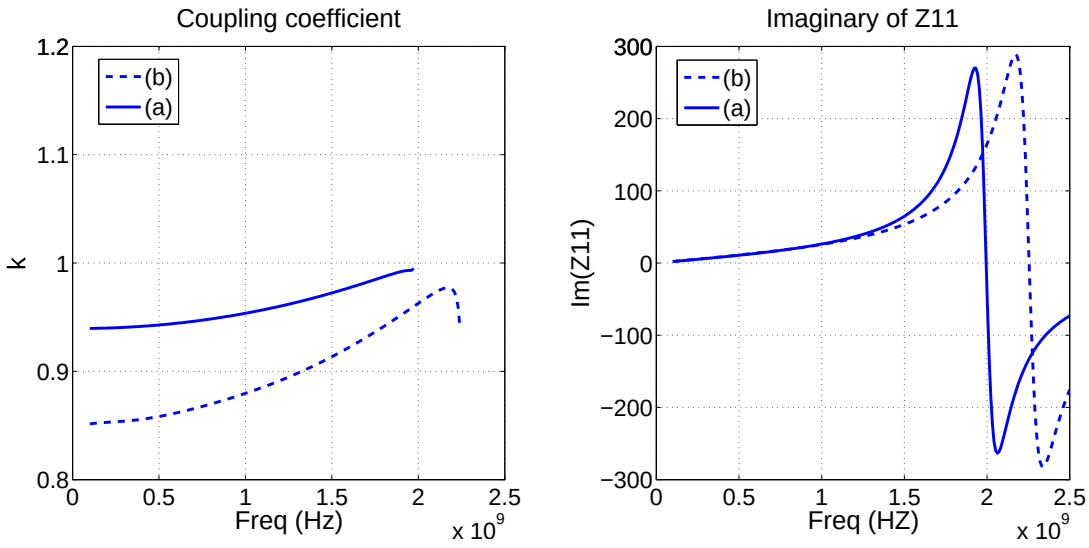

FIGURE 8.5: ADS analysis results; $Im(Z_{11})$ and k.

from 0 to 2V Volts, while in the bottom (b) circuit it remains constant at V Volts. The energy stored is therefore:

$$E_a = \frac{1}{2}\int_0^L C_l \left(\frac{2V}{L}l\right)^2 dl$$

$$E_b = \frac{1}{2}\int_0^L C_l V^2\, dl \tag{8.1}$$

for circuit (a) and (b) respectively. This gives:

$$E_a = \frac{2}{3}C_l L V^2$$
$$E_b = \frac{1}{2}C_l L V^2 \tag{8.2}$$

Eq. 8.2 shows that the energy stored in the parasitic capacitance of layout (a) is 33%

greater than layout (b). The effect this has on frequency is $f_a = \sqrt{\frac{E_b}{E_a}} f_b$, or 11% reduction in self-resonance frequency. EM simulation results of S_{11}, S_{21} and Z_{11} from ADS Momentum (Fig. 8.4 and 8.5) confirm the frequency shift. Z-parameters are used to determine the auto-transformer's characteristic parameters [72]. At the self-resonance frequency Z_{11} is resistive, so $Im(Z_{11})$ becomes zero. The result indicates a self-resonance frequency of 2.25 GHz for circuit (b). The following equations are used to calculate the primary and secondary inductances, L_P and L_S, the primary and secondary quality factors, Q_P and Q_S, and the coupling coefficient, k.

$$L_P = \frac{Im(Z_{11})}{2\pi f}, \qquad L_S = \frac{Im(Z_{22})}{2\pi f}, \tag{8.3}$$

$$Q_P = \frac{Im(Z_{11})}{Re(Z_{11})}, \qquad Q_S = \frac{Im(Z_{22})}{Re(Z_{22})}, \tag{8.4}$$

$$k = \sqrt{\frac{Im(Z_{12})\, Im(Z_{21})}{Im(Z_{11})\, Im(Z_{22})}}. \tag{8.5}$$

All these parameters are frequency dependent.

Fig. 8.5 also shows the coupling coefficient. It is applicable for frequencies below self-resonant and has a value of 0.96 for circuit (b) at 2 GHz. The high coupling coefficient confirms a strong vertical coupling between the thick metal layer and the second metal layer in the SOS process. We employed layout (b) for implementing the auto-transformer for the targeted frequency band (*L*-band).

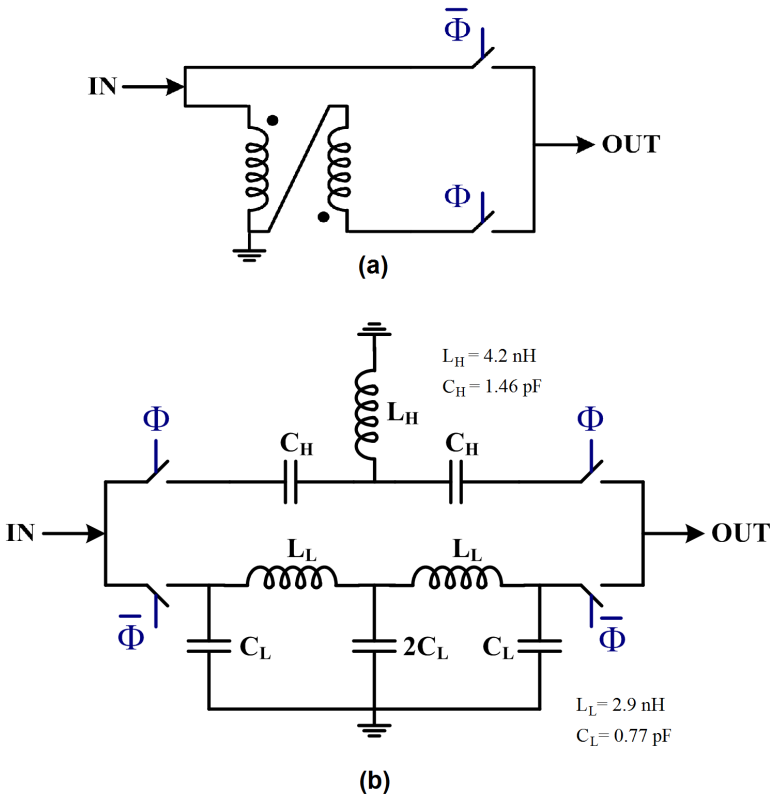

FIGURE 8.6: Schematic of (a) the proposed 180° phase shifter and (b) a conventional HP/LP circuit.

8.1.1.2 180° Phase Shifter

Fig. 8.6 shows circuit diagram of the proposed 180° phase shifter with switches included. A conventional HP/LP scheme is also designed for the same frequency band for comparison.

Switches play an important role in insertion loss and power handling of the designed phase shifter devices. Stacked switches are employed to increase the power handling and linearity. In the HP/LP structure there are two switches in each path, while in the proposed auto-transformer design, there is only one switch per path. However, switches in the latter design face double the voltage of the first circuit, thus they require twice as many devices in the stack. The insertion loss (R_{ON}) through the switch(es) will double

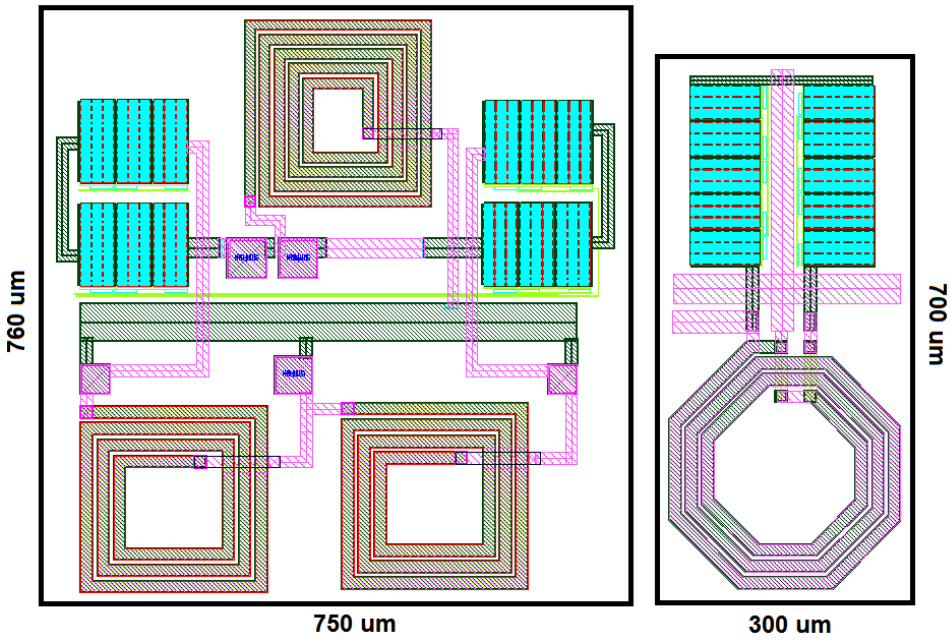

FIGURE 8.7: Layout of the HP/LP circuit and auto-transformer

as will the chip area. We conclude therefore that the switch size per path is the same for both circuits to deliver the same insertion loss and linearity.

The reduction in chip area between the two circuits is therefore caused by the reduced number of passive circuits (mainly inductors). Fig. 8.7 shows the layouts of both circuits, the auto-transformer chip-area is approximately 37% of the HP/LP area.

Post-layout simulation results for both gain and phase shift are shown in Fig. 8.8 and Fig. 8.9 for the frequency band of 1.8-2.4 GHz (auto-transformer) and 1.9-2.5 GHz (HP/LP). The maximum insertion loss is 1.7 dB for the auto-transformer and 1.8 dB for the HP/LP both at the low frequency band edge. The gain variation with phase is in general much less for the HP/LP circuit, even though the worst case variation at the lower band edge is the same (0.6 dB) for both circuits. The phase variation across the band is similar for both circuits 2° for the auto-transformer and 3° for the HP/LP. There is a constant group delay associated with the HP/LP circuit of 0.2 ns which is about

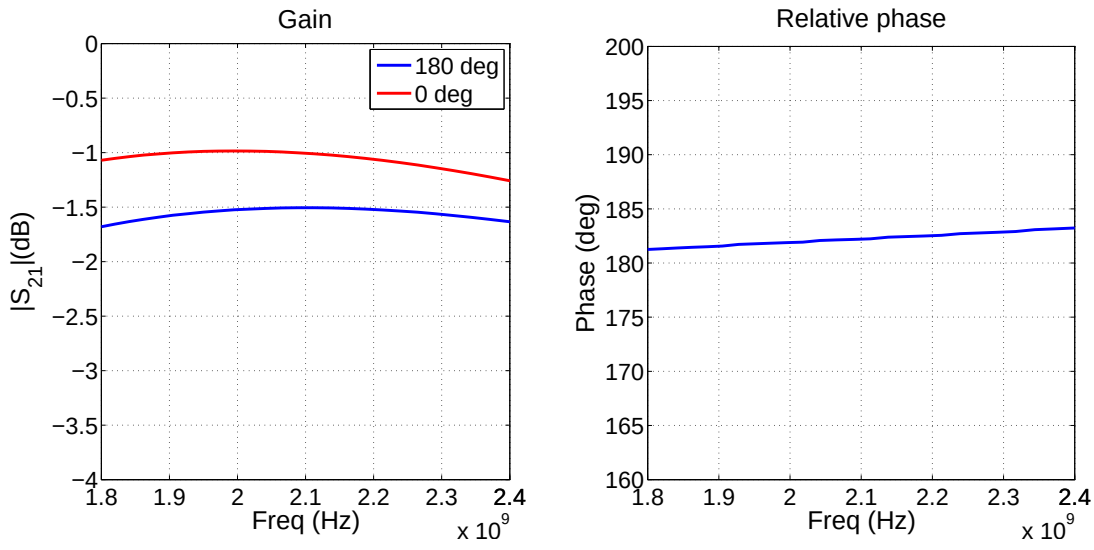

FIGURE 8.8: Simulated gain and phase of the proposed 180° phase shifter

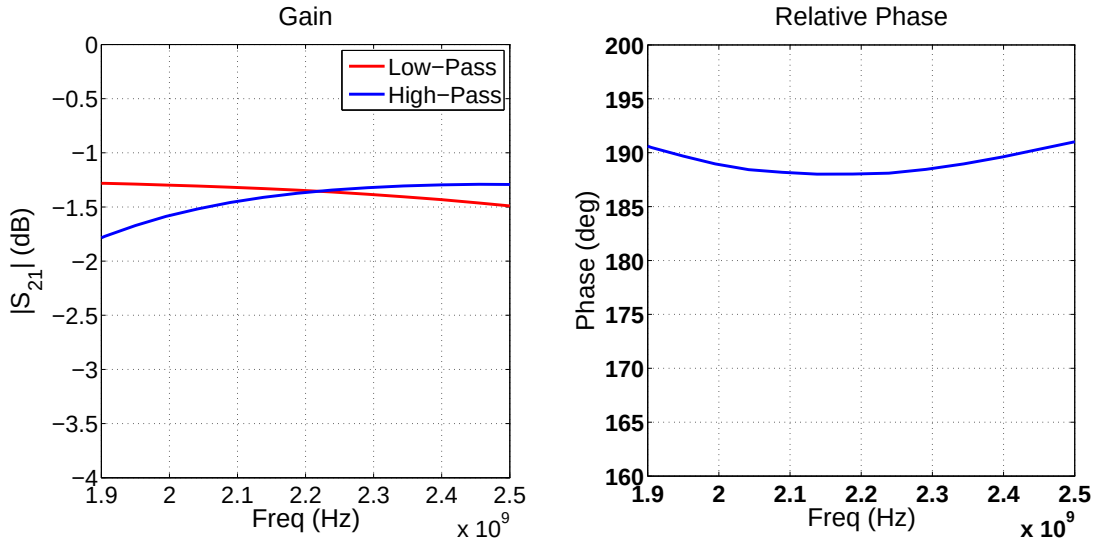

FIGURE 8.9: Simulated gain and phase of the HP/LP 180° phase shifter.

twice that experienced by the auto-transformer design (0.1 ns).

8.1.2 Tunable 45° Phase Shift Block

Fig. 8.10 shows a two stage low-pass π network with switched capacitor arrays, similar to the previous 9-bit phase shifter. Using two stages enables operation well below the cut-off frequency, since each stage has to provide only 22.5° variable phase shift,

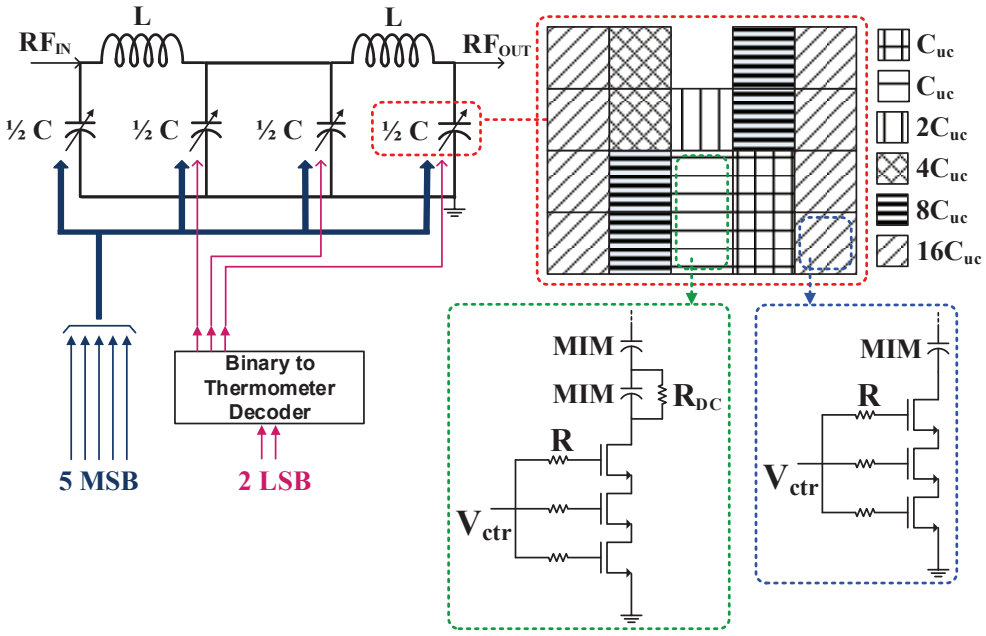

FIGURE 8.10: Schematic of the tunable phase shift block, and layout of the capacitor array

compared to 36° for the previous circuit. To obtain higher resolution, a smaller unit capacitor is required for the LSB. This was realized by a series connection of two minimum MIM capacitors, as shown in Fig. 8.10.

Power handling of the switches is increased by stacking three MOS transistors. The sizes were optimized considering the trade-off between C_{ON}/C_{OFF} and Q_{ON}. The $C/2$ capacitor bank, is a 5-bit binary weighted array with an extra LSB cell. Similar to the proposed control method of the 9-bit phase shifter, this extra LSB cell is individually controlled to increase the resolution by 2-bit, making the overall resolution 7-bit. The capacitor banks are thus controlled simultaneously for 5-MSB, while 2-LSBs control the LSB cells in the three capacitor banks individually.

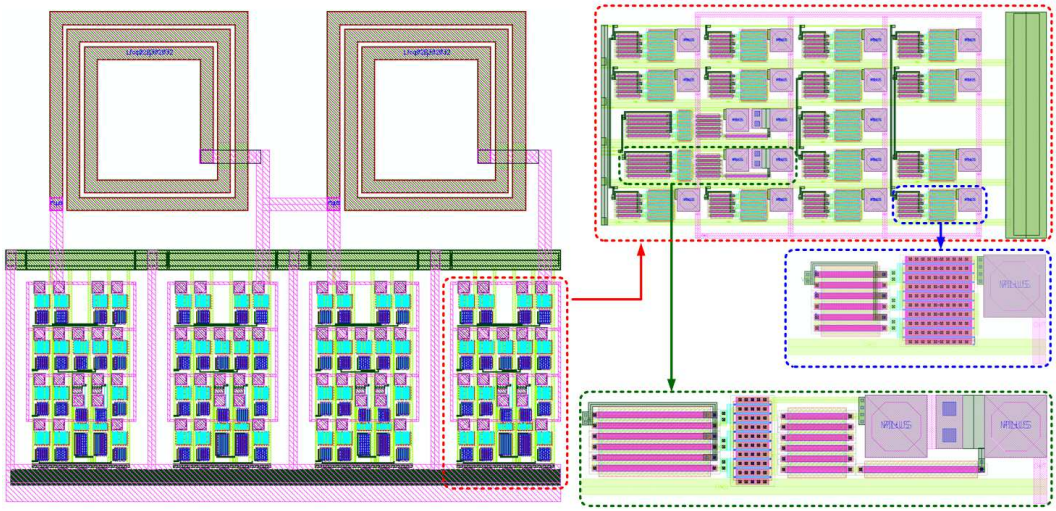

FIGURE 8.11: Layout of the tunable phase shift block, and layout of the capacitor array

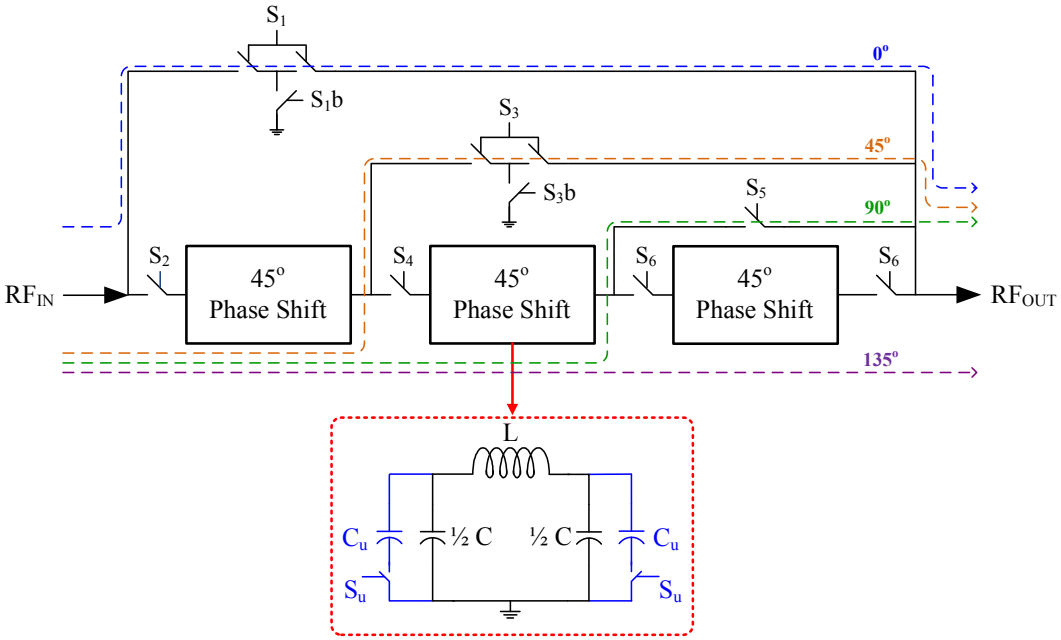

FIGURE 8.12: Block diagram of the switched phase stage.

8.1.3 Fixed 45° Phase Shift Block

The common topologies for realizing a 45° phase shift are switched networks, typically employing three inductors [43],[44]. In this block our main focus is on reducing the chip area, therefore, a low-pass π network was used to achieve 45° phase shift at 2 GHz, requiring just one inductor. As stated earlier (Eq. 7.2), the phase shift from a π

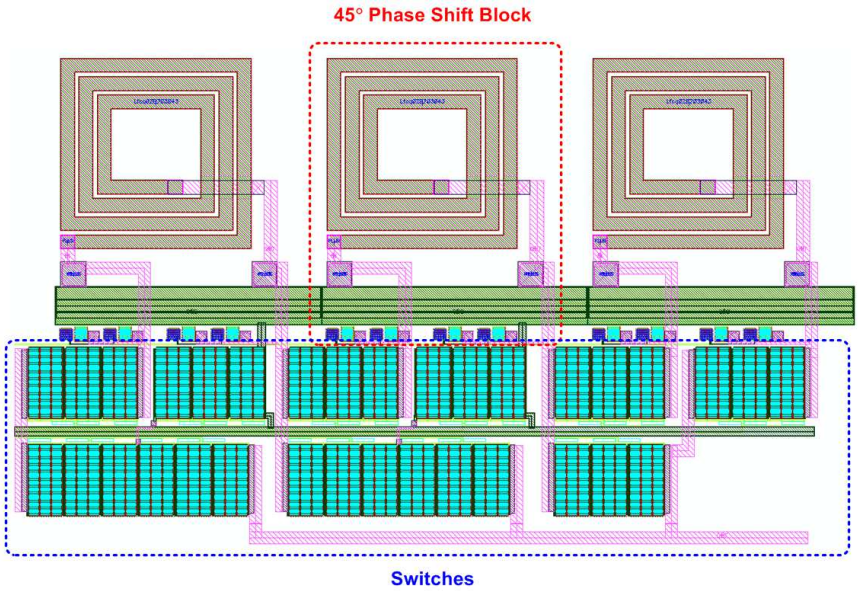

FIGURE 8.13: Layout of the switched phase stage.

circuit is frequency dependent. In order to boost the phase shift at lower frequencies, two small switched capacitors, C_u, are therefore added to each block, controlled by an individual control line, S_u, (Fig. 8.12). An advantage of using switched 45° phase shift blocks is that the absolute phase of the block is used, while in the tunable configuration of the previous device the differential phase shift was used, forcing the operation closer to the cut-off point with increased losses.

The circuit is sensitive to leakage through the switches. In particular, the bypass switches must have good 'OFF' isolation to stop non-phase shifter components from pulling the output signal's phase and altering its amplitude. A grounded switch topology is therefore employed on the more critical switches (S_1 and S_3 in Fig. 8.12).

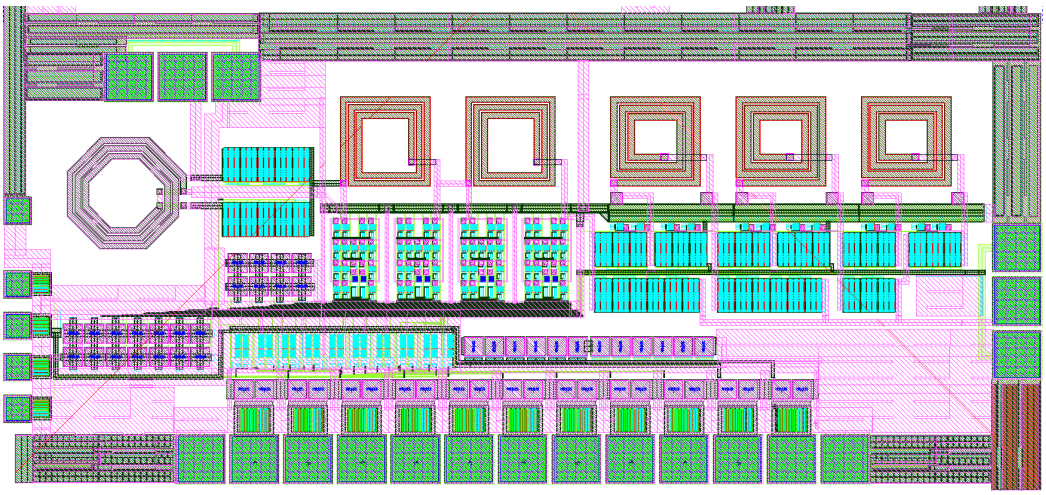

FIGURE 8.14: Final Layout of the 10-bit phase shifter.

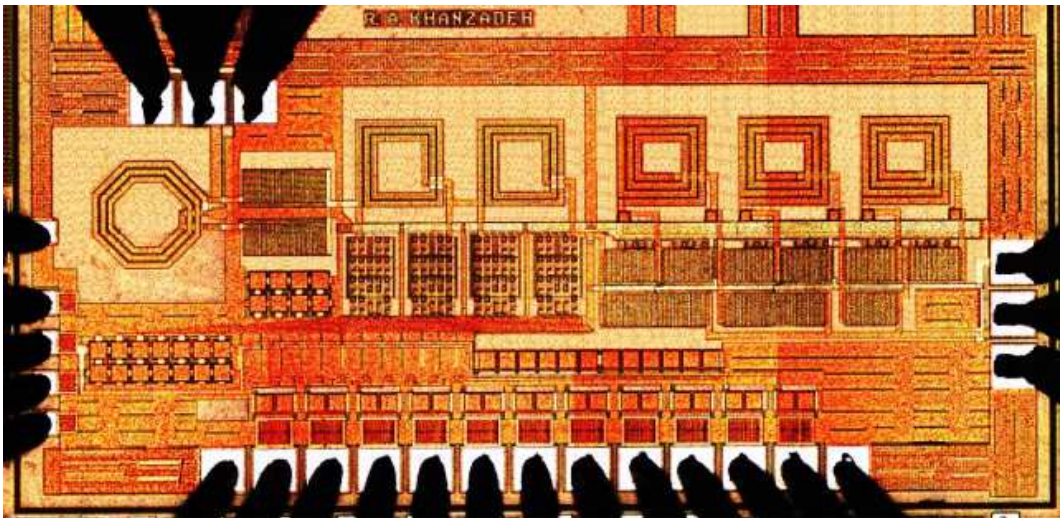

FIGURE 8.15: Chip photo of the 10-bit phase shifter.

8.2 Measurement Results

The device used the same technology as the previous circuit and had an area of 3.4 mm^2 (Fig. 8.15). Excluding pads the area is 1.95 mm^2, a reduction of about 50% on the previous circuit. The circuit was measured using GSG microprobes for the RF input/output pads, and DC probes supplied the digital control signals. The device had a minimum IL of 2.9 dB to 3.2 dB for the zero phase setting; see the top trace of Fig. 8.16.

The auto-transformer provides 180° phase shift for an additional insertion loss of

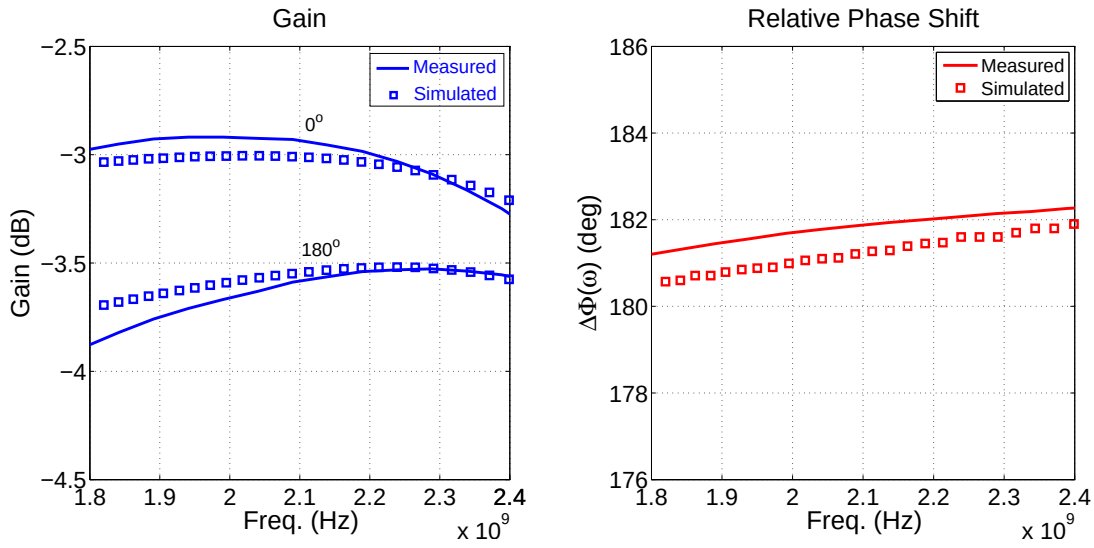

FIGURE 8.16: Measured and simulated gain and relative phase of 180° phase shift block.

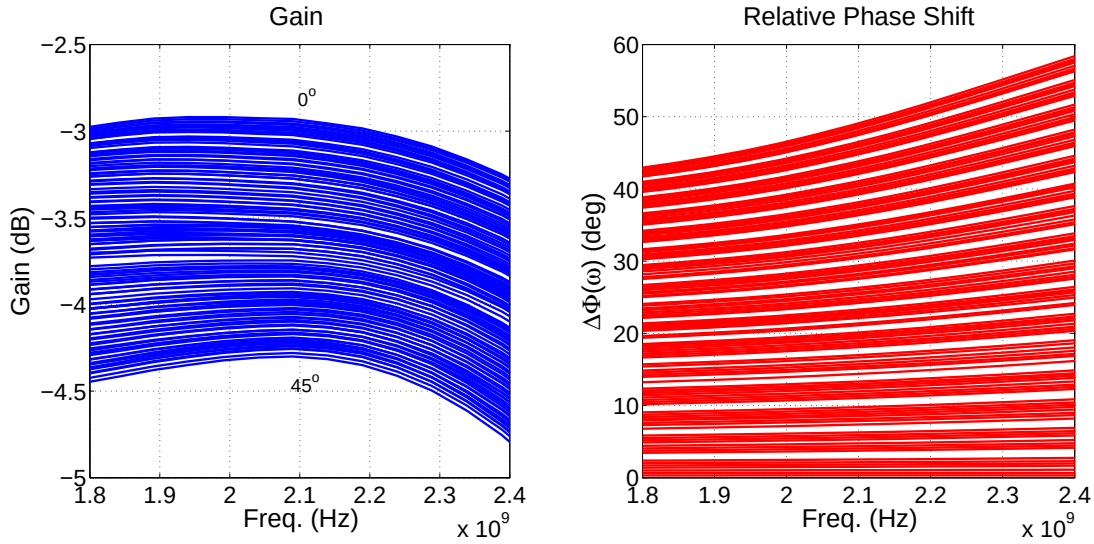

FIGURE 8.17: Measured gain and relative phase of the tunable phase shift block (7-LSB).

0.75 dB at 2 GHz (Fig. 8.16). It should be possible to reduce this loss variation by using asymetric switches, that is , using a smaller device width for the '0°' switch and a bigger device width for the '180°' switch, without changing the total switch area. This will increase the insertion loss in '0°' state and decrease it in '180°' sate. There is also a 1.5° phase offset in the '180°' state, which can be easily compensated by a slightly extended control range in the tunable phase block.

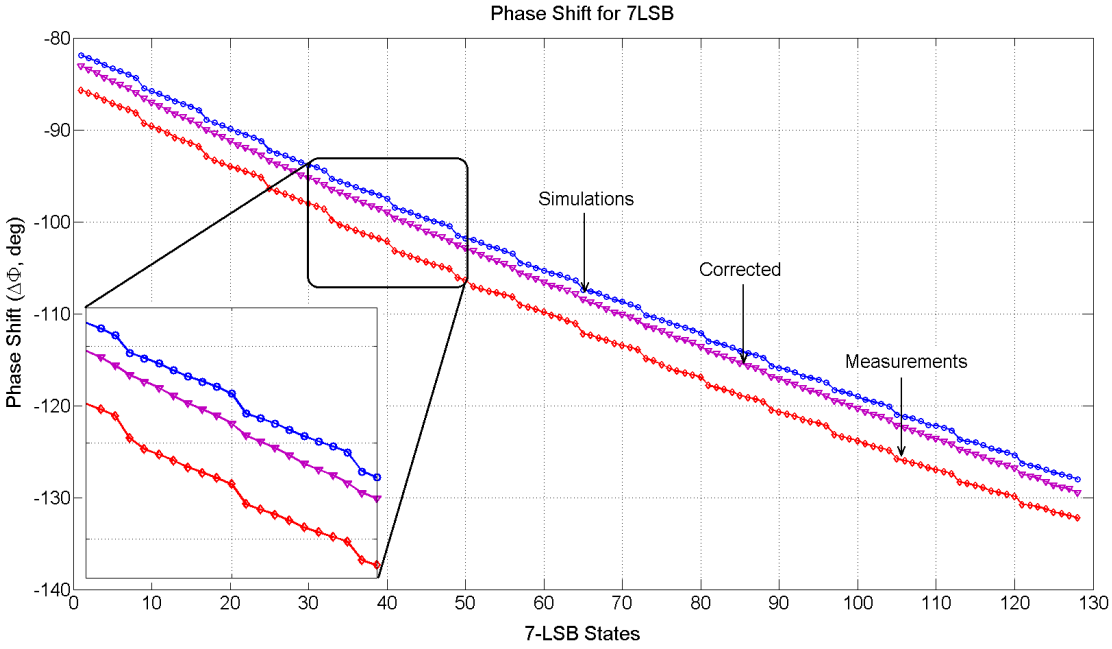

FIGURE 8.18: Measured and simulated phase variation over 7-LSB.

Measured gain and phase shifts for the 7-bit tunable block are shown in Fig. 8.17. The gain variation over the frequency and phase range is about 1.5 dB, and the phase control range is $\Delta\phi(\omega) = 49°$ at the center frequency of 2.1 GHz. Fig. 8.18 shows the measured and simulated phase variation for 7-LSB. There is a fixed phase offset between the measured and simulated results, but the phase steps have excellent agreement, even the jumps occurring every eighth state are predicted by the simulation. This indicates the correctable nature of the problem, which is caused by the changeover between the smaller unit capacitor and the standard unit capacitor. According to simulations, increasing the smaller unit cell by 15% corrected the problem as shown by the middle trace (Fig. 8.18). The average measured phase step size at 2.1 GHz is 0.38°, which is close to the theoretical value of 0.37°, however, the jumps occurring every eighth step cause a standard deviation of 0.26° over the adjustment range, which would improve to 0.11° with the correction.

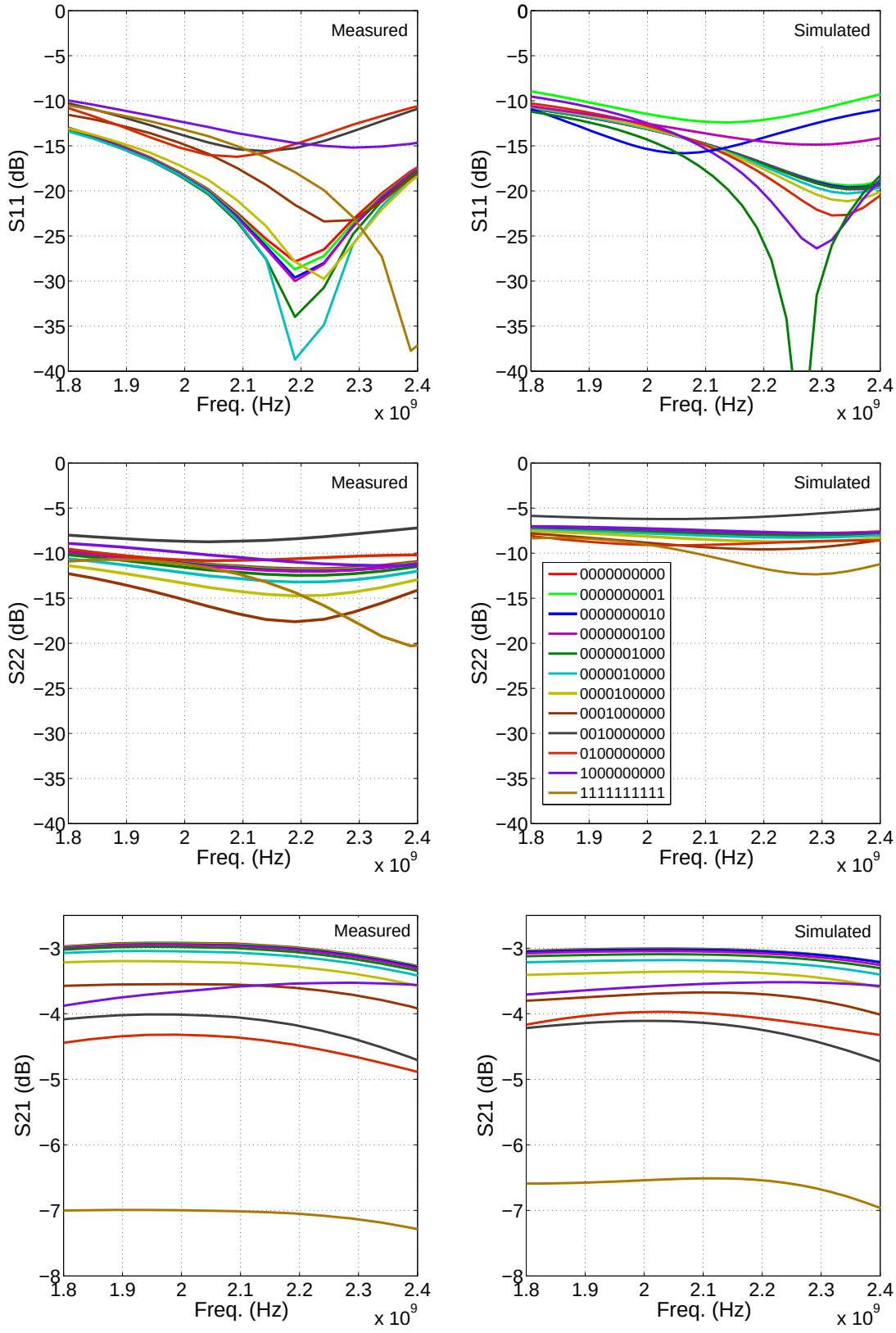

FIGURE 8.19: Measured and simulated S_{11}, S_{22}, and S_{21} for each bit of the control word.

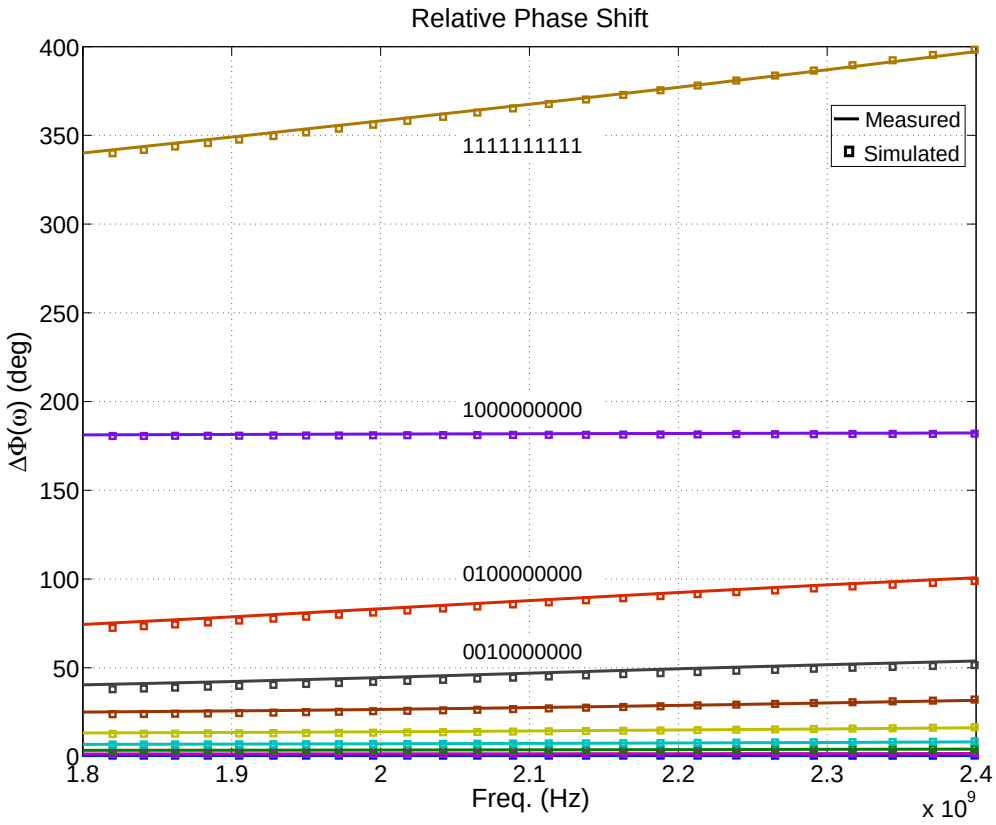

FIGURE 8.20: Measured and simulated phase shift relative to the 'All OFF' state (0000000000).

Fig. 8.19 shows the measured and simulated input/output return loss and insertion loss of the 10 phase control bits over the frequency range of 1.8 GHz to 2.4 GHz. Also, the maximum/minimum phase shift states are included. The input return loss is better than 10 dB and the output return loss is better than 7 dB. As expected, the IL is highest at the maximum phase shift (all bits ON), which is less than 7.3 dB over the entire frequency range. The measured and simulated relative phase shifts are shown in Fig. 8.20. The phase shift curves ($\Delta\Phi(\omega)$) from the top are for control words of (1111111111, 1000000000, 0100000000, 0010000000, ..., 0000000001), respectively. Two fixed phase stages (45°) are combined to give 90° phase shift for the 0100000000 control word.

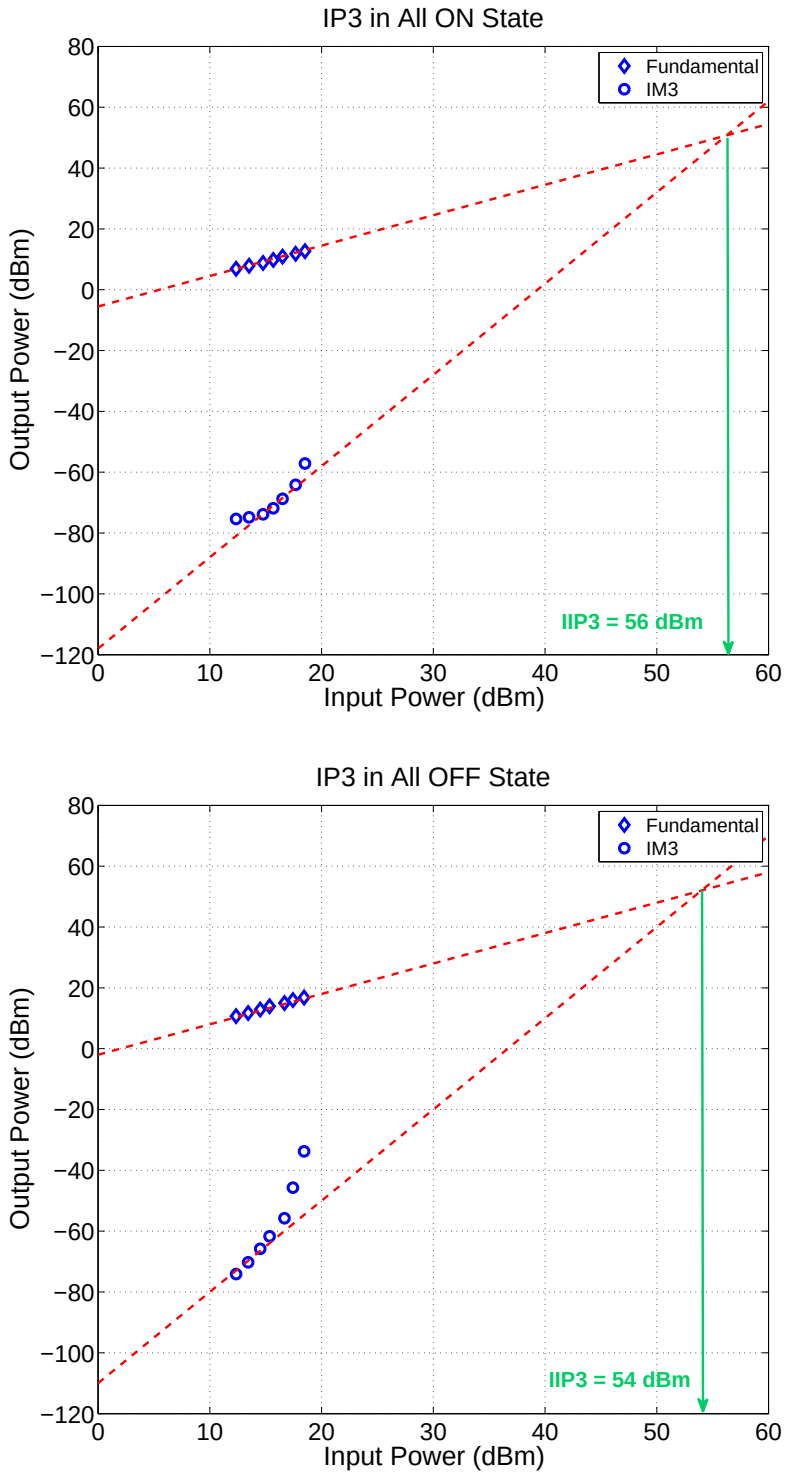

FIGURE 8.21: Measured IIP_3; 'All ON' (maximum phase shift) and 'All OFF' (minimum phase shift) states.

A respectable IIP_3 of 54 dBm for the all switches in 'OFF' state (minimum phase

shift) and 56 dBm for the all switches in 'ON' state (maximum phase shift) was measured by a two tone test (with 2 MHz spacing and using the measurement set up shown in Fig. 7.9). Fig. 8.21 shows the IP_3 measurement results. The obtained IIP_3 is 19 dB better than the adaptive duplexer specifications (refer to Subsection 4.2.2), implying that the number of stacked devices in the switch can be reduced from three to two.

8.3 Summary

The nominal 10-bit phase shifter, reported in this chapter, has high linearity and the highest reported resolution to date. High linearity is achieved by using stacked switches and high resolution is obtained by employing switched capacitor arrays. The 10-bit device has an insertion loss of 7.3 dB in the frequency range of 1.8 GHz to 2.4 GHz. The chip area is reduced to 3.4 mm^2 by employing an auto-transformer to obtain 180° phase shift. A respectable IIP_3 of 55±1 dBm is measured. The measured phase resolution of 0.38°/step with standard deviation of 0.ll° is equivalent to 9-bit resolution (@ worst case error of 3σ). This is enough to give an improved 35 dB isolation from the cancelling loop in the adaptive duplexer.

The next chapter provides a summary of the measurement results for both devices and compares the performance of the devices with state of the art published work and commercial devices.

Chapter 9

Conclusion

The cancelling loop in an adaptive duplexer requires precise gain and phase control. We show theoretically that a phase resolution of better than 1.15°, or approximately 9-bit, is needed for 35 dB loop isolation. Two digitally controlled phase shifters are developed for this purpose based on transmission line sections. The 9-bit and 10-bit devices implemented in the Peregrine SOS 0.25 μm GC process have high linearity and the highest reported resolution to date. Both devices use switched capacitor arrays for fine adjustments and stacked switches for better large signal performance. The 10-bit device has reduced insertion loss (0.76 dB/bit) and area (3.4 mm^2) by employing an auto-transformer to obtain 180° phase shift. The device out-performs GaAs devices in terms of linearity, area, and resolution, but under-performs in terms of bandwidth and gain variation.

Both devices presented in this thesis use switched capacitor arrays to obtain fine and predictable adjustments due to good matching of the capacitor cells. However the

many small unit cells in the array require interconnections that are a source of parasitic leakage. The $R_{ON} \times C_{OFF}$ figure of merit is therefore poor and results in a higher IL for a given tuning range. The second design reduces the number of tunable sections which enables a reduction in the IL and size, but still provides the required fine resolution. The fixed phase shift stages do not require the high accuracy implied by 10-bit resolution, as the error can be covered by slightly increasing the tuning range of the tunable stage.

A comparison of state-of-the-art published works and products is given in Table 9.1. In comparison with the silicon based circuits, our designs are larger, but provide higher resolution and power handling. Paper [37] also provides fine adjustments and has a very small size, but the frequency band is much higher (22-26GHz) and a DAC would be needed for control. Our 9-bit design has comparable IL to all three Si devices, but our 10-bit device has an IL that is at least 2dB lower, even when taking the worst case value of 5.1+2.2=7.3 dB. A potential problem for some applications is the large gain variation (±2.2 dB) over the phase control range which might need compensation. This is not a problem for situations (such as adaptive duplexing) where a gain control element is needed in any case.

GaAs circuits are more competitive with an increased operational bandwidth and up to 3 dB less IL than the 10-bit device. Their resolution is however limited to between 4 and 6 bits. Since every additional bit involves the signal incurring additional losses as it is switched into the appropriate network, it might be more appropriate to use IL per bit as a comparison measure (column 5 in Table 9.1). On this basis the 10-bit device has the same IL/bit (0.76 dB/bit) as the best of the GaAs devices [43], but achieves this with lower chip area and higher IIP_3. In fact, the 10-bit device outperforms all the

listed GaAs devices in terms of IIP_3 and all except for the 4-bit resolution device [42] in terms of chip area.

9.1 Future Work

The future work involves further improvement of the phase shifter device, and also design and implementation of the gain adjuster component of the cancelling loop. Improvement of the phase shifter can be listed as below:

- Reducing the gain variation with phase shift
- Decreasing the size and insertion loss of the phase shifter
- Improving the phase step standard deviation
- Considering alternative structures for gain/phase adjustments

TABLE 9.1: Performance Comparison

	No. of Bits	Frequency (GHz)	IL (dB)	IL/bit (dB)	IIP_3 (dBm)	Size mm^2	Technology	Topology
[37]	analog	22-26	15.3±0.8	-	28	0.44	0.18 μm CMOS	VS
[44]	6	2.5-3.2	13 *	2.16 *	27§	3.1**	0.18 μm CMOS	SN
[73]	4	11.6-12.6	9±0.5 *	2.25±0.12*	7§	1.72	0.18 μm RF CMOS	STL
9-bit PS	**> 8.1**	**1.4-1.7**	**9.3±3.3**	**1.15±0.4**	**40±1**	**5.94**	**0.25 μm SOS**	**SCTL**
10-bit PS	**> 9.6**	**1.8-2.4**	**5.1±2.2**	**0.53±0.23**	**55±1**	**3.4**	**0.25 μm SOS**	**SN**
[42]	4	1.4-2.4	3.8±0.4	0.95±0.1	32	2.6	0.4 μm GaAs	SN
[43]	6	1.4-2.4	3.8±0.8	0.63±0.13	-	3.8	0.5 μm GaAs pHEMT	SN
[74]	6	3.6-4.2	<6.4	<1.07	23	7.8	0.25 μm GaAs pHEMT	SN
M/A-COM MAPS-011007	6	1.2-1.4	3.8±1.6	0.63±0.26	48	-	GaAs pHEMT	-

*Exclude amplification, **Estimated based on the presented die photo, §Estimated based on 1-dB compression point
VS:Vectro-Sum, SN:Switched Network, VLTL:Varactor Loaded Transmission Line, STL:Switched TL, SCTL:Switched Capacitor TL

References

[1] [Online]. Available: http://www.3gpp.org/about-3gpp/about-3gpp

[2] S. Kannangara and M. Faulkner, "Analysis of an adaptive wideband duplexer with double-loop cancellation," *IEEE Trans. Veh. Technol.*, vol. 56, no. 4, pp. 1971–1982, July 2007.

[3] S. Kannangara, "Adaptive Duplexer For Software Radio," Ph.D. dissertation, Victoria Univ., Melbourne, Australia, 2006.

[4] B. Razavi, *RF Microelectronics*. Upper Saddle river, NJ:Prentice Hall, 1998.

[5] G. T. S. 36.101, "Evoluved Universal Terrestrial Radio Access (E-UTRA); User Equipment (UE) Radio Transmission and Reception." [Online]. Available: http://www.3gpp.org

[6] G. T. S. 36.104, "Evoluved Universal Terrestrial Radio Access (E-UTRA); Base Station (BS) Radio Transmission and Reception." [Online]. Available: http://www.3gpp.org

[7] S. Sesia, I. Toufik, and M. Baker, *LTE - The UMTS Long Term Evolution: From Theory to Practice*. Wiley, 2011. [Online]. Available: http://books.google.com.au/books?id=VF8MmzlcIKMC

[8] G. Kenworthy, "Self-cancelling full-duplex rf communication system," Nov. 25 1997, uS Patent 5,691,978. [Online]. Available: http://www.google.com/patents/US5691978

[9] S. Chen, M. Beach, and J. McGeehan, "Division-free duplex for wireless applications," *Electronics Letters*, vol. 34, no. 2, pp. 147–148, Jan 1998.

[10] M. Jain, J. I. Choi, T. Kim, D. Bharadia, S. Seth, K. Srinivasan, P. Levis, S. Katti, and P. Sinha, "Practical, real-time, full duplex wireless," in *Proceedings of the 17th Annual International Conference on Mobile Computing and Networking*, ser. MobiCom '11. New York, NY, USA: ACM, 2011, pp. 301–312. [Online]. Available: http://doi.acm.org/10.1145/2030613.2030647

[11] D. Bharadia, E. McMilin, and S. Katti, "Full duplex radios," *SIGCOMM Comput. Commun. Rev.*, vol. 43, no. 4, pp. 375–386, Aug. 2013. [Online]. Available: http://doi.acm.org/10.1145/2534169.2486033

[12] Y.-S. Choi and H. Shirani-Mehr, "Simultaneous transmission and reception: Algorithm, design and system level performance," *Wireless Communications, IEEE Transactions on*, vol. 12, no. 12, pp. 5992–6010, December 2013.

[13] D. Bharadia and S. Katti, "Full duplex mimo radios," *Proc. of 11th USENIX Conf. NSDI* , p. 359–372, Apr. 2014.

[14] J. McGeehan, A. Bateman, M. Beach, P. Kenington, and W. Slingsby, "Full-duplex radio transmitter/receiver," May 8 2001, uS Patent 6,229,992. [Online]. Available: http://www.google.com/patents/US6229992

[15] T. O'Sullivan, R. York, B. Noren, and P. Asbeck, "Adaptive duplexer implemented using feedforward technique with a bst phase shifter," in *Microwave Symposium Digest, 2004 IEEE MTT-S International*, vol. 3, June 2004, pp. 1299–1302 Vol.3.

[16] Y.-C. Jeong, J.-S. Park, D. Ahn, and J.-B. Lim, "A Rx cancellation loop configuration for power amplifier module," in *Microwave Conference, 2001. APMC 2001. 2001 Asia-Pacific*, vol. 3, 2001, pp. 1199–1202, vol. 3.

[17] Y.-C. Jeong, "A feedforward power amplifier with loops to reduce Rx band noises and intermodulation distortion," *Microwave J.*, vol. 45, no. 1, pp. 80-91, 2001.

[18] W. Schacherbauer, A. Springer, T. Ostertag, C. Ruppel, and R. Weigel, "A flexible multiband frontend for software radios using high if and active interference cancellation," in *Microwave Symposium Digest, 2001 IEEE MTT-S International*, vol. 2, May 2001, pp. 1085–1088 vol.2.

[19] J. Serraicco, "Compact phase-shifter deign using barium strontium titanate thin-film varactors," Master's thesis, University of California Santa Barbara, 2003.

[20] B. Sundaram and P. Shastry, "A novel electronically tunable active duplexer for wireless transceiver applications," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 54, no. 6, pp. 2584–2592, June 2006.

[21] J. Beyer, S. Prasad, R. Becker, J. Nordman, and G. Hohenwarter, "Mesfet distributed amplifier design guidelines," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 32, no. 3, pp. 268–275, Mar 1984.

[22] A. Roussel, C. Nicholls, and J. Wight, "Frequency agile rf feedforward noise cancellation system," in *Radio and Wireless Symposium, 2008 IEEE*, Jan 2008, pp. 109–112.

[23] C. Nicholls and A. Roussel, "Adaptive feedforward noise cancellation circuit," Oct. 7 2004, uS Patent App. 10/185,118. [Online]. Available: http://www.google.com/patents/US20040198295

[24] A. Roussel, "Feedforward interference cancellation system applied to the 800 mhz cdma cellular band," Master's thesis, Carleton University, 2003.

[25] A. Frotzscher and G. Fettweis, "A stochastic gradient lms algorithm for digital compensation of tx leakage in zero-if-receivers," in *Vehicular Technology Conference, 2008. VTC Spring 2008. IEEE*, May 2008, pp. 1067–1071.

[26] V. Aparin, G. Ballantyne, C. Persico, and A. Cicalini, "An integrated lms adaptive filter of tx leakage for cdma receiver front ends," *Solid-State Circuits, IEEE Journal of*, vol. 41, no. 5, pp. 1171–1182, May 2006.

[27] S. Kannangara and M. Faulkner, "Adaptive duplexer for multiband transreceiver," in *Radio and Wireless Conference, 2003. RAWCON '03. Proceedings*, Aug 2003, pp. 381–384.

[28] C. Berrou, A. Glavieux, and P. Thitimajshima, "Near shannon limit error-correcting coding and decoding: Turbo-codes. 1," in *Proc. IEEE Int. Conf. Communications, Technical Program*, vol. 2, May 1993, pp. 1064–1070.

[29] B. Lu, X. Wang, and K. Narayanan, "LDPC-based space-time coded OFDM systems over correlated fading channels: Performance analysis and receiver design," *IEEE Trans. Communications*, vol. 50, no. 1, pp. 74–88, Jan 2002.

[30] K.-J. Koh and G. Rebeiz, "0.13-μm cmos phase shifters for x-, ku-, and k-band phased arrays," *Solid-State Circuits, IEEE Journal of*, vol. 42, no. 11, pp. 2535–2546, Nov 2007.

[31] N. Joram, U. Mayer, R. Eickhoff, and F. Ellinger, "Fully integrated active cmos vector modulator for 802.11a compliant diversity transceivers," in *Microwaves, Communications, Antennas and Electronics Systems, 2009. COMCAS 2009. IEEE International Conference on*, Nov 2009, pp. 1–4.

[32] F. Ellinger, U. Lott, and W. Bachtold, "An antenna diversity mmic vector modulator for hiperlan with low power consumption and calibration capability," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 49, no. 5, pp. 964–969, May 2001.

[33] F. Ellinger and W. Bachtold, "Novel principle for vector modulator-based phase shifters operating with only one control voltage," *Solid-State Circuits, IEEE Journal of*, vol. 37, no. 10, pp. 1256–1259, Oct 2002.

[34] A. Asoodeh and M. Atarodi, "A 6-bit active digital phase shifter," *IEICE Electronics Express*, vol. 8, no. 3, pp. 121–128, 2011.

[35] A. Asoodeh and M. Atarodi, "A full 360° vector-sum phase shifter with very low rms phase error over a wide bandwidth," *IEEE Trans. Microw. Theory Tech.*, vol. 60, no. 6, pp. 1626–1634, June 2012.

[36] F. Ellinger, R. Vogt, and W. Bachtold, "A high yield ultra small passive vector modulator based phase shifter for smart antenna combining at c-band," in *Microwave Conference, 2000 Asia-Pacific*, 2000, pp. 794–798.

[37] C.-W. Wang, H.-S. Wu, and C.-K. Tzuang, "CMOS passive phase shifter with group-delay deviation of 6.3 ps at k-band," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 7, pp. 1778–1786, July 2011.

[38] F. Ellinger, H. Jäckel, and W. Bächtold, "Varactor-loaded transmission-line phase shifter at C-band using lumped elements," *IEEE Trans. Microw. Theory Tech.*, vol. 51, no. 4, pp. 1135–1140, Apr 2003.

[39] J. Wagner, U. Mayer, and F. Ellinger, "Passive transmission line phase shifter at C-band in CMOS using lumped elements," in *Proc. 17th Int. Conf. Microw., Radar and Wireless Communications*, May 2008, pp. 1–4.

[40] D.-W. Kang, H. D. Lee, C.-H. Kim, and S. Hong, "Ku-band MMIC phase shifter using a parallel resonator with 0.18-μm CMOS technology," *IEEE Trans. Microw. Theory Tech.*, vol. 54, no. 1, pp. 294–301, Jan 2006.

[41] C. Campbell and S. Brown, "A compact 5-bit phase shifter MMIC for K-band satellite communication systems," in *Proc. IEEE Int. Microw. Symp. Dig.*, vol. 1, June 2000, pp. 217–220.

[42] I. Bahl and D. Conway, "L- and S-band compact octave bandwidth 4-bit MMIC phase shifters," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 2, pp. 293–299, Feb 2008.

[43] Q. Xiao, "A compact L-band broadband 6-bit MMIC phase shifter with low phase error," in *Proc. European Microw. Integrated Circuits Conf.*, Oct 2011, pp. 410–413.

[44] M. Meghdadi, M. Azizi, M. Kiani, A. Medi, and M. Atarodi, "A 6-bit CMOS phase shifter for S-band," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 12, pp. 3519–3526, Dec 2010.

[45] G. Rebeiz and K.-J. Koh, "Silicon rfics for phased arrays," *Microwave Magazine, IEEE*, vol. 10, no. 3, pp. 96–103, May 2009.

[46] T. Yu and G. Rebeiz, "A 22 - 24 ghz 4-element cmos phased array with on-chip coupling characterization," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 9, pp. 2134–2143, Sept 2008.

[47] K.-J. Koh, J. May, and G. Rebeiz, "A millimeter-wave (40 - 45 ghz) 16-element phased-array transmitter in 0.18-μ m sige bicmos technology," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 5, pp. 1498–1509, May 2009.

[48] K.-J. Koh and G. Rebeiz, "An x- and ku-band 8-element phased-array receiver in 0.18-μm sige bicmos technology," *Solid-State Circuits, IEEE Journal of*, vol. 43, no. 6, pp. 1360–1371, June 2008.

[49] F. Ellinger and W. Bachtold, "Adaptive antenna receiver module for wlan at c-band with low-power consumption," *Microwave and Wireless Components Letters, IEEE*, vol. 12, no. 9, pp. 348–350, Sept 2002.

[50] F. Ellinger, R. Vogt, and W. Bachtold, "Calibratable adaptive antenna combiner at 5.2 ghz with high yield for laptop interface card," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 48, no. 12, pp. 2714–2720, Dec 2000.

[51] F. Ellinger, U. Mayer, M. Wickert, N. Joram, J. Wagner, R. Eickhoff, I. Santamaria, C. Scheytt, and R. Kraemer, "Integrated adjustable phase shifters," *Microwave Magazine, IEEE*, vol. 11, no. 6, pp. 97–108, Oct 2010.

[52] H. Hayashi, M. Muraguchi, Y. Umeda, and T. Enoki, "A high-q broad-band active inductor and its application to a low-loss analog phase shifter," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 44, no. 12, pp. 2369–2374, Dec 1996.

[53] F. Ellinger, R. Vogt, and W. Bachtold, "Ultra compact, low loss, varactor tuned phase shifter mmic at c-band," *Microwave and Wireless Components Letters, IEEE*, vol. 11, no. 3, pp. 104–105, March 2001.

[54] M. Tabesh, J. Chen, C. Marcu, L. Kong, S. Kang, A. Niknejad, and E. Alon, "A 65 nm cmos 4-element sub-34 mw/element 60 ghz phased-array transceiver," *Solid-State Circuits, IEEE Journal of*, vol. 46, no. 12, pp. 3018–3032, Dec 2011.

[55] M. Tabesh, A. Arbabian, and A. Niknejad, "60ghz low-loss compact phase shifters using a transformer-based hybrid in 65nm cmos," in *Custom Integrated Circuits Conference (CICC), 2011 IEEE*, Sept 2011, pp. 1–4.

[56] M. Hangai, M. Hieda, N. Yunoue, Y. Sasaki, and M. Miyazaki, "S - and c -band ultra-compact phase shifters based on all-pass networks," *IEEE Trans. Microw. Theory Tech.*, vol. 58, no. 1, pp. 41–47, Jan 2010.

[57] E. Taniguchi, M. Hieda, H. Kurusu, M. Funada, Y. Iyama, and T. Takagi, "A ku-band matched embedded-fet phase shifter," in *Microwave Conference, 1999. 29th European*, vol. 2, Oct 1999, pp. 357–360.

[58] E. Culurciello, *Silicon-on-Sapphire Circuits and Systems*. McGraw Hill, 2010.

[59] G. Imthurn, "The history of silicon-on-sapphire," *http://www.psemi.com/articles/History_SOS_73-0020-02.pdf*, Sep 2013.

[60] Peregrine Semiconductor Corp., "UltraCMOS® technology-the ultimate SOI," Apr 2014. [Online]. Available: http://www.psemi.compdf/sell_sheet-psg/DOC-35245-2web.pdf

[61] Peregrine Semiconductor Corp., "UltraCMOS™ 0.5um design manual." [Online]. Available: http://www.psemi.com/content/ultracmos/ultracmos_process_tech.html

[62] Peregrine Semiconductor Corp., "Ugx rev. 1.9 UltraCMOS™ 0.25um spice models." [Online]. Available: http://www.psemi.com/content/ultracmos/ultracmos_process_tech.html

[63] R. Amirkhanzadeh, H. Sjöland, A. Tikka, and M. Faulkner, "Comparative analysis of switching performance of transistors in SOS process for RF applications," in *Proc. IEEE Asia Pacific Circuits Syst.*, Dec 2010, pp. 1111–1114.

[64] R. Johnson, P. R. De La Houssaye, C. Chang, P.-F. Chen, M. Wood, G. A. Garcia, I. Lagnado, and P. Asbeck, "Advanced thin-film silicon-on-sapphire technology: microwave circuit applications," *Electron Devices, IEEE Transactions on*, vol. 45, no. 5, pp. 1047–1054, May 1998.

[65] J. Jeong, S. Pornpromlikit, P. Asbeck, and D. Kelly, "A 20 dBm linear RF power amplifier using stacked silicon-on-sapphire MOSFETs," *Microwave and Wireless Components Letters, IEEE*, vol. 16, no. 12, pp. 684–686, Dec 2006.

[66] R. Johnson, C. Chang, P. Asbeck, M. Wood, G. Garcia, and I. Lagnado, "Comparison of microwave inductors fabricated on silicon-on-sapphire and bulk silicon," *Microwave and Guided Wave Letters, IEEE*, vol. 6, no. 9, pp. 323–325, Sep 1996.

[67] D. M. Pozar, *Microwave Engineering*, 3rd ed. Hoboken, NJ : John Wiley, 2005.

[68] B. Baxter, T. Ranta, M. Facchini, D. Jung, and D. Kelly, "The state-of-the-art in Silicon-On-Sapphire components for antenna tuning," in *Proc. IEEE Int. Microw. Symp. Dig.*, June 2013, pp. 1–4.

[69] H. Gan, "On-chip transformer modeling, characterization, and applications in power and low noise amplifiers," Ph.D. dissertation, Stanford Univ., Stanford, CA, Mar. 2006.

[70] S. S. Mohan, "The design, modeling, and optimization of on-chip inductor and transformer circuits," Ph.D. dissertation, Stanford Univ., Stanford, CA, Dec. 1999.

[71] J. Long, "Monolithic transformers for silicon rf ic design," *Solid-State Circuits, IEEE Journal of*, vol. 35, no. 9, pp. 1368–1382, 2000.

[72] O. El-Gharniti, E. Kerherve, and J.-B. Begueret, "Modeling and characterization of on-chip transformers for silicon RFIC," *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 4, pp. 607–615, 2007.

[73] D.-W. Kang and S. Hong, “A 4-bit CMOS phase shifter using distributed active switches,” *IEEE Trans. Microw. Theory Tech.*, vol. 55, no. 7, pp. 1476–1483, July 2007.

[74] X. Yang and J. Shi, “C-band 6-bit phase shifter for a phase array antenna,” *J. Semiconductors*, vol. 34, no. 4, Apr 2013.