A TUNABLE LOW-ISOLATION DEVICE FOR ADAPTIVE DUPLEXERS

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Doctor of Philosophy

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To my loving parents

and

my dearest love, Sara

Doctor of Philosophy Declaration

I, Mohammadreza Pourakbar, declare that the Ph.D thesis entitled "A TUNABLE LOW-ISOLATION DEVICE FOR ADAPTIVE DUPLEXERS" is no more than 100,000 words in length including quotes and exclusive of tables, figures, appendices, bibliography, references and footnotes. This thesis contains no material that has been submitted previously, in whole or in part, for the award of any other academic degree or diploma. Except where otherwise indicated, this thesis is my own work.

Mohammadreza Pourakbar

Date: November 09, 2016

Abstract

Today's fourth generation (4G) long term evolution (LTE) handsets using frequency division duplex operate on two frequencies to provide simultaneous transmission and reception. A duplexer isolates the sensitive receiver (Rx) circuits from the high-power transmitter (Tx) output. The classical duplexer relies on two highly selective filters using surface acoustic wave or thin film bulk acoustic resonator technology. One is placed in the transmitter path to attenuate the Tx noise in the Rx band and another is placed in the receiver path to prevent the large Tx leakage signal from overloading the receiver. These filters have low insertion loss and high linearity, but support only one frequency band, are bulky and cannot be integrated into the receiver microcircuit. A set of duplexers connected to the antenna through an antenna switch is therefore required for multi-band operation, handicapping the radio handset in terms of cost and size. The lack of a tunable duplexer alternative is a major drawback. The current research trend is to make the duplexer frequency agile, adaptive and integrable.

In this thesis, single-band and multi-band integrated solutions of a low-isolation device (LID) are proposed to provide the initial isolation for an adaptive duplexer scheme employing cancelling loops. Firstly, two inductor-capacitor (LC) based single-band tunable duplex filters are designed. The filters cover long-term evolution band 1 in steps using digitally switched capacitor banks with stacked field-effect transistors for voltage handling. Bandpass-bandstop structures are used, and the insertion loss versus isolation trade-off is derived as a function of component quality factor (Q) and impedance level. A fully integrated 0.25-μm Silicon-on-Sapphire solution provides

isolation of 19 dB for the Tx leakage signal and 14 dB for the Tx noise that falls into the receive band. Using off-chip passives on a printed circuit board improves the above isolations to greater than 25 dB, primarily due to increased inductor quality factor (Q). Insertion losses are comparable to hybrid balancing schemes but are still above those of traditional solutions.

Secondly, two multi-band partially-integrated LIDs are evaluated. The first prototype is a quad-band tunable LID, providing the required tuning range for LTE Bands 1,2,3, and 7. The circuit is implemented in a 0.13-μm Silicon-on-Insulator process with off chip printed circuit inductors. Post layout simulations show isolations exceeding 30 dB at both transmit and receive frequencies for each specified LTE band. The insertion loss from the power amplifier output port to antenna port is below 2 dB in LTE band 1. The fabricated circuit occupies an area of $2.0mm \times 1.2mm$. The second prototype using the older 0.25-μm silicon on sapphire process is limited to LTE bands 1,2, and 3. The simulated isolation is well above 20 dB for LTE band 1 and almost 20 dB for the other two bands. Difficulties in flip-chipping the connections meant that testing could not be completed in the available time.

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First of all, I would like to thank Allah for spreading my life with the beauty of knowledge and lighting my heart with the amity of his fourteen Infallible and granting the ability of effort to fulfil my thesis.

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I dedicate my thesis to my dear parents and beloved wife who, despite being thousands of miles away always supported me and encouraged me with unconditional love through this journey. To my dearest sister to whom I will always owe a debt of gratitude for being there for my parents while my pursuit of education had taken me away from them.

Contents

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Abbreviations

1G	First Generation
2G	Second Generation
3G	Third Generation
3GPP	Third-Generation Project Partnership
4G	Fourth Generation
5G	Fifth Generation
ACLR	Adjacent Channel Leakage Ratio
ACS	Adjacent Channel Selectivity
AlN	Aluminium Nitride
ANT	Antenna
ATU	Antenna Tuning Unit
AX	Auxiliary transmitter
BAW	Bulk-Acoustic Wave

BESOI Bonding-and-Etched-back-SOI

BOX Buried Oxide

BPF Band-pass Filter

CA Carrier Aggregation

CC Carrier Component

CDM Charge Device Model

CDMA Code Division Multiple Access

CMOS Complementary Metal-Oxide-Semiconductor

CP Copper Pillar

CR Cognitive Radio

CW Continuous Waveform

DA Distributed Amplifier

DCR Direct Conversion Receiver

DCS Digital Cellular System

DSCB Digitally Switched Capacitor Bank

DSP Digital Signal Processing

DSP Digital Signal Processor

DTC Digitally-Tuned Capacitor

EBD Electrical Balanced Duplexer

EDGE Enhanced Data Rates for GSM Evolution

eNodeB Evolved NodeB

ESD Electrostatic Discharge

EVM Error Vector Magnitude

FBAR Thin-Film Bulk Acoustic Resonator

FDD Frequency Division Duplexing

FDMA Frequency Division Multiple Access

FOM Figure Of Merit

GaAs Gallium Arsenide

Gbps Gigabit per second

GPRS General Packet Radio Service

GSM Global System for Mobile Communications

HBM Human Body Model

HFN High-Frequency Network

HR-SOI High-Resistivity SOI

HSCSD High Speed Circuit Switched Data

HSPA High Speed Packet Access

HT Hybrid Transformer

IC Integrated Circuit

IL Insertion Loss

IMD Intermodulation Distortion

ISO Isolation

ITU International Telecommunication Union

ITU-R International Telecommunication Union-Radiocommunication Sector

LFN Low-Frequency Network

LID Low-Isolation Device

LMS Least-Mean Square

LNA Low Noise Amplifier

LTE Long Term Evolution

LTE-A Long Term Evolution-Advanced

LUT Look-Up Table

M2M Machine-to-Machine

Mbps	Megabit per second
MESFET	Metal-Semiconductor Field-Effect Transistor
MIM	Metal-Insulator-Metal capacitor
MM	Machine Model
MMIC	Monolithic Microwave Integrated Circuit
MMS	Multimedia Messaging Service
MPW	Multi-Project Wafer
OFDMA	Orthogonal Frequency-Division Multiple Access
OOB	Out-of-Band
PA	Power Amplifier
PCB	Printed Circuit Board
PCS	Personal Communications Service
PDK	Process Design Kit
PSD	Power Spectral Density
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RB	Resource Block

RF Radio Frequency

RFIC Radio Frequency Integrated Circuit

RFID Radio-Frequency Identification

RFPA Radio Frequency Power Amplifier

SAW Surface-Acoustic Wave

SB Solder Ball

SC-FDMA Single-Carrier Frequency-Division Multiple Access

SDR Software Defined Radio

SEM Spectrum Emission Mask

SIMOX Separation by IMplantation of Oxygen

SMS Short Message Service

SOI Silicon-on-Insulator

SOLT Short-Open-Load-Thru

SOS Silicon-on-Sapphire

SP Scattering-Parameter

SP9T Single-Pole Nine-Throw

SPI Serial-to-Parallel Interface

STI	Shallow Trench Isolation
TDD	Time Division Duplexing
TDMA	Time Division Multiple Access
TLP	Transmission Line Pulse
UE	User Equipment
UMTS	Universal Mobile Telecommunication System
WCDMA	Wideband Code Division Multiple Access

Symbols

$\mathbf{B}$	Susceptance
$\mathbf{BPF_{Rx}}$	Receiver band-pass filter
$\mathbf{BPF_{Tx}}$	Transmitter band-pass filter
$\mathbf{C_{off}}$	OFF-Capacitor
$\mathbf{C_{on}}$	ON-Capacitor
$\mathbf{C_{WB}}$	Parasitic capacitance of bondwire
$\mathbf{DR}$	Dynamic Range
f_d	Duplexing offset
$\mathbf{F_r}$	Receiver noise figure
f_{res}	Resonant frequency
$\mathbf{F_t}$	Transmitter noise figure
$\mathbf{G}$	Conductance
$\mathbf{IIP3}$	Input third-order intercept point
$\mathbf{IL_{PA\text{-}to\text{-}ANT}}$	Insertion loss from PA output to Antenna
$\mathbf{IL_{Rx}}$	Insertion loss in receive band

$\mathbf{IL_{Tx}}$	Insertion loss in transmit band
IM2	Second-order non-linearity
IMP	Intermodulation Product
IP2	Second-order intercept point
IP3	Third-order intercept point
$\mathbf{ISO_{Rx}}$	Isolation in receive band
$\mathbf{ISO_{Tx}}$	Isolation in transmit band
$\mathbf{ISO_{Tx\text{-}Rx}}$	Isolation from transmitter to receiver
$\mathbf{K_B}$	Boltzmann constant
kTB	Thermal noise in the reference bandwidth
$\mathbf{L_s}$	Self-inductance
$\mathbf{L_{SB}}$	Least-Significant Bit
$\mathbf{L_{WB}}$	Parasitic inductance of bondwire
M	Mutual inductance
$\mathbf{n_{eff}}$	Effective stack height
NF	Noise Figure
$\mathbf{P_{Jam}}$	Jamming signal power
$\mathbf{P_{Tx,Ant}}$	Transmitter power at antenna port
$\mathbf{P_{Tx,Leakage}}$	Transmitter leakage power
Q	Quality-factor

$\mathbf{Q_{off}}$	Quality-factor in the OFF state
$\mathbf{Q_{on}}$	Quality-factor in the ON state
$\mathbf{r}$	Ohmic-loss
$\mathbf{r(t)}$	Transmit signal
RFESENS	Reference Sensitivity
$\mathbf{R_L}$	Load resistance
$\mathbf{RL_{ANT}}$	Antenna return loss
$\mathbf{R_{on}}$	ON-Resistance
$\mathbf{R_{WB}}$	Series resistance of bondwire
$\mathbf{S}(\omega)$	Scattering-parameter
SINR	Signal-to-Interference-plus-Noise Ratio
$\mathbf{T}$	Room Temperature
$\mathbf{t_{ox}}$	Oxide-thickness
$\hat{V}$	Peak voltage
$\mathbf{X}$	Reactance
XMD	Cross-modulation distortion
$\mathbf{Y}$	Admittance
$\mathbf{y(t)}$	Output signal
$\mathbf{Z}$	Impedance
$\mathbf{z(t)}$	Cancelling signal

δ	Skin depth
τ	Switching Time
ω	Angular frequency
Δ	Fractional duplex frequency

Chapter 1

Introduction

1.1 Background

The popularity of smart phones, cloud computing and the growing market for machine-to-machine (M2M) communications is fuelling the growth of mobile broadband. More spectrum is therefore being allocated to mobile services [1]. Today, nearly half the spectrum below 3.0 GHz has been earmarked for public radio communications somewhere in the world. Unfortunately, for historical reasons, the spectrum allocations are fragmented, poorly harmonised between different countries and no longer large enough for the ever-increasing broadband data rates. The next wireless standard, LTE-A (Long Term Evolution-Advanced), calls for data rates of 100Mbps (mobile) and 1Gbps (fixed). Considerable spectrum (up to 100MHz) is required for these services, and is not available in any one band. Carrier aggregation (CA), or operation on two or more bands at once, will be necessary. A future wireless terminal capable of global roaming would have to handle more than 44 bands, four generations of operating standards, and two duplexing methods and be capable of carrier aggregation. This is the research challenge.

1.2 Carrier Aggregation Concept

The Carrier Aggregation (CA) is the key part of LTE-A standard. It was defined in 3GPP Release 10 and commercial network launches followed in Korea in 2013 [2]. In principle, the CA aggregates multiple carriers to extend the maximum bandwidth in the uplink or downlink (or both) directions. Consequently, it increases the practical data rates, enhances the network capacity, and simplifies the traffic management in spectrum usage. The evolution of data rates through the CA is shown in Fig.1.1. Commercial LTE networks initially supported 100 to 150Mbps with continuous 20MHz spectrum. However, the data rate is doubled by introducing the CA and using two 20 MHz channels. CA ultimately enables the combinations of many carrier components (CC) with bandwidths of less than 20MHz achieving a maximum aggregated bandwidth of 100MHz, see Fig.1.1. The CA can basically take

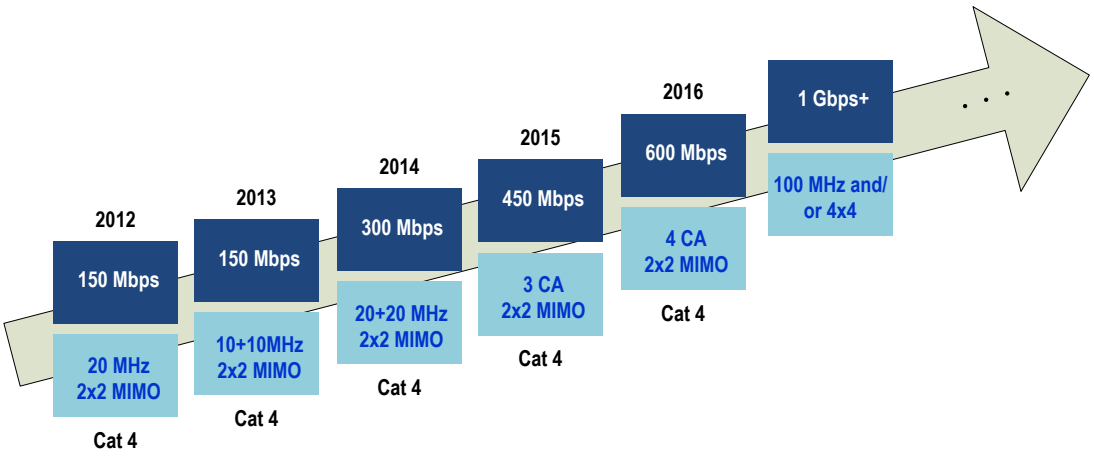


Figure. 1.1: Data rate evolution in downlink with the CA.

place both within the frequency band and between frequency bands. Three scenarios exist: intra-band contiguous and intra-band non-contiguous occurring within the same frequency band while inter-band non-contiguous occurs between different frequency bands. Intra-band schemes are handled by baseband DSP filtering, while inter-band scheme is an RF problem. Fig.1.2 illustrates these scenarios for the LTE-Advanced

standard. Spectrum fragmentation is a key issue and inter-band non-contiguous could potentially accommodate this issue. Today's LTE transceivers should be able to emulate all three CA scenarios, particularly the inter-band non-contiguous arrangement. The latter must receive signals on two separated frequency bands simultaneously.

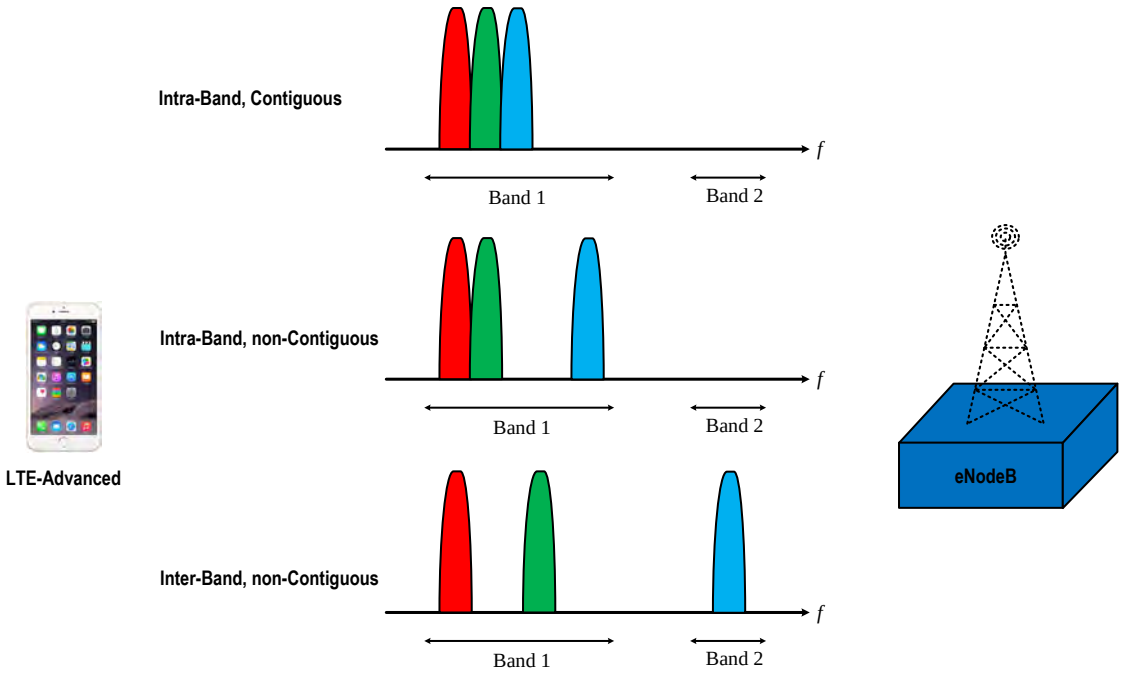


Figure. 1.2: LTE-A carrier aggregation scenarios; Intra-band and inter-band aggregation alternatives.(eNodeB means "evolved NodeB". The LTE basestation that has evolved from the previous (third) generation UMTS.)

Cognitive Radio (CR) schemes also benefit from the ability to receive more than one signal concurrently. Traditionally, this form of wireless communication detects the occupied and vacant channels by means of inserting blank periods in the transmission, allowing CR users to sense for un-occupied channels and instantly move between them. Thus the use of available radio frequency (RF) spectrum is utilised while minimising interference to the other users. Although the blank periods are useful, they introduce a loss of throughput. This issue could be avoided if a CR receives on two frequency bands at once, one is used for receiving data (without blank periods) while the other

band senses for vacant channels. In this thesis, we will only consider intra-band contiguous scenario for combined bandwidth between 5MHz (UMTS channel) and 20MHz (LTE channel).

1.3 Software Defined Radio

Software Defined Radio (SDR) was introduced by Mitola in 1995 [3]. It is the key enabler of CR. The waveforms or the radio parameters such as carrier frequency and bandwidth, power, modulation and coding scheme are stored for each channel. In operation, the entire spectrum is initially scanned to identify vacant channels. The waveform for the selected channel is then generated using digital processing techniques such as digital filtering, demodulation and coding. The method effectively eliminates traditional analogue hardware functions and replaces them with software algorithms which are executed in high-speed Digital Signal Processors (DSPs). The beauty of the SDR architecture is that it provides the possibility of implementing a multi-mode, multi-band and multi-functional transceiver in a single device.

In cellular systems, an SDR mobile handset must cover multiple frequency bands as well as multiple standards such as GSM, WCDMA, and the most recent LTE. Unfortunately, the carrier frequencies involved are not suited to DSP implementation, thus, this necessitates that the few remaining RF functions of an SDR must be featured as multi-band components. This a significant issue since these components are often fixed frequency devices, hence, they operate at a single frequency and cannot be tuned. In order to cover a wide range of frequency bands, multiple components are therefore required, resulting in substantial cost.

1.4 Duplexing

Duplexing is required for the simultaneous transmission and reception of signals which is required for voice and other multimedia applications. Today's wireless terminals

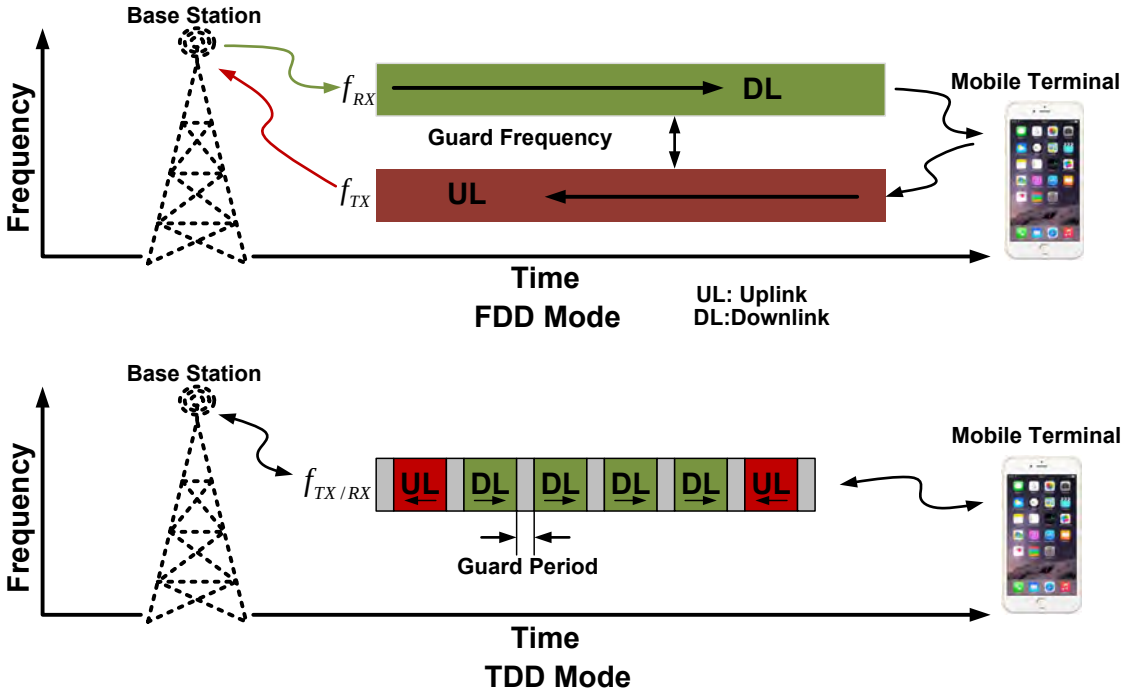
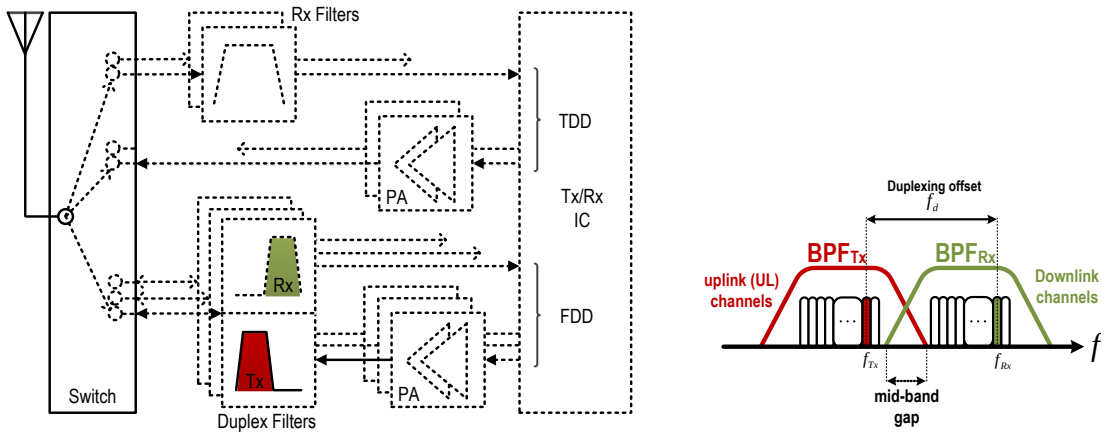


Figure. 1.3: Duplexing modes used in modern mobile communication systems.

are a mixture of software radio baseband circuits running on digital signal processing (DSP) cores and an analogue circuit that does the up/down conversion to radio frequency (RF). The RF signal is switched through an appropriate off-chip duplexing network before reaching the antenna. There are two types of duplexing in use today; time division duplexing (TDD), where the base-station and terminal transmit in turn, and frequency division duplex (FDD) where simultaneous transmission occurs, see Fig.1.3. FDD operation is used by about 90% of handsets (100% in Australia) and is the subject of this thesis.

FDD uses two closely spaced sub-bands for simultaneous up-link transmission (talk) and down-link reception (listen). The problem is that the transmitter power amplifier (PA) amplifies both the desired transmitter (Tx) signal as well as the noise over a wide frequency range. Some of this noise falls in the receiver (Rx) band and desensitises the receiver. Duplex filters separate out the Tx and Rx frequencies

(Fig.1.4). They need to provide about 50dB isolation between the strong Tx signal and the sensitive receiver circuits. The band pass filter in the transmitter path (BPF_{Tx}) passes the Tx signal through to the antenna but stops the transmitter noise (at the receive frequency). The bandpass filter in the receiver path (BPF_{Rx}) allows the incoming Rx signal to enter the receiver but stops the strong Tx signal from overloading (blocking) the receiver circuits. The filters are implemented in SAW (surface acoustic wave) or BAW (Bulk Acoustic Wave) technologies. They are expensive external components in a radio communications solution. Today's terminal has three to five duplexers, so when the phone roams to another country, not all bands will be supported and there is reduced capability, or sometimes no capability.*Some thirty-one duplexers! would be needed for global coverage of all the FDD bands specified by the International Telecommunications Union (ITU).*



(a) (b)

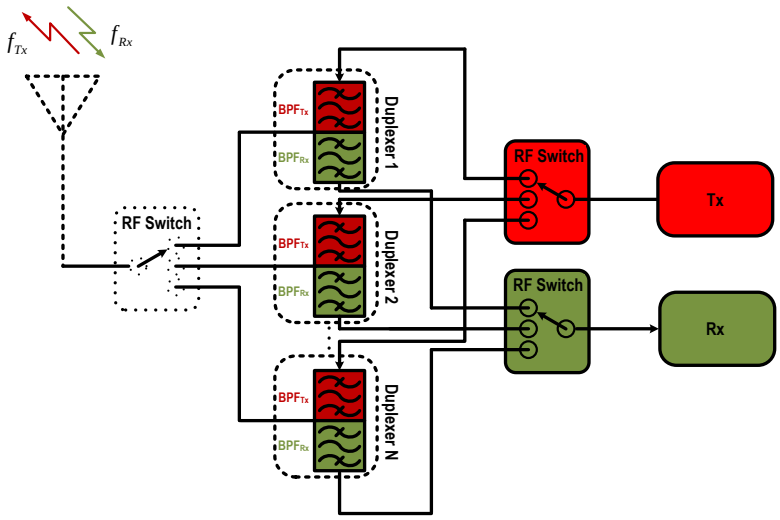
Figure. 1.4: Multi-band RF front-end solution: (a) using number of switched duplexers (b) using an adaptive duplexer with a low-isolation device (LID) and an active cancellation unit.

1.5 Adaptive Duplexers

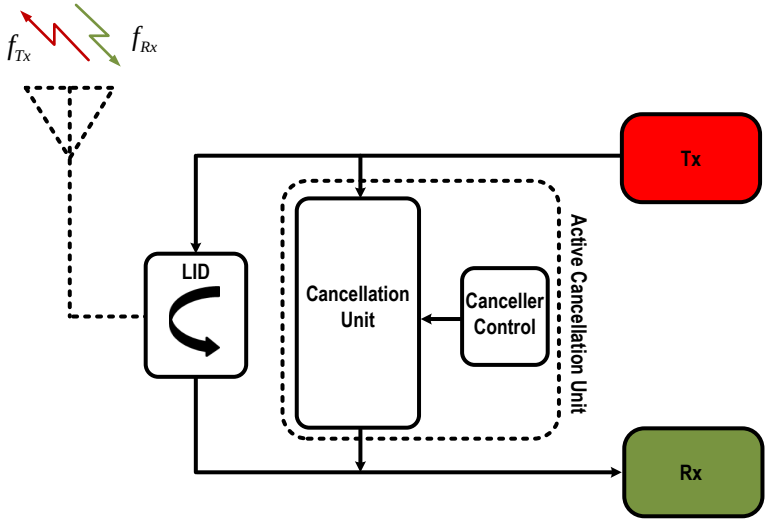
Existing duplexers not only demonstrate low-noise and high-linearity features, but also have bulky size and require an additional off-chip inductor at their balanced port. To provide support for many operating bands in an LTE/LTE-Advanced system, these many duplexers must be switched as shown in Figure Fig.1.5a. The research goal is to replace this "switched bank" of duplexers with a generic low cost solution integrated onto the existing radio transceiver integrated circuit (IC). To relax the complexity of the RF frond-end (RFFE) imposed by passive switched duplexers, an adaptive duplexer architecture has been developed [4]. It eliminates the need for multiple switched duplexers by using a reduced low-isolation device (LID) combined with a cancellation unit and controller, see Fig.1.5b. In operation, the LID needs to create an initial isolation of about 20dB (in the range of 15dB to above 20dB) and then an active double-loop cancelling technique is used to further increase transmit-to-receive isolation. The cancelling circuit can form up to two nulls at separate frequencies (shown in Fig.1.6) set by the gain and phase settings of each loop coefficient. The adaptive duplexer scheme is explained in detail in Chapter 3.

1.6 Implementation in Silicon

Single chip implementation requires the use of a technology that has good RF performance and can be easily integrated with other elements in the radio. Currently, GaAs and silicon-on-insulator (SOI) are used for RF switching as shown in Fig.1.5a. These technologies have good isolation (ISO) and low insertion loss (IL). High resistivity substrate reduces the parasitic capacitance in the active devices and the loss in the passive components. In particular, the Q-factor of passives are generally 20% higher than their conventional Bulk-CMOS counterparts. GaAs technology is relatively expensive for mass production, therefore, the SOI is the preferred solution [5].



(a)



(b)

Figure. 1.5: Multi-band RF front-end solution: (a) using number of switched duplexers (b) using an adaptive duplexer with a low-isolation device (LID) and an active cancellation unit.

1.7 Research Goals

The aim of this research is to study the feasibility of implementing the LID as tunable filters in a variety of media, namely on-chip and discrete (PCB). Two simple band-pass

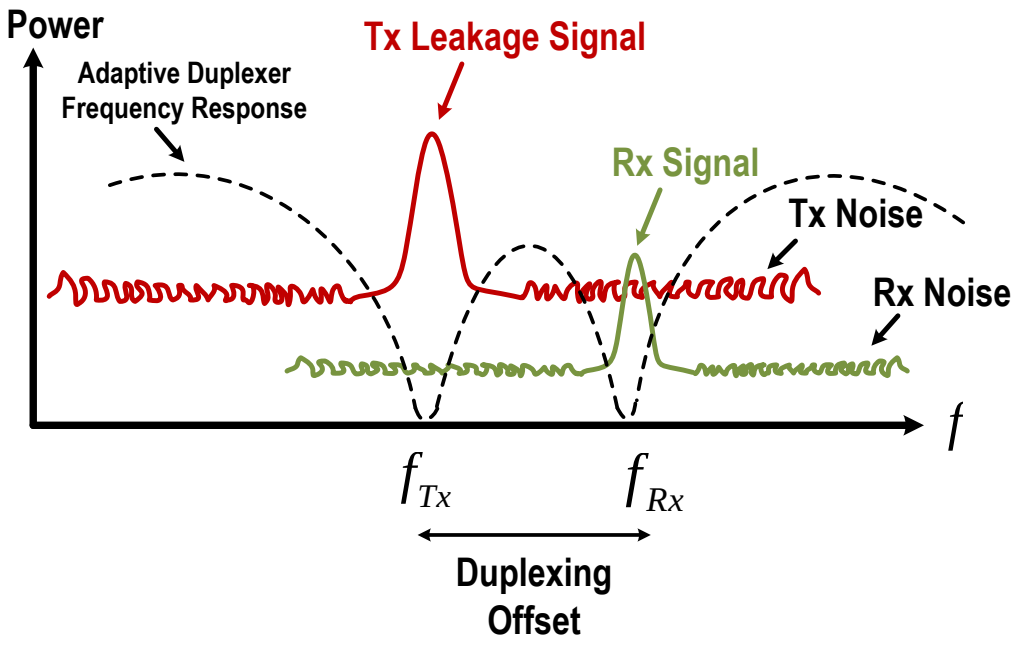


Figure. 1.6: Spectrum of the transmitter output (red), the receiver input (green) and the frequency response of the cancelling loops (black) required to cancel both the strong Tx signal and Tx noise in the vicinity of the received signal.

band-stop structures will be considered, their performance in terms of Q-factor and tunability will be analysed, and the pros and cons of the different implementation alternatives will be discussed. More specifically the main goals of this work are summarised:

- To identify the specifications and design requirements for the LID based on existing cellular standards. This includes frequency range, channel bandwidth, duplexing offset (Fig.1.6), power handling, isolation (ISO) and insertion loss (IL).
- To demonstrate a proof of concept for a single cellular band. LTE band 1 is targeted here.
- To extend the design for multi-band operation e.g. LTE 1, LTE 2, and LTE 3.

- To fabricate the above on-chip designs using SOI technologies.
- To improve the performance by using a hybrid solution of high-Q inductors combined with discreet tunable capacitors on a PCB.

1.8 Research Contributions

The research has led to the following publications:

1. **M. Pourakbar**, M. Törmänen, H. Sjöland, D. Nobbe, M. Faulkner, " Frequency-Agile LC Duplex Filter for Adaptive CMOS Duplexer," Submitted to IEEE Transaction on Circuits and Systems II: Express Briefs, Dec. 2014.
2. **M. Pourakbar**, R. Eslampanah, M. Faulkner, M. Törmänen, H. Sjöland, "An SDR Duplex Filter in SOI Technology," in Proc. 1^{st} Australian Microwave Symposium (AMS), Jun. 2014.
3. R. Eslampanah, **M. Pourakbar**, S. Ahmed, J.M. Redoute, and M. Faulkner, "RF Modulator Design for a Low Level Pilot Sub-System," in Proc. 1^{st} Australian Microwave Symposium (AMS), Jun. 2014.
4. **M. Pourakbar**, L. Linton, F. Rivet, M. Faulkner, "Studies on die-to-substrate interconnects for High-Q PCB inductors," in Proc. IEEE 20^{th} International Conference on Electronics, Circuits, and Systems (ICECS), pp.633-636, Dec. 2013.
5. **M. Pourakbar**, M. Törmänen, M. Faulkner, H. Sjöland, "An LC-based tunable low-isolation device for adaptive duplexers," in Proc. NORCHIP, 2013, pp.1-4, Nov. 2013.
6. **M. Pourakbar**, L. Linton, M. Törmänen, and M. Faulkner, "Tunable duplex filter for adaptive duplexers of advanced LTE handsets," in IEEE MTT-S International Microwave Symposium Digest, pp.1-4, Jun. 2013.

7. **M. Pourakbar**, R. Amirkhanzadeh, M. Törmänen, J. M. Redoute, and M. Faulkner, "High Power and High Performance RF SOS FET Switches," in Proc. GigaHertz Symposium, pp.65, Mar. 2012.

8. R. Amirkhanzadeh, **M. Pourakbar**, J. M. Redoute, and M. Faulkner, "Design Considerations for Switched Passive Circuits on Silicon-on-Sapphire (SOS) Process Technology," in Proc. 17^{th} Asia and South Pacific Design Automation Conference (ASP-DAC), Feb. 2012.

9. **M. Pourakbar**, J. M. Redoute, and M. Faulkner, "Design and implementation of high power, high linearity stacked RF FET switches in a 250-nm silicon on sapphire process," in Proc. IEEE Asia-Pacific Microw. Conference (APMC), pp.299-302, Dec. 2011.

1.9 Contents and Organisation of the Thesis

This thesis is organised in seven chapters. A brief description of each chapter is outlined below:

- Chapter 2 outlines the background of this research focusing on cellular standards and the implications on the RF design aspects of FDD transceiver. It overviews the key issues associated with the duplexing such as receiver desensitisation and blocking.

- Chapter 3 surveys the current duplexer structures as used in today's handsets based on RF filtering. The chapter then continues to overview the alternative duplexing architectures proposed by the research community. Passive and adaptive techniques are emphasised. The latter concentrates on cancelling techniques which require an LID, the main target of the thesis.

- Chapter 4 is the main theoretical contribution of the work. It introduces

two types of notch filter so called "Low-Frequency Network (LFN) and High-Frequency Network (HFN) filters", utilised in the LID.

- Chapter 5 briefly reviews the Silicon-on-Insulator (SOI) and the Silicon-on-Sapphire (SOS) processes, and their features as well as available active and passive devices for Analog/RF functions. The chapter also briefly explains the RF switching performance of SOI/SOS process.

- Chapter 6 presents an on-chip silicon solution followed by the experimental results of the SOS prototype. It is also concerned with improving the IL and the ISO by employing the second proposed configuration of the LFN filter. An off-the-shelf prototype of a tunable duplex filter is demonstrated as a proof of concept. This is the main practical contribution of the thesis.

- Chapter 7 demonstrates two fully-integrated solutions for the LID. The filters cover multiple LTE frequency bands. SOI and SOS processes are chosen for the implementation. Simulation results are provided.

- Finally, Chapter 8 summarises the measured results for both integrated and discrete duplex filter solutions. It also gives direction for potential future work.

Chapter 2

Background Information

In this Chapter, the RF design requirements and challenges of LTE transceivers in handsets are presented. Section 2.1 contains a brief history of cellular systems and their specifications from 1G to 4G. LTE frequency bands and a simplified 4G/LTE transceiver architecture are provided in Section 2.2 and Section 2.3, respectively. The main RF requirements related to user equipment (UE) for an LTE transmitter and receiver are described in Section 2.4. In Section 2.5, the minimum requirements are employed to derive the minimum duplexer isolation for LTE-FDD transceivers. Finally, a summary is provided in Section 2.6.

2.1 Cellular Systems

The rapid expansion of mobile communication has been hindered by the existence of a variety of standards used in cellular systems as shown in Fig.2.1. The first generation (1G) of cell phones was introduced by Motorola in mid-80's operating in the 450MHz frequency band. It was designed for voice communications which is essentially an analogue system. Frequency Division Multiple Access (FDMA) was used to provide a number of orthogonal channels for multiple access. The 1G system had numerous issues such as lack of security in speech transmission, low quality speech

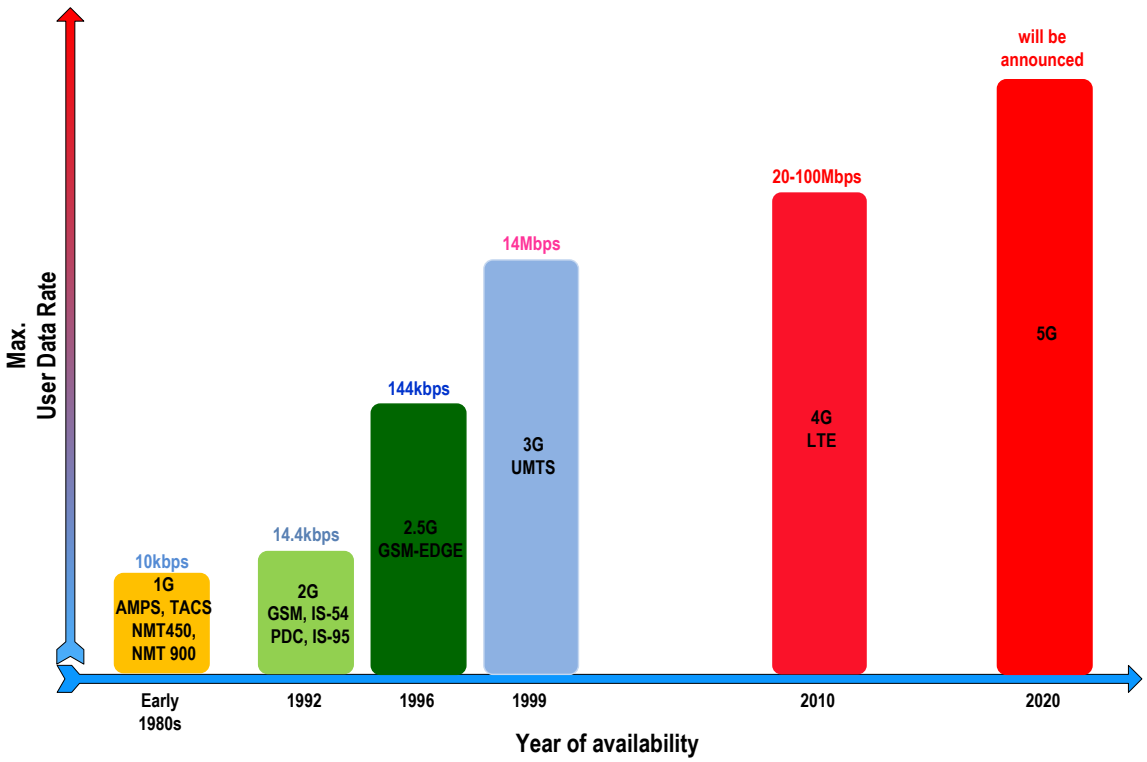


Figure. 2.1: History of cellular communication standards.

due to cross-talk between co-channel users, no roaming capability across the globe because of hardware incompatibilities, and a limited number of users per communication channel. In 1992, digital transmission opened a new horizon and the second generation (2G) was launched. Global System for Mobile potentially increased the number of subscribers by reducing the reuse distance between co-channel users. GSM (Global System for Mobile Communications) is a combined FDMA and TDMA (Time Division Multiple Access) system. GSM is still in operation and uses three frequency bands: 900 MHz (GSM900), 1800MHz (DCS1800) and 1900MHz (PCS1900). The low data rate makes this standard suitable for voice, or simple services such as SMS and MMS. However, demand for new and faster data services was soon acknowledged and the GSM standard was equipped with new features like HSCSD (High Speed Circuit Switched Data), GPRS (General Packet Radio Service) and EDGE (Enhanced

Data Rates for GSM Evolution). In 1999, the third Generation Partnership Project (3GPP) unified the telecommunication standards and released third generation (3G) cellular network known as Universal Mobile Telecommunications System (UMTS) [6]. It was based on the spread spectrum approach and multiple access technology referred to as Wideband Code Division Multiple Access (WCDMA), which allows all users of the same network to use the same frequency band simultaneously. UMTS adjusts its output power according to the distance between handset and base-station, in order to reduce interference and save energy. Packet transmission techniques allow it to be constantly connected to the Internet and its high spectral efficiency makes it 2 to 3 times more efficient than GSM.

Further demand for mobile networks offering mobile Internet services as fast as fixed home internet services led to the introduction of the fourth generation (4G) Long-Term Evolution (LTE) standard in 2010. It allows maximum user data rates of 100Mbps downstream and 50Mbps upstream, while reducing the cost per Megabit of data transport. Recent achievements have demonstrated that greater data bandwidth of 400Mbps could be obtained by aggregating up to three frequency bands simultaneously. LTE uses multicarrier transmission technology, Orthogonal Frequency-Division Multiple Access (OFDMA) in the downlink, Single-Carrier Frequency-Division Multiple Access (SC-FDMA) in the uplink, and MIMO transmission. LTE includes the previous 2G and 3G standards which allows network mobility with a single standard. Thus, the communication data rate will be optimized depending on the standard implemented within the user's geographic location. Beyond 4G will be 5G with transmission speeds up to 10Gbps. The European Commission has committed to fund the research with the aim of delivering 5G by 2020 [7].

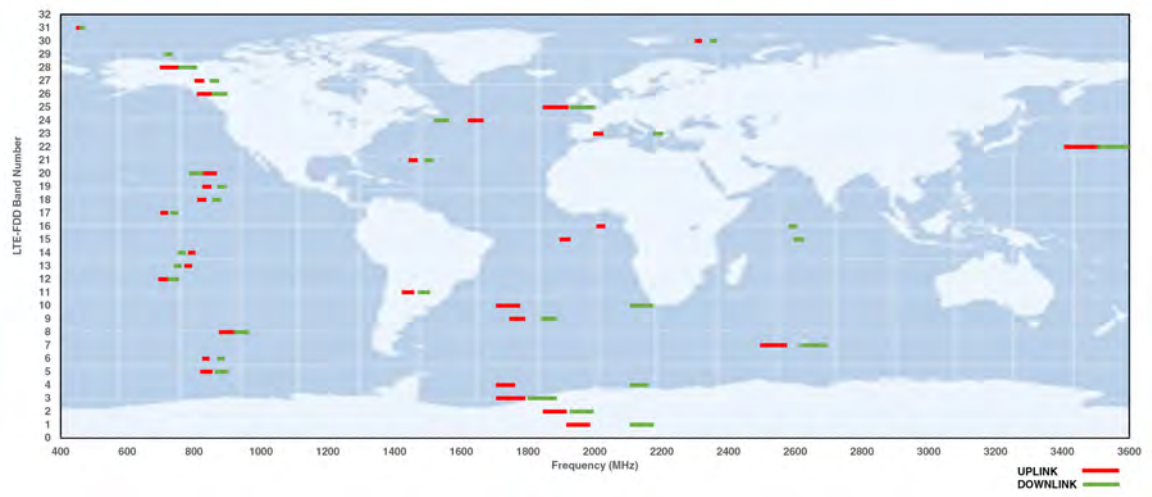


Figure. 2.2: LTE-FDD frequency band fragmentation showing uplink (red) and down-link (green) frequencies.

2.2 LTE Frequency Bands and Arrangements

To date, 44 frequency bands have been specified for LTE operation by 3GPP standardisation body. As mentioned earlier in Chapter 1, there are two types of duplexing schemes in use today; time division duplexing (TDD), where the base station and terminal transmit in turn, and frequency division duplex (FDD) where simultaneous transmission occurs. FDD uses two closely spaced sub-bands for simultaneous up-link transmission (talk) and down-link reception (listen). It should be noted that the FDD method is the focus of this research work. Fig. 2.2 shows the spectrum allocations of 32 LTE-FDD bands. Each frequency band is defined by three features (see Fig.2.3) given by

$$\text{Width of Band} = f_{UL\,high} - f_{UL\,low} = f_{DL\,high} - f_{DL\,low} \tag{2.1}$$

$$\text{Band Gap} = f_{UL\,high} - f_{DL\,low} \tag{2.2}$$

$$\text{Duplex Spacing} = f_{UL\,low} - f_{DL\,low} = f_{UL\,high} - f_{DL\,high} \tag{2.3}$$

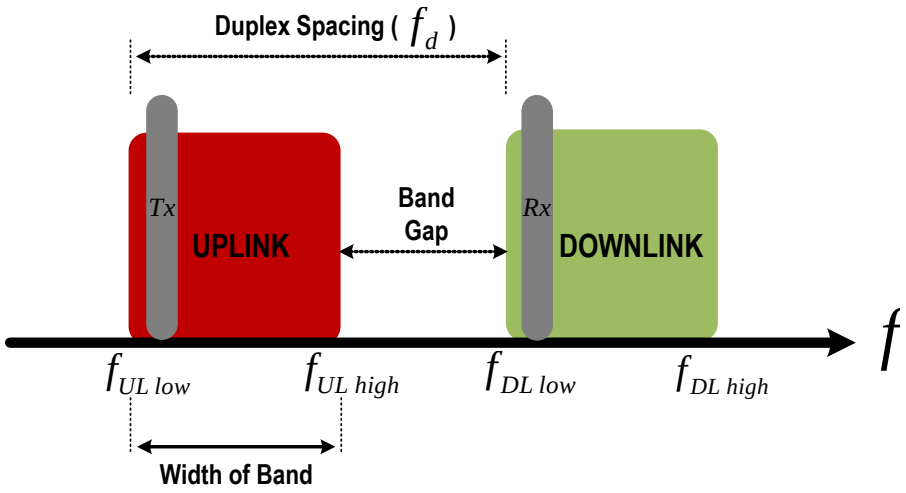


Figure. 2.3: LTE-FDD frequency band definitions.

Table 2.1 summarise the details of the LTE-FDD frequency bands. LTE band 1 is chosen for the duplexer application in this thesis since the duplex spacing is relatively large (190MHz), hence, a passive filtering approach is doable.

Table 2.1: LTE-FDD frequency band definitions [8].

LTE-FDD Bands & Frequencies					
LTE Band Number	**Uplink (MHz)**	**Downlink (MHz)**	**Width of Band (MHz)**	**Duplex Spacing (MHz)**	**Band Gap (MHz)**
1	1920-1980	2110-2170	60	190	130
2	1850-1910	1930-1990	60	80	20
3	1710-1785	1805-1880	75	95	20
4	1710-1755	2110-2155	45	400	355
5	824-849	869-894	25	45	20
6	830-840	875-885	10	35	25
7	2500-2570	2620-2690	70	120	50
8	880-915	925-960	35	45	10
9	1749.9-1784.9	1844.9-1879.9	35	95	60
10	1710-1770	2110-2170	60	400	340
11	1427.9-1452.9	1475.9-1500.9	20	48	28
12	698-716	728-746	18	30	12
13	777-787	746-756	10	-31	41
14	788-798	758-768	10	-30	40
15	1900-1920	2600-2620	20	700	680
16	2010-2025	2585-2600	15	575	560
17	704-716	734-746	12	30	18
18	815-830	860-875	15	45	30
19	830-845	875-890	15	45	30
20	832-862	791-821	30	-41	71
21	1447.9-1462.9	1495.5-1510.9	15	48	33
22	3410-3500	3510-3600	90	100	10
23	2000-2020	2180-2200	20	180	160
24	1625.5-1660.5	1525-1559	34	-101.5	135.5
25	1850-1915	1930-1995	65	80	15
26	814-849	859-894	30 / 40		10
27	807-824	852-869	17	45	28
28	703-748	758-803	45	55	10
29	N/A	717-728	11	N/A	N/A
30	2305-2315	2350-2360	10	45	35
31	452.5-457.5	462.5-467.5	5	10	5
32	N/A	1452-1496	44	N/A	N/A

2.3 4G LTE Transceiver Architecture

Today's 4G LTE transceivers use SDR baseband circuits together with an analogue circuit that performs the up/down conversion to RF. The RF signal is switched through an appropriate *off-chip* duplexing network before reaching the antenna (ANT). Fig.2.4 illustrates a simplified transceiver architecture of a 4G LTE handset.

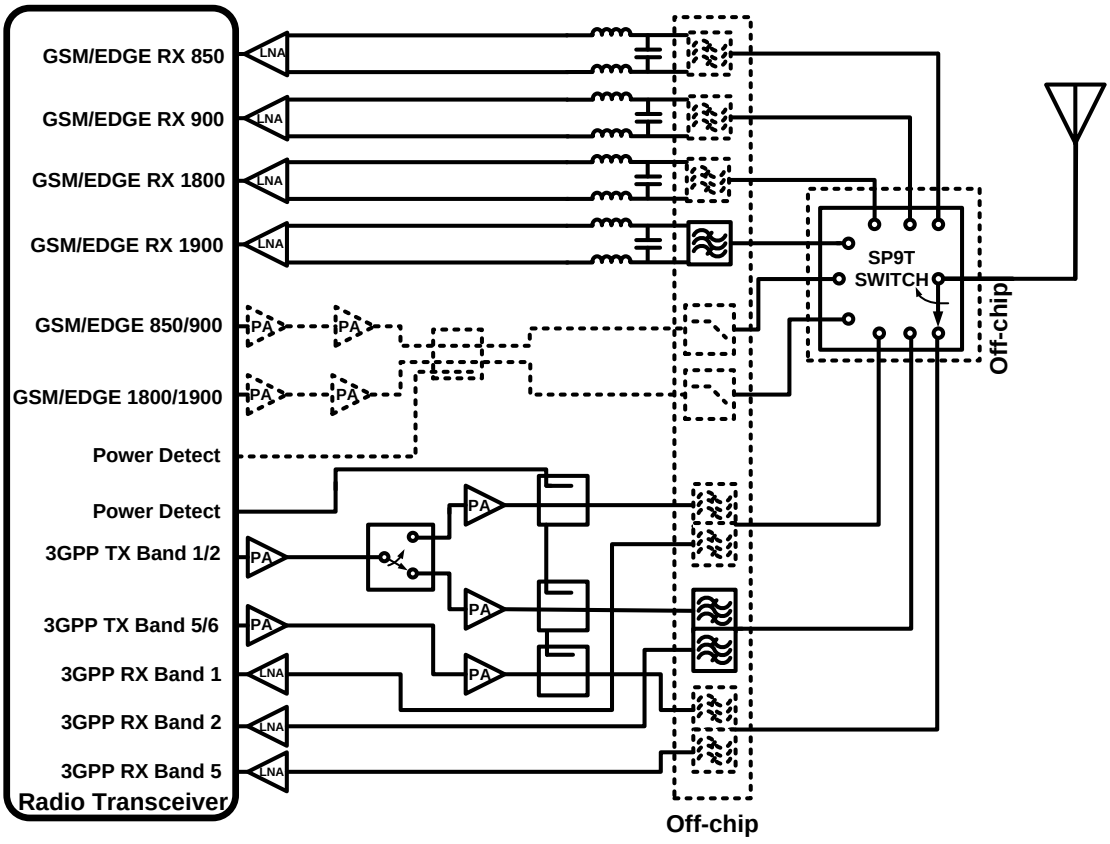


Figure. 2.4: A simplified typical transceiver architecture of a 4G cellular phone.

As mentioned earlier, the duplexer plays an important role in FDD systems since it isolates the receiver from the transmitter through two front-end band-pass filters (BPFs) as shown in Fig.2.5. The RFPA (radio frequency power amplifier) amplifies both the Tx signal and the noise floor by a gain of G (denoted in Fig.2.6). The noise PSD (power spectral density) shown as K_BTF_tG is typically ≈35dB above the

receiver noise floor (K_BTF_r). BPF_{Tx} attenuates the transmitter wideband noise PSD at the Rx frequency band which would eventually avoid the increase of receiver noise figure, see Fig.2.6. On the other hand, BPF_{Rx} prevents the strong transmit signal leaking into the Rx path causing receiver desensitisation and blocking the receive signal as shown in Fig.2.7.

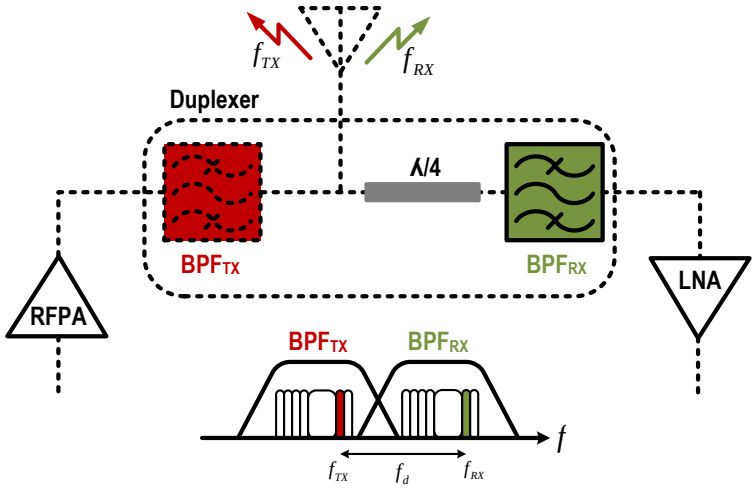


Figure. 2.5: Conventional duplexer consists of two front-end BPFs.

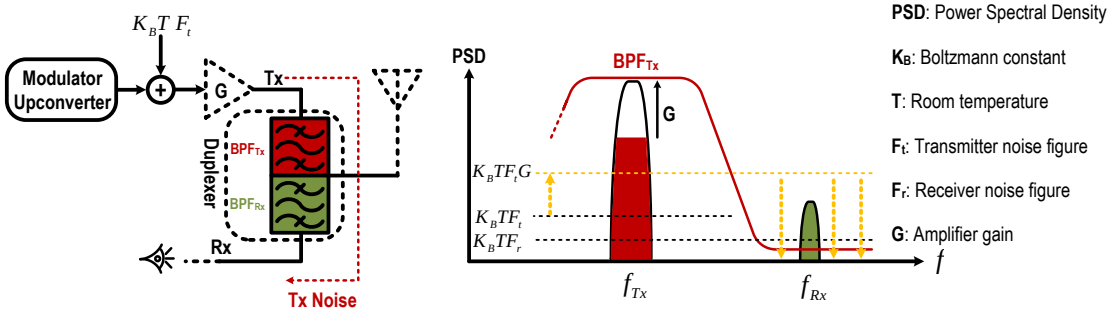


Figure. 2.6: Transmitter noise in the Rx band is attenuated by BPF_{Tx}.

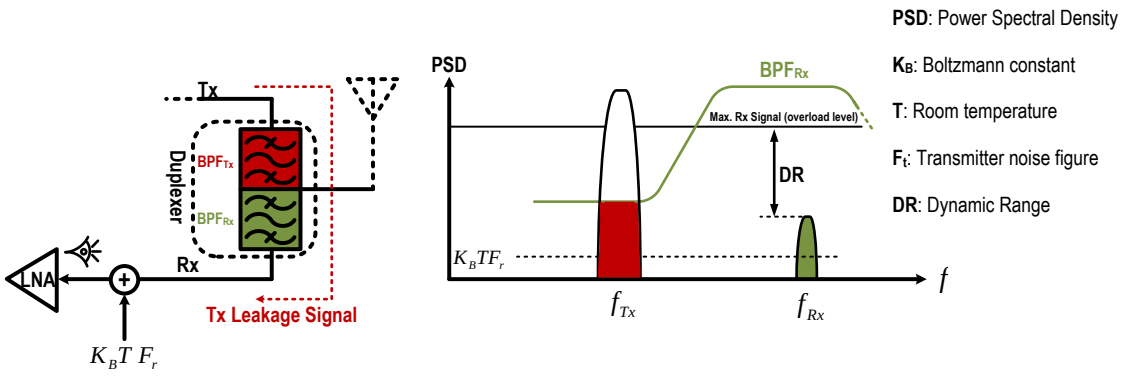


Figure. 2.7: Receiver desensitisation due to overload by the Tx signal unless attenuated by BPF_{Rx}.

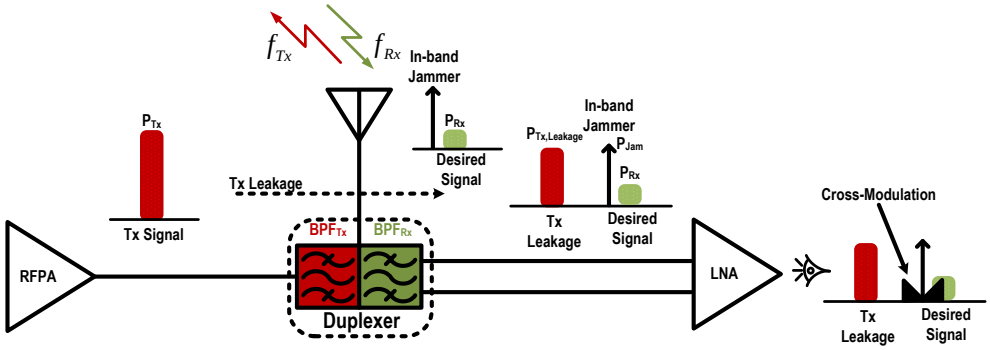


Figure. 2.8: Cross-modulation distortion effect due to the strong Tx leakage.

2.3.1 Impact of Tx Leakage on the Receiver

The high power Tx signal can desensitise the receiver through several mechanisms. First, the transmitter noise leakage in the receive band is added to the Rx noise floor unless adequate Tx-Rx isolation is obtained by the duplexer at the Rx band.

Second, cross-modulation distortion (XMD) between the transmitter leakage and a jamming signal can potentially overlap in frequency with the wanted signal as shown in Fig.2.8. Using the Taylor series power expansion for the receiver non-linearity, the

generated XMD can be calculated as

$$XMD(dBm) = P_{Jam}\ (dBm) + 2\ P_{Tx,Leakage}\,(dBm) - 2\ IIP3\ (dBm) \tag{2.4}$$

where IIP3 is the 3rd order input intercept point. (2.4) indicates that every 10dB

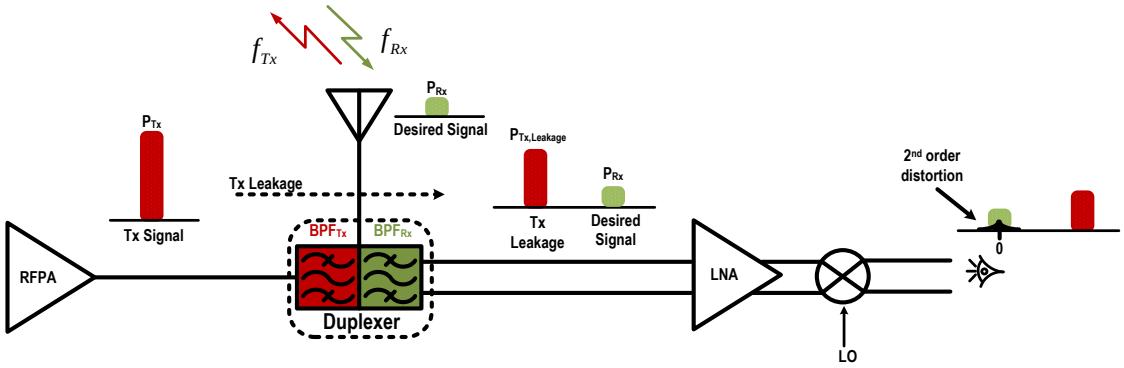


Figure. 2.9: Second-order nonlinearity effect due to the strong Tx leakage.

improvement in duplexer isolation results in a 20dB improvement of the XMD.

Third, in a direct conversion receiver (DCR), self-mixing of the Tx leakage signal causes second-order non-linearity (IM2) products at baseband, see Fig.2.9. The IM2 can be characterised by the 2^{nd} order intercept point (IP2). Two equal-amplitude RF tones are applied at the input and the resultant IM2 products are observed at the output. IP2 can then be obtained by extrapolating the plotted fundamental tone and the IM2 product versus the input power. For instance, a two-tone Tx leakage signal generates the IM2 product given by

$$IM2(dBm) \approx 2\ P_{Tx,Leakage}\,(dBm) -\ IIP2\ (dBm) - 6\ dB \tag{2.5}$$

where IIP2 is the second order input intercept point and the 6dB factor is used when two-tones with half of the Tx leakage power are applied.

Finally, LO phase noise can produce reciprocal mixing with the Tx leakage signal that falls in the Rx band (particularly when the duplex offset is low) as illustrated

in Fig.2.10. The aforementioned challenges place the most stringent requirements on the design of the duplexer as well as the transceiver. Enhancing the duplexer isolation eases the Tx noise and the Rx linearity and phase-noise requirements.

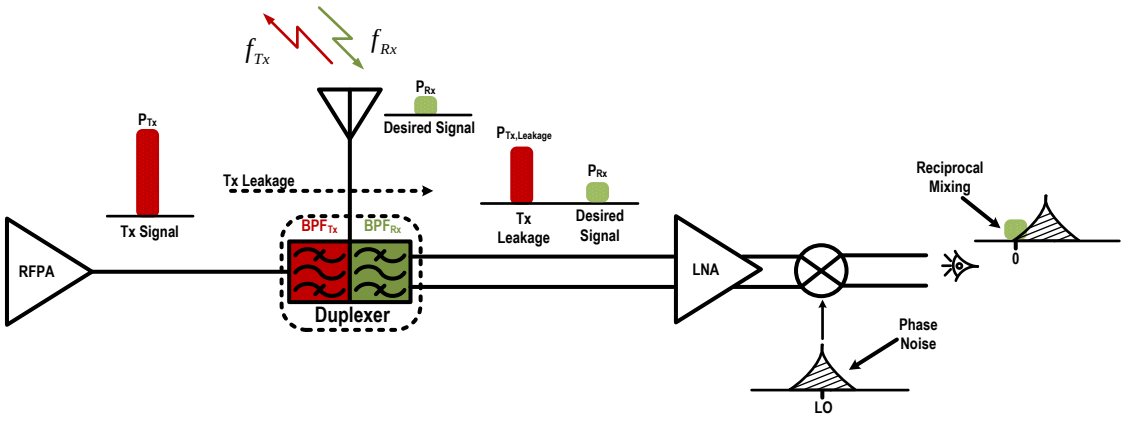


Figure. 2.10: Reciprocal mixing effect.

2.4 LTE UE Transceiver Design Requirements

In 4G handsets, LTE functionality is included into the existing the 2G GSM/EDGE and 3.5G WCDMA/HSPA architecture. The main design requirements related to the LTE UE transmitter and the receiver are described in this section. Further information may be obtained from the 3GPP technical documents [8, 9].

2.4.1 RF Transmitter Requirements

LTE transmitters must satisfy two general sets of requirements: one related to the power level and modulation accuracy of the intended transmitted signal (known as signal quality), and the other related to the level of unwanted emissions.

2.4.1.1 Intended Transmission Requirements

- **UE Transmit Output Power**

  The LTE UE power class depends on the operating band. It is defined as the maximum output power for Quadrature Phase Shift Keying (QPSK) modulation at the antenna port. The main UE power class is set to 23dBm with a tolerance of ±2dB for all bands [8].

- **Signal Quality**

  The transmitted UE signal deviates from an ideal modulated signal due to RF imperfections in the transmitter mainly caused by the non-linearity of the PA. The signal quality is measured by the Error Vector Magnitude (EVM) of the modulated signal constellation. It fundamentally defines the maximum SNR that can be achieved at the receiver when the channel is ideal and noiseless. The EVM requirement in LTE relates to the modulation scheme. The LTE 64 Quadrature Amplitude Modulation (64QAM) places the most stringent requirement on the EVM budget being less than 8%. However, 16 Quadrature

Amplitude Modulation (16QAM) and QPSK are required to meet EVM budgets of 12.5% and 17.5%, respectively [8].

2.4.1.2 Unwanted Emission Requirements

The ITU-R recommendation classifies unwanted emissions from the transmitter into two categories, Out-of-Band (OOB) emissions and spurious emissions as shown in Fig.2.11. Intermodulation in the PA causes OOB emissions in adjacent channels, while spurious emissions occur outside the RF carrier region. The boundary between the OOB and spurious domains is defined by ITU-R at a frequency separation from the RF carrier of 2.5 times channel bandwidths.

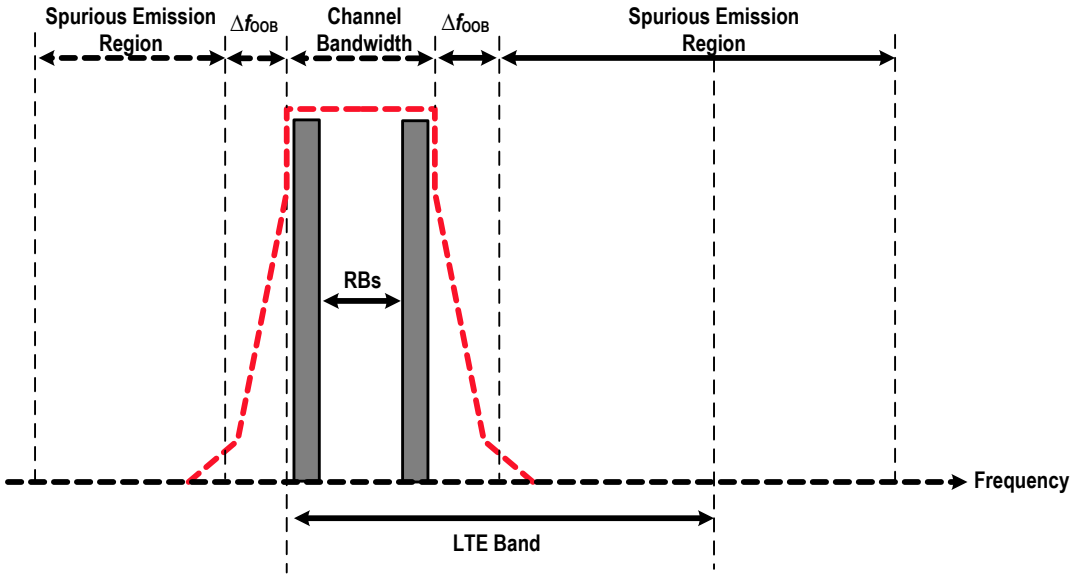


Figure. 2.11: LTE transmitter spectrum [8]. (RBs: Resource Blocks).

- **Out-of-Band Emissions**

  Since OOB emissions are generated by the PA non-linearity, decreasing the transmit power will reduce these undesired signals. The bandwidth of LTE system is not fixed; it is more practical to consider the OOB requirement to

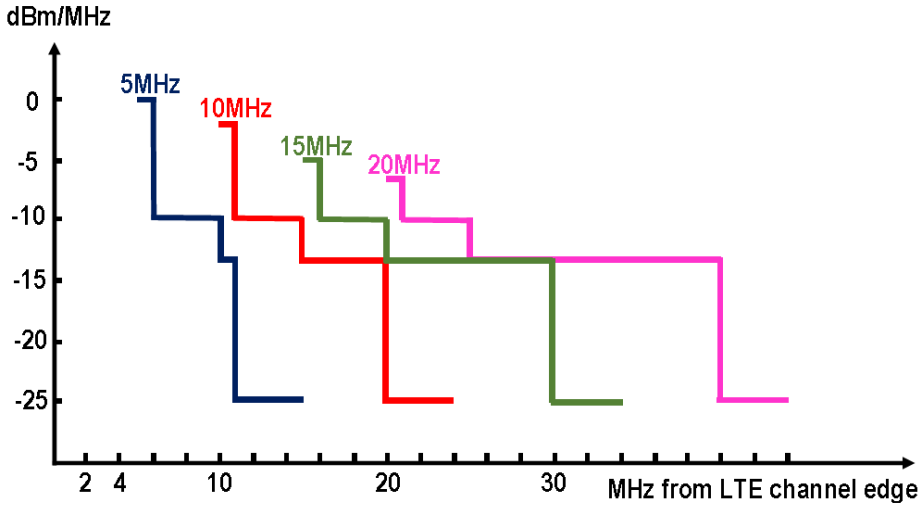


Figure. 2.12: SEM for a UE transmitter for various LTE channel bandwidths [8].

the edge of the channel bandwidth compared to that of measured to the centre frequency of the channel in UMTS radio. Here, two overlapping requirements are defined: Spectrum Emission Mask (SEM) and Adjacent Channel Leakage Ratio (ACLR). SEM specifies the maximum permissible OOB emissions in dBm/MHz outside of the necessary channel bandwidth. Fig.2.12 illustrates the SEMs for different LTE channel bandwidths. The ACLR measures the unwanted fraction of signal power falling in the neighbouring radio channel as per Fig.2.13. It should be noted that the increase in ACLR is mostly due to occupancy of the adjacent channel by the 3^{rd} and 5^{th} order intermodulation distortion (IMD) products.

The ACLR of handsets is set to be <-30dBc for an adjacent 20MHz LTE channel, and <-33dBc for adjacent UMTS channel measured at 5MHz of the OBB spectrum and <-36dBc for the second adjacent UMTS channel found 10MHz separated from the desired channel.

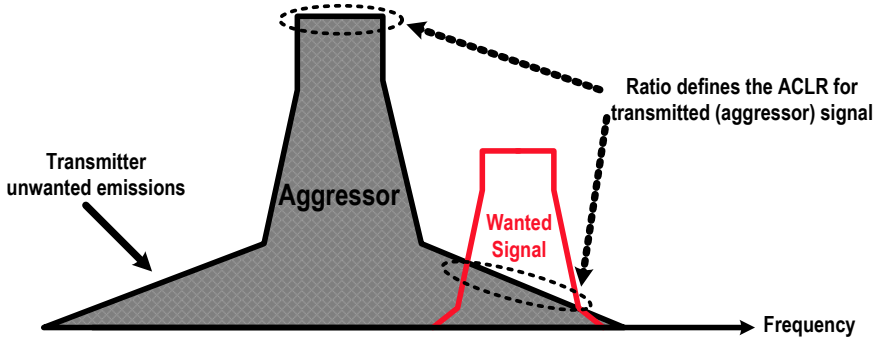


Figure. 2.13: Illustration of ACLR for two nearby radio channels.

- **Spurious Emissions**

  Spurious emissions are mainly due to unwanted transmitter effects such as harmonic emissions, parasitic emissions, intermodulation and frequency conversion products. Table 2.2 shows the spurious emission requirements for the UE. In FDD systems, the spurious emissions can fall in the receive channel blocking the weak wanted receive signal. Hence, the spurious requirement is very stringent in this part of the spectrum. In LTE, the spurious emissions must be <-130dBc/Hz at the maximum transmit power of 23dBm for a mobile terminal.

Table 2.2: UE LTE spurious emission requirements [9].

Frequency Range	**Maximum Level**	**Measurement Bandwidth**	**Note**
9kHz$\leq$ f $<$ 150kHz	-36dBm	1kHz	
150kHz$\leq$ f $<$ 30MHz	-36dBm	10kHz	
30MHz$\leq$ f $<$ 1000MHz	-36dBm	100kHz	
1.0GHz$\leq$ f $<$ 12.75GHz	-36dBm	1MHz	
12.75GHz$\leq$ f $<$ 5th harmonic of the upper frequency edge of the UL operating band in GHz	-30dBm	1MHz	1
NOTE 1: Applies for Band 22, Band 42, and Band 43			

2.4.2 RF Receiver Requirements

In this sub-section, two main requirements are highlighted: receiver sensitivity and dynamic range, and receiver susceptibility to interfering signals.

2.4.2.1 Sensitivity Level and Dynamic Range

The LTE receiver should detect a weak wanted signal. The reference sensitivity (REFSENS) of a receiver is the minimum received signal strength required to guarantee a throughput of 95% of maximum throughput (for a given modulation and coding scheme). Practically, RFESENS is given by

$$REFSENS = kTB + NF + SINR + IM - 3 \ (dBm) \tag{2.6}$$

where kTB is the thermal noise in the reference bandwidth, NF is maximum overall noise figure of the receiver, SINR is selected based on the applied modulation and coding scheme, IM is the implementation margin which is 2.5dB for QPSK 1/3 and 4dB for 64QAM 3/4, and -3dB is added for the diversity gain. Table.2.3 shows the REFSENS requirement for a UE at different channel bandwidths. The measurement assumes the FDD transmitter is at full power (23dBm).

Table 2.3: REFSENS of UE LTE receiver for Band 1.

Modulation Scheme	Channel Bandwidth	kTB (dBm)	NF (dB)	SINR (dB)	IM (dB)	REFSENS (dBm)
QPSK 1/3	5MHz	-107.5	9	-1	2.5	-100
	20MHz	-101.4	9	-1	2.5	-94
64QAM* 3/4	5MHz	-107.5	9	17.5	4	-80
	20MHz	-101.4	9	17.5	4	-74
*The REFSENS is specified for QPSK modulation.						

The dynamic range requirement for the receiver ensures that it can operate at an Rx signal level considerably higher than REFSENS. For the UE, the dynamic range is defined as the maximum signal level at which the required throughput is achieved minus (dB scale) the minimum signal level at which the throughput is met [8].

2.4.2.2 Receiver Susceptibility to Interfering Signals

LTE requires handheld devices to receive the wanted signal in the presence of a strong interfering signal. The receiver sensitivity should not be reduced by more than 0.5dB when the transmitter operates simultaneously as required in FDD systems. The receiver selectivity and blocking measures are briefly explained below.

- **Blocking**

  There are two types of blockers, one outside the operating band (out-of-band blocker) and the other inside the operating band (in-band blocker). In both cases, they are not adjacent to the wanted signal. In LTE, Out-band blockers are positioned 15MHz or more from the band edge and must be suppressed to >-44dBm. In-band blockers are severe issues because they cannot be removed by filtering. Signals as high as -25dBm must be tolerated in the adjacent channel.

- **Adjacent Channel Selectivity (ACS)**

  The ACS is a measure of the receiver's ability to reject signals in the adjacent channel. It is basically defined by the ratio of the receive filter attenuation on the assigned channel (passband) to the receive filter attenuation in the adjacent channel (stopband). According to [9], the required ACS is 33dB for 5MHz channels and 27dB for a 20MHz channels.

- **Narrowband Blocking**

  Narrowband blockers are unwanted narrowband continuous waveform (CW) interferers occurring at frequencies less than the nominated channel spacing. They should be attenuated to -55dBm at least [9].

- **Receiver Intermodulation**

  The intermodulation products are caused by non-linearities and can sometimes fall in the desired receive band, therefore, they should be less than -94dBm to be below the receiver sensitivity level of a 5MHz channel.

2.5 Typical Duplexer Requirements for LTE

As mentioned in Section 2.3.1, the Tx leakage signal and the Tx leakage noise are two interferers that can potentially desensitise the receiver. LTE requires the Tx noise leaking into the Rx band to be <-183dBm/Hz. The Tx leakage signal level is predominantly determined by the ISO_{Tx-Rx}. Given the spurious emission level of -107dB/Hz for the Rx band, the required duplexer isolation of 76dB and 59dB is obtained for LTE and UMTS, respectively. However, today's RF mobile platform manufacturers have improved their spurious emissions to a level of -133dBm/Hz resulting in a reduced isolation requirement ISO_{Tx-Rx} ≈50dB. This scenario is illustrated in Fig.2.14. The Tx leakage power at the receiver input is given by

$$P_{Tx,Leakage}(dBm) = P_{Tx,ANT}\ (dBm) + IL_{PA-to-ANT}\,(dB) - ISO_{Tx-Rx}\ (dB) \quad (2.7)$$

where $IL_{PA-to-ANT}$ is the insertion loss from the PA output to the ANT, which includes the RF switch, duplexer and the PCB routing. $IL_{PA-to-ANT}$ can be as high as 2dB. In LTE, the maximum PA output power can be 25dBm, resulting in a $P_{Tx,ANT}$ of 23dBm at the antenna port. Assuming a typical duplexer isolation of 50dB, the receiver will face Tx leakage of -25dBm (23dBm+2dB-50dB), which is just below the blocking limit of the receiver.

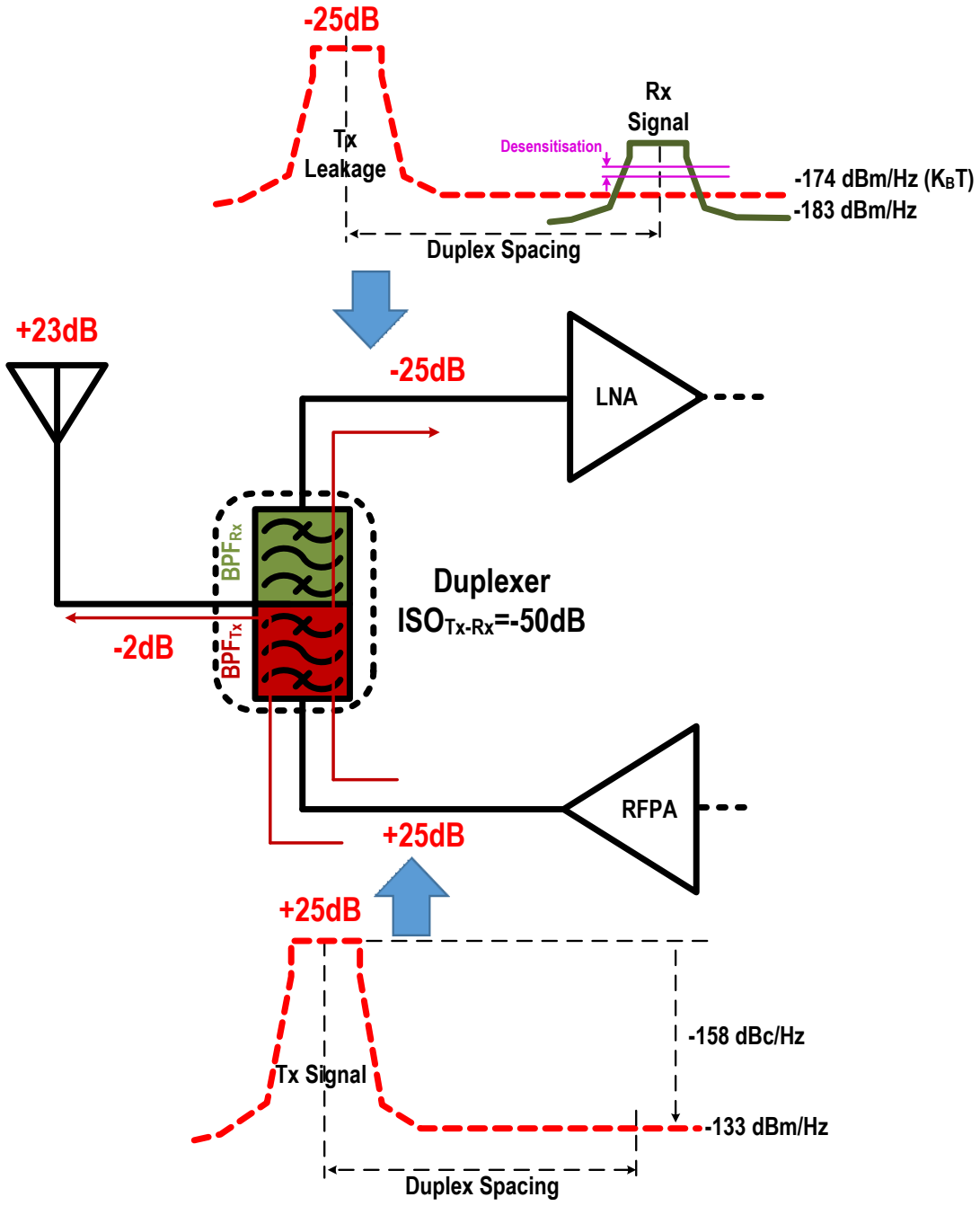


Figure. 2.14: Tx leakage problem in LTE-FDD UE transceiver [8].

2.6 Summary

In this chapter, a brief history of cellular standards is given. Nowadays, LTE systems known as 4G networks are commonly used operating in either the FDD or the TDD modes. Here, the LTE-FDD is introduced and a simplified transceiver architecture is shown. Duplexers are the key components used in the FDD transceivers to attenuate the Tx leakage signal and the Tx leakage noise in the receiver chain. Therefore, the impact of a high power Tx signal on the receiver are explained with particular emphasis on cross-modulation, reciprocal mixing, and second-order non-linearities. The UE RF requirements for the transmitter and the receiver are discussed. Finally, typical requirements for an LTE duplexer are provided from which it is concluded that the duplexer isolation must be at least 50dB in both Tx and Rx bands.

This Chapter introduced the basic requirements for the LTE-FDD system emphasising the duplexer. The next Chapter reviews the literature on duplexers and adaptive duplexing methods.

Chapter 3

Duplexing Techniques: Literature Survey

FDD systems use two closely spaced carriers for simultaneous uplink transmission and downlink reception. We previously explained the potential desensitization of the receiver by the two strong leakage signals (the Tx leakage and the Tx noise). Therefore, a 3-terminal component was introduced known as a duplexer that isolates the receiver from the strong transmitter while allowing them to share the same antenna, see Fig.2.5. In that figure, it is shown that a conventional duplexer consists of two fixed frequency bandpass filters (BPF_{Tx} and BPF_{Rx}) and a transmission line which acts as a matching network. As previously described, increasing the number of operating frequency bands has resulted in the switching of multiple duplexers as a feasible solution for current handset manufacturers. The duplexer is a bulky component which means that putting an array of duplexers into a cellular phone will result in increased size and cost of the handset. The theory of a circulator-based duplexer is reviewed in Section 3.1. Section 3.2 introduces passive duplexing methods including non-tunable filters, separated antennas, directional couplers and hybrid transformers known as electrical balancing circuits. Active cancellation architectures are discussed in Section 3.3 and a summary is given in Section 3.4.

3.1 Theory of The Duplexer

In 1964, the theory of a circulator-based duplexer was studied by Carlin [10]. An RF duplexer is a linear time invariant three-port network that can be described by the scattering parameter (SP) matrix:

$$S(\omega) = \begin{bmatrix} S_{11}(\omega) & S_{12}(\omega) & S_{13}(\omega) \\ S_{21}(\omega) & S_{22}(\omega) & S_{23}(\omega) \\ S_{31}(\omega) & S_{32}(\omega) & S_{33}(\omega) \end{bmatrix} \tag{3.1}$$

where port 1 is connected to the Tx, port 2 is the antenna connection, and the LNA input is port 3. The duplexer performance metrics are the insertion loss in the Tx (IL_{Tx}) and the Rx (IL_{Rx}) bands, isolation in both bands (ISO_{Tx} and ISO_{Rx}), and the antenna return loss (RL_{ANT}). The insertion loss in the Tx path dissipates the expensive PA output power, degrading its efficiency and shortening handset battery life. The insertion loss is given by

$$IL_{TX}(\omega) = -20\log_{10}(|S_{12}(\omega_{TX})|) \tag{3.2}$$

Attenuation of the Tx leakage is the most important duplexer figure of merit and is defined as

$$ISO_{TX}(\omega) = -20\log_{10}(|S_{31}(\omega_{TX})|) \tag{3.3}$$

Every decibel of insertion loss in the Rx path is directly added to the cascaded noise figure of the receiver, degrading the total sensitivity level. Such an insertion loss is formulated as

$$IL_{RX}(\omega) = -20\log_{10}(|S_{32}(\omega_{RX})|) \tag{3.4}$$

The PA output is associated with noise having powers well above the receiver sensitivity. This also increases the receiver noise figure. The duplexer should provide

enough isolation in the receive band to eliminate the noise increase.

$$ISO_{RX}(\omega) = -20\log_{10}(|S_{31}(\omega_{RX})|) \tag{3.5}$$

The return loss parameter indicates how well each duplexer port is matched to the reference impedance. The duplexer is often placed close to the transmitter and receiver in most handsets, therefore only the antenna is connected through the PCB trace. Matching is effected by close proximity body effects. The return loss at the antenna port is given by

$$RL_{ANT}(\omega) = 20\log_{10}(|S_{22}(\omega_{TX,RX})|) \tag{3.6}$$

In order to meet the minimum required RL_{ANT}, the Tx (Rx) impedance at the antenna port must be large to minimise the unwanted loading effect on the Rx (Tx) circuitry. A transmission line in series with the Tx (Rx) path is typically used to rotate the impedance on the Smith chart. Fig.3.1 shows a typical frequency response for the duplexer.

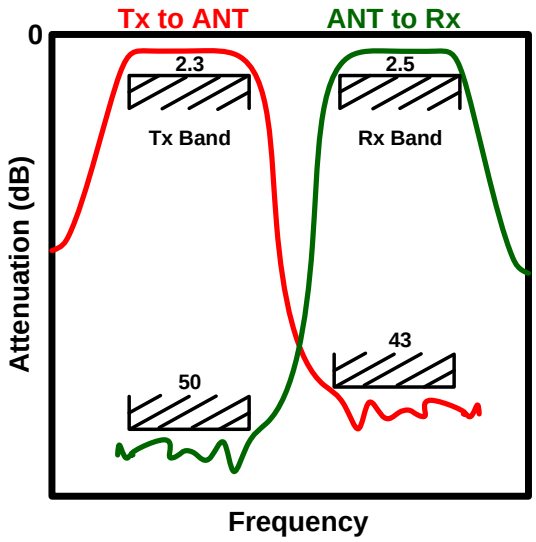


Figure. 3.1: Typical frequency response of the duplexer.

When a duplexer is designed, a number of contradictory design trade-offs need to be considered as shown in Fig.3.2. Insertion loss and isolation are the most important electrical parameters which directly affect the duplexer size. In most duplexers, improving the insertion loss degrades the isolation.

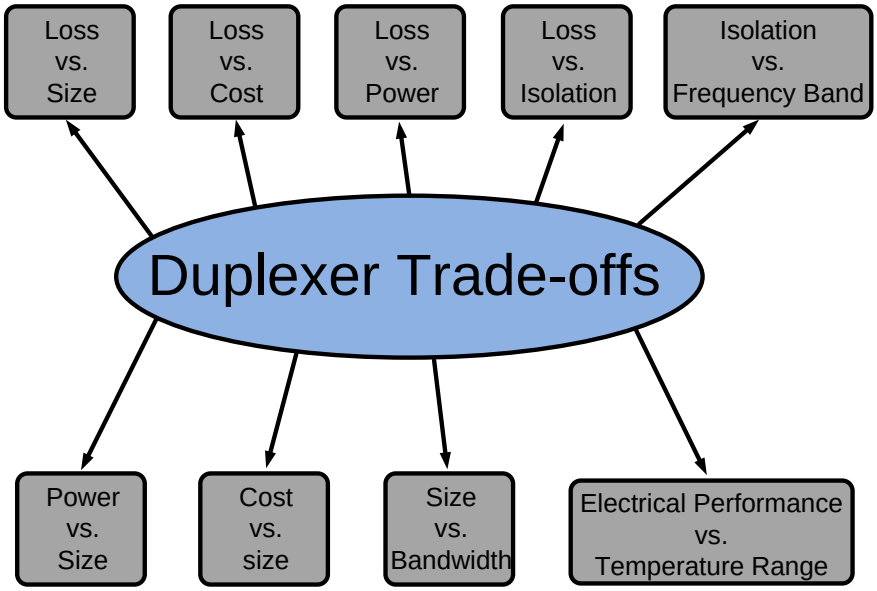


Figure. 3.2: Design trade-offs for duplexers.

3.2 Passive Duplexing Methods

3.2.1 SAW and FBAR Technology

Surface-acoustic wave (SAW) and thin-film bulk acoustic resonator (FBAR) filters are usually fabricated on a piezoelectric substrate such as quartz or lithium-tantalate. These filters have intrinsically linear phase and sharp roll-offs resulting in high quality-factor (Q) and low insertion loss characteristics. They are also difficult to monolithically integrate with other components on a single chip. Two solutions have been proposed in recent publications to address the latter issue. In [11], a SAW filter has

been mounted on top of a transceiver chip while in [12, 13], an FBAR has been integrated at the wafer level (Fig.3.3). However, these configurations require additional matching networks and expensive masks and costly procedures in the fabrication process.

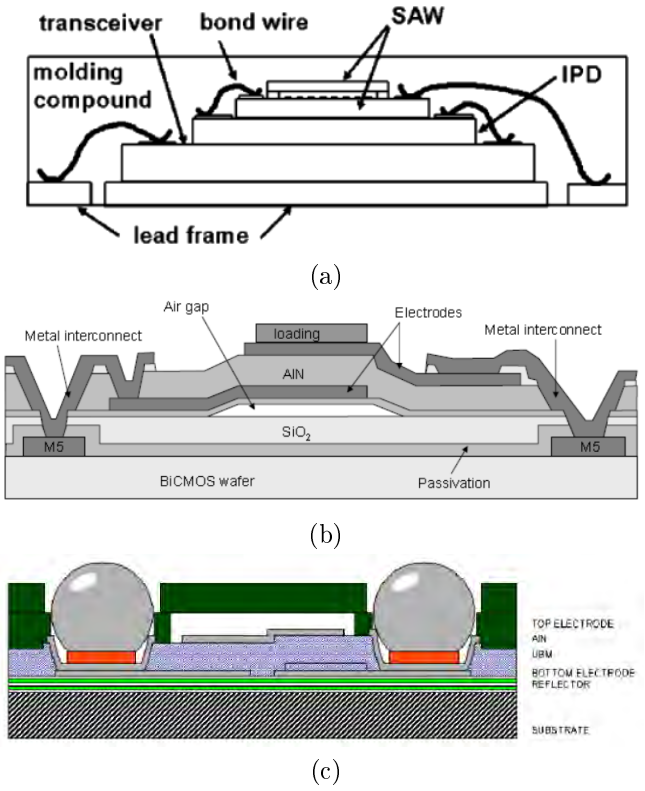


Figure. 3.3: Cross section of (a) stacked SAW filter on a transceiver [11] (b) FBAR filter integrated above IC [12] (c) BAW resonator with solder bumps [13].

A low insertion loss and high rejection duplexer using FBAR technology was developed by Feld et al. [14]. The ladder topologies for both transmitter and receiver dice have been employed, which contain 3 series- 3 shunt and 3 series-4 shunt topology respectively. In addition to the above technique, a quarter wavelength microstrip transmission line (at the transmit frequency) was used as a phase shifter in the receiver path (see in Fig.3.4). Although this design approach can meet all the required specifications, the dimension of the chip (3.8mm x 3.8mm x 1.4mm) and cost were

the two main drawbacks which occurred due to the length of microstrip and FBAR technology.

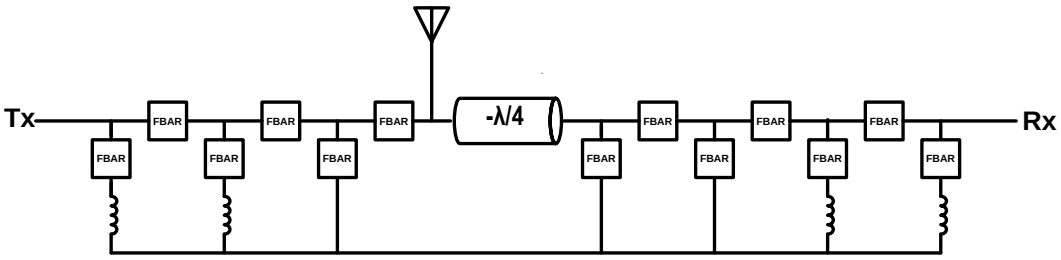


Figure. 3.4: UMTS-1 duplexer topology [14].

Nam et al. [15] have proposed a new ladder topology for Tx and Rx filters by modifying the Feld structure. The duplexer mainly comprises Tx and Rx filters, phase shifter, and packaging cap which are fabricated on high resistive silicon substrate. The highest insertion loss of Tx and Rx filters are 2.5dB and 3.1dB, respectively. The overall isolation is higher than 42dB and the size is 2.5mm x 2.5mm. Although all duplexer parts have been integrated, the insertion loss of the pass bands does not meet the 3GPP specifications.

Kawai et al. [16] proposed a novel tunable ring resonator filter that can tune the centre frequency, bandwidth, and out-of-band features. It is obvious that the receiver band pass filter has not only a low insertion loss at receiver frequency but also high insertion loss at transmitter frequency to prevent the transmitting signal from interfering with the receiver. The schematic of the tunable duplexer is shown in Fig.3.5. The achieved insertion loss and isolation from 3GHz to 4GHz are 2dB and 30dB, respectively. It is fabricated on an alumina substrate using microstrip lines. Therefore, this structure is not compatible with the required fabrication process needed for a single silicon device.

Wang et al. [17] proposed a new wide bandwidth duplexer structure based on FBAR technology. Aluminium Nitride (AlN) has been used as a piezo-active layer and a ladder topology is used for both transmitter and receiver filters. External

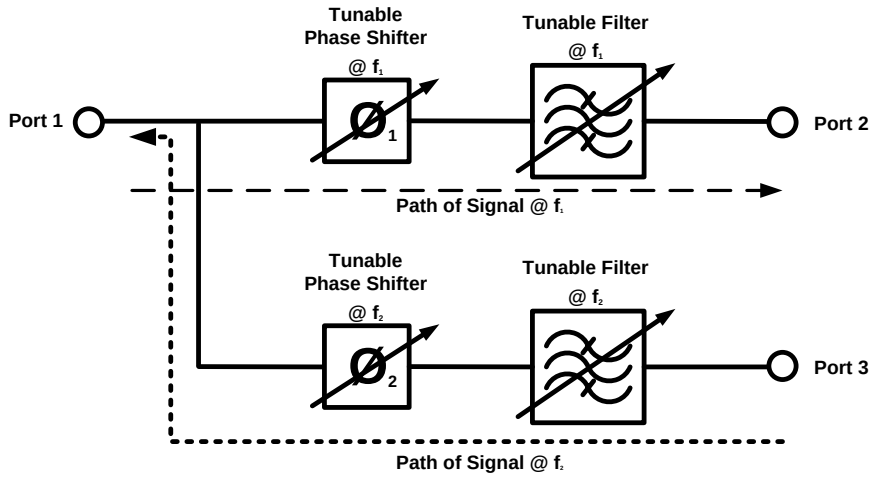


Figure. 3.5: Schematic of tunable duplexer [16].

inductors have been employed to compensate the electromechanical coefficient of the resonator and to adjust locations of filter zeros so as to get a proper attenuation in the stopband. This technique provides 50dB isolation and less than 2dB insertion loss. However, the size of the duplexer, which is 3mm x 3mm, is not suitable for handsets.

With the advancements in fabrication processes and newly explored substrate materials, the size of passive commercial duplexers have progressively reduced for handheld devices as illustrated in Fig.3.6. The performance metrics of various commercial SAW and FBAR duplexers for LTE-enabled mobile phones are summarised in Table 3.1. It can be observed that the required isolation for an integrated duplexer is of selected better than 45dB, resulting in a slight improvement in the insertion loss of the Tx path. This isolation ensures the signal level at the receiver input does not desensitise the receiver in any circumstances.

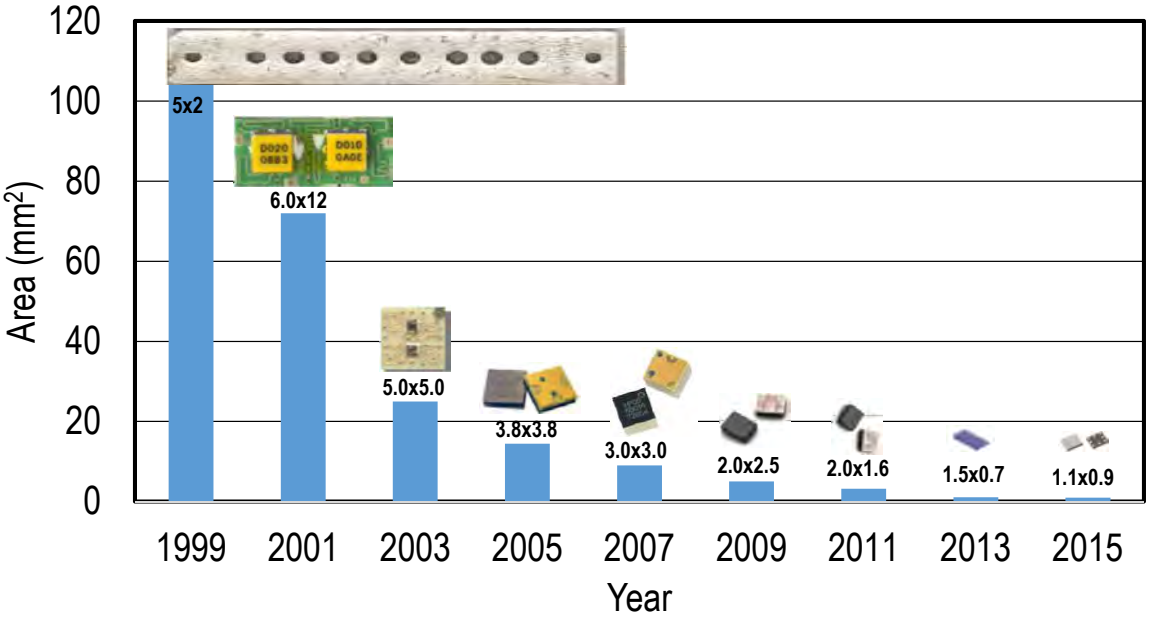


Figure. 3.6: Size reduction of passive duplexers for handsets.

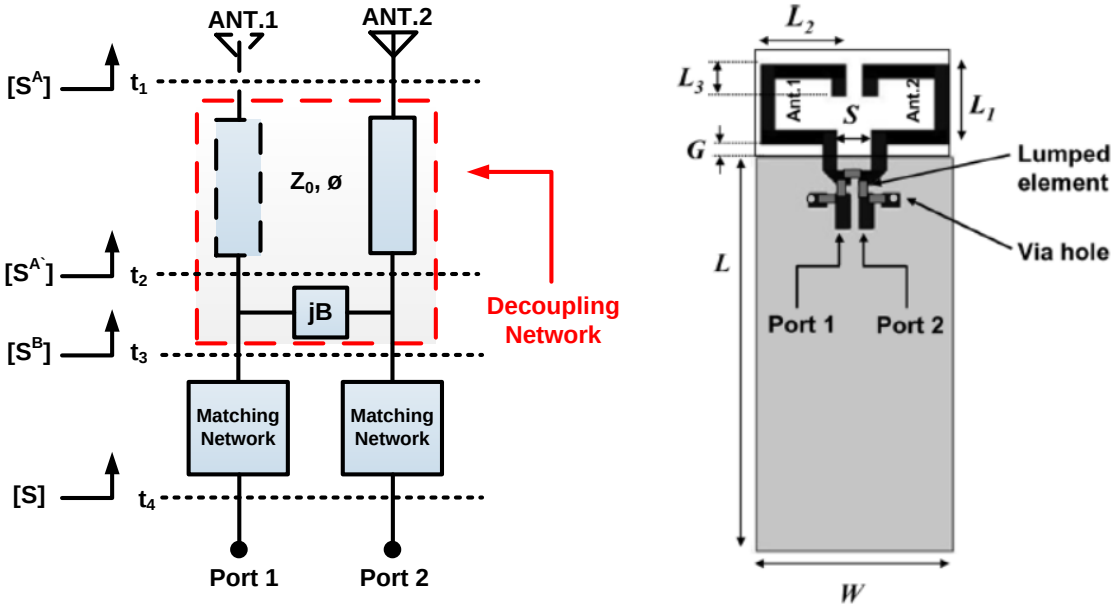
Table 3.1: Commercial SAW and FBAR duplexer performance for different popular LTE bands.

Parameter	**SAW [18]**			**FBAR [19]**		
	LTE Band 1	**LTE Band 2**	**LTE Band 3**	**LTE Band 1**	**LTE Band 2**	**LTE Band 3**
f_d **(MHz)**	190	80	95	190	80	95
IL_{Tx} **(dB)**	1.7+0.9* =2.6	2.5+0.9* =3.4	NA	1.9+0.9* =2.8	4.0+0.9* =4.9	3.5+0.9* =4.4
ISO_{Tx} **(dB)**	50	53	NA	48	50	55
IL_{Rx} **(dB)**	2.3+0.9* =3.2	3.7+0.9* =4.6	NA	2.2+0.9* =3.1	3.8+0.9* =4.7	4+0.9* =4.9
ISO_{Rx} **(dB)**	45	41	NA	45	45	50
RL_{ANT} **(dB)**	10.8	11.7	NA	9	NA	10
Area (mm^2)	3.2	3.2	NA	5	5	3.2

* Assumes Peregrine PE42694 SP9T switch and 0.3dB PCB loss.

3.2.2 Dual Antenna Scheme

The isolation between two antennas is important in mitigating self-interference. A dual antenna approach is proposed in [20, 21] for full-duplex communication where only cancellation at one frequency is required. Chen et al. [20] propose a decoupling technique for enhancing the isolation between two closely spaced antennas. The technique contains two transmission lines and a shunt reactive component connected to an impedance matching network at each port as shown in Fig.3.7a. Two miniaturised monopole antennas (see Fig.3.7b) have been fabricated and an isolation of more than 20dB between the two antennas has been reported. However, the bandwidth is narrow. Larger spacing increases bandwidth and real-estate.



(a) (b)

Figure. 3.7: Decoupling technique for two antennas (a) function blocks (b) two closely spaced miniaturised monopole antennas [20].

Kenworthy [21] presents a slightly different technique to improve the isolation between two antennas. A dual antenna scheme (Tx and Rx) combined with an analogue canceller and an adaptive digital baseband filter is utilised as illustrated in

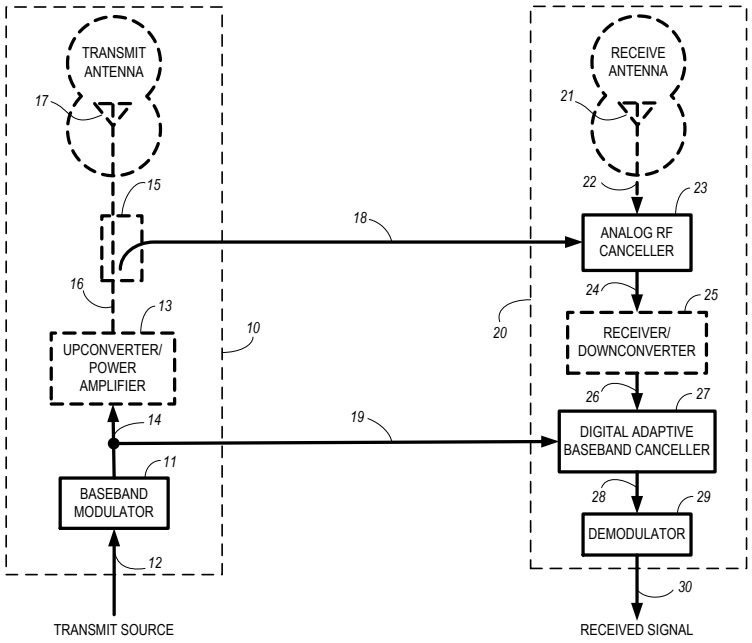


Figure. 3.8: Block diagram of self-cancelling technique for full-duplex RF communication systems [21].

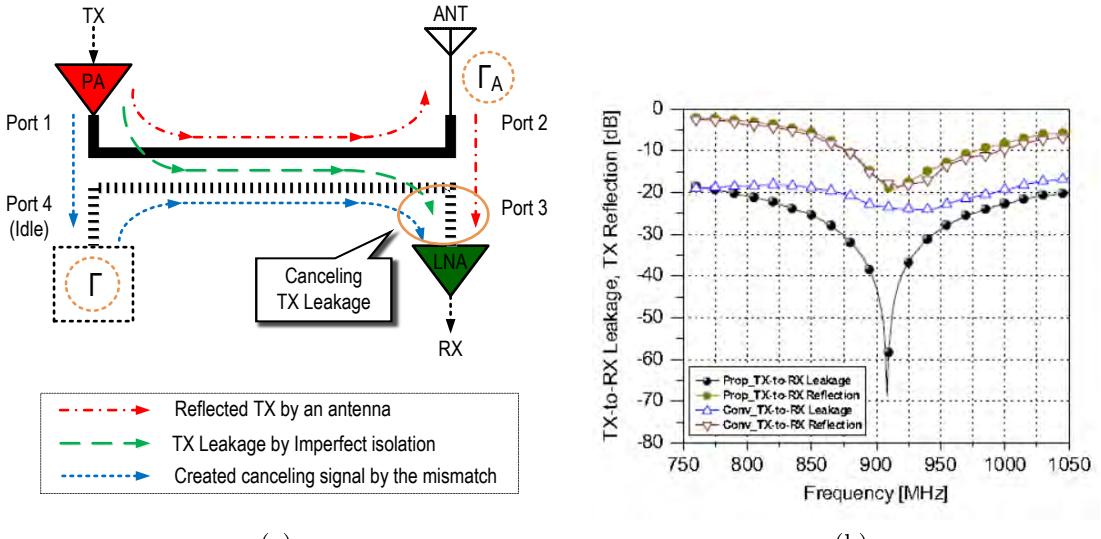
Fig.3.8. The two separated antennas provided 20dB of leakage suppression, while the analogue canceller and digital filter create isolations of 15dB and 25dB, respectively. This approach mainly suffers from the large area required by the second antenna.

Other researchers have developed systems that operate with dual separated Tx and Rx antennas [22–25]. However, multi-antenna methods prevent efficient integration and can also degrade the antenna radiation pattern by causing un-intentional beamforming.

3.2.3 Microstrip Directional Couplers

Directional couplers are widely used to isolate the Rx signal from the strong Tx signal of radio-frequency identification (RFID) systems. Unequal phase velocity between the even and odd mode components of microstrip couplers can degrade performance.

Researchers in [26, 27] utilise a directional coupler as shown in Fig.3.9a. The PA, the antenna, and the LNA are connected to Port 1, Port 2, and Port 3, respectively. The Tx signal is transferred to the antenna via the through port with an associated IL_{Tx} related to the coupling factor. The receiver is connected to the coupled port. The coupling factor which is the IL_{Rx} is often set in the range 10∼20dB to keep transmission losses (IL_{Tx}) at a minimum [26]. To improve isolation, the idle port (Port 4) can be deliberately mismatched so its reflected power cancels out the power leaking from the Tx port to the Rx port combined with the reflected power from any antenna mismatch (Fig.3.9a). [27] reported a measured isolation greater than 40dB over a 25MHz bandwidth (Fig.3.9b). The receiver IL_{Rx} can be reduced by increasing IL_{Tx}. When $IL_{Rx} = IL_{Tx}$ there is minimum 3dB loss in both paths, a high penalty for mobile handsets. Additionally, it is difficult to integrate microstrip couplers into small form factor transceivers.



(a) (b)

Figure. 3.9: Proposed reflected power canceller employing the coupled-line directional coupler (a) operating principle (b) measured Tx-to-Rx isolation and Tx reflection [26].

3.2.4 Spatial Duplexing

The spatial duplexing method has attracted significant research attention [28–30]. Multiple Tx antennas are used to create transmission nulls in the vicinity of the Rx antennas as shown in Fig.3.10. If the Rx antenna is placed midway between two Tx antennas the mutual coupling from each Tx antenna to the Rx antenna can be cancelled. Proper antenna placement and appropriate beam-forming can therefore increase isolation. Isolations as high as 60dB have been reported, but real estate for antennas is scarce in mobile handsets.

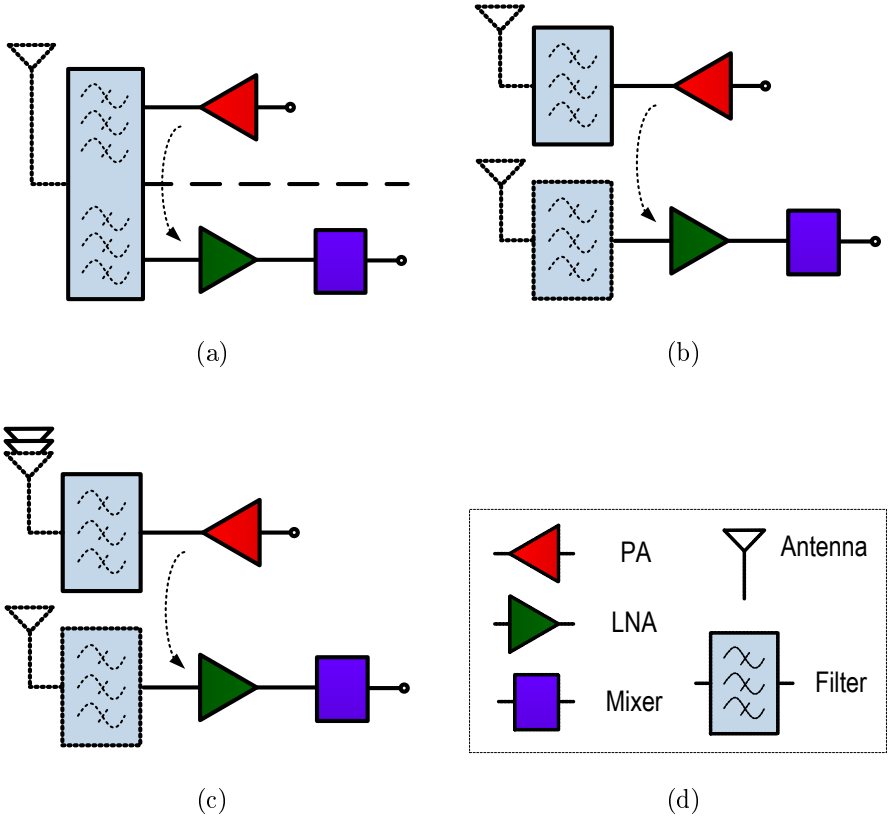


Figure. 3.10: Evolution of spatial duplexing concept. (a) conventional duplexing. (b) Tx-Rx separation mode by dual antenna. (c) a spatial duplexing filter (d) notations [28].

3.2.5 CMOS and Lumped Component Solutions

A bi-directional distributed amplifier (DA) is a potential solution for single chip Tx/Rx implementation. Leisten et al. [31] proposed the first duplexer/circulator structure using the versatile distributed amplifier. This structure was non-tunable. An electronically tunable active duplexer using DAs is shown in Fig.3.11 [32]. The Tx/Rx DA module consisted of MESFET transistors [33], fabricated in a monolithic microwave integrated circuit (MMIC). For mobile applications, the technique has issues of noise, distortion and cost.

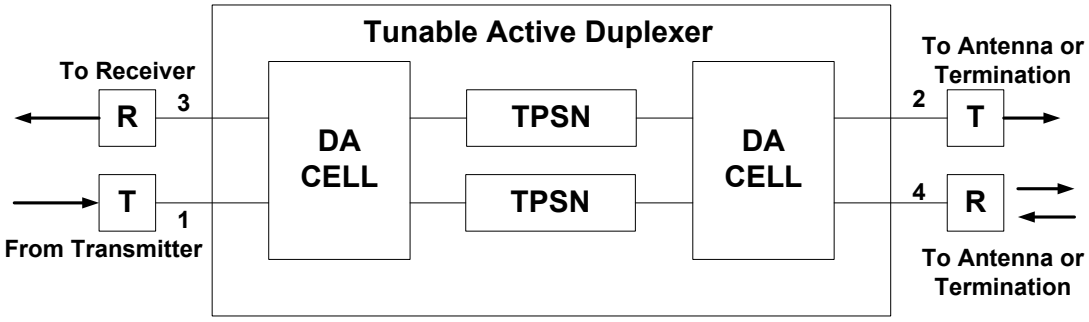


Figure. 3.11: Tx/Rx module schematic [31].

El.khatib et al. [34] proposed a CMOS based bi-directional DA as a tunable duplexer. This architecture achieves -26dB isolation and 10dB gain improvement by using an on-chip differential loop antenna, which is usually used at frequencies more than 6GHz. This circuit is impractical at UMTS frequencies and also the duplexing curve was not reported.

A filter based design employing bond wire inductors was proposed by Khatri et al. [35]. The architecture included a differential LNA with an integrated on-chip passive filter to suppress the transmitter leakage in which the receiver signal is present. To reduce packaging parasitics and chip area, a differential configuration for the filter was used as shown in Fig.3.12. In this structure the coupling capacitors are smaller than the shunt capacitors. By using mode analysis [36], the mutual coupling effect on filter response was considered. The results showed that closely placed bond wires

have a non-negligible mutual coupling effect, and as a result the ISO_{Tx} was only 10dB. The proposed circuit has been fabricated in 0.18 µm CMOS technology and

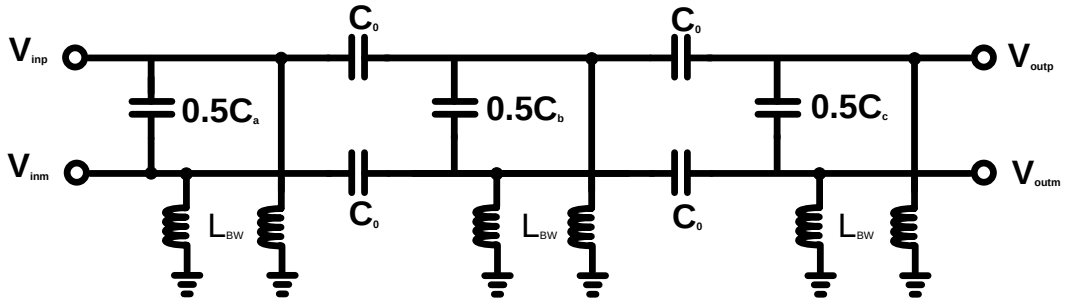


Figure. 3.12: Differential filter with equal value bond wires as inductor replacements [35].

occupies 615 µm^2 chip area. The circuit has only a transmitter leakage suppression of 10dB at 1920MHz and achieves a gain of 9.5dB at 2110MHz. However, the input and output return losses are less than -13dB. Higher performance can be attained at the expense of a higher noise figure and additional area for the filter itself.

The ninety-year-old hybrid transformer (HT) used to isolate the GO and RETURN paths on a wired telephone line was recently implemented at RF [37–40]. As presented in Fig.3.13a, the first tunable integrated electrical balanced duplexer (EBD) in CMOS technology is based on the hybrid autotransformer. The balance network is tuned to the same impedance as the antenna at both Tx and Rx frequencies, therefore, half of the Tx and Rx powers are dissipated in this network. The implemented solution achieved an acceptable isolation of 50dB, although the insertion loss of the Tx and Rx paths (4.2dB) would not attain the required UMTS duplexer requirement. To address narrowband isolation and high insertion loss issues, a new structure co-integrated with a noise matched LNA was proposed as per Fig.3.13b. Isolation of 55dB over a 250MHz bandwidth and an insertion loss of 2.5dB were measured. Fig.3.13c presents a differential implementation to address the common-mode

Tx-Rx rejection issue at the receiver port of the previous architecture. A peak isolation of -70dB was measured over a bandwidth of 190MHz at a frequency of 1950MHz.

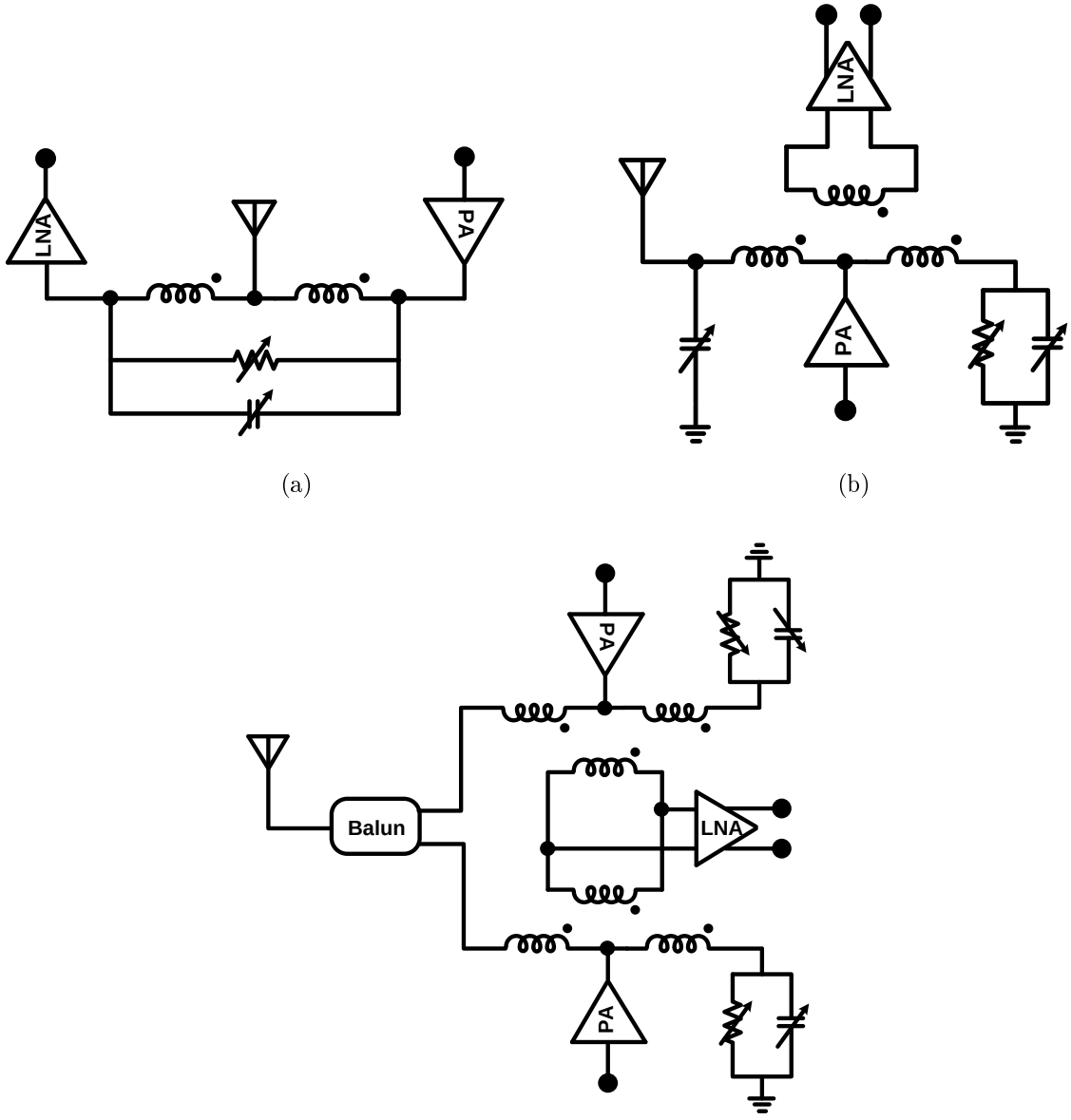


Figure. 3.13: Integrated electrical balance duplexers using (a) hybrid autotransformer [38] (b) hybrid transformer [39] (c) differential transformers [40].

In the previously discussed EBDs, the balancing load dissipates half the power and needs to be adjusted to within 0.3% of the antenna impedance to meet the 50dB isolation requirement; a very tough ask for the dynamically changing environment of a mobile handset. However, the scheme does have a wide bandwidth and could be useful in providing the first 20dB of a two-stage isolation process.

3.3 Adaptive Duplexing Methods

3.3.1 Reducing Isolation Requirements

Improving transceiver performance can reduce the Tx noise and Rx tolerance to jammers and therefore reduce the duplexer isolation requirements [41]. A feed-forward loop around the PA can cancel the receive band noise [42]. The key problem is eliminating the large Tx signal from the loop, without introducing more off-chip filters [43]. Similarly, frequency translational feed-forward and feedback loops around the receiver LNA can be used to remove strong blocking signals [44, 45]. Feedback has stability and bandwidth issues while feed-forward has phase mismatching and LO leak problems, but is still a viable option.

3.3.2 Cancelling Loops

Since the transmitter is the original source of the unwanted transmit signal and desensitising noise signal, it should be possible to isolate these signals at the transmitter and feed them into the receiver input appropriately scaled to cancel the Tx leakage. In this way the Duplexer isolation requirements can be relaxed. A number of related schemes have been reported.

Among them, a controlled amount of transmitter signal is bled into the receiver in anti-phase to cancel the unwanted transmitter leakage [46–48]. An integrated cancellation system with an analogue control loop was demonstrated in [46] as illustrated in Fig.3.14. The cancellation is applied at the LNA output to lower noise degradation

generated by the cancelling loop. The analogue control loop is implemented by a least-mean-square (LMS) adaptive filter. The output signal y(t) is correlated with the transmit signal r(t) to generate the cancelling signal z(t) such that the correlation E(r(t), y*(t)) equals to zero. This approach does not eliminate the need for the duplexer because noise in the receiver band was not cancelled. The main pros are the relaxed specifications for the duplexing filter and lower insertion loss for bands with small duplexing offset.

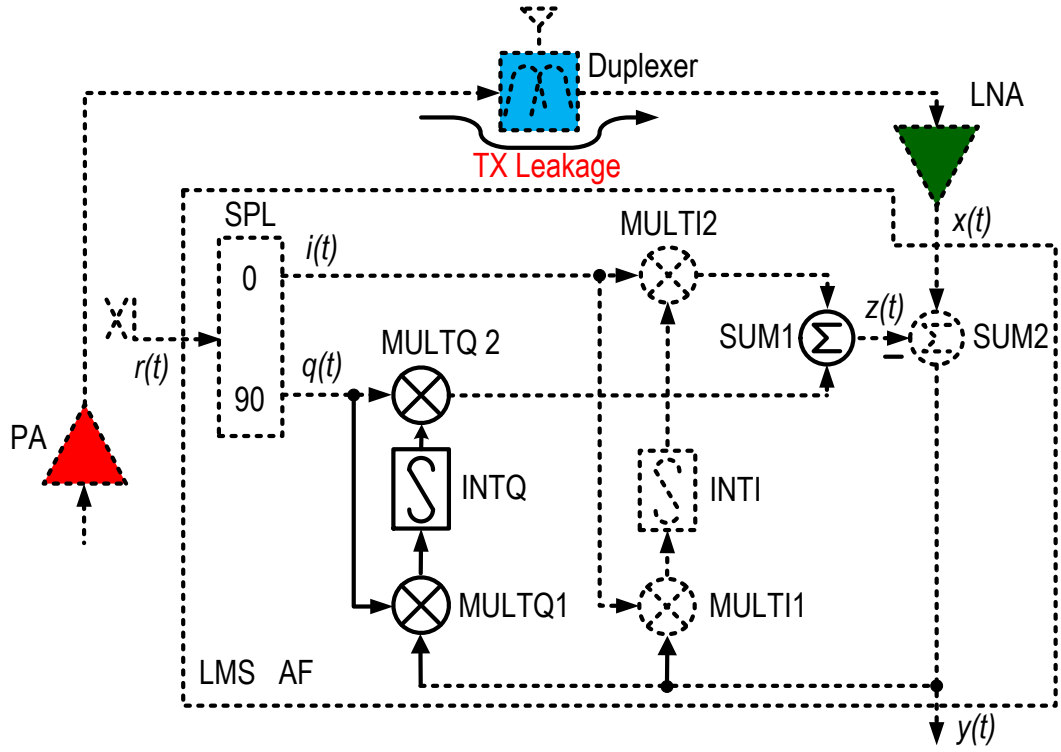


Figure. 3.14: LMS adaptive filter architecture proposed by [46].

An auxiliary up-conversion chain replaced the cancelling loops in [49, 50]. The Tx cancelling signal is generated in the baseband then up-converted with an auxiliary transmitter (AX) (Fig.3.15). This is a costly exercise and again does not cancel the Tx noise at the Rx band. Moreover, the noise from the AX is added to the noise from

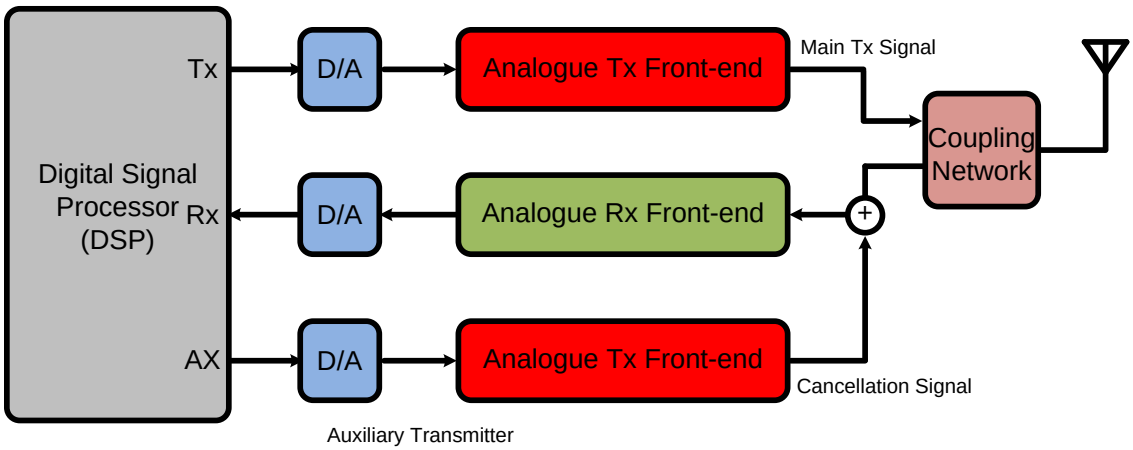


Figure. 3.15: An auxiliary up-conversion chain for active cancellation concept [49].

the main transmitter.

Only O'Sullivan et al. [51] attempted to cancel the receive band noise to enhance an existing SAW duplexer as shown in Figure 3.16. A single cancellation path was initially proposed (Fig.3.16a), however, only a narrow 2MHz cancelling bandwidth with 20dB isolation was obtained. In fact, SAW devices naturally add considerable delay to the main signal, hence, the single-path approach suffers from poorly matched group delay between the leakage and feed-forward path. In order to widen the isolation bandwidth, double-loop feed-forward paths were deployed to create two nulls at the Rx band, see Fig.3.16b. An isolation of 20dB over a 4.5MHz bandwidth was reported. The gain and phase adjustment was done by sweeping through predefined look-up-tables (LUTs). This is not realistic since antenna impedance continuously changes in handsets.

In all the above cases, the role of the cancellation unit was limited to enhancing isolation in one band only (either transmit or receive), while relying on existing duplex filters for the other band.

The most relevant work to this research, presented by Kannangara et al. [4,52,53] is a wideband adaptive duplexer architecture, attempting to obtain cancellation at both duplex bands. It is based on a two step isolation technique consisting of a low isolation

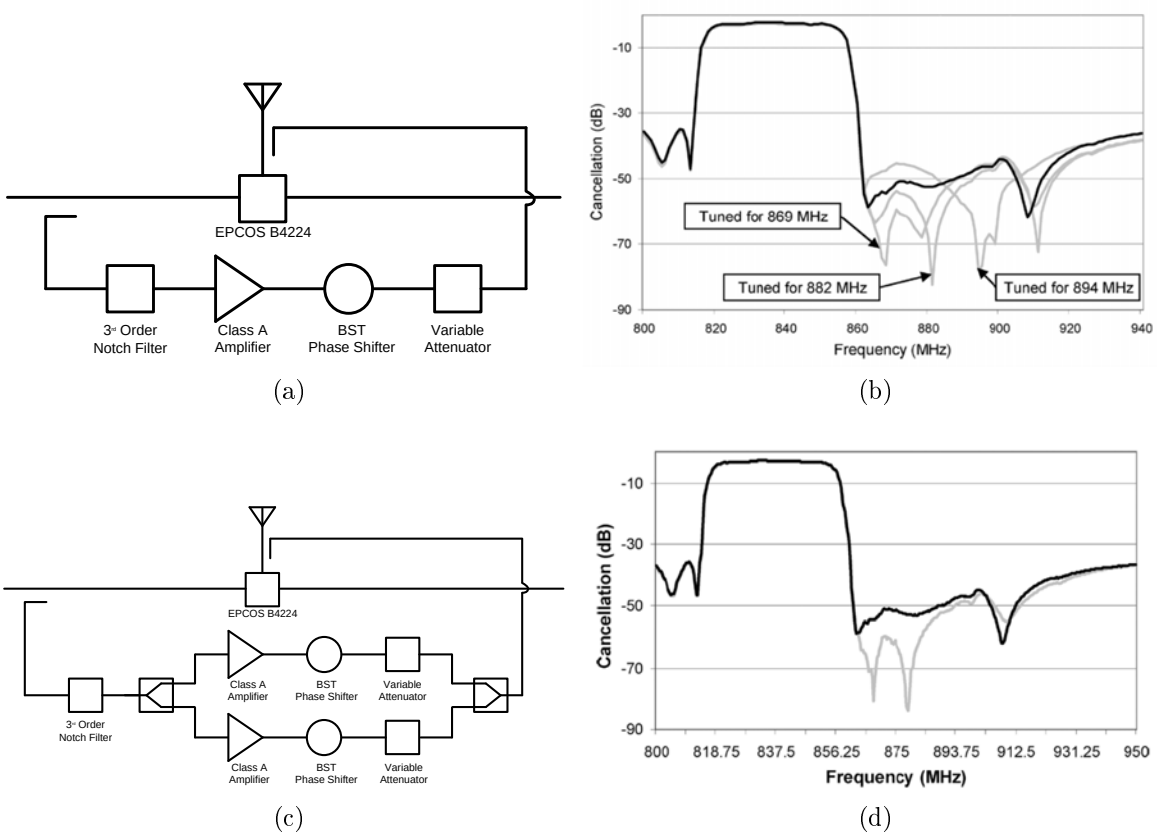
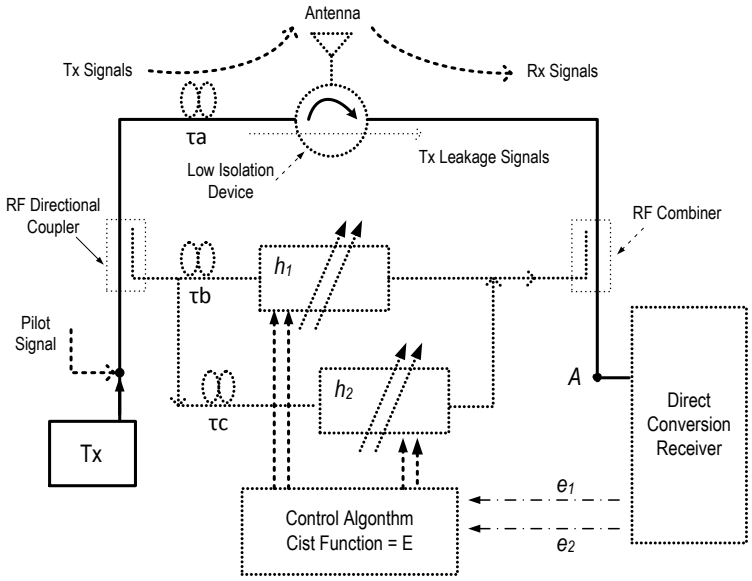
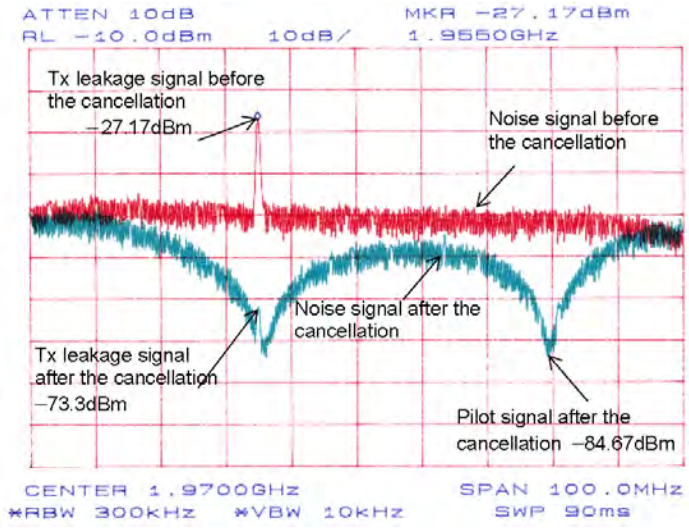


Figure. 3.16: Block diagram for the adaptive duplexer (a) single-path feed-forward operation. (b) dual-path feed-forward operation [51].

device (LID) providing approximately 20dB of initial isolation, followed by cancelling loops providing the extra 30dB. Fig.3.17a shows the proposed configuration. A passive wideband circulator is used as the LID. As discussed in Section 3.2, other alternatives for the LID are separate antennas, directional couplers, and low selectivity strip-line filters. All these devices cannot be integrated on a single chip. For further isolation, two adaptive feed-forward cancellation loops control the amount of out-of-phase signal needed to null out the remnants of the transmitter signal leaking through the LID. The circuit has two degrees of freedom which enables the formation of two nulls corresponding to the transmit and receive frequencies. The transmit signal, a low-level pilot signal, and an adaptive algorithm are used to control the cancellation loop



(a)



(b)

Figure. 3.17: Adaptive duplexer (a) a dual-path feed-forward architecture. (b) the spectrum of the received signal [52].

nulls. A basic test bed showed 66dB of cancellation (including the 20dB circulator) in the transmit band and 37dB in the receive band (Fig.3.17b); adequate for a CDMA

system [4]. The wideband circulator is only suitable for the base station when the antenna is matched. However, this would not be suitable for handheld devices due to the undetermined impedance of the antenna. A solution to the handheld problem is the focus of this Thesis.

3.4 Summary

Passive and adaptive duplexing techniques are discussed in this chapter. Passive duplexing methods include SAW and FBAR filters, dual antenna schemes, microstrip directional couplers, spatial duplexing, and duplexers manufactured using CMOS and lumped component technology. Electrical balancing duplexers are also reviewed in the latter. Adaptive duplexing architectures are mainly based on two methods: reducing the isolation requirements of transceiver and employing the cancelling loops. Both methods use various feed forward techniques implemented in analogue and digital domains, and with auxiliary transmitters.

The most relevant literature [4], presents active cancellation techniques for both Tx leakage signals and Tx noise signals in the receiver, as is discussed in Section 3.3.2. Unfortunately, the proposed architecture cannot be integrated since the passive circulator requires matched ports and is physically large in its wideband form. The major aim of this research is to replace this bulky low isolation device (LID) by tunable duplexing filters as discussed in the next chapter.

Chapter 4

Tunable Duplex Filter Design: Theory

Mobile phones must support multiple frequency bands, requiring the handset industry to include a set of RF switches and duplexers for each FDD frequency band, resulting in substantial cost. With the growing number of frequency bands, the lack of a tunable duplexer architecture is prominent. In the previous chapter, the two null adaptive duplexing architecture uses a low isolation device (LID) to provide ≈20dB of initial isolation over the target frequency range. The initial isolation is required to reduce the signal level in the cancelling loops and minimise the insertion loss of the coupler and combiner (Fig.3.17). As such it should be at least 10dB and preferably above 20dB. As mentioned, the LID is usually implemented using a circulator, a directional coupler, or an L-C duplex filter. The latter could potentially be integrated on-chip. In this chapter, the theory of such a filter is presented. It uses two different combinations of notch filters which resonate at the Tx and the Rx frequencies. Tuning and losses are key parameters to be addressed. RLC resonance theory is briefly discussed in Section 4.1. Two bandpass-bandstop filter topologies are analysed in Section 4.2, and finally a summary is given in Section 4.3.

4.1 RLC Resonance Theory

RLC resonators can be simplified to either a series or a parallel combination in order to compute the effective quality factor (Q-factor) of the network. The most fundamental definition of Q-factor (Q) relates peak energy stored in the reactive components to the average power loss of resistive elements per period. If the network can be presented as a series connection of resistances with total value of r and reactance with total value of X_{eff} ($=X_L + X_C$), then the Q_{eff} can be obtained from [54]

$$Q_{eff} = Q_s = \frac{f}{2R}\left(\frac{dX_{eff}}{df} + \frac{|X_{eff}|}{f}\right) \tag{4.1}$$

The first term of (4.1) represents the Q-factor at resonance, when the reactance X_{eff} is zero. The second term contributes to the Q-factor below and above the resonant frequency, f_{res}. The combined expression results in the $Q = \omega_{res}/R$ where the inductance is the dominant impedance ($f > f_{res}$) and $Q = 1/(\omega_{res}CR)$ where the capacitance is the dominant impedance ($f < f_{res}$), see Fig. 4.1. The stored energy is governed by the component with the highest impedance. The inductance stores most energy above f_{res}, since its reactance is larger than the reactance of the capacitance. Thus, the overall impedance has an inductive component. Below f_{res}, the capacitance stores most energy resulting in overall impedance with a capacitive behaviour.

In the parallel RLC circuit, the complex admittance ($Y = G + jB$) defines the Q-factor given by

$$Q_{eff} = Q_p = \frac{f}{2G}\left(\frac{dB_{eff}}{df} + \frac{|B_{eff}|}{f}\right) \tag{4.2}$$

For frequencies below the f_{res}, the inductance stores most energy and determines the Q_{eff}, while the capacitance element determines the Q_{eff} for frequencies above f_{res}, see Fig. 4.1. Note the Q increases when operating off resonance.

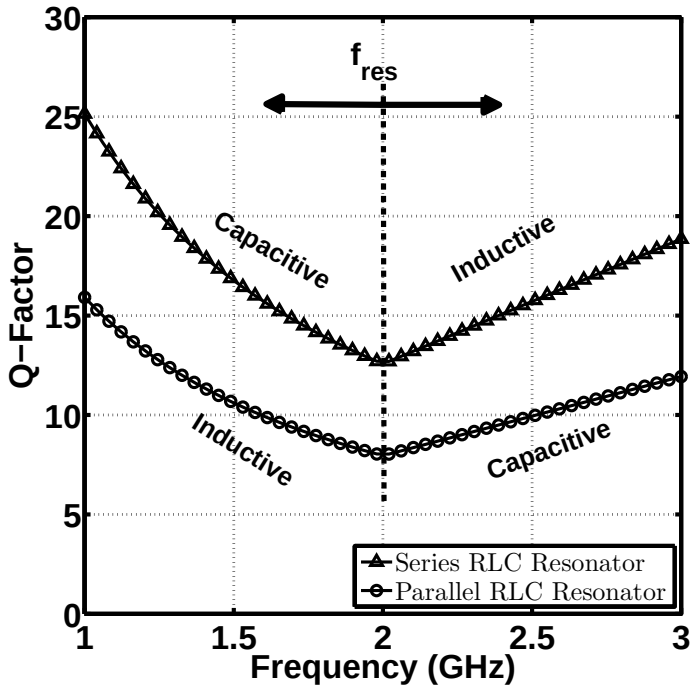
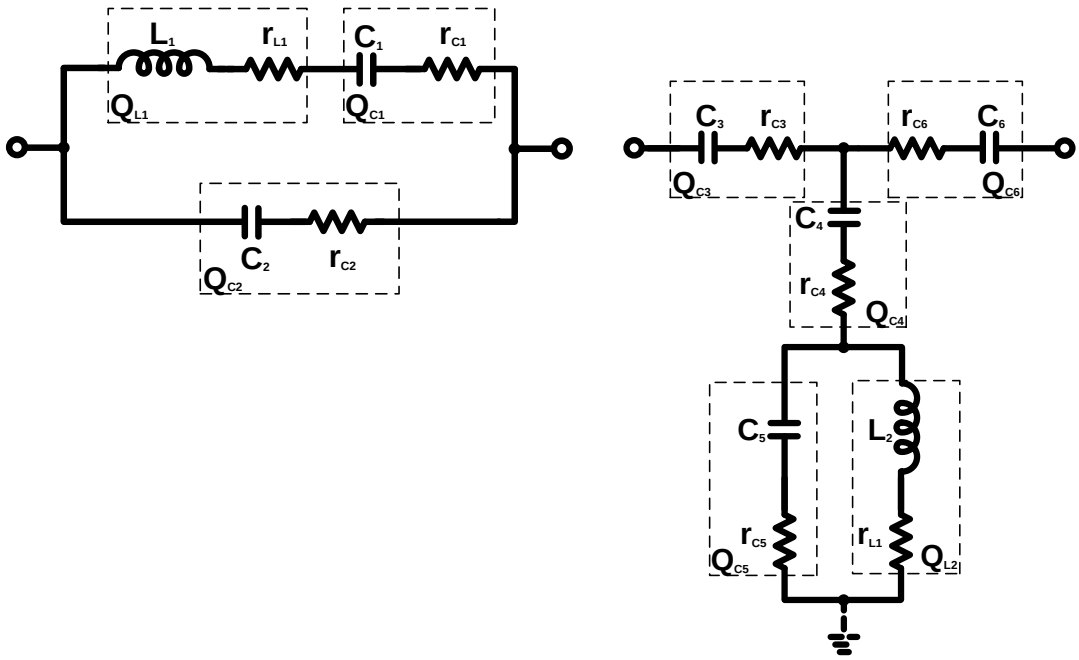


Figure. 4.1: Q-factor of an RLC resonator (f_{res}=2GHz, R=1Ω, G=0.01S, L=1nH, C=6.33pF).

4.2 Design of the Tunable Duplex Filter

On the transmit side, the duplex filter passes the transmit signal and attenuates the transmitter noise at the receive frequency. On the receive side, the transmit leakage signal is suppressed and the receive signal from the antenna passes through to the LNA. These functions can be implemented using a bandpass and notch combination. The filter can be realised by a pair of complex poles and zeroes. The pole and zero frequencies (ω_p and ω_z) determine whether the filter has a $low-frequency$ $(passband) network$ (LFN), or a $high-frequency$ $network$ (HFN) with respect to the stop-band. In order to maintain a low implementation cost of the filter, a coil-saving configuration should be used. The topology chosen uses only a single coil for the desired filter response. Fig. 4.2 illustrates the possible LFN and HFN structures to achieve the duplexing function [55].



(a) (b)

Figure. 4.2: Coil-saving filter topologies:(a) LFN (b) HFN.

4.2.1 Low-Frequency Network (LFN) Filter

The LFN is used at the Tx side to pass the low frequency transmit signal and block any noise at the higher frequency Rx band. The series combination of L_1 and C_1 resonates at the transmit angular frequency ω_{tx} and provides a low-ohmic characteristic. This resonant combination forms a reactance X_{eff} which resonates with C_2 at the receive frequency angular frequency ω_{rx} and provides a high-ohmic impedance at that frequency (Fig. 4.2a). The equivalent impedance (Z_{eq}) of the circuit in Fig. 4.2a can be written as (4.3).

$$Z_{eq}(s) = \frac{1 + s\left(C_1\left(r_{L1} + r_{C1}\right) + C_2\, r_{C2}\right) + s^2\left(C_1 C_2\, r_{C2}\left(r_{L1} + r_{C1}\right) + L_1 C_1\right) + s^3\left(L_1 C_1 C_2\, r_{C2}\right)}{s\left(C_1 + C_2\right)\left(1 + s\left(C_T\left(r_{L1} + r_{C1} + r_{C2}\right)\right) + s^2 L_1 C_T\right)} \tag{4.3}$$

For simplicity, we initially assume that the LFN network is perfectly lossless, i.e. all the series resistances are equal to zero. As a result, the Z_{eq} is simplified to (4.4).

$$Z_{eq}(s) \simeq \frac{1+s^2(L_1C_1)}{s(C_1+C_2)(1+s^2L_1C_T)} \simeq \frac{1+\frac{s^2}{\omega_z^2}}{s(C_1+C_2)\left(1+\frac{s^2}{\omega_p^2}\right)} \tag{4.4}$$

The latter expression has zero and pole complex pairs with angular frequencies

$$\omega_z \simeq \frac{1}{\sqrt{L_1C_1}} \qquad\qquad \omega_p \simeq \frac{1}{\sqrt{L_1C_T}} \tag{4.5}$$

where $C_T = \frac{C_1C_2}{C_1+C_2}$. If $C_1 << C_2$, the zero is directly adjacent to the pole creating a steep transition region between them in the plot of Z_{eq}. This is illustrated in Fig. 4.3 which plots $|Z_{eq}|$ of (4.3) versus frequency.

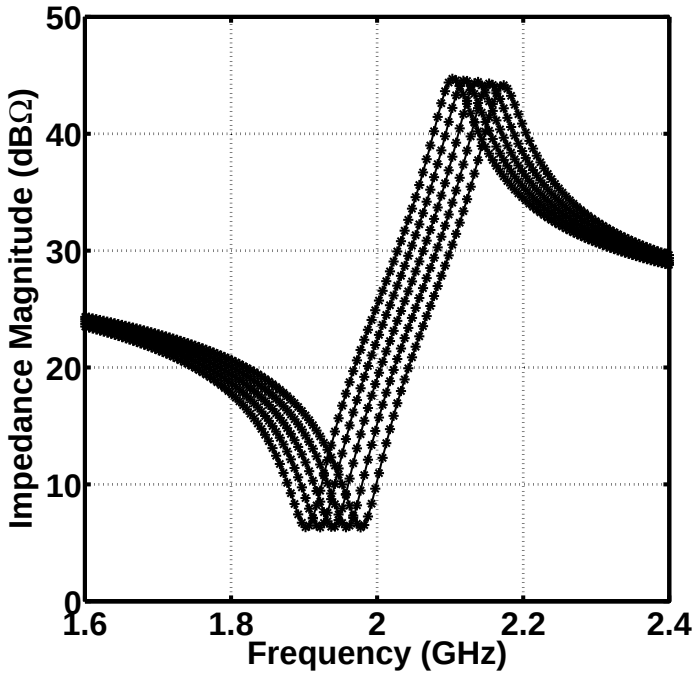


Figure. 4.3: Magnitude of Z_{eq} vs frequency for 2% increments in the nominal value of C_1 (from the right). ($Q = 100$)

We now discuss the tuning and losses of the LFN network.

4.2.1.1 Tuning

The angular duplex offset frequency (ω_d) is the difference between ω_{tx} and ω_{rx} ($\omega_d = \omega_{rx} - \omega_{tx}$). Combining the two expressions from (4.5) and noting that $\omega_z = \omega_{tx}$ and $\omega_p = \omega_{rx}$, we obtain

$$\omega_{rx} = \omega_{tx}\left(1 + \frac{C_1}{C_2}\right)^{1/2} \tag{4.6}$$

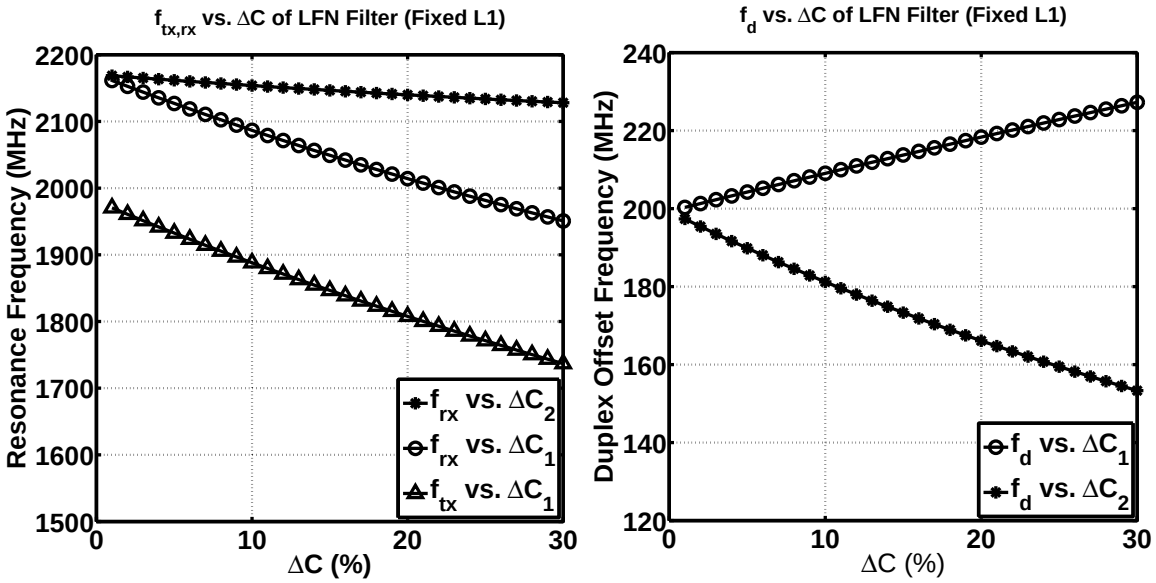
Assuming the duplex offset is small compared to ω_{tx} (i.e. small $(\frac{C_1}{C_2})$), the above equation can be simplified by using a first order Taylor expansion

$$\omega_{rx} \approx \omega_{tx}\left(1 + \frac{1}{2}\frac{C_1}{C_2}\right) \tag{4.7}$$

from which ω_d can be approximated as

$$\omega_d \approx \frac{1}{2}\omega_{tx}\left(\frac{C_1}{C_2}\right) \approx \frac{1}{2\sqrt{L_1 C_1}}\left(\frac{C_1}{C_2}\right) \tag{4.8}$$

It is clear from these equations that C_1 controls ω_{tx} and the ratio $(\frac{C_1}{C_2})$ controls ω_d. The smaller ω_d the larger is the value of C_2. From the above, a design approach would be to use C_1 to adjust ω_{tx} and then use C_2 to adjust ω_d; note C_2 does not change ω_{tx}. According to (4.8), when $C_2 >> C_1$ both the Tx and the Rx frequencies are concurrently changed when C_1 is varied resulting in an almost stable ω_d (see also Fig. 4.3 and Fig. 4.4). In most cellular frequency bands f_p is larger than f_z, for example LTE1 has $2110MHz < f_p < 2170MHz$ and $1980MHz < f_z < 1980MHz$. A frequency change in f_{tx} of 20 MHz (a typical operator allocation in LTE1) produced by a 2.2% change in C_1 causes a change in duplex offset of barely 2.47 MHz, which, in many circumstances, can be accommodated in the f_{rx} null bandwidth. Consequently, C_2 can be held constant over the whole band ($\pm$ 30 MHz) on the other hand changing C_2 will alter the duplexing frequency.



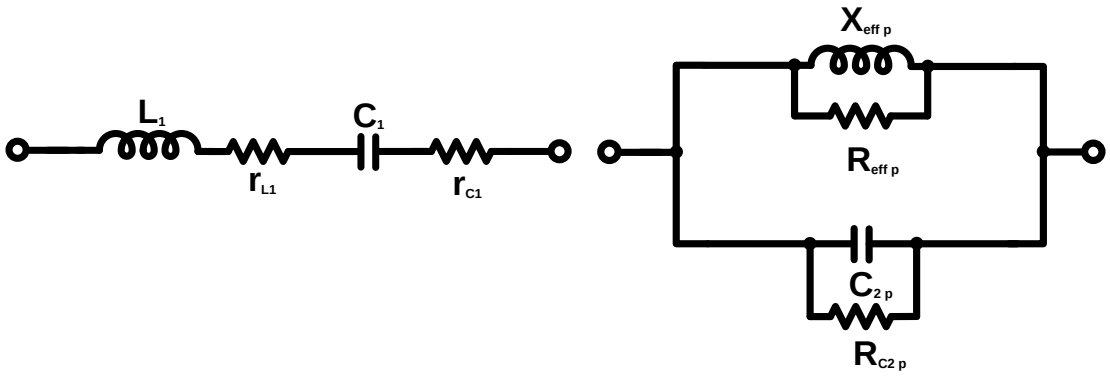
(a) (b)

Figure. 4.4: LFN frequency sensitivity to C_1 and C_2 (targeting LTE1 with $L_1 = 8.4nH$, $C_1 = 0.77pF$, and $C_2 = 3.82pF$): (a) f_{tx} and f_{rx} (b) f_d.

4.2.1.2 Losses

There is a loss associated with any passive component determined by its Q. It can be modelled as either a series or a parallel resistance. In this work, the losses related to all passive elements are modelled by series resistances r_{L1}, r_{C1}, r_{C2}, etc. The key parameters insertion loss and null depth are determined by the component Q's. In this thesis all Q's, reactances and impedance levels are defined at f_{tx} unless otherwise stated. In Fig. 4.2a, the series combination of L_1 and C_1 resonates at ω_{tx} providing a resistance $r_{tot} = r_{L1} + r_{C1}$. The Q of the resonator is $Q_{tx} = \frac{\omega_{tx} L_1}{r_{tot}}$ (Fig. 4.5a), and the insertion loss is

$$IL_{TX} = 20 \log_{10} \left(1 + \frac{r_{tot}}{R_s + R_L} \right) \tag{4.9}$$



(a) (b)

Figure. 4.5: LFN equivalent circuit resonating at: (a) f_{tx} (b) f_{rx}.

When source and load resistances are equal ($R_S = R_L$), the insertion loss becomes

$$IL_{TX} = 20\log_{10}\left(1 + \frac{\left(\frac{X_{L1}}{R_L}\right)\Big/ Q_{L1} + \left(\frac{X_{C1}}{R_L}\right)\Big/ Q_{C1}}{2}\right) \tag{4.10}$$

At ω_{rx}, which is above ω_{tx}, the resonant combination L_1,C_1 provides an effective reactance X_{eff} with an associated Q_{eff}.

$$\begin{aligned} X_{eff} = \omega_{rx}L_1 - \frac{1}{\omega_{rx}C_1} = \omega_{rx}\left(\frac{L_1C_1\omega_{rx}^2 - 1}{C_1\omega_{rx}^2}\right) \\ Q_{eff} = \frac{\omega_{rx}}{r_{tot}}\left(\frac{L_1C_1\omega_{rx}^2 - 1}{C_1\omega_{rx}^2}\right) \end{aligned} \tag{4.11}$$

Converting to a parallel circuit representation better suited to the evaluation of the parallel resonance at ω_{rx} yields

$$\begin{aligned} X_{eff\,p} = X_{eff}\left(\frac{1 + Q_{eff}^2}{Q_{eff}^2}\right) \\ R_{eff\,p} = Q_{eff}\ X_{eff} \end{aligned} \tag{4.12}$$

The effective parallel resistance is combined with the parallel resistance representation of the lossy capacitor C_2 (Fig. 4.5b), $R_{C2\,p} = r_{C2}(1 + Q_{C2}^2/(1+\Delta)^2)$ where Δ is the fractional duplex frequency ($\Delta = \frac{f_d}{f_{tx}}$) and the $(1-\Delta)^2$ term converts Q_{C2} (defined at f_{tx}) to f_{rx}. At ω_{rx}, $X_{eff\,p}$ resonates with $C_{2\,p}$ giving a resistance between the ports of R_{tot}. The null-depth becomes

$$ISO_{RX} = 20\log_{10}\left(1 + \frac{R_{tot}}{R_s + R_L}\right) \tag{4.13}$$

where $\frac{1}{R_{tot}} = \frac{1}{R_{eff\,p}} + \frac{1}{R_{C2\,p}}$. Fig. 4.6a and Fig. 4.6b show the IL_{TX} and ISO_{RX} for different Q's of the inductance L_1 and the capacitances C_1 and C_2. Component values are the same as for Fig. 4.4. There is little to be gained by vastly increasing the Q of one component over the other. The Q of C_2 has little impact on the null-depth indicating losses are heavily dependent on the primary resonant circuit ($L_1 - C_1$). The closer in frequency the null is to the passband, the lower the Q_{eff} of the resonator; setting $\omega_{rx}^2 = 1/(L_1C_1)$ in (4.11) would result in Q_{eff} equal to zero. There is also a trade-off between null-depth and insertion loss. Choosing components with the higher impedance (larger L and smaller C) will improve null-depth at the expense of insertion loss. Fig. 4.6.c and Fig. 4.6.d show contours of IL_{TX} and ISO_{RX} plotted against normalised inductor impedance ($\frac{X_L}{R_L}$) for different Q; where all components have the same Q. Note that the load impedance (R_L) is not always 50Ω. The left hand plot is for Δ of 10% and the right hand plot is for 5%. These two values cover most of the common LTE bands. The plots describe the trade-off between insertion loss and isolation. For example, starting with the upper red curves, a specified null-depth (isolation) of 10dB with component Q's of 25 requires a normalised impedance of 8.5 (marked 1). Using this value of normalised impedance and the lower blue curves (marked 2), the resulting insertion loss of $2.7dB$ is obtained (marked 3). At the lower duplexing offset, the same Q and null-depth require a normalised impedance of 25 and results in a somewhat degraded insertion loss of $6.0dB$. Similarly, increasing the isolation to $20dB$ increases the impedance to 35 and the insertion loss to $7.9dB$. Peak voltage

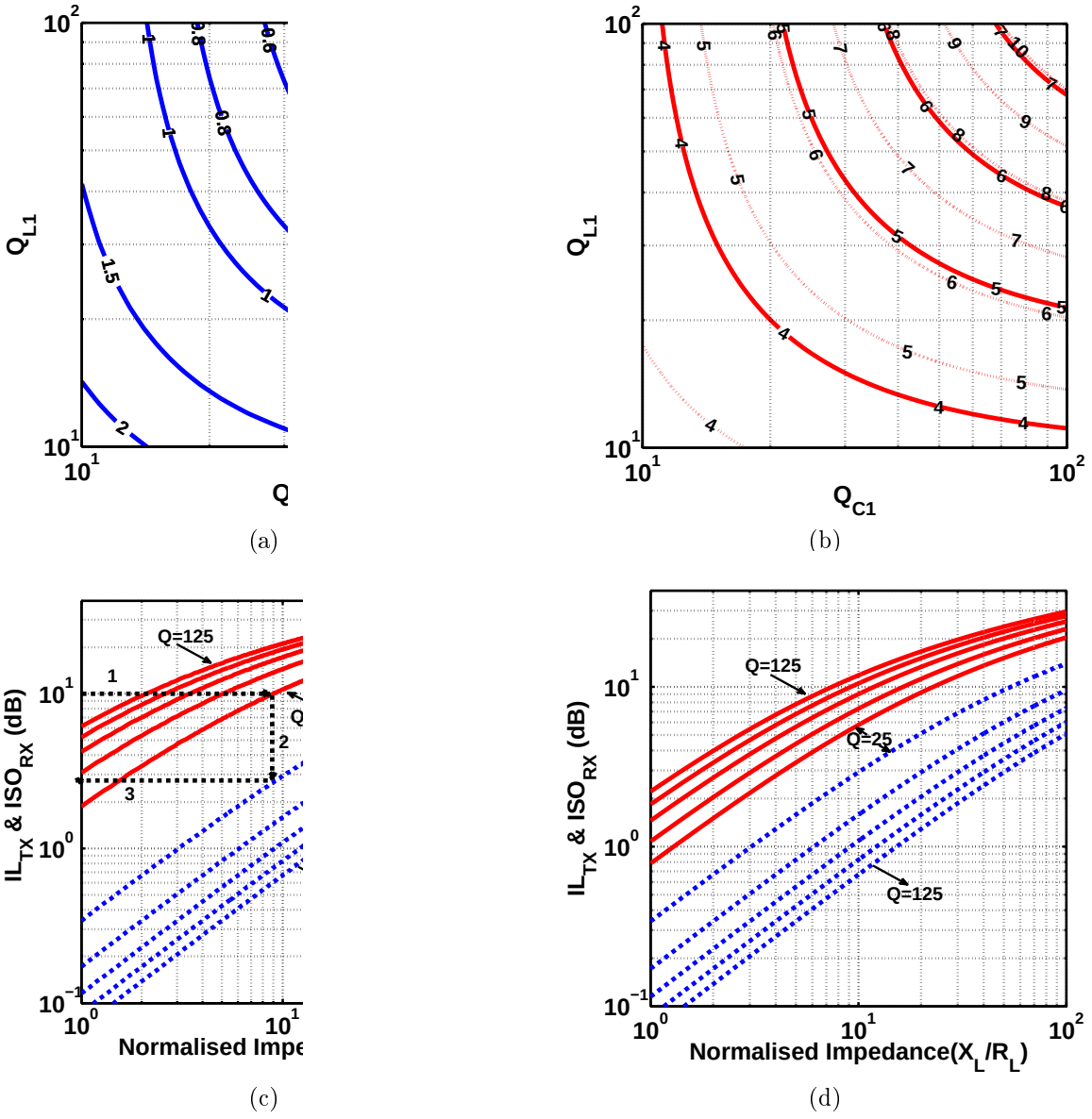


Figure. 4.6: LFN design trade-offs (a) IL_{TX} for different Q_{L1} and Q_{C1} (contours in dB) (b) ISO_{RX} for different Q_{L1}, Q_{C1} with Q_{C2}=10 (Solid) and Q_{C2}=120 (Dotted). IL_{TX} (Dotted blue) and ISO_{RX} (Solid red) plots versus normalised impedance level for different Q's (increments of 25) (c) $\Delta = 10\%$ (190 MHz) (d) $\Delta = 5\%$ (95MHz).

constraints give one practical limit to the maximum usable impedance, another is the inductor chip area which increases with inductance. Improving the insertion loss can be achieved by higher Q's and operating at lower normalised impedances.

Table 4.1 summarises the IL_{Tx} versus ISO_{Rx} trade-off. Typically the performance at a Q of 25 is what might be hoped for in a fully integrated SOS solution which benefits from the improved inductors relative to bulk CMOS. Even so IL_{Tx} at 5dB is a bit high at the minimum required 15dB isolation. In reality the all integrated solution is limited to LTE band 1 ($\Delta = 10\%$). On the other hand, chip inductors now have Q's above 100 and therefore a discrete solution would have insertion loss of less than 0.5dB at the same isolation level. Even with a lower $\Delta = 5\%$ the insertion loss is still a respectable 2.8dB.

Table 4.1: Summary of IL_{Tx} versus ISO_{Rx} for three Q's in the LFN filter. ($\Delta = 10\%$)

IL_{Tx} **(dB)**	ISO_{Rx}**=10dB**	ISO_{Rx}**=15dB**	ISO_{Rx}**=20dB**
Q=25	2.7	4.93	7.9
Q=50	0.85	1.8	3.2
Q=100	0.2	0.47	0.9

4.2.2 High-Frequency Network (HFN) Filter

The HFN network is on the receive side and blocks low frequency Tx and passes the high frequency Rx signals. In Fig. 4.2b, the parallel combination of L_2 and C_5 resonates at ω_{rx} providing a high-ohmic impedance. This resonant tank provides a reactance X_{eff} that resonates with C_4 at ω_{tx}, resulting in a low impedance. For simplicity, we initially assume that the HFN network is perfectly lossless and the effects of C_3 and C_6 are also neglected. The zero and pole complex pairs are

$$\omega_z \simeq \frac{1}{\sqrt{L_2 C_T}} \qquad\qquad \omega_p \simeq \frac{1}{\sqrt{L_2 C_5}} \tag{4.14}$$

where $C_T = C_4 + C_5$. If $C_4 << C_5$, the pole is directly adjacent to the zero creating a steep transition region in the plot of Z_{eq}.

4.2.2.1 Tuning

Setting $\omega_z = \omega_{tx}$ and $\omega_p = \omega_{rx}$ and assuming that the duplex offset is small compared to ω_{tx} (i.e. small (C_4/C_5)), ω_d can be simplified similar to the LFN case

$$\omega_d \approx \frac{1}{2}\omega_{rx}\left(\frac{C_4}{C_5}\right) \approx \frac{1}{2\sqrt{L_2 C_5}}\left(\frac{C_4}{C_5}\right) \tag{4.15}$$

It is clear that C_5 controls ω_{rx} and the ratio C_4/C_5 controls ω_d. The smaller ω_d the smaller the value of C_4. From the above, a design approach would be to use C_5 to adjust the notch to ω_{rx} and then use C_4 to adjust the passband. Fig. 4.7 shows that when $C_4 << C_5$, a frequency change in f_{rx} of 20MHz produced by a 2% change in C_5 causes a change in duplex offset of 4.9MHz. Consequently, C_4 can be adjusted to compensate the f_d change or held constant depending on the null bandwidth.

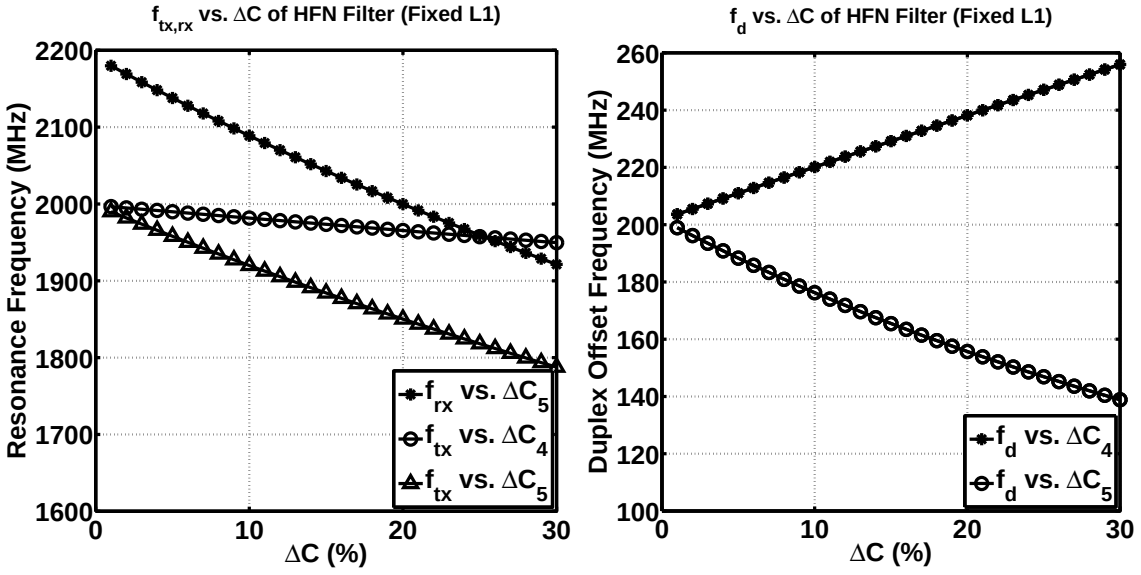


Figure. 4.7: HFN frequency sensitivity to C_4 and C_5 (targeting LTE1): (a) f_{tx} and f_{rx} (b) f_d.

4.2.2.2 Losses

In Fig. 4.8a, the parallel combination of L_2 and C_5 resonates at ω_{rx} giving the resistance $\frac{1}{R_{tot}} = \frac{1}{R_{L2}} + \frac{1}{R_{C5}}$. The Q of the primary resonator is $Q_{rx} = \frac{R_{tot}}{\omega_{rx} L_2}$ and the insertion loss is

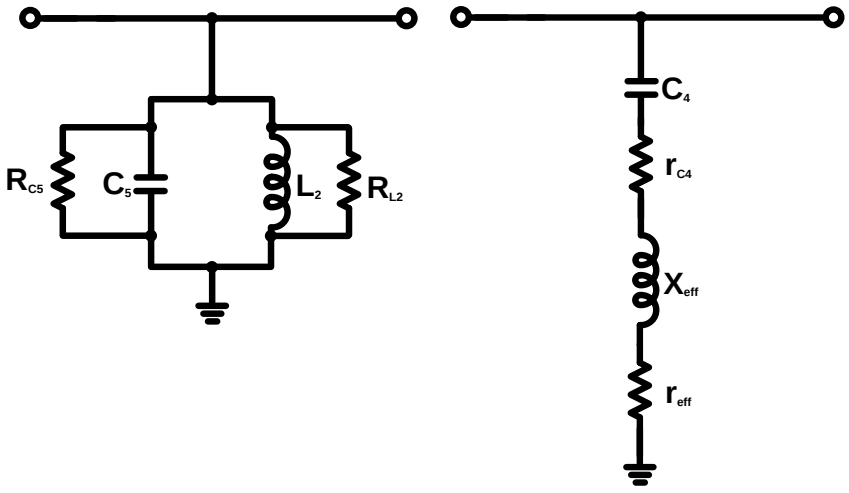
$$IL_{RX} = 20\log_{10}\left(\frac{R_L\left(R_s + R_L \| R_{tot}\right)}{\left(R_s + R_L\right)\left(R_L \| R_{tot}\right)}\right) \tag{4.16}$$

At ω_{tx}, the series representation of the tank, X_{eff}, and its associated Q_{eff} are

$$\begin{aligned} Q_{eff} &= \frac{R_{tot}}{\omega_{tx}\left(\frac{L_2}{1-L_2C_5\omega_{tx}^2}\right)} \\ X_{eff} &= \omega_{tx}\left(\frac{L_2}{1-L_2C_5\omega_{tx}^2}\right)\left(\frac{Q_{eff}^2}{1+Q_{eff}^2}\right) \end{aligned} \tag{4.17}$$

from which $r_{eff} = \frac{X_{eff}}{Q_{eff}}$. At ω_{tx}, X_{eff} resonates with C_4 giving a resistance r_{tot} and the null-depth becomes

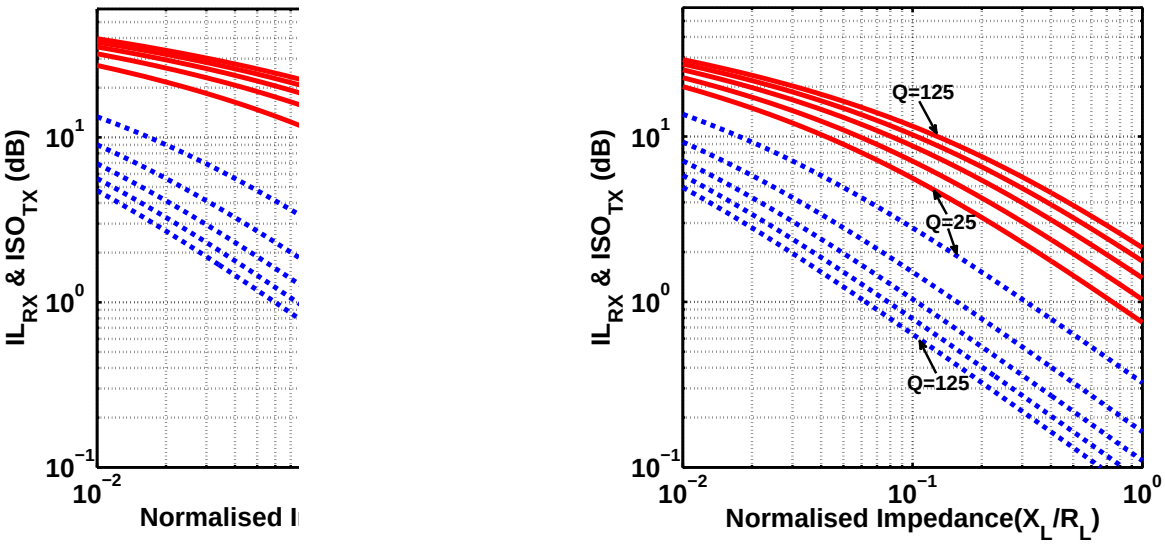
$$ISO_{TX} = 20\log_{10}\left(\frac{R_L\left(R_s + R_L \| r_{tot}\right)}{\left(R_s + R_L\right)\left(R_L \| r_{tot}\right)}\right) \tag{4.18}$$



(a) (b)

Figure. 4.8: HFN equivalent circuit resonating at: (a) f_{rx} (b) f_{tx}.

where $r_{tot} = r_{eff} + r_{C4}$. If all components have the same Q then Fig. 4.9 shows the IL_{RX}/ISO_{TX} trade-off with normalised inductor impedance level and Q. For f_d equal to 10% of f_{tx}, a normalised impedance of 0.18 at Q of 50 gives an IL_{TX} and ISO_{Rx} of 0.83dB and 10dB, respectively. The Q must be increased to about 95 to obtain the same performance at an f_d equal to 5% of f_{tx}. Lower impedance levels are required for increased null-depths.



(a) (b)

Figure. 4.9: HFN IL_{RX} (Solid red) and ISO_{TX} (Dotted blue) plots versus normalised impedance level and different Q's (increments of 25): (a) $\Delta = 10\%$ (b) $\Delta = 5\%$.

4.2.3 Duplexing Concept

The LFN and HFN are combined together as depicted in Fig. 4.10. The HFN on the receive side would short the antenna to ground at the Tx frequency unless they are separated by an impedance. A traditional duplexer design would use a ninety degree transmission line in order to transform the short-circuit impedance to an open-circuit characteristic seen by the antenna [56, 57]. This would require too large chip area to be a practical alternative, thus a capacitor C_3 is used here instead. An inductor

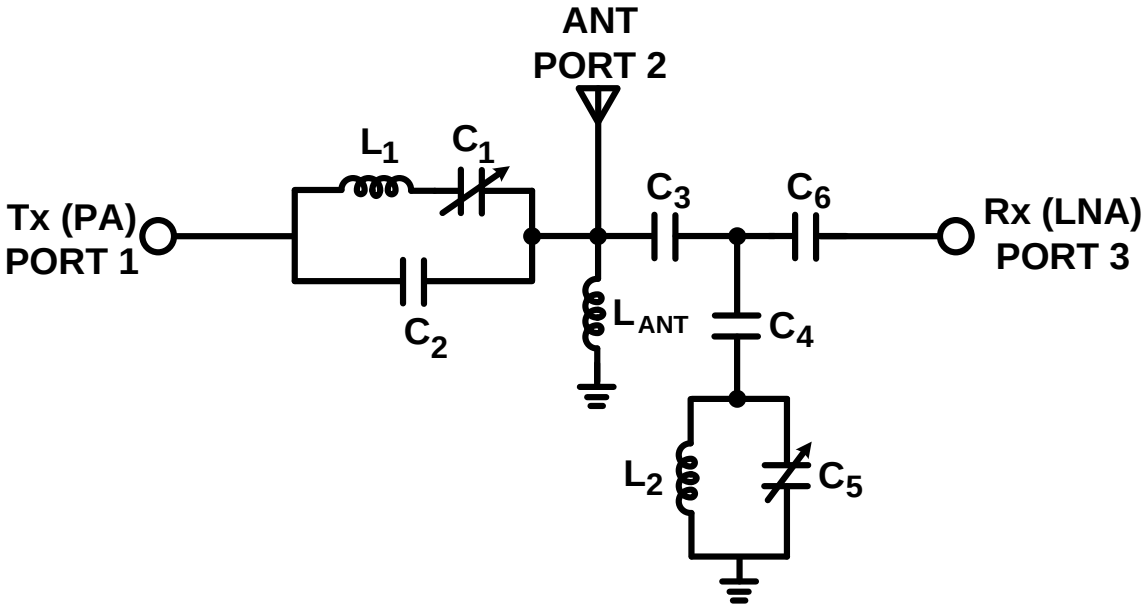


Figure. 4.10: Proposed tunable duplex filter configuration.

(L_{ant}) resonates with C_3 to present an open-circuit. Such an inductance can be absorbed into an antenna-tuning unit (ATU), which is common in mobile phones. These components introduce a penalty in IL_{RX} of about 1.5dB. The capacitances C_1 and C_5 are adjusted to give channel-tuning range of 80MHz in eight steps using a binary weighted digitally switched capacitor bank (DSCB). Resonance can produce high voltages, which prevents the possibility of using varactor devices. A feasible solution is to use a switched capacitor bank with a number of stacked transistors for handling higher voltages. It is possible to estimate a worst-case voltage by assuming lossless components. The LFN resonant circuit on the transmit side (L_1-C_1) must pass a current equal to that passing through the load $I_L = \sqrt{\frac{P}{R_L}}$. The voltage across C_1 ($\widehat{V}_{C1}$) has the same amplitude as that across L_1, equal to $I_L X_{L1}$. This leads to the following equation for $\widehat{V}_{C1}$

$$\log_{10}\left(\frac{\hat{V}_{C1}}{\sqrt{R_L}}\right) = \log_{10}\left(\frac{X_L}{R_L}\right) + \frac{P_{dBm}}{20} - 1.5 + \log_{10}\left(\sqrt{2}\right) \tag{4.19}$$

A similar equation can be derived for the HFN network, noting the resonance now occurs between X_{eff} and X_{C4},

$$\log_{10}\left(\frac{\hat{V}_{C4}}{\sqrt{R_L}}\right) = \log_{10}\left(\frac{C_3}{C_4}\right) + \frac{P_{dBm}}{20} - 1.5 + \log_{10}\left(\sqrt{2}\right) \tag{4.20}$$

Both equations can be plotted on the same axis shown in Fig. 4.11. Note the log axes and contours as well as the voltage normalisation by $\sqrt{R_L}$.

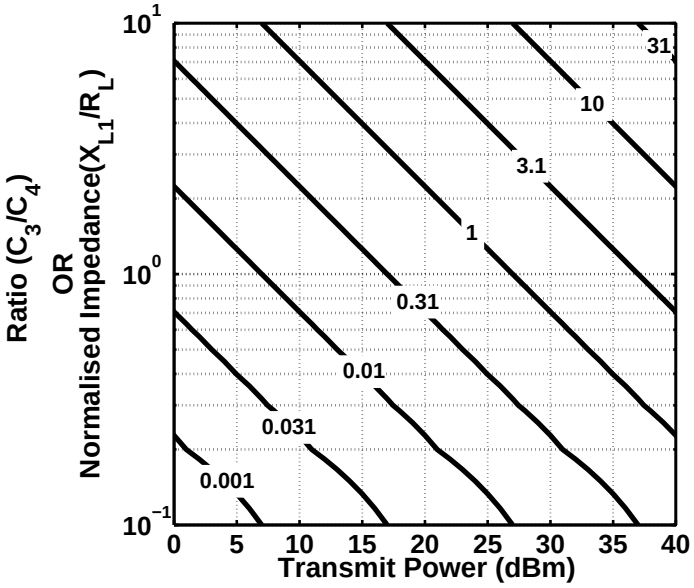


Figure. 4.11: Normalised peak voltage ($\frac{\widehat{V}_C}{\sqrt{R_L}}$) contours across C_1 and C_4 at f_{tx} versus TX power and normalised impedance. (note: The component Q's are pinned to infinity.)

If a peak power of 30dBm is expected in the LFN case and $\frac{X_{C1}}{R_L}$ is 5.1, the $\widehat{V}_{C1}$ is approximately 51V. Such a high voltage has implications on the number of stacked transistors required for the switches. In the next section, we will further discuss the implementation of the switched-capacitor bank.

To address the large voltage peak issue, a 'dual' LFN filter topology is proposed, see Fig.4.12; the structure has a lower peak voltage, however, the circuit experiences

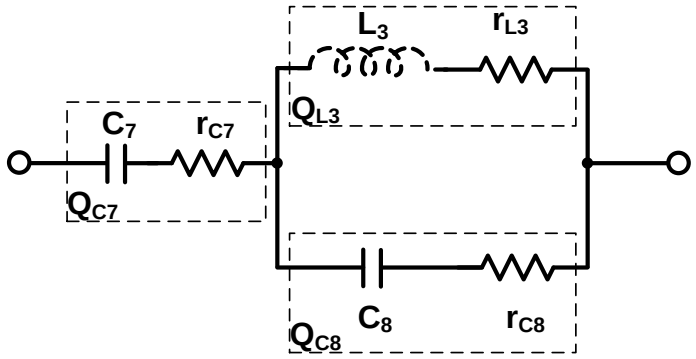


Figure. 4.12: Proposed coil-saving (dual) LFN filter topology.

a higher peak current at resonance. It is worthwhile to highlight that since the maximum voltage level is lower, less transistors are stacked in a switched capacitor unit, increasing Q-factor. Assuming lossless components, the f_{tx} and the f_{rx}, and consequently f_d vary with C_7 and C_8 as per Fig. 4.13a and Fig. 4.13b. The parallel combination of L_3 and C_8 resonates at ω_{rx} producing a high impedance. This resonant combination forms a reactance X_{eff} which resonates with C_7 and creates a low impedance at ω_{tx}. The IL_{TX} and ISO_{RX} versus normalised inductance value (X_{L3}/R_L) and Q are plotted in Fig. 4.13c and Fig. 4.13d. The circuit operates at much lower impedance levels, which reduces footprint, but can make the circuit sensitive to small resistances in the interconnect between components. Again with $\Delta = \frac{f_d}{f_{tx}}$ as the fractional duplex frequency, the X_{eff} at the f_{tx} is given by

$$X_{eff} = \frac{X_{L3}}{2\Delta}\left(\frac{(1+\Delta)^2}{1+\Delta/2}\right) \tag{4.21}$$

which is equal to X_{C7} at resonance ω_{tx}. The worse-case peak voltage across C_7 ($\hat{V}_{C7}$) and X_{eff} is equal to $\sqrt{\frac{P}{R_L}}X_{C7}$, leading to

$$\log_{10}\left(\frac{\hat{V}_{C7}}{\sqrt{R_L}}\right) = \log_{10}\left(\frac{X_{C7}}{R_L}\right) + \frac{P_{dBm}}{20} - 1.5 + \log_{10}\left(\sqrt{2}\right) \tag{4.22}$$

which is the same as (4.19) with X_{L1} replaced by $X_{C7}(= X_{eff})$. The peak current in

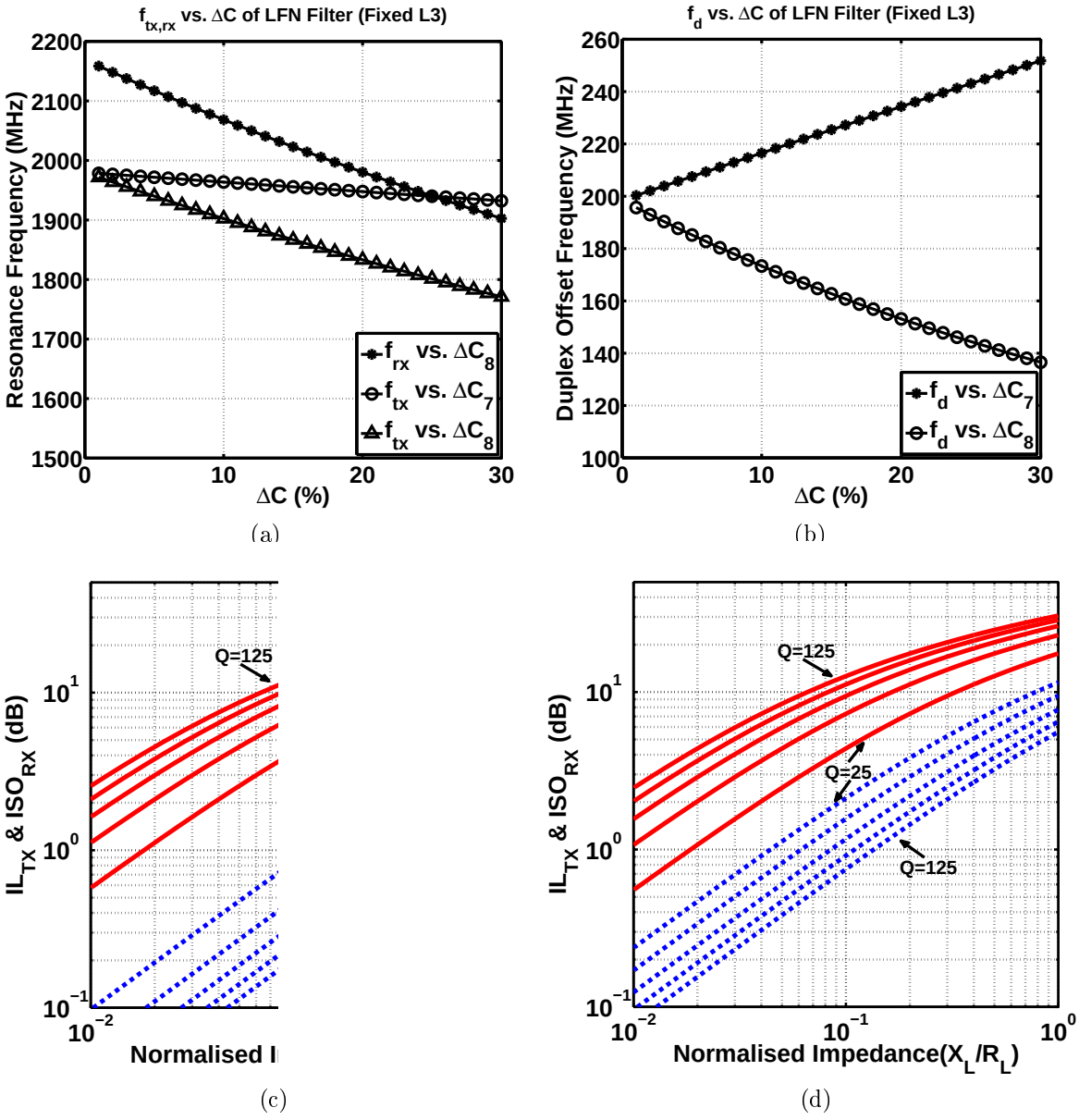


Figure. 4.13: The LFN filter performance- TOP: Tuning of C_7 and C_8: (a) f_{tx} and f_{rx} (b) f_d. BOT: IL_{TX} (Solid red) and ISO_{RX} (Dotted blue) plots versus normalised impedance level for different Q's (increments of 20) (c) $\Delta = 10\%$ (d) $\Delta = 5\%$.

the inductor (L_3) relative to the load current (i_{R_L}) is given by $\alpha = i_{L_3}/i_{R_L}$.

$$\alpha_{L_3} = \frac{X_{eff}}{X_{L_3}} = \frac{(1+\Delta)^2}{2\Delta\left(1+\Delta/2\right)} \tag{4.23}$$

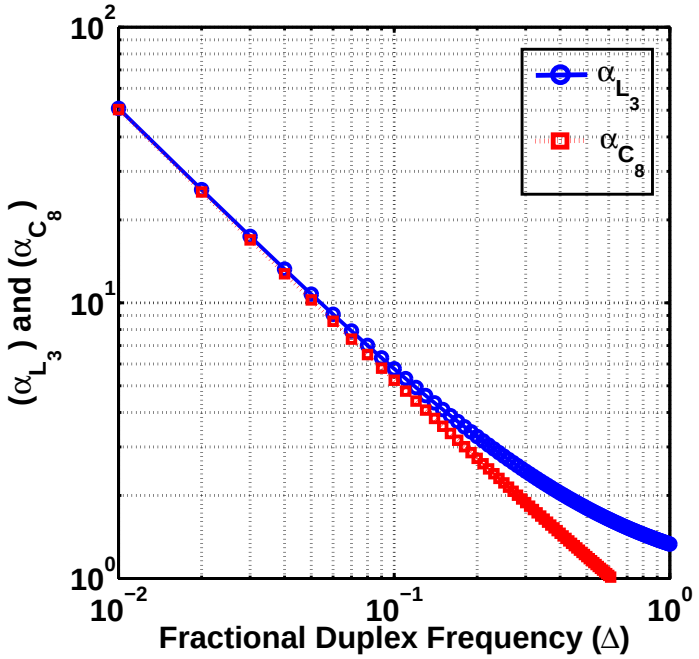


Figure. 4.14: Peak Current through L_3 (Solid blue) and C_8 (Dotted red) normalised to the load current versus Δ for Fig. 4.12.

similarly for capacitor C_8

$$\alpha_{C_8} = \frac{X_{eff}}{X_{C_8}} = \frac{(1+\Delta)}{2\Delta\left(1+\Delta/2\right)} \tag{4.24}$$

which is plotted in Fig. 4.14. The peak current increases as the fractional duplex frequency reduces. For a 10dB null-depth with a Q of 50 at LTE1, a normalised impedance level of 0.158 is required and this gives an IL_{TX} of 0.83dB (Fig. 4.13c). X_{eff} (obtained from (4.21)) can be used in (4.22) or Fig.4.11 to calculate a peak voltage across C_7 of 9.1V. This is about 18% of that experienced by C_1 in the first circuit. However, the peak current is considerably increased with the inductor experiencing 1.15A, or $\alpha_{L_3} = 5.7$ times the load current, compared with $\alpha_{L_1} = 1$ for the original LFN circuit. The capacitor C_8 carries slightly less current with $\alpha_{C_8} = 5.2$, which is close to the voltage magnification of the first LFN circuit (as would be expected considering the dual nature of the circuits). The large current magnification

has implication on the width of the FET switches. If (I^2R_{ON}) losses are to be the same for both circuits, the R_{ON} of the second LFN should be $1/(\alpha_{C_8})^2$ of that of the first LFN. Consequently, the active switching area of both circuits is the same with the stack reducing by α_{C_8} and the width increasing by α_{C_8}. Fig.4.15 illustrates the new LFN in a tunable duplex filter topology.

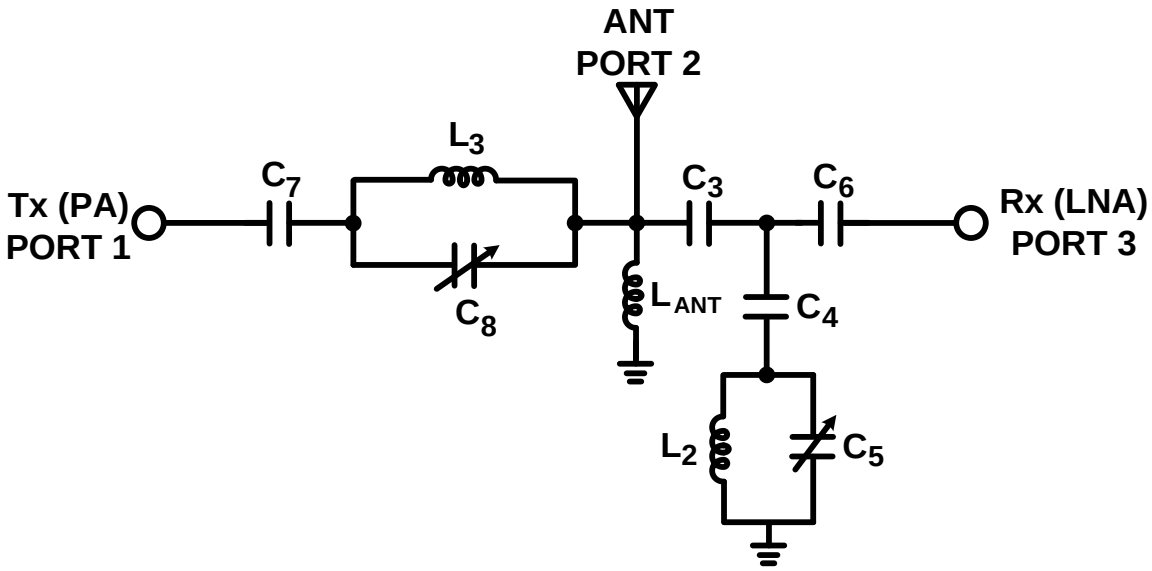


Figure. 4.15: Proposed tunable duplex filter configuration modified for the LFN filter.

4.3 Summary

In this chapter, two bandpass-bandstop filters are introduced named "LFN and HFN" to act as an LID required for the adaptive duplexing structure. We theoretically show that null-depth and insertion loss are determined by the impedance level and Q of the components; higher impedance levels improve isolation (null-depths) at the expense of insertion loss for the LFN, and vice-versa for the HFN. Considering LTE1 having a 10% duplex frequency offset, an LFN with 10dB isolation (null-depth) requires a normalised impedance level of $(5.1 \times R_L)$ for component Q's of 50. This gives an insertion loss of 0.85dB. Higher Q passive components are required to achieve lower

insertion loss and higher isolation.

There are two possible LFN networks, which are duals of each other. For input powers of 30dBm, one suffers from enhanced peak voltages (≈51V), while the other has enhanced current (≈1.15A) in the resonant circuits. The choice of network depends on the implementation technology.

If the proposed tunable duplex filters are to be integrated on-chip it is important to employ a silicon-based technology compatible with existing wireless systems. For example, wireless front-end modules are implemented on Silicon-on-Sapphire (SOS) or Silicon-on-Insulator (SOI) technologies due to the low parasitic effect of the substrate as well as relatively high-Q passive components. These technologies were therefore chosen.

The next chapter compares Peregrine 0.25 µm UltraCMOS and STMicroelectronics 0.13 µm HR-SOI processes in terms of process flow, available devices, and RF switching performance.

Chapter 5

Silicon-on-Insulator Technologies

The ever-increasing demand for wireless data bandwidth and the development of the LTE-Advanced standard has increased the push for higher levels of integration of the wireless's radio frequency functions. All the while, the ever increasing number of bands the RF circuits must contend with leads to toughening specifications. Today, the entire radio is contained in a few devices (chips) with some external passive components. There are two major silicon technologies found in every corner of a mobile handset, Bulk CMOS (Complementary Metal-Oxide Semiconductor) and SOI (Silicon-on-Insulator).

SOI technology has been around since the 1960s when the first so-called silicon-on-sapphire (SOS) process was introduced. It differs from the traditional bulk CMOS process due to the presence of a buried oxide layer under the active area of the silicon substrate, which forms a dielectric-ally isolated transistor [58]. This oxide layer has a very important impact on the physical behaviour of MOS transistors and the provided benefits are numerous such as improved immunity to radiation and latch-up phenomena, lower leakage currents and lower junction capacitances.

SOI was first studied for hardening circuits such as spacecraft electronics and devices operating in a radiative nuclear environment. However, the poor quality of SOI materials had long limited its industrial development for the electronics consumer

market. Improving the quality of the buried oxide of thin silicon films on top of an insulator recently revived interest in the technology [59]. In the eyes of industry, it has many advantages in terms of integration, power consumption and immunity to soft errors. Unlike the Bulk CMOS process, it is only in recent years that SOI technology has found its pathway into cellular phones. The low parasitics of SOI have recently been exploited as a switching technology for RF signals. It is now replacing GaAs technology in the RF front-end of mobile phones.

This chapter focuses on SOI/SOS technology and its properties. Section 5.1 addresses the realization of SOI materials, giving the main fabrication methods and the latest technology. Section 5.2 briefly compares Bulk CMOS technology with the SOI/SOS processes. Peregrine UltraCMOS and STMicroelectronics HR-SOI process features are briefly discussed in Section 5.3 and Section 5.4, respectively. Section 5.5 presents the basic theory and resulting design compromises regarding RF FET switches. The trade-off between the latter's power handling capability, linearity and insertion loss is provided for the SOS case. The figure of merit (FOM) for a FET switch is defined, then SOS and SOI structures are compared. Keysight ADS software and SOI/SOS PDKs are used to obtain the simulation results. A summary in Section 5.6 concludes the chapter.

5.1 SOI Fabrication Process: Background

The SOI substrate has a tri-layer structure, consisting of thick silicon, an insulator (note BOX for "Buried Oxide") and the active silicon layer [60]. The last layer forms the conduction area on which the transistors are defined. In practice, the SOI term is usually reserved for a substrate consisting of a layer of silicon over a silicon-oxide (SiO_2) layer, itself located on a silicon substrate. This structure is most common because it is the easiest to make, and the more economical to produce.

The presence of an insulating buried layer under the silicon film induces significant differences between the operation of the transistor on bulk silicon and the transistor

on SOI. The first commercial use of the latter was motivated by the need to obtain more resistant devices to radiation [61,62] for space and military applications. These radiations can excite the atoms of silicon and generate latch-up in standard CMOS processes. In SOI, only the thin top layer of silicon (film or active area) of the wafer is used. Insulation made by the BOX, between the active region and the rest of the substrate, minimizes the risk of malfunction of the circuit by the excitation of atoms, under the transitory effect of radiation. SOI entered the world of commercial microelectronics because of increased performance compared to the bulk silicon technology. This is evident at high frequencies where reduced parasitics and reduced substrate losses improve performance. Table 5.1 summarises the main pros and cons of SOI devices.

Table 5.1: Summary of SOI process features.

Advantages	Disadvantages
+ Isolation between the devices + Reduction of parasitic capacitances + Less parasitic leakage currents of junction substrate + Reduction of the short channel effect + Decreasing the polarization effect of the substrate + Limited vertical area of the Source/Drain + Tolerance to radiation and relatively high temperature	- Floating substrate effect - Self-heating effect - Existence of the parasitic lateral bipolar transistor - Relatively large contact resistance (for thin STI layer) - Reduced drain breakdown voltage

In the past five years, the semiconductor industry has seen different SOI substrate flavours such as silicon-on-insulator, silicon-on-sapphire (SOS) and high-resistivity SOI substrates (HR-SOI). These enable higher performance at reduced overall system cost and footprint. SOI substrates can be manufactured by three techniques, oxygen implant/anneal (SIMOX) method, bonding-and-etched-back-SOI (BESOI), and UNIBOND (Smart-Cut).

5.1.1 The SIMOX Method

The SIMOX ("Separation by IMplantation of OXygen") method [6] consists of two steps. First, oxygen ions are implanted in the substrate surface, and thereafter, annealing at high temperature (1300-1350°C) forms the BOX. The BOX thickness is determined by the implanted dose and its energy. Although this method was developed in the late 1970s [63], the first SIMOX substrate were marketed in 2000. Mass production was linked to the development of a machine capable of implanting oxygen ions without contaminating the substrate at very high energy and dose. For instance, forming a 400nm BOX and a silicon (Si) film of 200nm requires oxygen implantation of 2×10^{18} /cm3 at an energy of 180keV. Since the demand for thinner BOX layer of 80nm were placed in 1990s, the implantation dose were decreased to $4{\times}10^{17}$ $/cm^3$. Furthermore, the implantation energy was lowered to 70KeV to obtain a thin active film of 50nm for fully-depleted transistors. Currently, the SIMOX method provides SOI substrate with uniform thickness of $\pm 10nm$ for the BOX and $\pm 5nm$ for the Si film.

5.1.2 The BESOI Method

The bonding-and-etched-back-SOI (BESOI) technique, as an alternative to SIMOX, has the advantage of a cleaner interface between the silicon and oxide layers with less defects and charge-up effects at the buried oxide [64]. The above fabrication uses a material which is generated by oxidizing the seed and/or handle wafers, followed by bonding the two wafers. The active device region is created on the seed wafer by lapping and etching to the desired film thickness. Even though this method is suitable for the fabrication of 600nm SOI, the presence of an etch stop layer is essential to achieve SOI wafers with a nominal thickness of 500nm or less [60].

5.1.2.1 The Smart-Cut Method

The Smart-Cut process, is currently the most promising for manufacturing SOI substrates in large volume [65]. It consists of a bond between a wafer (A) and another wafer (B), the wafer (A) having been pre-oxidized and then implanted with hydrogen (formation of micro-cavities) and then cleaned (Fig.5.1). Bonding is provided by Van

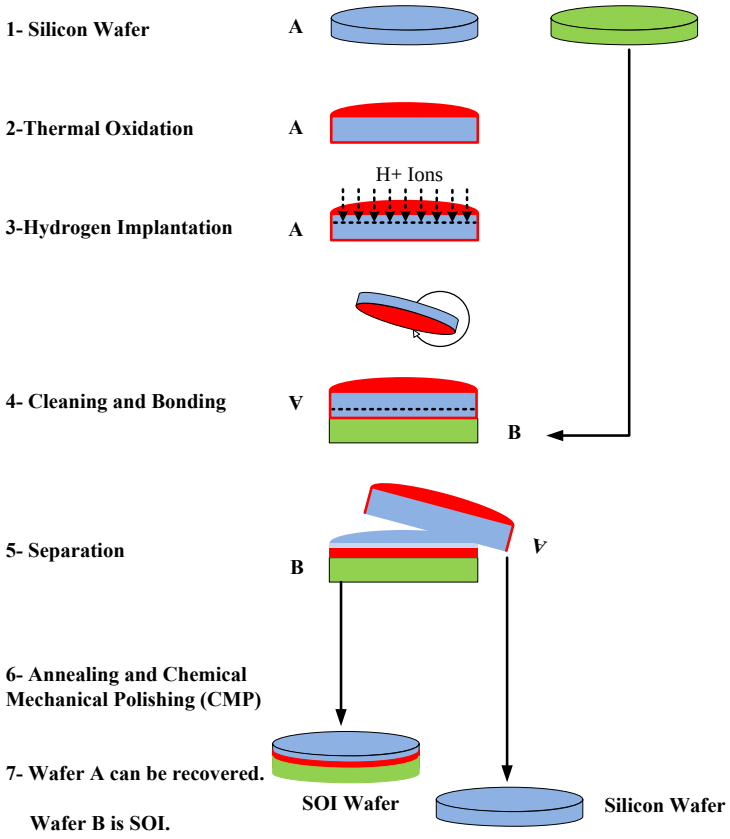


Figure. 5.1: SOI wafer manufacturing from SMART-Cut^{TM} UNIBOND ^{TM} wafer bonding process.

der Waals forces originally between crystal silicon and silica. A first annealing at around 800°C, can stabilize the bonding. A second annealing is then carried out to fracture the silicon wafer (B), at the implanted zone with hydrogen, by coalescence

of the micro-cavities. The thickness of the silicon film is finally adjusted by chemical mechanical polishing. The wafer (A) can be recovered and reused, the manufacturing cost is thus reduced and the quality of the material is eventually improved.

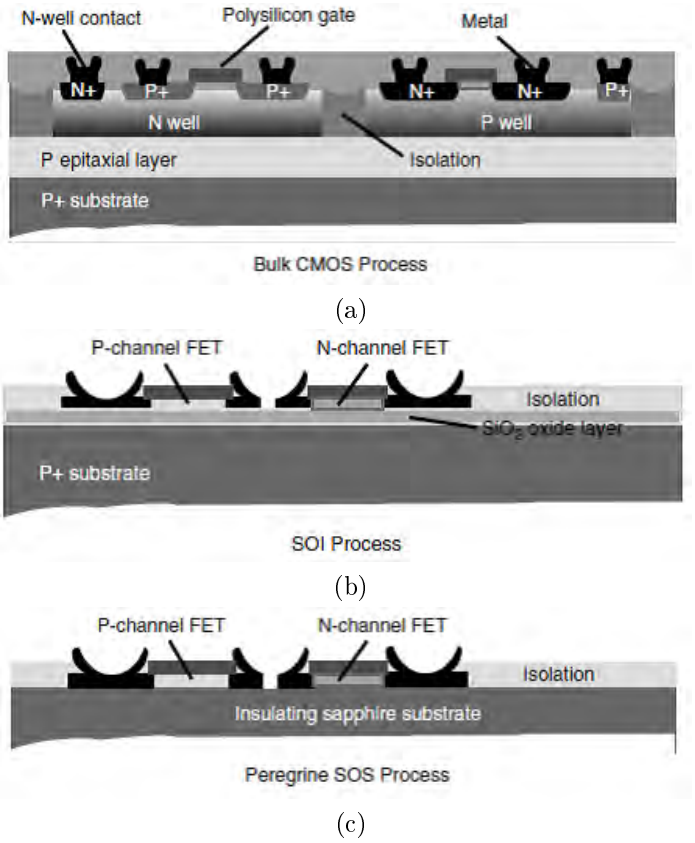


Figure. 5.2: Cross-section of an inverter circuit in (a) bulk CMOS (b) SOI (c) SOS process [66].

5.2 Bulk CMOS vs. SOI and SOS

In the SOI process, active and passive devices are fabricated in and on the thin layers of silicon. Fig.5.2 shows an inverter circuit in a bulk CMOS and an SOI and SOS processes. The main difference is clearly visible that the CMOS process requires several layers to design NMOS and PMOS devices. In addition, these devices must be placed in wells to insulate them from each other as well as the conductive substrate.

Eventually, the wells need to be biased to a reverse potential in order to reduce the parasitics. The SOI/SOS process takes advantage of its simplicity to reduce the number of fabrication masks for the same inverter circuit. It is noteworthy to mention that the SOS active devices are developed in an ultra-thin (100nm) silicon (UTSi) film grown on top of a crystallised sapphire (Al_2O_3) substrate. The method has been patented by Peregrine Semiconductor Corp. [67]. The work in this thesis uses the 250nm SOS Peregrine process and the 130nm SOI process of STMicroelectronics.

5.3 Peregrine SOS Process Features

Peregrine offers several varieties of UltraCMOS processes targeting wireless infrastructure, land-mobile-radios, automotive, military, radar and space. Each process option includes three aluminium metallisations, where the top metal thickness is 3.1 µm for FC, GC, and PC processes. This top conductor is often used to design relatively low-ESR interconnects and inductors. Metal-Insulator-Metal (MIM) capacitors are also formed between the two top metallisations. Table 5.2 summarises key features of the process options.

Since shorter gate lengths are preferable in the design of any switching application, the UltraCMOS GC process is chosen for this research work. There are 9 types of field-effect transistors (FET) in that process variant: 5 different N-channel and 4 different P-channel transistors covering three V_t settings and a thick oxide variant. These devices could potentially be used for RF and high-performance digital low-leakage applications. The transistor types and their specifications are shown in Table 5.3. TIN devices were used in this work because the thick oxide increased the voltage breakdown. The near zero V_t lowered the R_{on} but necessitated the use of a $-v_e$ gate voltage to switch the device off.

Table 5.2: Summary of Peregrine SOS process variants [68–70].

Features	Units	Process Variants					
		FA	FC	GA	GC	PA	PC
Min. Gate Length	nm	500		350	250	250	
Application		Com./Auto/Mili.		Com./Auto/Mili.		Com./Auto/Mili.	
Supply Voltage	V	3.0/3.3		2.5/3.3		2.5/3.3	
Transistors (NMOS/PMOS)		5/4	5/4	5/4	5/4	5/4	5/4
F_t (IN Transistor)	GHz	15		30		30	
f_{max}	GHz	45		90		90	
Resistors*		1/1/1/1		0/1/0/1		1/0/0/1	
Interconnect Layers		3	3†	3	3*	3	3*
Inductors		No	Yes	No	Yes	No	Yes
MIM Capacitors		No	Yes	No	Yes	No	Yes
MMM Capacitors‡		Yes	No	Yes	No	Yes	No

* N^+/P^+/Polycide/SN.
† Top conductor is a 3.1 µm thick metal layer.
‡ The MMM Capacitor is a triple layer metal capacitor.

Table 5.3: Transistor type descriptions for GC process [68–70].

Device Type	**Gate Oxide Thickness**	**Threshold Voltage (V)**	**Application**
HN	25Å	0.7	Digital and low-leakage
RN	25Å	0.43	Digital and low-leakage
IN	25Å	0.08	High-performance digital
HP	25Å	-0.6	Digital and low-leakage
RP	25Å	-0.41	Digital and low-leakage
IP	25Å	-0.05	High-performance digital
TRN	50Å	0.64	Digital and low-leakage, High breakdown RF
TIN	50Å	0.09	High-performance digital and RF
TRP	50Å	-0.45	Digital and low-leakage, High breakdown RF

5.4 STMicroelectonics SOI Process Features

STMicroelectronics offers SOI UNIBOND wafers with a high resistivity $\approx 3-4k\Omega$ .cm substrate under a BOX layer of thickness of 400nm. A thin silicon layer of 160nm with a resistivity of 8-22 Ohm.cm is used for the active devices. This process features a 50Å gate oxide, cobalt silicide on junctions and polysilicon gates. A shallow trench isolation technique is used between active devices. The back-end offers 6 metal layers which are all made of Damascene copper. The last metal layer has a thickness and a sheet resistance of 0.96 µm and 22 mOhm/sq, respectively. This conductor is often used for inductors and major signal distribution in Analog/RF applications. An aluminium layer (ALUCAP) on top of the last copper level is also used for the pad openings and bumping processes. The manufacturing process requires at least a set of 28 masks for the selected SOI option [71]. Table 5.4 summarises the process features.

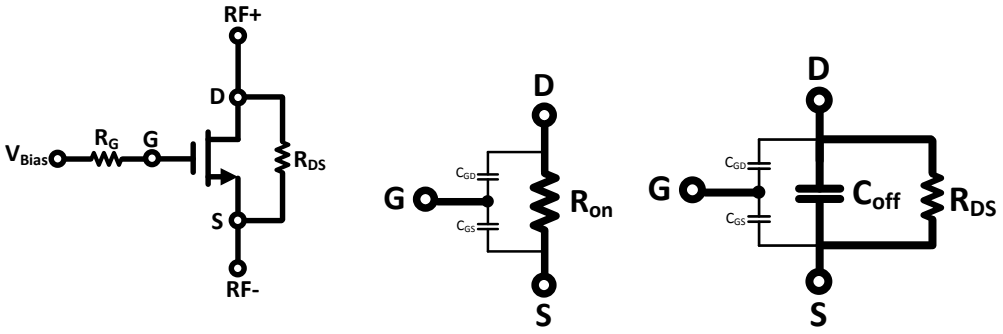
Table 5.4: Summary of STMicroelectronics SOI process [71].

Features	**Units**	**HCMOS9 SOI Process**
Min. Gate Length	nm	130
Application		Com./Auto/Military
Supply Voltage	V	2.5
Transistors (NMOS/PMOS)		2-Feb
Ft (IN Transistor)	GHz	95
fmax	GHz	115
Resistors (N+/P+/Polycide/RHIPO)		1/1/0/1
Interconnect Layers		6
Inductors		3*
Capacitors		Poly/MIM/MOM

* High-Q inductors are available.

5.5 SOI/SOS FET Switch Performance

When a FET operates as a switch, it is biased in strong inversion, and is characterised by its on-resistance (R_{on}) and off-capacitance (C_{off}). Fig.5.3 shows an RF FET switch with its equivalent circuit in ON and OFF states. The gate bias resistance



(a) (b) (c)

Figure. 5.3: Circuit model of (a) switch (SW) FET (b) FET equivalent model in the ON-state (c) FET equivalent model in the OFF-state.

(R_G) should be much higher than the parasitic capacitances of the transistor, (C_{off}), defined as the series combination of C_{GS} and C_{GD} in parallel with C_{DS}. In the on-state of a series connected (floating) device, a small value of R_G would cause loss due to a large current flowing through the parasitic capacitances to AC ground [72]. In addition, small R_G prevents the proper voltage division in off-state across C_{GS} and C_{GD}, resulting in a reduction in the $1dB$ compression point and sacrificing the switch linearity. The importance of this gate resistor R_G will be covered in detail in Section 5.5.1.

Insertion loss and isolation are key parameters that indicate the efficiency of a single FET switch which can be approximated by the $R_{on} \times C_{off}$ figure of merit (FOM) [73]. Nowadays, the SOI manufacturers put much effort into scaling down this figure. The smaller FOM the better RF switching performance. The first task of this research was to investigate the R_{on} and the C_{off} per millimetre FET gate

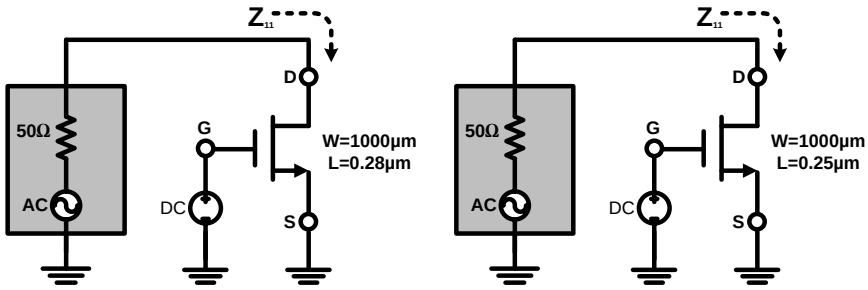


Figure. 5.4: A switch FET test circuit: SOI process (left) and SOS process (right).

width at cellular frequencies. Fig.5.4 shows the test circuit in a 50Ω system. The aforementioned fundamental parameters of a switch FET are given by

$$R_{on} = Re\left(Z_{11}\right)|_{ON-state} \tag{5.1}$$

$$C_{off} = \frac{1}{2\pi f \times Im\left(Z_{11}\right)|_{OFF-state}} \tag{5.2}$$

Table 5.5 compares the $(R_{on} \times C_{off})$ FOM from the 130nm SOI and the 250nm SOS process technologies at 2GHz. The improved FOM of the more modern 130nm SOI technology is predominantly due to a lower on-resistance. The work in this thesis used both technologies.

Table 5.5: Survey of FOM from the SOI and the SOS technologies at 2GHz.

Process Technology	R_{on} (Ω/mm)	$C_{off}(fF/mm)$	$R_{on} \times C_{off}(fs)$
130nm SOI	1.0	278	278
250nm SOS	1.6	280	448

A small FOM results in less insertion loss and a higher linearity. The insertion loss of a switch is given by:

$$\text{IL } (dB) = 20\log_{10}\left(1 + \frac{R_{on}}{2R_0}\right) \tag{5.3}$$

Where R_0 is the impedance of the source and load in a 50Ω system. Using $250nm$ SOS

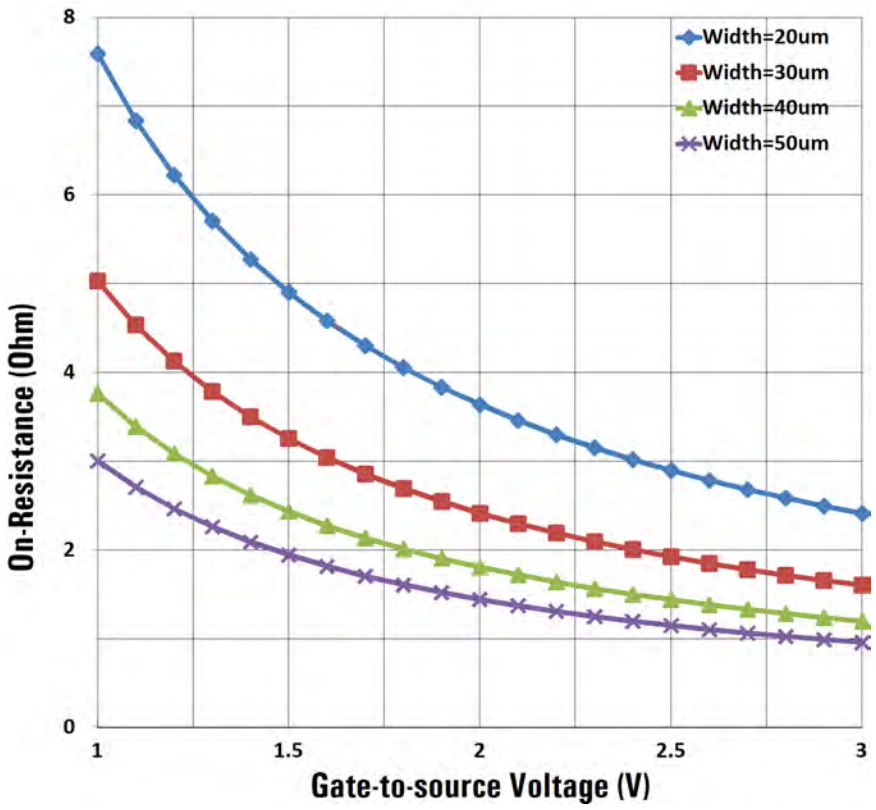


Figure. 5.5: The on-resistance of a 58 finger device as a function of the gate voltage (V_{Bias}) and FET periphery (finger width).

technology with an oxide thickness (t_{ox}) of 50Å and $W = 2.75mm$, a single optimised switch has an R_{on} equal to 1.55Ω and C_{off} to $782.5fF$, resulting in an insertion loss of $0.133dB$ at $Vg = 2V$. The R_{on} is varied by the applied DC gate voltage (V_{Bias}) and the periphery (W) of the switch. Fig.5.5 illustrates the reduction of R_{on} as a function of increasing V_{Bias} and W with an identical number of 58 fingers.

There are two common measures of distortion, third order intercept point (IP3) and the 1dB compression point (P_{1dB}). The former is measured by applying two closely spaced tones to the switch under test and measuring the generated third and higher order products. The third order intercept point (IP3) is defined where the input and distortion powers are equal [74]. The latter is the measured output level where it is a 1dB deviated from the linear gain.

Intermodulation products (IMP) are created due to the non-linearity of the switch. In order to guarantee the performance in wireless applications, the transmitted power via a turned-on switch should not be distorted. The third order intermodulation harmonic power should be $60dB$ less than the power of the desired signal for a typical handheld device [75].

Two compression points can be distinguished for a switch. The first (P_{1dBVth}) results from high power transmissions through an ON device. The second (P_{1dBbk}) occurs when the drain and the source voltages exceed the breakdown conditions in the OFF state. For the given periphery and biasing voltage of the above switch, P_{1dBVth} and $P1_{dBbk}$ are $25.81dBm$ and $18.78dBm$, respectively.

5.5.1 Biasing Considerations

The bias network determines five important operating features of an RF FET switch, which are the minimum operating frequency (f_{min}) of the switch, the switching time (τ), ohmic losses in the bias network, the maximum power handling (P_{max}), and the uniformity of distributed voltage across the transistor during switching states. Among different bias network topologies fabricated on silicon substrates, the resistive one is the most suitable network in terms of high yield and compactness. SOS technology provides a diffusion resistor with large sheet resistance of $2500\frac{\Omega}{sqr}$, enabling a large resistance value occupying a small area. The switching time for the above FET transistor (Fig.5.3) is given by $\tau = RC_g$ where C_g is the effective capacitance connected to the gate node, defined as the parallel value of C_{GS} and C_{GD} in the off-state. This time constant establishes the simultaneous switching condition in stacked transistors.

The bias resistor plays a vital role in affecting the minimum operating frequency (f_{min}) of the switch, estimated as:

$$f_{\min} \approx \frac{7}{\pi RC_g} \tag{5.4}$$

As described earlier, the OFF state voltage swing should be divided equally between

drain-to-gate (V_{DG}), and drain-to-source (V_{DS}). For a single FET, this voltage swing is derived as [76]:

$$\frac{V_{DG}}{V_{DS}} = \left(\frac{1 + (\pi f R C_g)^2}{1 + 4 (\pi f R C_g)^2} \right)^{\frac{1}{2}} \tag{5.5}$$

Where f is the frequency at which the switch operates. Note that V_{DG} cannot exceed its breakdown value which is defined as $(V_{DGbk} - V_{th})/2$, where V_{DGbk} and V_{th} are the drain-to-gate breakdown and threshold voltages, respectively. This limitation for a SOS transistor ($t_{ox} = 50\text{Å}$) with intrinsic threshold voltage is $1.33V$. In practice, the maximum voltage across the drain-to-source (V_{DSM}) must be less than the ($V_{DSbk} - V_{th}$), so that the gate resistor value can be derived from:

$$R = \frac{1}{\pi f C_g} \left(\frac{1 - 4 \left(\frac{V_{DSM}}{V_{DSbk}} - V_{th} \right)^2}{4 \left[\left(\frac{V_{DSM}}{V_{DSbk}} - V_{th} \right)^2 - 1 \right]} \right)^{\frac{1}{2}} \tag{5.6}$$

The gate voltage swings superposed on the gate DC supply voltage can reach up to half of V_{DSM} because the gate-to-source and gate-to-drain impedances are equal. During the first half of the period, the gate voltage should not fall below the threshold voltage. Moreover, the drain-gate voltage should not exceed its breakdown value during the whole cycle. These two constraints lead to:

$$V_{DSM} = V_{DGbk} - V_{th} \tag{5.7}$$

$$V_{Bias(\max)} = \frac{V_{DGbk} + V_{th}}{2} \tag{5.8}$$

The maximum power handling capability of a single FET switch is given by:

$$P_{\max} = \frac{(V_{DSbk} - V_{th})^2}{2 R_0} \tag{5.9}$$

For a given SOS transistor, the power magnitude of $139mW$ can be handled by a single transistor. The dissipated power in the bias network is inversely related to the

gate resistor: a larger value reduces the power dissipation but degrades the switching speed.

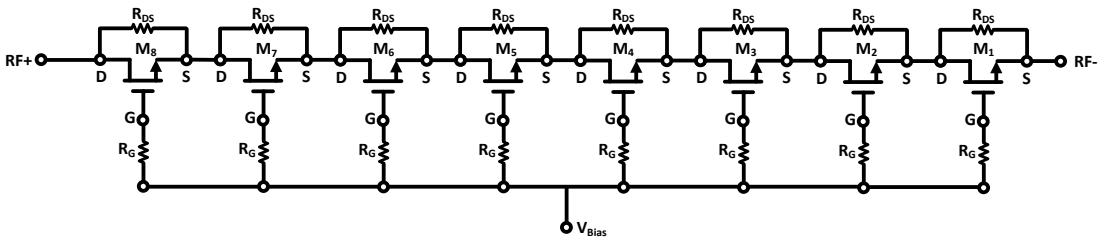


Figure. 5.6: Stacking FET's approch.

5.5.2 Stacking FET's Approach

To achieve the required high power handling in cellular systems such as GSM ($35dBm$), a stacked configuration of n FETs can be used. While this improves the switch's ability to handle power as well as increases the $1dB$ compression point, the total insertion loss is degraded. The following expressions apply for eight ($n = 8$) stacked transistors with the above periphery (Fig.5.6). The periphery is defined as the number of gate fingers times the unit gate width.

$$\text{IL } (dB) = 20\log_{10}\left(1 + \frac{nR_{on}}{2R_0}\right) \longrightarrow \text{IL}_{\text{n=8}} = 1\,dB \tag{5.10}$$

$$\begin{aligned} &\text{P}_{1dBV_{th}}\,(dBm) = 10\log_{10}\left(\tfrac{2(n(V_{th}-V_{OFF}))^2}{R_0}\right) + 30 \\ &\longrightarrow \text{P}_{1dBV_{th}} = 38.74\,dBm \end{aligned} \tag{5.11}$$

$$\begin{aligned} &\text{P}_{1dBbk}\,(dBm) = 10\log_{10}\left(\tfrac{(nV_{bk})^2}{2R_0}\right) + 30 \\ &\text{P}_{1dBbk} = 36.84\,dBm \end{aligned} \tag{5.12}$$

When stacking n identical FET switches, the minimum value of the combined gate resistor (R_{min}) is a function of the individual gate resistors (R), and can be calculated

by:

$$R_{\min} = \frac{R\,(2n-1)}{n} \tag{5.13}$$

Therefore, the minimum time constant that turns on all the stacked FET's simultaneously can be derived from:

$$\tau_{\min} = (2n-1)\,R\,C_g \tag{5.14}$$

ON-OFF transient characteristics were simulated to guarantee breakdown compliance when switching at different phases of the RF carrier. Fig.5.7 illustrates the simulated off-state voltages of the drain node, drain-to-source, gate-to-source, and gate-to-drain of M1-M8 at a maximum input power of $39.5dBm$. The maximum drain voltage in the off-state [with the gate bias of $-1.5V$] translates to $21.1V$. Regardless of this; the peak voltage drops across each transistor's terminals should remain below $2.6V$ to avoid breakdown phenomena, allowing the whole stack to withstand a large voltage swing before any switch breaks down. The number of stacked transistors can be obtained from the peak RF voltage across the switch divided by the drain-source breakdown voltage (sufficiently de-rated for safety margin). The gate voltage of $2.5V$ combined with the periphery (width) of each transistor keeps the total on-resistance as low of 1.55Ω/transistor in the saturation regime [76].

Fig.5.8 shows the compression behaviour of the ON current through the stacked transistors at $2GHz$. As can be observed in this figure, a $1dB$ gain compression point of $49.2dBm$ is achieved. At this power level the switches would be operating above their breakdown voltage if taken to the OFF condition. A two-tone test signal with a frequency spacing of $10MHz$ resulted in an extrapolated input IP3 measurement of $54.3dBm$.

Fig.5.9 illustrates the linearity and intermodulation trend of the configuration. The above (P_{1dB}) measurement appears too high for the IP3 result; (as a rule of thumb the P_{1dB} measurement is $\approx 15dB$ below the IP3). Discussions with the Engineers at

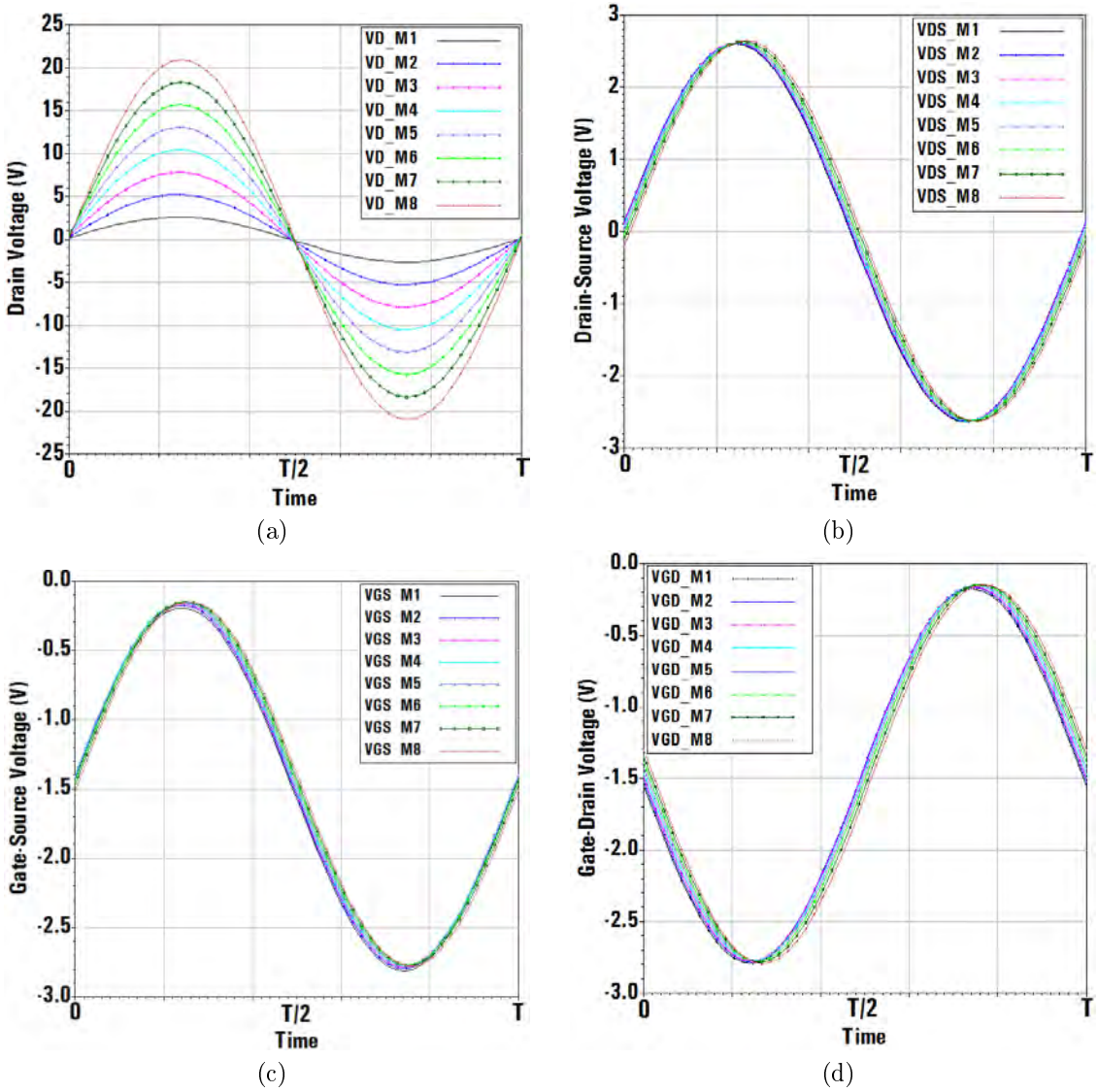


Figure. 5.7: Voltage distribution for eight stacked SOS FET's switches when the input power hits 39.5dBm. (a) Voltage waveforms at different drain nodes (V_D) of transistors M1-M8, (b) Drain-to-source Voltages ($V_{DS1} \sim V_{DS8}$). (c) Gate-to-source voltages ($V_{GS1} \sim V_{GS8}$). (d) Gate-to-drain voltage waveforms ($V_{GD1} \sim V_{GD8}$). Simulations in ADS (Advanced Design System) using TIN device models.

Peregrine indicated that the cause was most likely due to poor non-linearity models in the Peregrine PDK at high power levels.

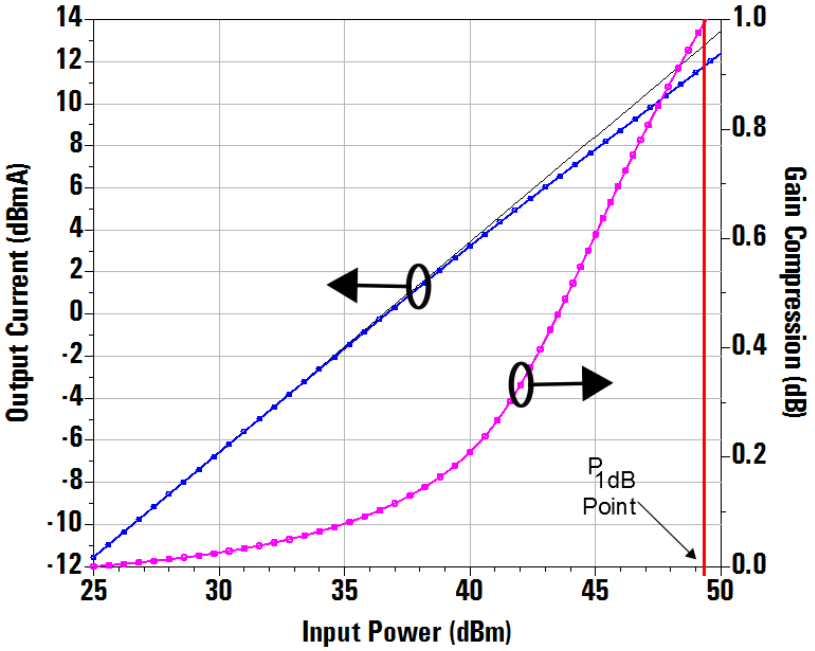


Figure. 5.8: Linearity and compression behaviour of the SOS stacked FET's switch.

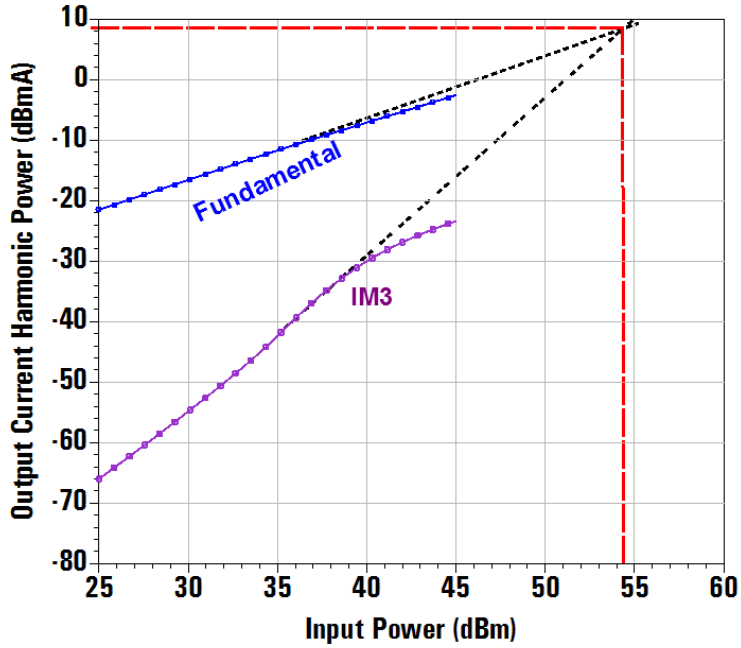


Figure. 5.9: Linearity and intermodulation behaviour of the SOS stacked FET's switch.

5.6 Summary

In this chapter, we presented the materials and industrial techniques for manufacturing SOI substrates. This eliminates the intrinsic parasitic effects of the silicon substrate for RF applications. SOI technology has superior features such as immunity to coupled noise and a reduction in the short channel effect [60]. The technology is therefore a prime candidate to continue the downscaling of RF passive components with the goal of a single chip RF front-end solution. Two world leading SOI technologies, 130nm SOI and 250nm SOS processes, were compared. Both processes offer relatively high quality-factor (Q) inductors and capacitors as a result of the high resistivity substrate [66, 77].

We chose the above processes to investigate their RF switching performance for the described tunable duplex filters of the previous chapter. As mentioned in Chapter 4, FET switches are the key elements of a digital switched capacitor bank. Therefore, the design fundamentals of a FET switch was explained, emphasising the on-resistance, off-capacitance, insertion loss, linearity and biasing. High power handling requires a stacked configuration. Keysight ADS software with a Peregrine PDK are used to simulate the operation of a switch with eight stacked FETs, with a transmitter power of 36.5dBm. The simulated P_{1dB} and $IIP3$ were somewhat approximate at 49.2dBm and 54.3dBm respectively, due to poor simulation models at these powers.

The remainder of the Thesis describes four implementations of the LID circuit: three fully integrated solutions as well as a discreet solution with off-the-shelf components. The next Chapter describes single band LID solutions.

Chapter 6

Single-Band Tunable Duplex Filter: Implementation

A low isolation device is an essential building block of the adaptive duplexer. This chapter studies the feasibility of implementing channel selectable filters in a fully integrated Silicon-on-Sapphire (SOS) solution and a partially integrated solution using off-chip PCB components. Digitally switched capacitor banks (DSCBs) are employed to tune the LID to the desired channel of LTE band 1. The tunable capacitor is part of the resonant circuit, therefore, a large peak voltage appears across the FET device. Since the FET switch has a breakdown voltage of less than 3V, FETs are stacked to handle the higher peak voltages.

Section 6.1 describes an integrated solution for a single-band tunable LID. Important design aspects of the DSCB are highlighted. The Peregrine SOS process is used for fabrication. A discrete solution is provided in section 6.2 using high-Q components on a multilayer FR-4 PCB. The performance of these solutions are compared. A summary (section 6.3) concludes the chapter.

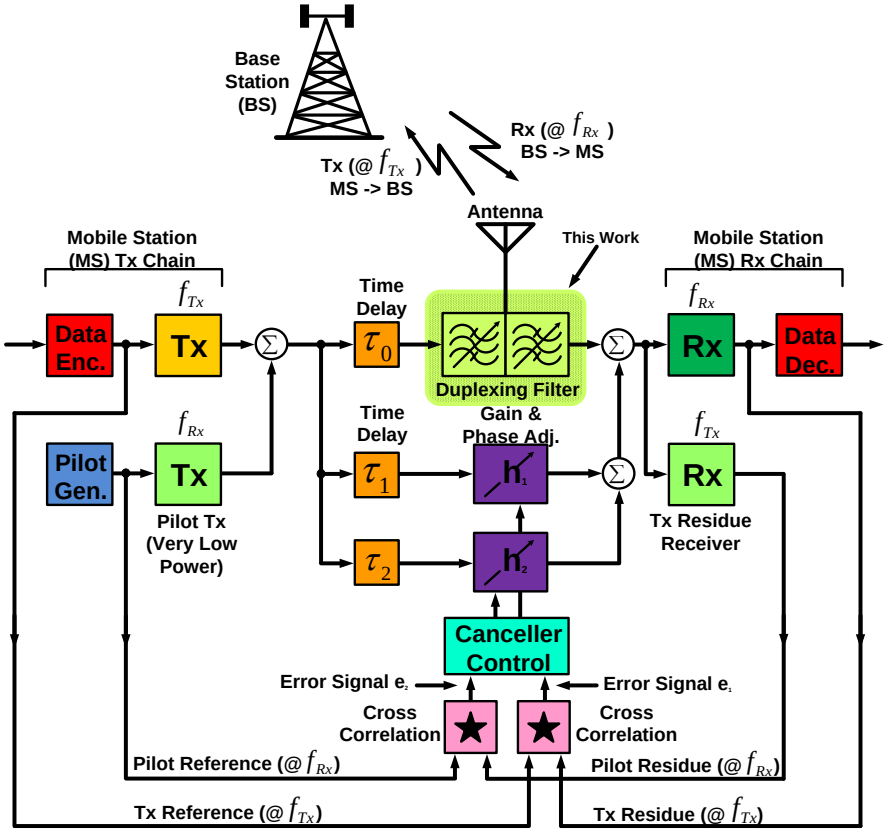


Figure. 6.1: Adaptive duplexer architecture. (The wideband circulator is replaced by L-C duplexing filters.)

6.1 SOS Duplex Filters: Overview

Fig.6.1 illustrates a detailed block diagram of the adaptive duplexer for a two loop cancellation path described in Chapter 3. In this work, the circulator is replaced by a tunable set of L-C duplex filters which enable the scheme to cover multiple channels and bands. The duplex filter (Fig.6.2) was designed to operate at LTE1, which has a relatively large duplex offset of 190 MHz. According to (4.8) and (4.15), the selected capacitance ratios (C_1/C_2) and (C_4/C_5) for this frequency band are 0.191 and 0.175, respectively. The Peregrine 0.25-μm UltraCMOS SOS process was chosen for implementation due to the low parasitic capacitances, relatively high-Q inductors

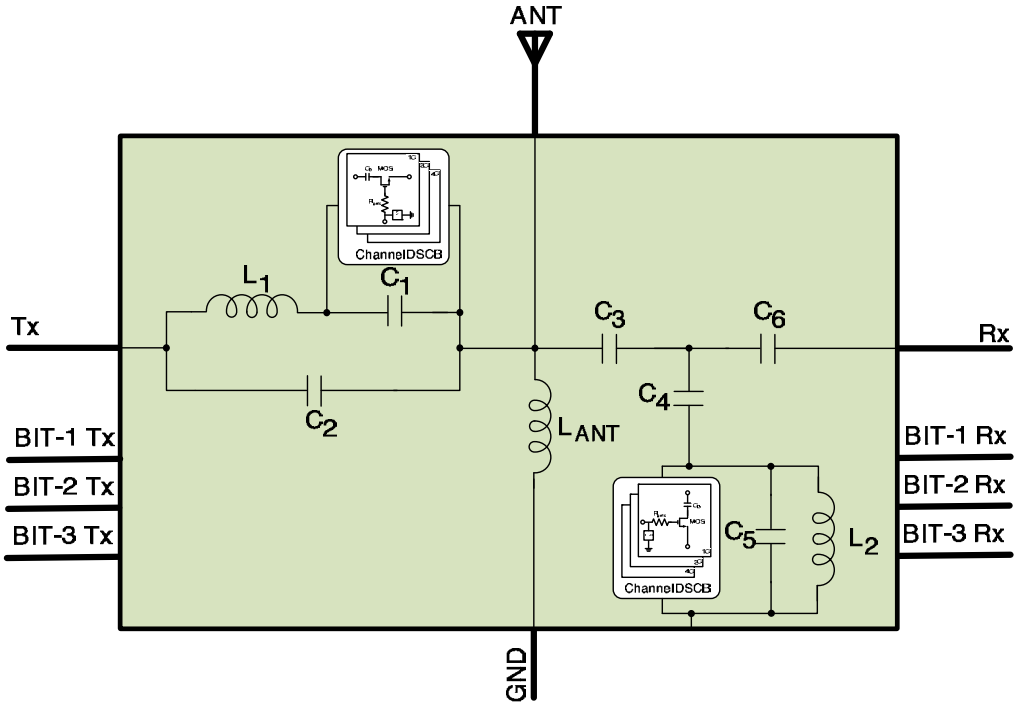
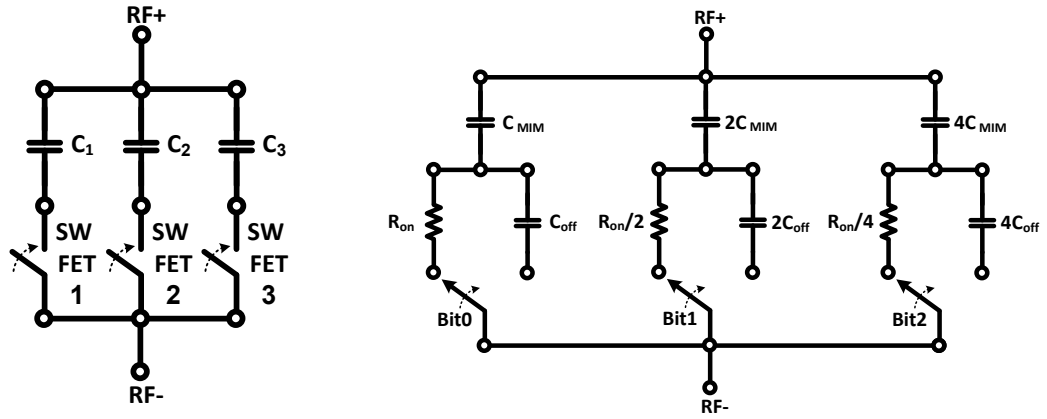


Figure. 6.2: Single-band tunable SOS duplex filter.

and a high linearity performance. Since the purpose of this implementation was to study the limitations of an on-chip solution for a duplex filter; on-chip passive elements were used. SOS metal-oxide-metal (MIM) capacitors can tolerate a peak voltage of 15V. Therefore, both capacitors as well as FET's need to be stacked.

6.1.1 Digitally Switched Capacitor Bank (DSCB)

A series connection of a fixed MIM capacitor and NMOS switch forms a switched capacitor (SC). The main performance metrics of the SC are the Q in both OFF and ON states, and the achievable capacitance ratio (C_{on}/C_{off}). A simplified model of a 3-bit DSCB is shown in Fig.6.3. The MIM capacitor values and the FET transistor sizes are weighted in a binary manner. For instance, the least-significant capacitor C_1 is designed to have the lowest capacitance of C_{LSB}. The next capacitor, C_2, should have a capacitance value of twice C_{LSB}. In general, each significant capacitor has



(a) (b)

Figure. 6.3: 3-bits DSCB (a) simplified model (b) model in ON and OFF conditions.

a value that is twice that of the previous significant capacitor. Finally, the most significant capacitor should have a value of $2^{(b-1)} \times C_{LSB}$, where b is the number of bits. The size of FET's are accordingly binary weighted to the respective series MIM capacitor. Assuming that C_{MIM} is much larger than C_{off} and its parasitic resistance is not also comparable with the R_{on}, the (C_{on}/C_{off}) and the Q_{min} of the least-significant bit (LSB) are given by

$$\frac{C_{on}}{C_{off}} = \frac{C_{\max}}{C_{\min}} = 1 + \frac{C_{MIM}}{C_{off}} \tag{6.1}$$

$$Q_{\min} = \frac{1}{\omega C_{MIM} R_{on}} = \frac{1}{\omega \left(\frac{C_{\max}}{C_{\min}} - 1\right) R_{on} C_{off}} \tag{6.2}$$

where ω is the operating frequency of the DSCB. Generally, the capacitance ratio is set by a desired Q_{min} and vice versa per the following equations.

$$\frac{C_{on}}{C_{off}} = 1 + \frac{1}{\omega Q_{\min} FOM} \tag{6.3}$$

$$Q_{\min} = \frac{1}{\omega \times FOM \times \left(\frac{C_{on}}{C_{off}} - 1\right)} \tag{6.4}$$

The two above equations indicate the limitation of the (C_{on}/C_{off}) based on process and the Q requirement. Considering the 250nm SOS process, Table.6.1 summarises the (C_{on}/C_{off}) for different Q_{min} at four common LTE frequencies.

Table 6.1: Required (C_{on}/C_{off}) for different Q_{min} across four common LTE frequencies.

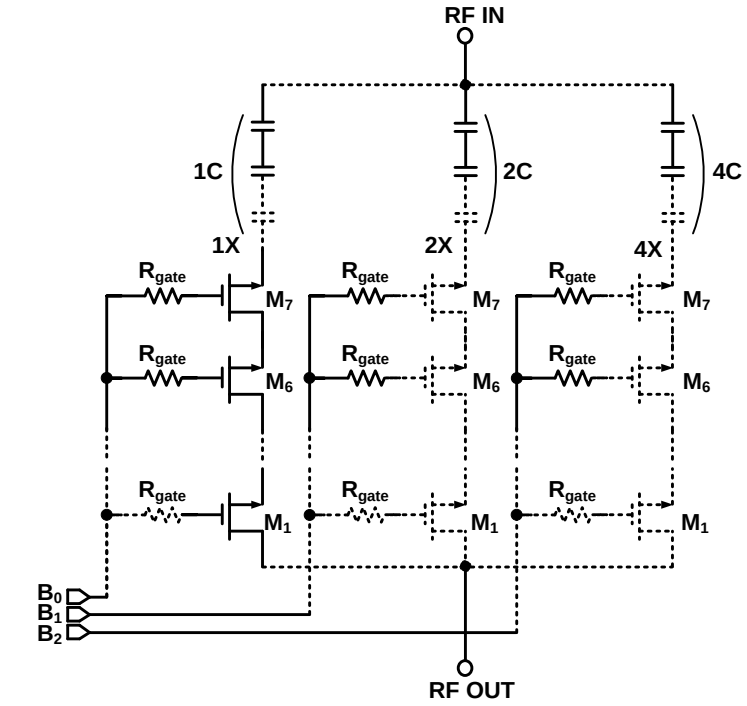
Frequency (MHz)	(C_{on}/C_{off}) $Q_{min} = 50$	(C_{on}/C_{off}) $Q_{min} = 70$	(C_{on}/C_{off}) $Q_{min} = 100$
900	8.89	6.64	4.95
1800	4.95	3.82	2.97
2200	4.23	3.31	2.61
3700	2.92	2.37	1.96

The DSCB is usually used in series or parallel with an inductor. Therefore, its Q-factor becomes prominent and has a major impact on the total Q of the tank resonator. On the other hand, the above results clearly indicate that the (C_{on}/C_{off}) shrinks when frequency increases at constant Q_{min}. A rational trade-off is a must when larger (C_{on}/C_{off}) is required i.e. switch between frequency bands.

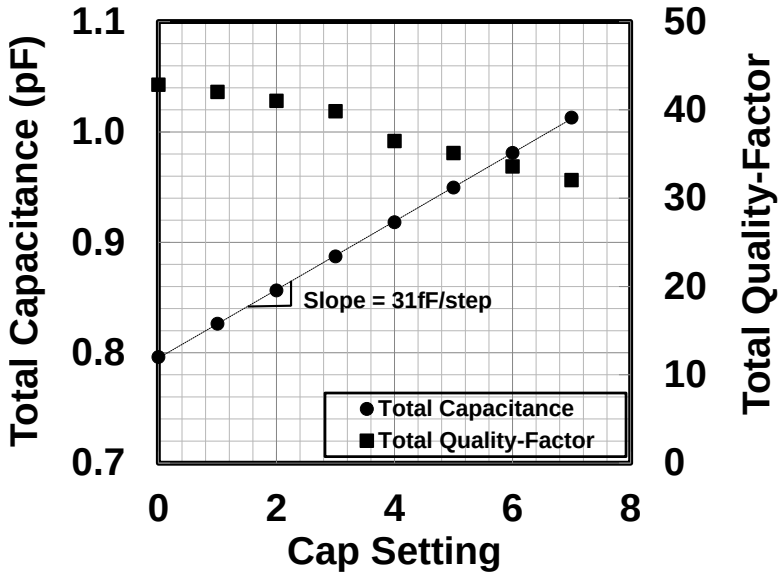
The peak voltage across the FET switch could be much higher than the rated voltage at the resonance. Consequently, stacking n number of FET's could prevent breakdown. The effective number of FET's in the stack is determined by

$$n_{eff} = n + \frac{C_{off}}{C_{MIM}} \tag{6.5}$$

The simulated performance of a 3-bit DSCB is shown in Fig. 6.4. The device widths are scaled to maintain the same (C_{on}/C_{off}) ratio for each bit. The $R_{on}C_{off}$ figure of merit for this process is 448fs. The leakage capacitance C_{off} in series with the MIM capacitor reduces the voltage across the stack in the OFF state. In this case, the SC peak voltage can be increased by $\frac{2}{7}$ to 24 V when a stack of seven TIN thick-oxide ($t_{ox} = 50\text{Å}, BV_{DS} = 2.75V$) transistors is used [78]. The series MIM capacitors



(a)



(b)

Figure. 6.4: 3-bit DSCB: (a) 7 FET stack (b) capacitance control range and Q.

are used for the 1C, 2C, and 4C in the DSCB for similar voltage reasons. The gate bias resistor should be much larger than the resistance of the leakage capacitances ($R_{gate} >> X_{C_{GD}}$) for uniform voltage division across the stack and good Q_{off} and Q_{on} performance (section 5.6). However, R_{gate} should also be small for high switching speed and low footprint. An R_{gate} of 20kΩ was chosen, resulting in a Q_{off}, Q_{on}, and (C_{on}/C_{off}) of 42, 32, and 1.3, respectively. A negative gate control voltage improved linearity in the off condition due to the near zero threshold voltage of the transistor, but was limited to the -2.75V NMOS breakdown.

6.1.2 Pad-based ESD Protection Circuitry

An Electrostatic Discharge (ESD) device protects the circuit from any unwanted large pulse from environmental or peripheral sources. Generally, the principle behind ESD protection is to create a low-impedance discharge path between any two pins. This shunts ESD current and clamps the pad voltages to a sufficiently low level [79, 80].

The protection performance is impacted by the particular mechanism, process technology, parasitic effects, and resistance of the ESD device. The protection device introduces parasitic effects that degrade the normal operation of the circuit, in particular at RF. Parasitics are often due to inappropriate layout design such as spacing between the tracks and so forth. If the impedance of the ESD discharge path is not significantly lower than that of the main circuit path, the voltage strike might not have enough suppression. It is therefore vital to have a wide metal track to take the ESD current and a low resistance ESD protection device. Larger device sizes lower the resistance but increase the parasitics. Therefore, there is a trade-off between the parasitic effect and ESD current handling capability.

To protect the DSCBs from any unforeseen electrostatic charge, a special pad-based ESD protection was designed, due to the passive nature of the LID circuit (no supply voltages). The traditional diode clamps to Vdd and ground cannot be used. The control voltages must swing to both +ve and -ve values during normal operation.

Fig.6.5 shows the proposed ESD protection circuitry. It includes two current paths, each one composed of large ESD diodes (160 µm) connected to a clamp (480 µm), which ensures protection during negative and positive ESD events.

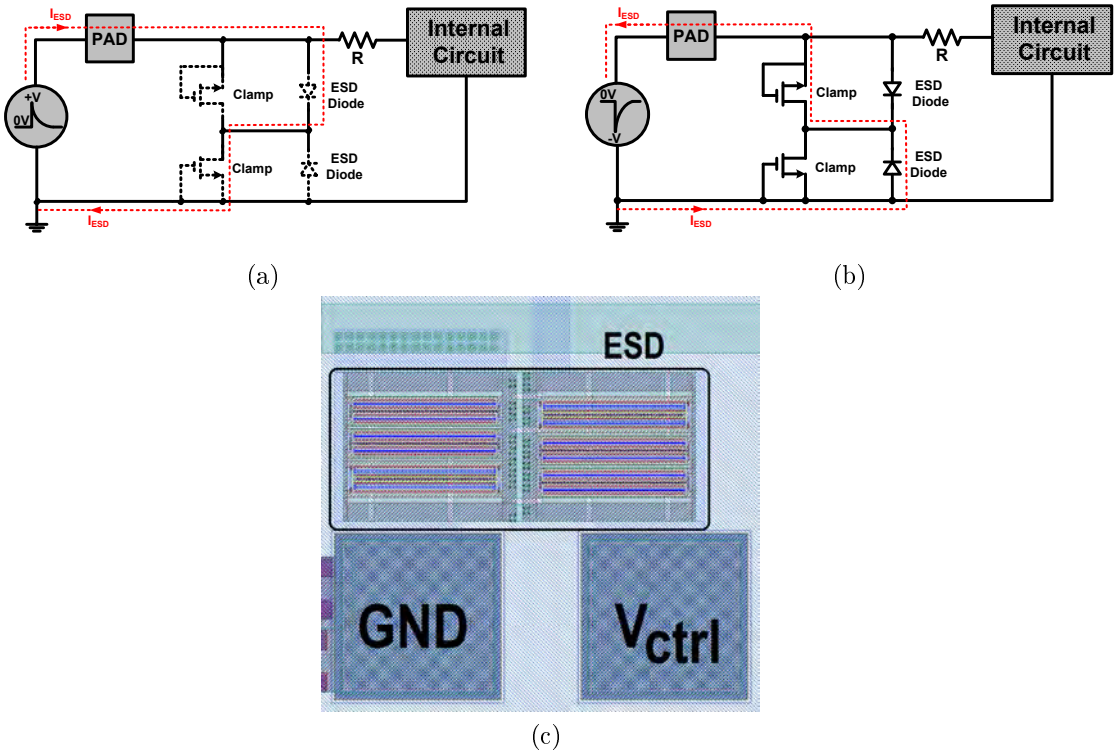
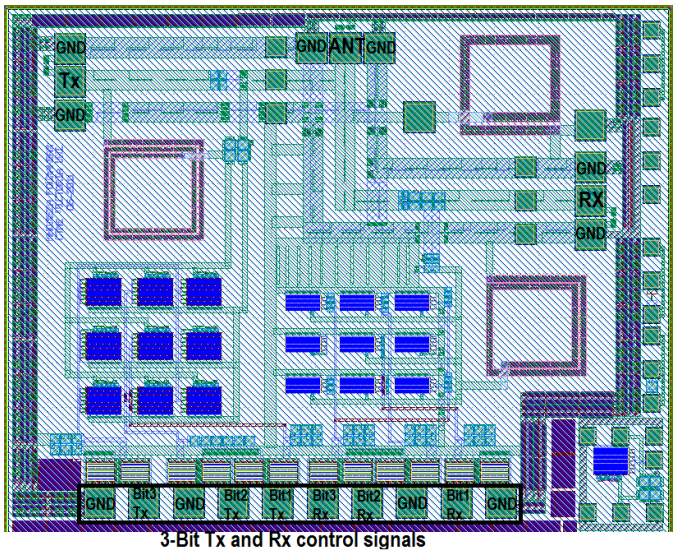


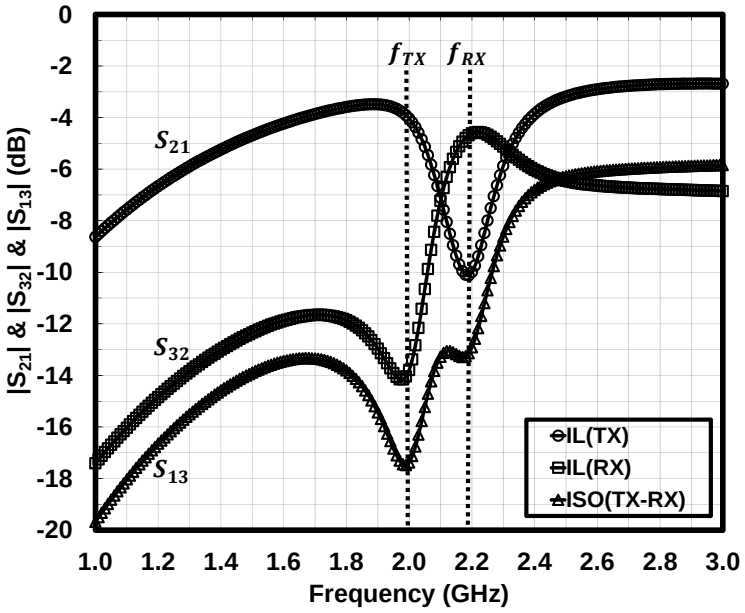
Figure. 6.5: Pad-based ESD protection circuitry: the path of ESD current pulse during a (a) positive (b) negative ESD event, (c) ESD layout.

6.1.3 Simulation Results

RF circuit design for cellular frequencies requires fairly accurate modelling of active and passive devices as well as interconnects. In this work, parasitics of FET switches are extracted by Cadence software. Scattering parameters for the interconnects are extracted by ADS momentum and are then included into the final simulation in Cadence. Fig.6.6 shows the final layout and the frequency response of the duplex filter with all passive components and the layout extracted DSCB's. The Tx null of



(a)



(b)

Figure. 6.6: Single-band tunable duplex filters: (a) final layout (b)post-layout simulation when DSCB's are OFF.

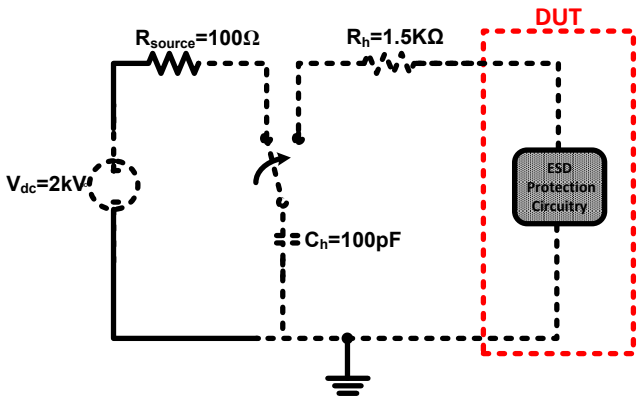
17.5dB is close to the required specs but the Rx null is 14dB. However, the latter is a less critical specification compared to the Tx null-depth [8]. Insertion losses are 3.8dB and 4.8dB for the Tx and Rx, respectively. The circuit appears to marginally

outperform the the calculated values in Table 4.1, with Q=25. The simulated Rx isolation is 1dB worse but the Tx insertion loss is 1dB lower than the calculated 4.9dB. The analysis assumed all components had the same Q which is clearly not the case for the circuit, where each component is designed to have as high a Q as possible within the constraints of chip area and process characteristics.

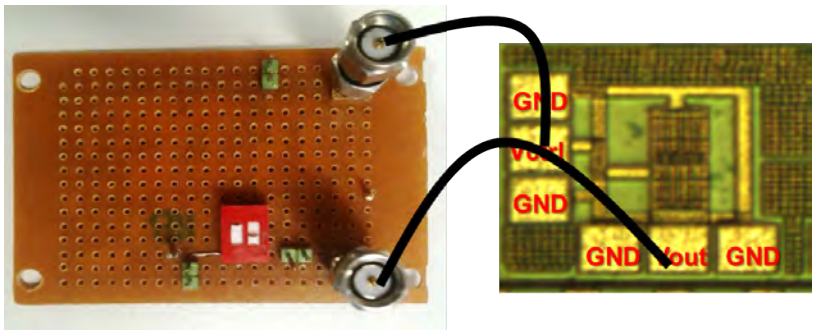
6.1.4 Measurement Results

6.1.4.1 ESD Protection

An ESD protection circuit must withstand a certain amount of peak voltage depending on the application. A typical peak voltage is 2kV. There are four conventional test models to examine the ESD performance, human body model (HBM), machine model (MM), charge device model (CDM), and transmission line pulse model (TLP). Amongst them, the HBM is usually used to initiate the testing approach as shown in



(a)

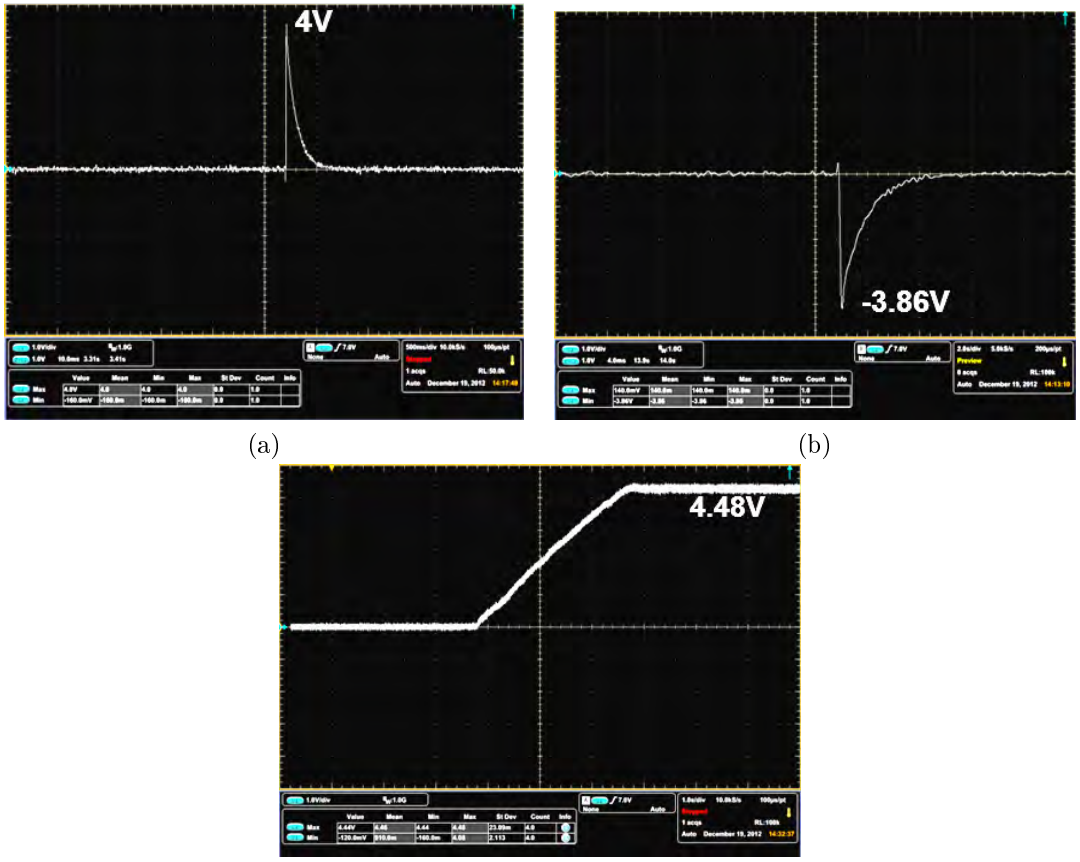


(b)

Figure. 6.7: HBM testbench for ESD protection measurement: (a) HBM model (b) PCB testbench.

Fig.6.7a. The capacitor C_h is charged to a peak voltage and then discharged through a resistor R_h to the DUT by a change-over switch. An ESD test circuit was fabricated as a standalone circuit on the SOS die. Its performance was tested using

a HBM built on a dot matrix board (Fig.6.7b). Connections to the chip were via a CASCADE probe station (not shown). Charging the C_h to a large voltage was not practical in the lab, thus, the capacitor was only charged to 30V. Two possible ESD strikes as well as a ramp voltage were generated and the measured results show that the ESD output voltage does not exceed $\pm 4V$ under any of these circumstances (Fig.6.8).



(a) (b)

(c)

Figure. 6.8: Measurement results of the output voltage of the ESD protection circuit for an input: (a) positive ESD strike (b) negative ESD strike (c) ramp voltage up to 30V.

6.1.4.2 Tunable Duplex Filter

The fabricated duplex filter chip has an active area including ESD protections and pads of $2.42mm^2$. Fig.6.9 shows the micro-photograph of the chip. The die was

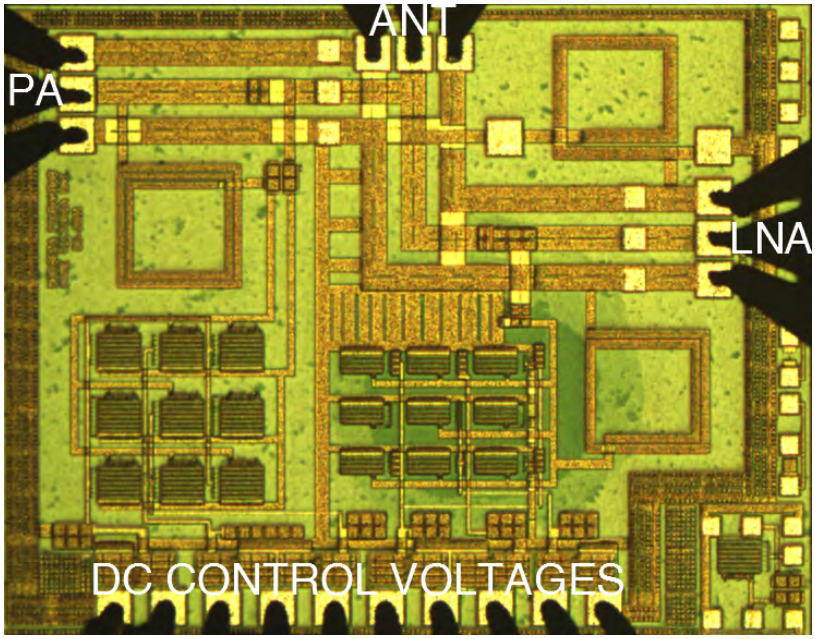
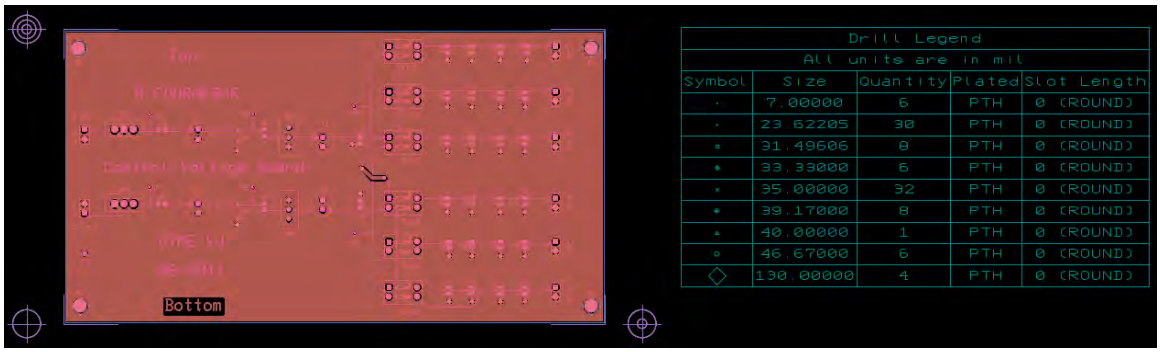


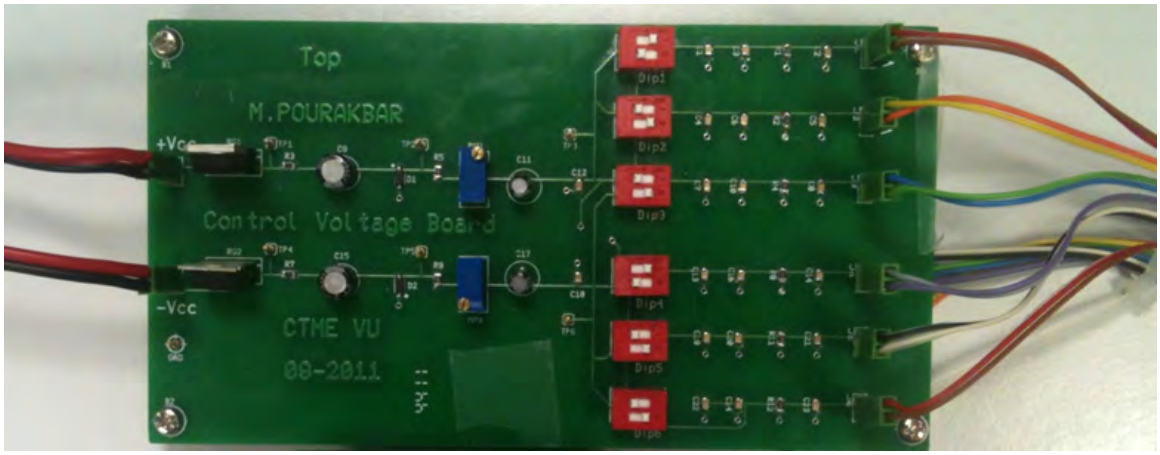
Figure. 6.9: Die micro-photograph of the duplex filter.

directly measured by CASCADE GSG RF micro-probes for three RF pads, and a multi-finger DC probe supplied the required control voltages for the DSCB's. Since the DSCB requires a negative voltage to turn off the FET switches, a PCB was designed to provide adjustable bipolar control voltages to cover all possible 64 states of the DSCB (Fig.6.10).

Fig.6.11a illustrates the measured Tx to Rx isolation with Tx powers up to 28dBm. The measured null frequencies are approximately 10% below the post-layout simulation results, with the lower null shifting more than the upper null producing an unwanted increase in the frequency offset. However, the critical Tx isolation of 19dB and Rx isolation of 13-14dB at the specified $f_d = 190MHz$ are close to simulations.



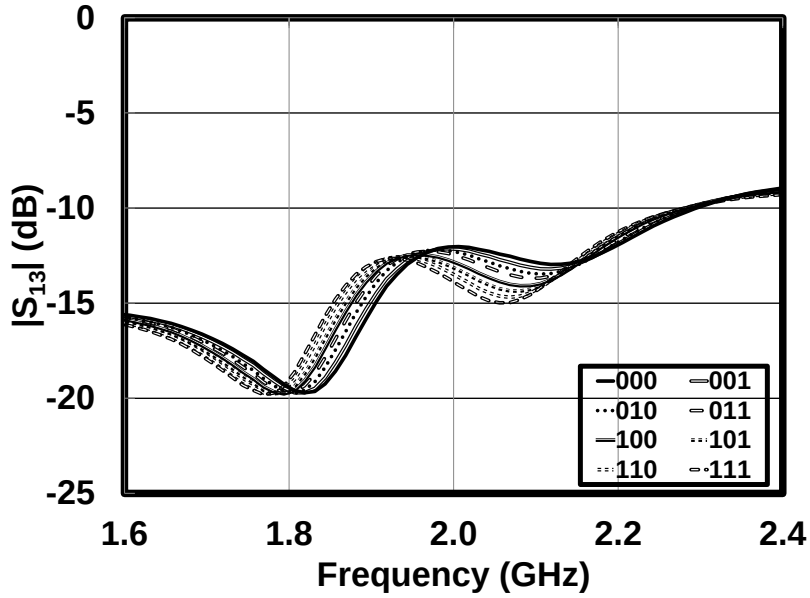
(a)



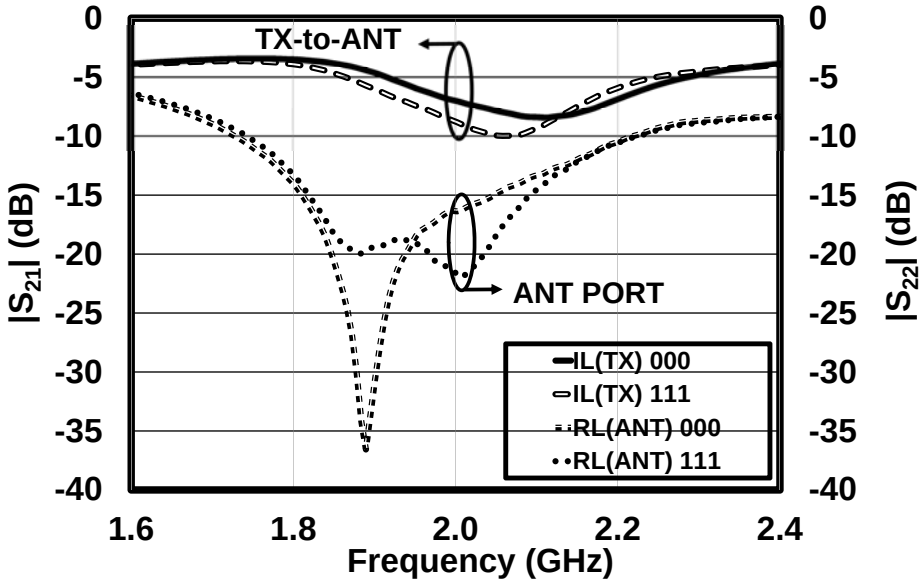
(b)

Figure. 6.10: DC control voltage board: (a) layout (b) manufactured PCB.

The DSCB's provide a tuning range of 96 MHz, which is slightly more than the designed 80MHz and more than the required 60MHz for LTE1. The insertion loss from PA port to antenna is better than 3.8dB (Fig. 6.11b), and at the Rx band, it is 5.8dB. The latter is 1dB more than simulated. Antenna matching is good with a return loss of better than -15dB, but PA port matching at -6.5dB is poor, explaining some of the Tx insertion loss. The Tx frequency is operating down the skirt rather than the centre of LFN passband as a result of process variations (unexpected extra parasitic elements) and poor Q's (higher component loss) de-tuning the network.



(a)



(b)

Figure. 6.11: Measured frequency response: (a) Tx-to-Rx isolation for different DSCB settings (b) Tx insertion loss and the return loss at antenna port for two major states (000-111).

A post-measurement study shown in Fig. 6.12 varied the inductance Q in the post-layout simulation. It indicated that an inductor with a minimum Q of 43 results

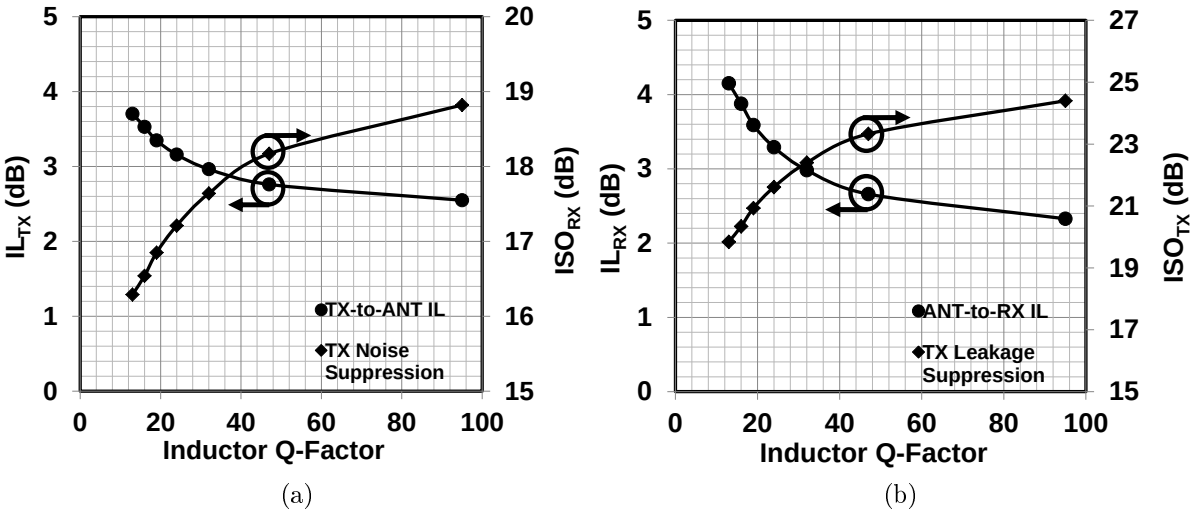
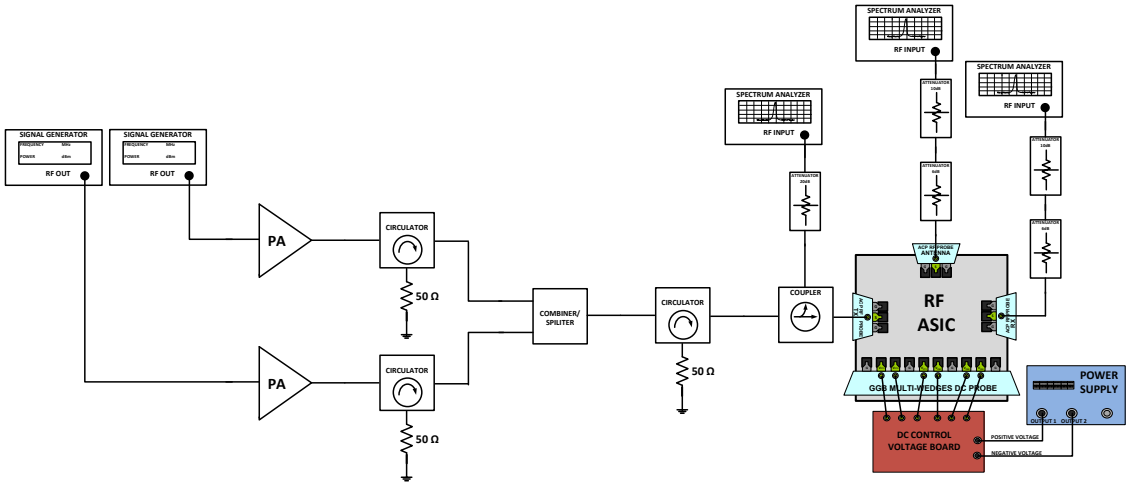


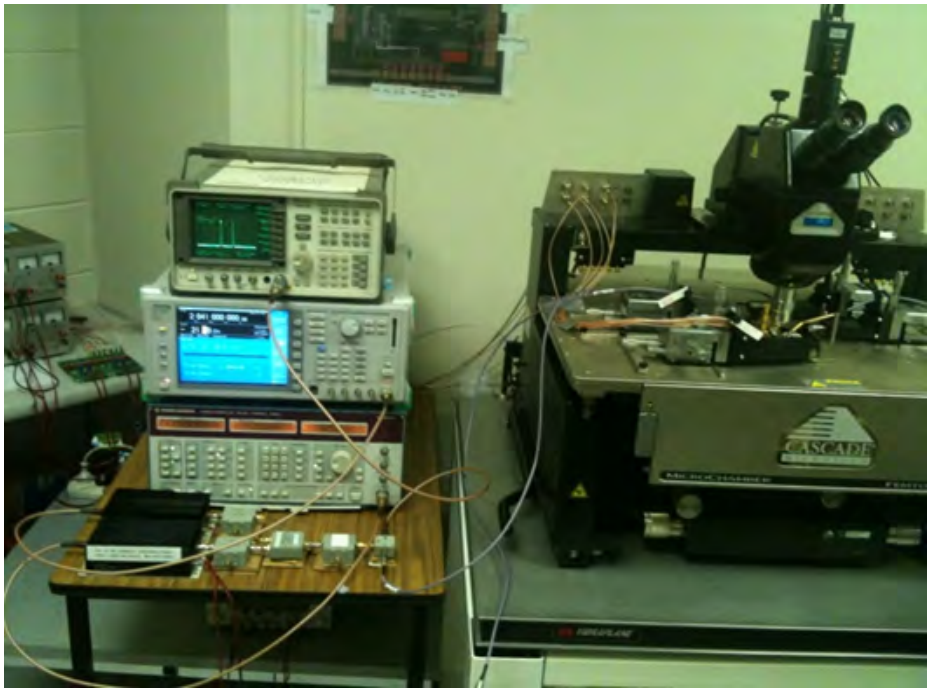
Figure. 6.12: Post-measurement study: (a) Tx filter (LFN) performance (b) Rx filter (HFN) performance.

in an IL_{Tx} of 2.8dB while it improves the ISO_{Rx} by 4.2dB to 18.2dB; the IL_{Rx} drops to 2.7dB whereas ISO_{Tx} also increases by an extra 4.3dB to 23.3dB. The circuit is clearly sensitive to inductor Q. Off-chip inductors will therefore be introduced in the next section.

It is important to avoid the generation of intermodulation distortion in adjacent channels (ACP), therefore, linearity needs to be measured. Two tones spaced 2MHz apart and with powers of 24.5dBm each were applied to the PA port in the Tx passband, see Fig.6.13. All losses associated with the discreet components of the experimental set-up were then de-embedded from the initial measured results. The worst-case relative 3^{rd} order product (IM3) occurs when the DSCB's are fully ON. The Tx-to-ANT IM3 then equals -50dB, falling to -68dB in the OFF condition; enough to meet LTE spectrum mask requirements.



(a)



(b)

Figure. 6.13: Measurement set-up for the IMDs analysis: (a) building blocks (b) experimental set-up.

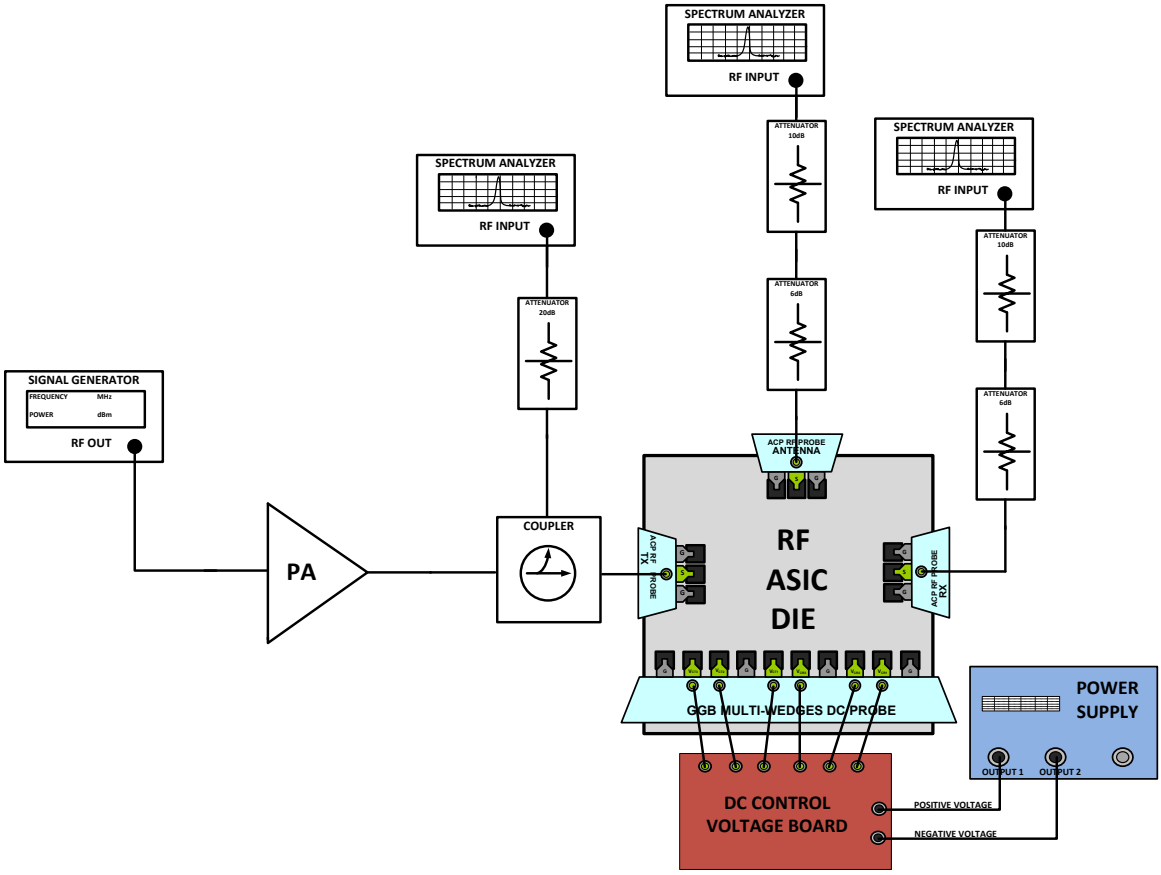


Figure. 6.14: Measurement set-up for the P_{1dB} analysis.

Fig.6.14 shows the experimental set-up to obtain the P_{1dB} points when the DSCB's are fully OFF (000) and fully ON (111). The measured results indicate that both filters have relatively linear response until the input power hits to 27dBm, see Fig.6.15. However, measurements at higher power are not valid since the output power starts to expand due to the compression of the spectrum analyser measuring the input signal power.

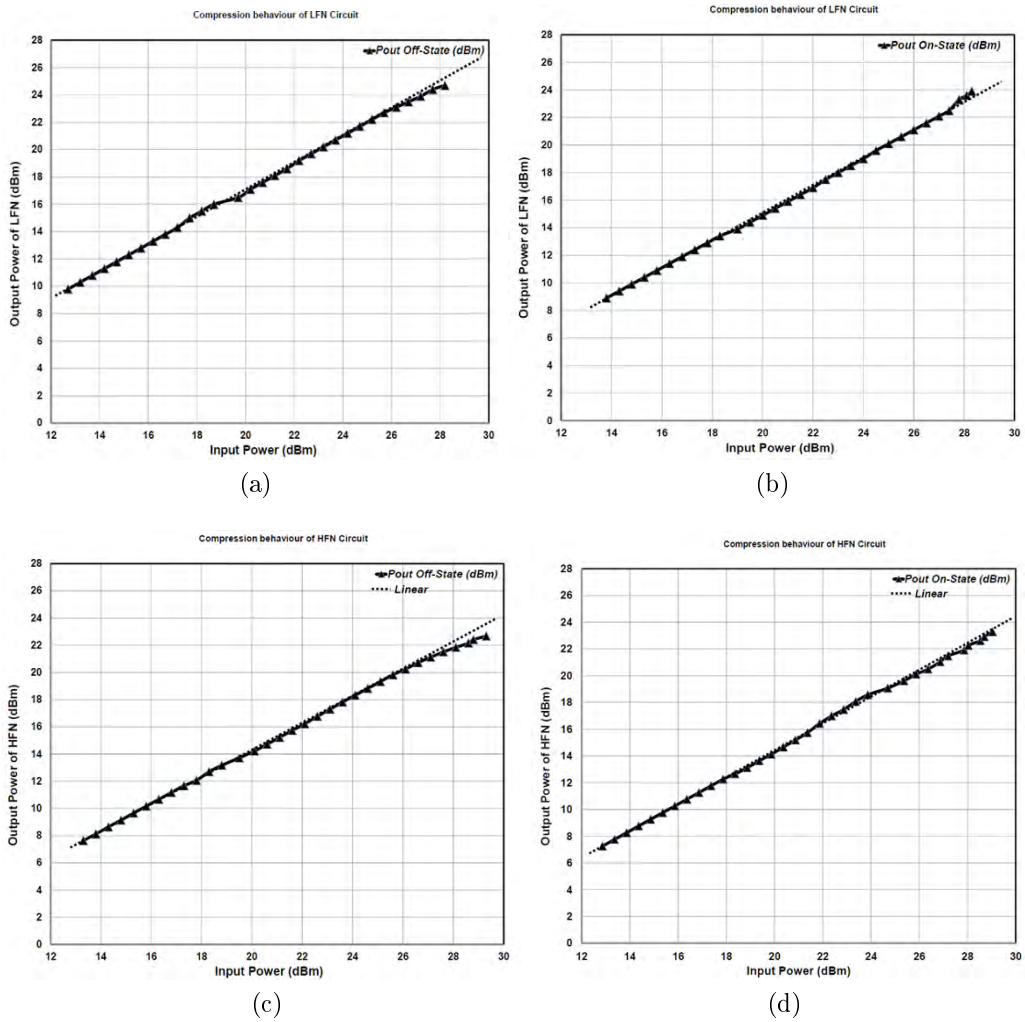
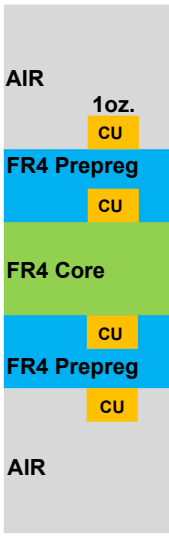


Figure. 6.15: Measured compression behaviour of the filters for Tx-to-Ant (a) Tx upper band edge (000) (b) Tx lower band edge (111), and for Ant-to-Rx (c) Rx upper band edge (000) (d) Rx lower band edge (111).

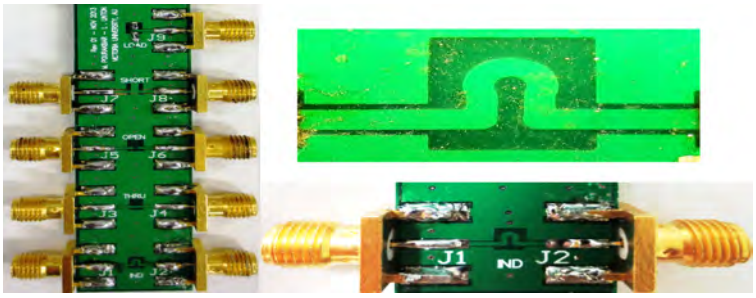
6.2 PCB Duplex Filters: Proof of Concept

The previous section indicates the need for high-Q inductors.This section describes a PCB variant with high-Q components. The switches and capacitors are commercial off-the-shelf products. Due to voltage limitations on the switches, the 'dual' LFN filter topology described in Chapter 4 is employed. This addresses the large peak voltage

issue associated with its counterpart. The structure has a lower peak voltage, however, the circuit experiences a higher peak current at resonance. The post-measurement study in the previous section indicates that the inductor Q-factor must be increased. Since on-chip inductors have a relatively low-Q, a high-Q PCB inductor was fabricated on a four-layer FR4 substrate as depicted in Fig. 6.16. In order to obtain a high Q, all the metallizations underneath the inductor loop were etched away. After SOLT (Short-Open-Load-Thru) de-embedding, the measured inductance and Q at 2GHz was 1.19nH and 125, respectively.



(a)



(b)

Geometrical Data	
Parameter	**Inductor**
Width/Spacing	0.5 mm /0.389 mm
Outer Diameter	1.490 mm
Ind. Length	2.723 mm
De-embedded Interco. Length	5.37 mm

(c)

Figure. 6.16: Laminated inductor: (a) Cross-section (b) layout from bottom: DUT, Short, Open, Thru, Load (c) Geometry.

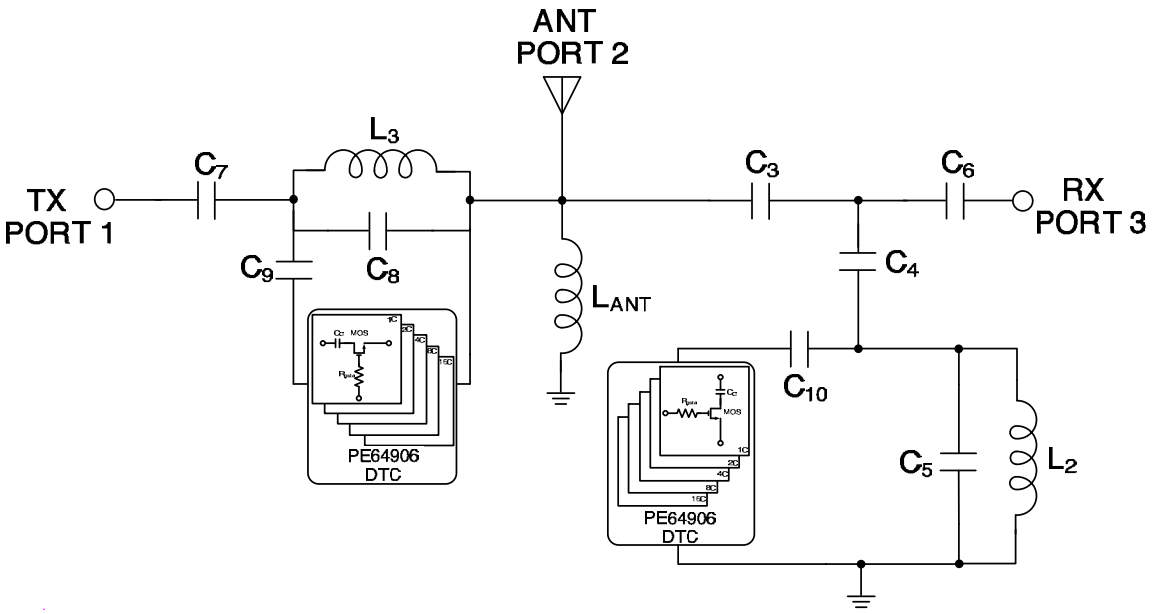


Figure. 6.17: Tunable duplex filter schematic using discrete off-the-shelf components.

Fig. 6.17 depicts the modified duplexer schematic. Commercial Silicon-on-Sapphire 5-bit digitally-tuned capacitors (DTC) were used with a tuning range of 0.9pF to 4.6pF and a Q of 40 to 13, respectively. Due to the lower Q of the DTC, it is used in series-parallel with high-Q Thin-film TDK capacitors, thus trading-off the capacitance tuning range for Q. The resulting Q of the C_8, C_9, and DTC combination varies between 89.3 to 108.2 for a capacitive adjustment of 12%. This is more than two times the Q of the DSCB and C_1 combination of Fig. 6.2 ($32.8 < Q < 34.5$). A PCB prototype according to the schematic in Fig. 6.17 was fabricated. Software was developed on an FPGA (Xilinx Virtex-5) to program the DTC's serial interface to the desired state ($00000 \sim 11111$) as shown in Fig.6.18.

The HFN filter was initially disconnected from the antenna port in order to characterise the LFN separately. Fig. 6.19 shows the test circuit and the measured frequency response of the LFN network after appropriate de-embedding. The 32 responses cover approximately twice the bandwidth specified by the LTE1 standard. The LTE1 band is marked on the figure. The IL_{Tx} and ISO_{Rx} in the band of interest are better

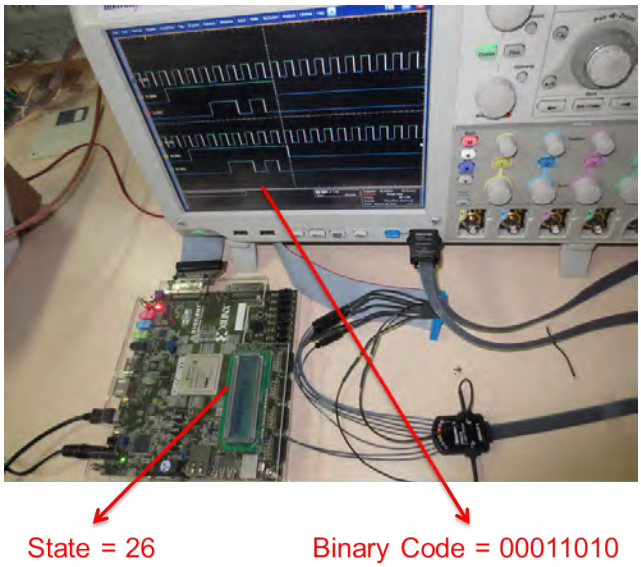
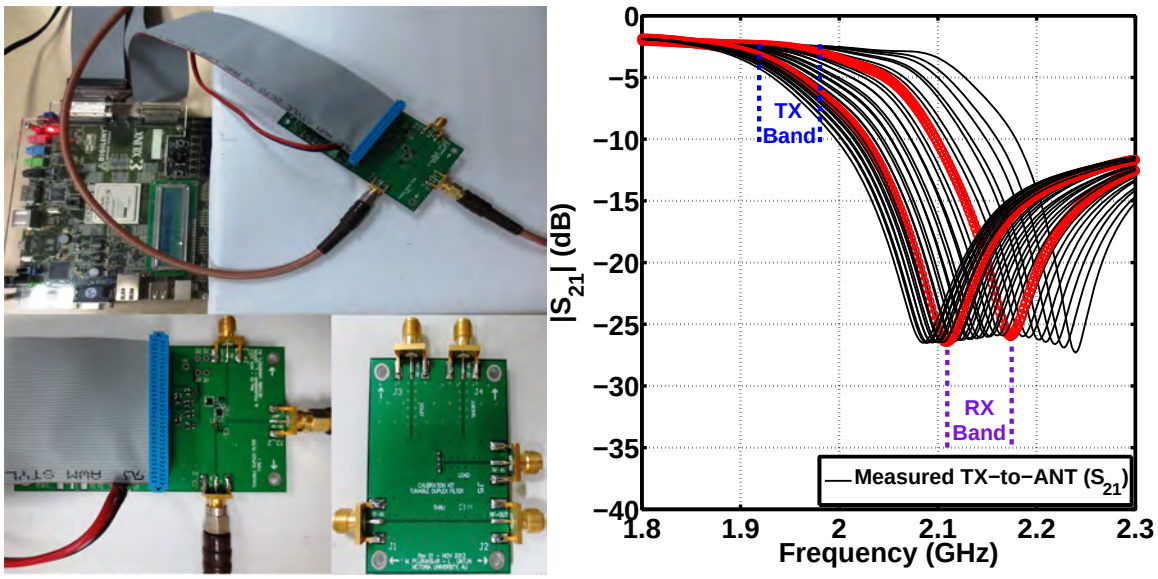


Figure. 6.18: FPGA Virtex-5 interface with a high-speed VHDC port and real-time display of decimal DTC state.



(a) (b)

Figure. 6.19: The LFN filter: (a) Top:FPGA interface. Bot LHS:PCB. Bot RHS:SOLT calibration-kit (b) measured frequency response for 32 DTC settings.

than 3.3dB and 26dB, respectively. The frequency response curves between the thick highlighted traces provide optimum ISO performance, (but not optimum IL). It is possible to trade-off isolation and insertion loss by not selecting the exact null position and operating on the null skirt. Moving the left hand boundary four traces to the right reduces isolation to 23.5dB (still better thatn the 20dB target) but improves IL to 2.9dB.

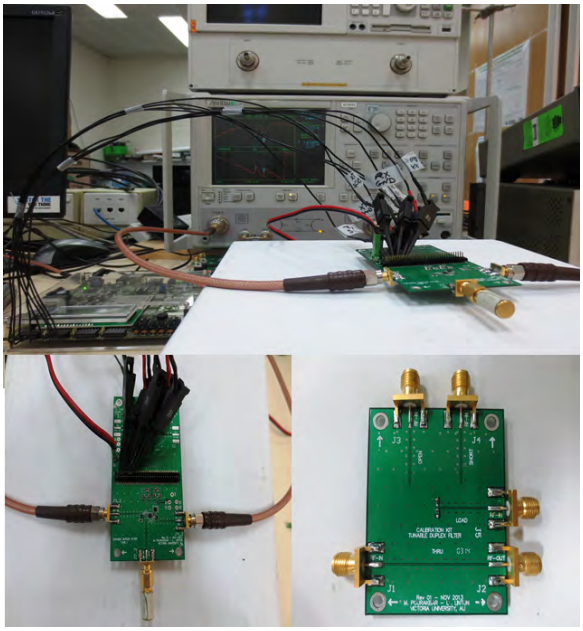


Figure. 6.20: Measurement set-up for PCB duplex filter: Bot LHS: PCB. Bot RHS: SOLT calibration-kit.

The complete tunable duplex filter was then measured (see Fig.6.20) with results shown in Fig. 6.21. The isolation is better than 25dB at Tx and 31dB at Rx frequencies, an improvement of 7dB and 18dB, respectively on the fully integrated circuit. EM-simulations predicted 10dB and 14 dB improvements. Worst-case Tx and Rx insertion loss is 3.6dB and 3.7dB, an improvement of 0.2dB and 2.1dB respectively. A lower than predicted 1.1dB improvement in IL_{Tx} occurs at one end of the band only and is due to a combination of passband frequency shift (see section 4.2) and the predicted f_d variation which could be compensated by making C_7 and C_4 tunable.

As the circuit stands a small improvement in IL can be obtained by selecting the appropriate traces as previously described.

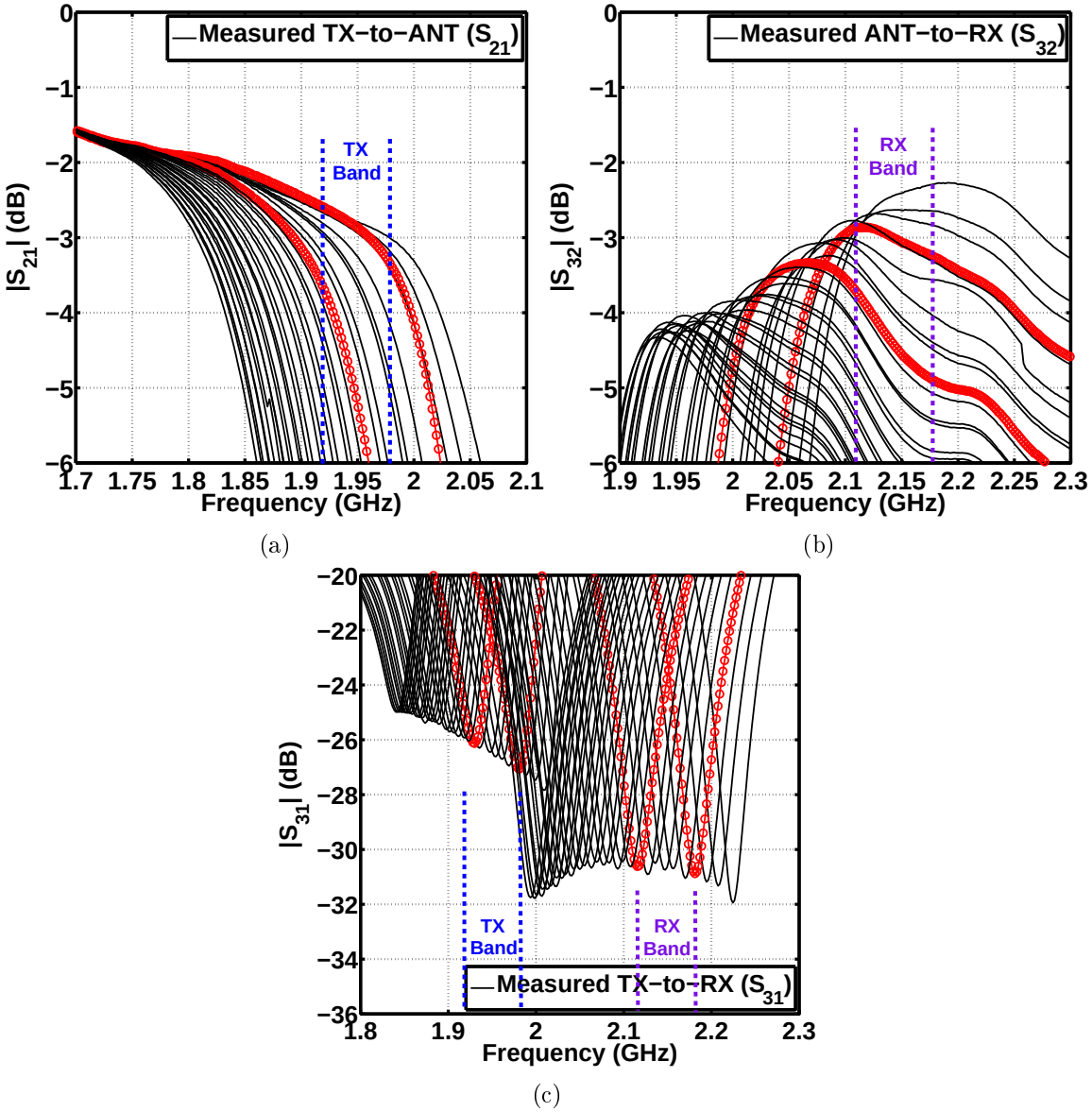


Figure. 6.21: Measured frequency response of PCB duplexer (5-bit tuning): (a) Tx-to-ANT (b) ANT-to-Rx (c) Tx-to-Rx. (LTE1 band edges shown dotted)

6.3 Summary

This chapter contains two implementations on the single-band tunable duplex filters for the LID. The fully integrated solution was developed on the SOS process. The obtained isolation is 19dB and 13-14dB for ISO_{Tx} and ISO_{Rx}, respectively. It is close to the minimum specification of 15dB for the LID. However, the insertion loss is still not competitive with the existing duplexers.

The off-the-shelf solution with PCB high-Q inductors improved the isolation performance to well above 20dB for both bands and reduced the insertion loss to 3.6dB and 3.7dB for IL_{Tx} and IL_{Rx}, respectively. These results are within 1dB and 0.5dB for the commercial SAW/BAW duplexers (Table 3.1). Further improvement is still necessary and can be addressed by improving the DTC using a combination of custom designs and modern SOI technologies with lower FOM. A recent announcement indicates three times improvement in FOM is now available [81].

The next chapter considers a multi-band solution by expanding the tuning range and controlling the duplex offset.

Chapter 7

Multi-band Tunable Duplex Filters: Simulation

High-Q passives are essential to increase the isolation and reduce the insertion loss of the LID. On the other hand, more tunable capacitors are needed to tune the structure to different LTE bands with different duplex offsets (Chapter 4). The previous chapter demonstrated high-Q inductors can be fabricated on laminates with small footprints. Therefore, multiple DSCBs connected to high-Q laminate inductors via interconnects is a potential solution to the LID problem.

Wire-bond, solder ball, and copper pillar are generally utilised as chip-to-substrate interconnects. In this chapter, the impact of these joints on the achievable quality factor of a planar inductor is investigated. Each joint is mathematically analysed using a simple pi-model in Section 7.1. Results show good agreement between model and EM-simulation results (within 10%). Two multi-band LTE duplex filter prototypes are presented in Section 7.2 and Section 7.3. The work in Section 7.2 was completed while on an internship at Ericsson and Lund University, Sweden where access to the SOI process and fabrication was provided. A summary concludes in Section 7.4.

7.1 Die-to-Substrate Interconnects for High-Q PCB Inductors

Inductors have a direct impact on the duplex filters circuit performance. Since the silicon inductors possess a low quality factor, high-Q inductors can be realised either by discrete surface mount devices or by ceramic or organic substrates. Wire-bonding or flip-chip processing are common integration methods. These processes affect the overall performance by adding extra parasitic elements to the nominal value of the inductor [82]. This section addresses the impact of chip-to-substrate interconnections on high-Q inductors in organic substrates.

7.1.1 Chip-to-Substrate Interconnections

7.1.1.1 Wire-bond Connection Model

The wire bonding process generally uses gold (Au) or aluminium (Al) wires due to their high electrical conductivity and resistance to oxidation. However, the bond wire and its large pad size introduces parasitics that substantially degrade the electrical characteristics of the designed circuit at GHz frequencies. Thus, it is necessary that the electrical parameters of the wire-bond be extracted and modelled properly. A wire bond trace is normally characterised by its inductance (L_{WB}), series resistance (R_{WB}), and the parasitic capacitance (C_{WB}) to the ground of the substrate. Fig. 7.1 shows the layout and the equivalent scalable π-model of a wire-bond. The inductance is mainly dominated by length (l) and radius (r) of the wire, and can be approximated as

$$L_{WB} \simeq \frac{\mu l}{2\pi}(\ln(\frac{2l}{r} - 0.75)) \tag{7.1}$$

where μ is the permeability in free space. At frequencies in the GHz region, the skin and proximity effects become severe resulting in the series resistance of the wire bond being frequency dependent. In order to accurately model the skin effect, the

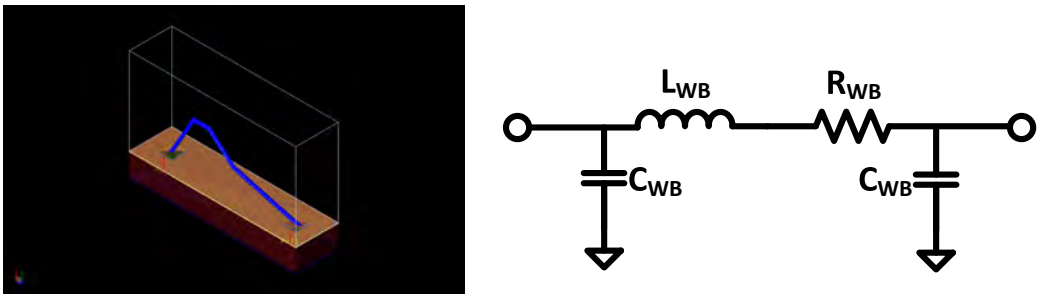
skin depth ($\delta \simeq \frac{0.075}{\sqrt{f}}$) and the conductivity ($\sigma$) of the material must be considered. Therefore, R_{WB} can be estimated by

$$R_{WB} \simeq \frac{l}{\pi r^2 \sigma} + \frac{l}{2\pi r \delta \sigma} \tag{7.2}$$

The parasitic capacitance between the wire-bond and the substrate ground (C_{WB}) can be estimated as follows [83]

$$C_{WB} \simeq \frac{2\pi\epsilon l}{\arctan(\frac{d}{r})} \tag{7.3}$$

where ϵ and d are the permittivity, and the distance between the centre of the wire-bond and the substrate ground metallisations, respectively. It should be noted that the effect of fringing capacitances is neglected in order to simplify the total capacitance expression.



(a) (b)

Figure. 7.1: Wire-bond Interconnection: (a) 3D structure of a wire-bond (b) Equivalent circuit of a wire-bond.

7.1.1.2 Flip-chip Connection Model

A flip-chip solution offers several bumping options including solder ball, gold stud bump, micro bump, and copper pillar [84]. Among these type of connections, the solder and copper pillar bumps are normally used due to their low cost, short electrical connection length, and high reliability. A flip-chip contact is generally formed

by a ball of solder paste (SB), or a copper pillar (CP), as shown in Fig. 7.2. Flip-chip contacts can be modelled as a transmission line. Considering the structure of a circular cylinder, the transition signal from die to the board is affected by the parasitic elements of the connections which are self-inductance (L_{SB} & L_{CP}), capacitance (C_{SB} & C_{CP}), and resistance (R_{SB} & R_{CP}) of the bump. For operating frequencies in the GHz region, the impact of these parasitic effects becomes severe. The Pi-model can be used to predict the behaviour of the flip-chip connections. A scalable model of a bump and a copper pillar is illustrated in Fig. 7.3. The inductance of the flip-chip connection is proportional to the bump height, radius, and overlap of the top and bottom pads. The self-inductance of a cylindrical bump is given by [85]

$$L_{SB\,\&CP} = \frac{\mu h}{2\pi}[\ln\{\frac{h}{a} + \sqrt{(1+\frac{h^2}{a^2})} - \sqrt{(1+\frac{a^2}{h^2})} + \frac{a}{h}\}] \tag{7.4}$$

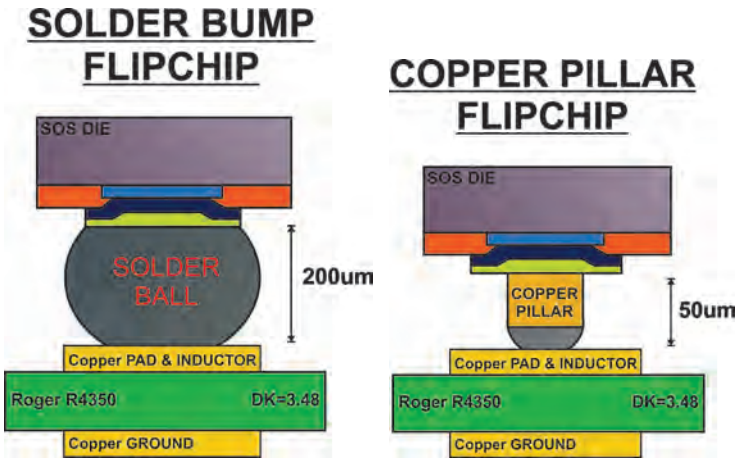
where a is the bump radius and h is the bump height. By taking the skin effect into account, the resistance of the bump can also be estimated as follows

$$R_{SB\,\&CP} \simeq \frac{\sqrt{\mu\pi\sigma f}}{\sigma\pi a}h \tag{7.5}$$

The parasitic capacitance from the flip-chip to the substrate, or chip ground metallisation, is also given by

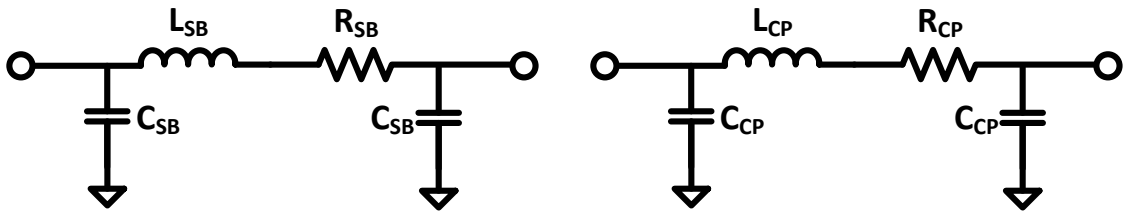
$$C_{SB} = 4\pi\epsilon a \qquad C_{CP} = \frac{2\pi\epsilon h}{\ln(1+\frac{d}{a})} \tag{7.6}$$

where ϵ is the relative permittivity of the dielectric; and d is the distance between the copper pillar and the substrate/chip ground. Simulations using Matlab and ADS Momentum were used to verify the accuracy of the models. Scattering parameters were extracted by the EM-simulator and the admittance matrix generated. The series inductance, series resistance, and shunt capacitance, of the model are computed. Table 7.1 summarises the values of the model elements at frequency of $2GHz$ for



(a) (b)

Figure. 7.2: Flip-chip bumping process: (a) Solder ball (b) Copper pillar.



(a) (b)

Figure. 7.3: Flip-chip scalable Equivalent circuit model: (a) Solder bump (b) Copper pillar.

different types of interconnects. The interconnections were simulated in a real scenario where a pad was included at each end of the connection. It should be noted that the extracted parameters of the wire-bond, the solder ball, and the copper pillar include the metal contacts at both ends. Therefore, the simulated values slightly deviate from the calculations which don't include the pads.

Table 7.1: Summary of Interconnect Modelling Parameters

	Equivalent Circuit Parameters					
Method	$L_{eff}(pH)$		$R_{series}(m\Omega)$		$C_{shunt}(fF)$	
	Cal.	Sim.	Cal.	Sim.	Cal.	Sim.
Wire-Bond	1005	1031	326	437	20.37	35
Solder Bump	50.82	56.46	34.04	31.95	10.84	6.87
Copper Pillar	25.41	26.44	23.03	24.52	7.33	8.72

7.1.2 Planar Laminate Inductor Design

7.1.2.1 Theoretical Consideration

Planar inductors are commonly used in most radio frequency integrated circuits (RFICs). Their performance is generally assessed by the effective inductance per unit area (L_{eff}), the quality factor (Q), self-resonance frequency (f_{res}), and maximum current rating. Depending on design requirements, several other temperature dependent parameters should be considered. Inductors are often constructed in different geometric shapes such as rectangular, square or circular spiral, meander, and simple stub lines. The L_{eff} depends on the inductor geometry and consists of two components given by

$$L_{eff} = L_s \pm M \tag{7.7}$$

where L_s is self-inductance, and M is mutual inductance. L_s is dominated by the conductor trace length (l), width (W), and thickness (t), while M is caused by the coupling between the adjacent conductor tracks. The mutual inductance can be either positive, where the current vectors are in the same direction, or negative if the current vectors are in opposite directions. The meander inductor is a good example of a design with negative M as the current flows as shown in Fig. 7.4. Therefore, this particular shape has a lower inductance compared to a spiral inductor with the same area. In order to calculate the L_{eff} of an arbitrary shape, [86] introduced an expression based on current sheet approximation that applies the concepts of geometry mean distance

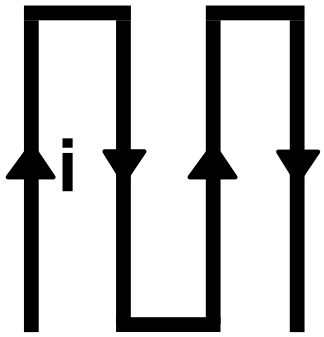


Figure. 7.4: Current (i) direction in a meander inductor shape.

(GMD) and formulates the L_{eff} as

$$L_{eff} = [\frac{\mu n^2 D_{av} C_1}{2}](\ln(\frac{C_2}{\rho} + C_3\rho + C_4\rho^2)) \tag{7.8}$$

where the coefficients for different inductor geometries are given in Table 7.2. The fill ratio (ρ) and the average diameter (D_{av}) of the inductance are functions of the outer and inner diameters of the geometry:

$$\rho = \frac{D_o - D_i}{D_o - D_i} \qquad D_{av} = 0.5(D_o + D_i) \tag{7.9}$$

Table 7.2: Coefficients for inductance expression [86].

	Coefficients			
Geometry	C_1	C_2	C_3	C_4
Square	1.27	2.07	0.18	0.13
Hexagonal	1.09	2.23	0	0.17
Octagonal	1.07	2.29	0	0.19
Circular	1	2.46	0	0.2

The accuracy of the above formula is limited to cases where $\frac{Spacing}{Width} < 3$. However,

practical inductors can be designed with a smaller spacing that improves the inter-winding magnetic coupling as well as reducing the inductor footprint. L_{eff} is dependent on the inductor shape. Fig. 7.5 compares different shapes with the same track width, spacing, and various number of turns. Increasing n adds additional conductor trace length translating to higher L_{eff} and also lower f_{res}. Equation (7.8) gives a good initial prediction for the required n. Generally, the L_{eff} is more dependent on geometry than sheet resistance and conductor trace width. The Q-factor is closely

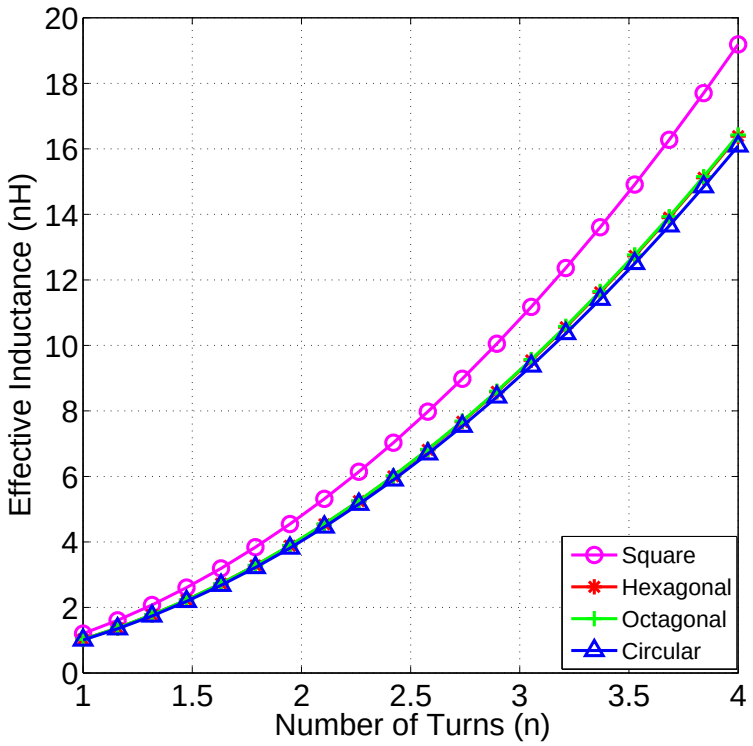


Figure. 7.5: Effective inductance value for different inductance geometries ($D_o = 1.5mm$).

coupled to the loss mechanisms in a planar inductor, which are mainly dominated by parasitic resistance and capacitance. In other words, the eddy current, skin effect, and proximity, limit the achievable Q-factor. At DC and low frequencies, the Q-factor is determined by the series resistance of the conductor turns. At RF frequencies, current cannot deeply flow into the conductor trace due to the skin effect, therefore,

the total series resistance becomes frequency dependent resulting in increased dissipation loss with frequency. To reduce this effect, a wider conductor width should be chosen. However, a wide conductor increases the parasitic capacitance between the conductor trace and the substrate, causing a reduction in f_{res}. The distance between an inductor and a nearby ground plane or ground ring plays an important role in inductor losses. This proximity effect is due to the dissipation of the magnetic energy in the ground tracks which is created by eddy currents. To alleviate this, the ground trace/plane has to be considered as an image of the inductor and must be placed at a distance of at least two times the substrate thickness from the inductor.

7.1.2.2 Practical Consideration

Silicon-based inductors exhibit a lower Q-factor compared to off-chip inductors. This is mainly due to two factors: the low resistivity of the silicon substrate, and the thinness of the metallisation (a few micrometres). Both factors encourage circuit designers to consider off-chip inductors on the printed circuit board (PCB) where a low loss dielectric can be chosen, and the copper tracks can be quite thick. However, PCB fundamentals need to be considered to avoid designing inductors that are impractical or impossible to build. Generally, the main loss mechanisms are dielectric, conductive, radiative, and design induced [87]. Nowadays, it is very common for designers to select dielectric materials with the lowest loss tangent. However, these materials seem to be difficult to manufacture and are costly. A good understanding of the loss factors may help achieve the best performance from cheaper materials. Fig. 7.6 shows that the simulated insertion loss of a transmission line on different substrates are equal for frequencies below $3GHz$. However, the impact of the substrate loss tangent becomes more dominant as frequencies increase beyond $9GHz$. In addition, the dielectric constant (Dk) can be impacted by moisture and temperature. A good material with very low moisture absorption and temperature coefficient is PTFE. Thermal conductivity should also be considered. If the inductor is used with high power signals, as expected in this work, substrates with poor thermal conductivities

will degrade the overall performance. For this reason PTFE was not chosen for the LID. Roger core material of R4350 has better thermal conductivity compared to the FR4, therefore, it was chosen here.

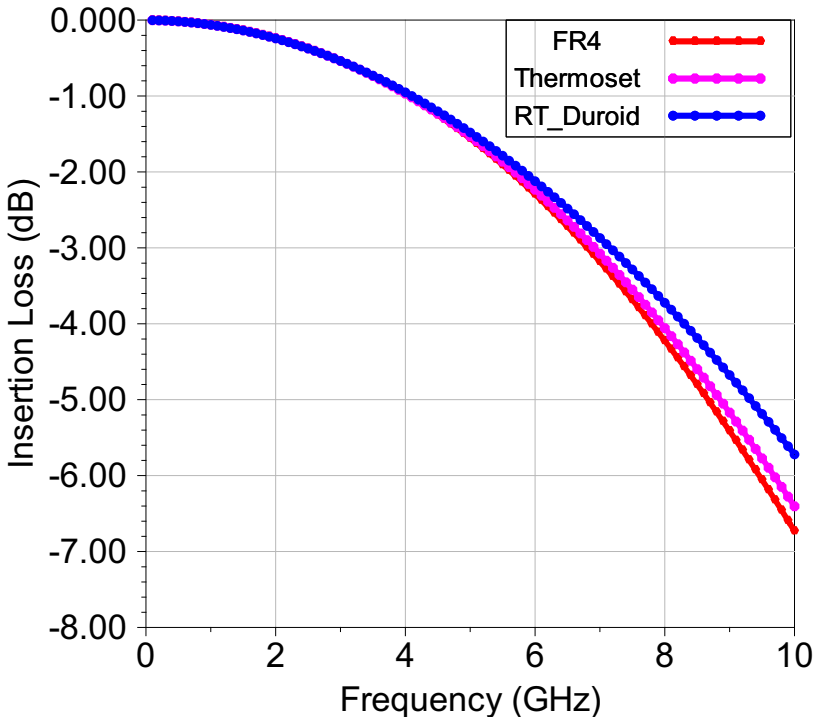
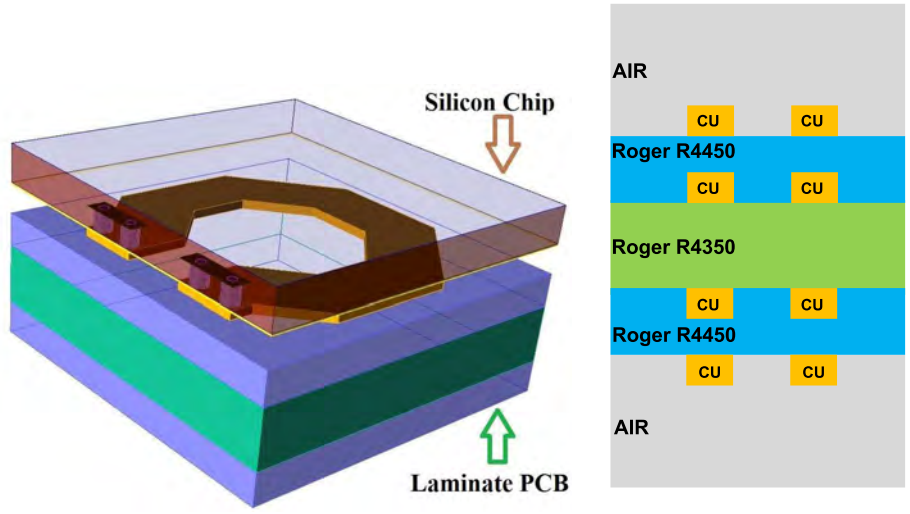


Figure. 7.6: Insertion Loss of a transmission line simulated on different laminate materials.

The conductor loss is proportional to the resistance of the metal trace, therefore the surface finish is very crucial due to the skin effect phenomena. A smooth finish would substantially decrease the loss.

Transmission lines are widely used in PCBs and are a source of radiation loss. Generally, microstrip traces on the outer layers of the PCB radiate more energy, than striplines on the inner layers. Also, discontinuities in the signal traces cause improper transitions (matching) between different transmission lines. Other PCB design factors such as, a practical PCB stack-up, proper selection of the via type, and process tolerance specification can affect the quality factor of the inductor.



(a) (b)

Figure. 7.7: Laminated inductor: (a) 3D structural geometry (b) Organic substrate cross-sectional view.

7.1.3 Simulation Results

To evaluate the flip-chip lumped model and its impact on the achievable Q-factor, a single turn hexagonal inductor of $1nH$, with a track width of $354.30\mu m$ and a spacing of $371.2\mu m$ is simulated using ADS momentum as shown in Fig. 7.7a. In order to increase the Q-factor, the standard FR4 core material is replaced by a thermoset material (RO4350) with a relative permittivity of 3.48. Fig. 7.7b shows the proposed organic substrate layer stack-up. The contact resistance between the die and the PCB changes the total resistance of the inductor and should be co-simulated with the inductor. Fig. 7.8 illustrates a comparison of performance characteristics of the inductor before and after the flip-chip process. The results indicate that the bumping method changes the L_{eff} from $1.26nH$ for the inductor on a bare PCB to $1.06nH$ and $908pH$ for the inductor connected to a silicon chip through solder balls and copper pillar, respectively. The reduction in inductance is because the bump areas reduce the length of the inductor. As mentioned earlier, the bump parasitics affect the Q-factor and f_{res}. The quality factor is degraded in the case of solder balls and copper pillars

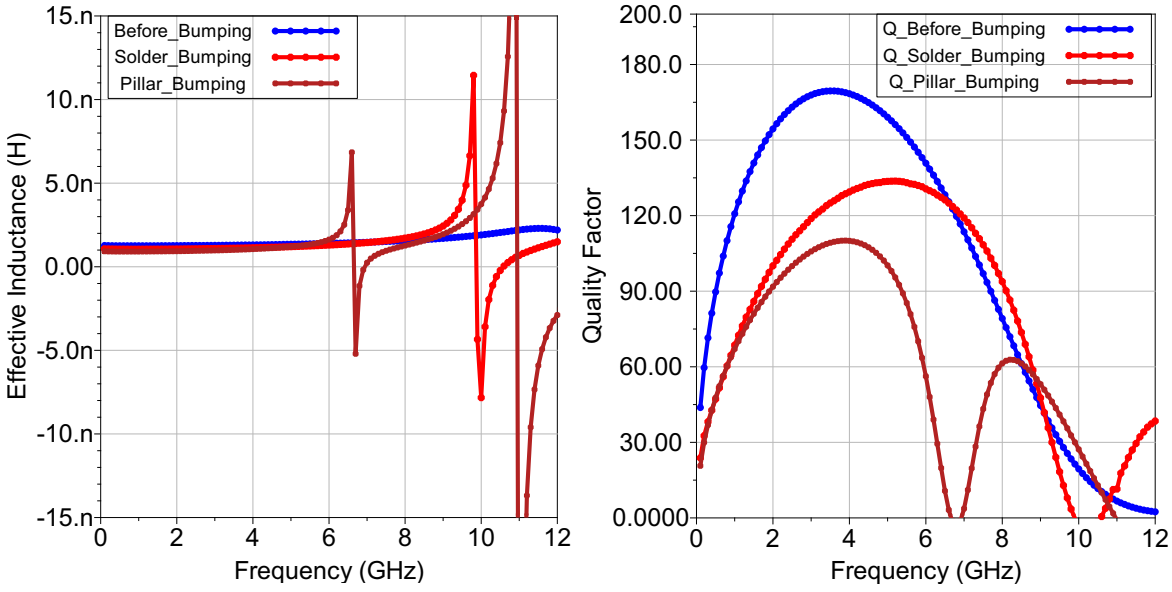


Figure. 7.8: EM-simulation results of a laminated inductor with different interconnections: (a) Effective inductance (L_{eff}) (b) Q-factor.

by 35% and 38.7%, respectively. Additionally, both cases reduce the f_{res} as shown in Fig. 7.8a. For our LID application, solder bumps are preferred. They have slightly better performance and lower manufacturing cost. Copper pillars lead to a higher density of interconnects with a smaller pitch which is not required for the LID.

7.2 Quad-band SOI Duplex Filter

The previous chapter described two solutions for the single-band LID. This section is devoted to an integrated SOI solution of the multi-band low-isolation device using the ST Microelectronics 130nm process. A passive filtering approach, relying on small footprint inductance and capacitance elements is used. Since silicon inductors are generally low Q, high-Q PCB inductors are employed. We choose a flip-chip integration approach that provides low-ohmic contacts between the silicon die and the PCB.

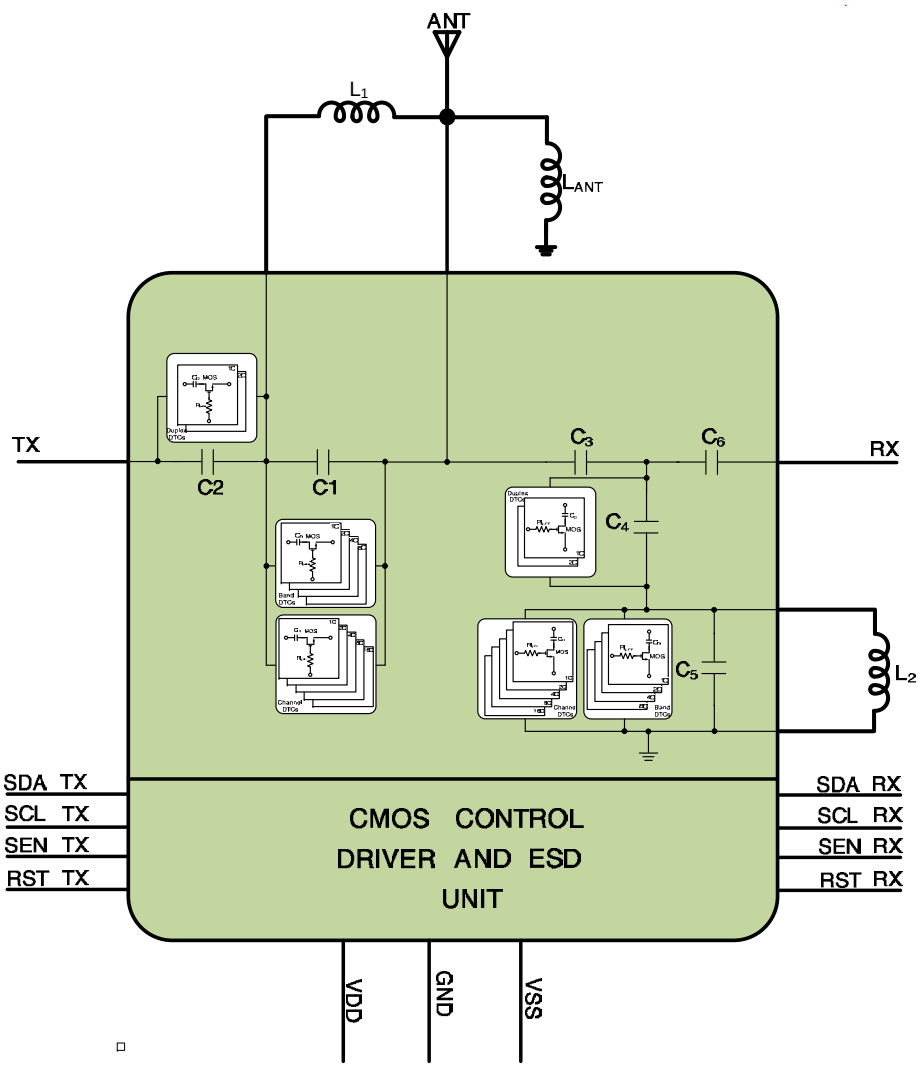


Figure. 7.9: Multi-band tunable SOI duplex filter.

The low-isolation device was designed to cover LTE band 1,2,3, and 7, for which the duplex distance is 190MHz, 80MHz, 95MHz, and 120MHz, respectively (Table 7.3). Fig. 7.9 shows the schematic of the combined LFN and HFN filters. A 130nm Silicon-on-Insulator (SOI) process was chosen due to its lower FOM of $280fs$. The LTE UE transmitter power (class 3) is currently specified at $23dBm \pm 2dBm$. Since no DC current flows through the duplex filters, SOI passive components can easily tolerate such a power. A number of FET devices are stacked to accommodate the power level.

The circuit is the same as Section 6.2 but with additional tuning on C2 and C4. The additional antenna matching inductor, (L_{ANT}), is similarly included.

Table 7.3: Frequency information of the LTE FDD bands.

	LTE Frequency Bands			
Parameter	**Band 1**	**Band 2**	**Band 3**	**Band 7**
Tx (MHz)	1920-1980	1850-1910	1710-1785	2500-2570
Rx (MHz)	2110-2170	1930-1990	1805-1880	2620-2690
f_d **(MHz)**	190	80	95	120

7.2.1 SOI DSCB Design

The DSCB consists of a number of Metal-Oxide-Metal (MOM) capacitor-FET switch sections in parallel. The tuning state is programmed through an on-chip serial interface. The channel selection, the frequency band selection, and the duplex distance are tuned by a 5-bit, 4-bit, and 2-bit DSCBs, respectively. The required frequency shift covering the frequency range sets the $\frac{C_{on}}{C_{off}}$ ratio. In this design, the band, channel, and duplex tuners have a $\frac{C_{on}}{C_{off}}$ of 3.8, 2.1, and 1.5, respectively. The designed DSCBs have the $Q_{off} > 120$, $Q_{on} > 65$. To achieve the required high power handling as well as cater for the high peak voltages seen in the resonating elements, a stacked configuration of five thick-oxide (50Å) 2.5V RF NMOS devices is used for each DSCB cell. As the large voltage swing is divided between the MOM capacitor and the MOS switch, the effective stack height (n_{eff}) (6.5) provides a maximum handling voltage of $18.5V$. Due to the high linearity requirements, a negative voltage is applied to turn OFF the FET stacks. It should be noted that the more negative the control voltage is, the better the linearity. However, this control voltage must not exceed the FET's negative breakdown voltage of $-2.5V$.

The DSCB design includes a number of layout tricks. In order to increase the breakdown of the MOS transistor while maintaining a low R_{on}, all DSCB banks use floating body NMOS transistors with a gate length of $280nm$. The contact areas

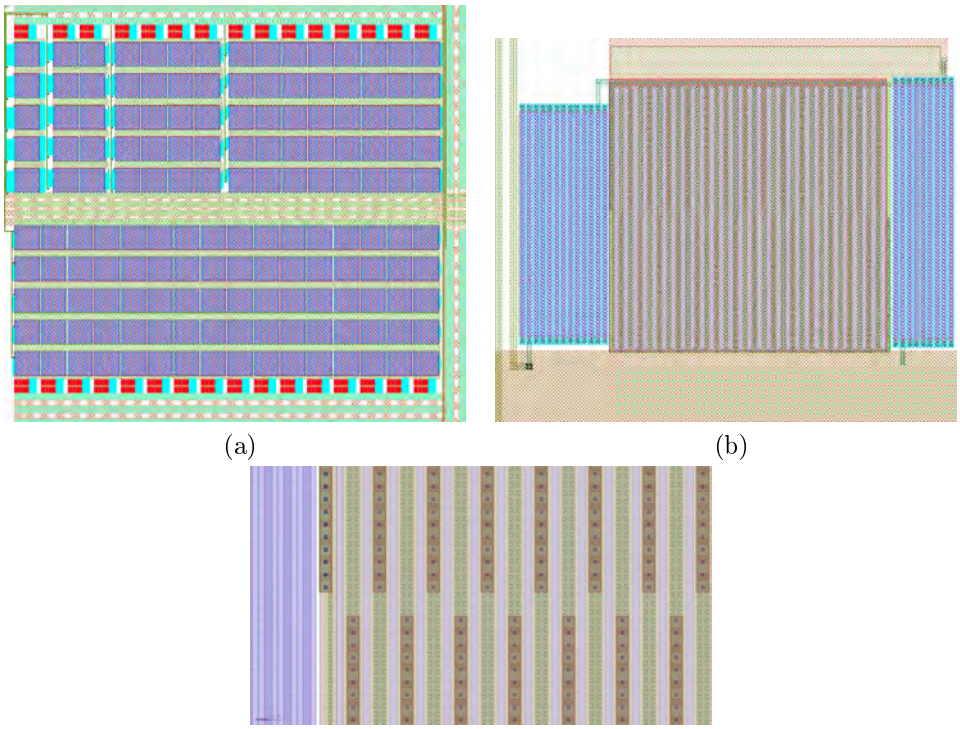


Figure. 7.10: 5-bit DSCB for fine channel tuning: (a) final layout (b) switch FET layout (c) interdigit routings for the drain/source, green: metal-1, dark brown: metals-1 to -6.

of the drain and source were expanded for multiple metallisations to reduce R_{on}. Interdigit routing lowered the C_{off}. The layout of the 5-bit DSCB for channel tuning is illustrated in Fig.7.10.

Serial-to-Parallel Interface (SPI) and ESD protection circuits are included on the chip. In order to control the LFN and the HFN independently, two 12-bit SPIs are used in the design (Fig.7.11), which select the desired LTE frequency band and channel through a serial bit stream at their inputs. The negative control voltages are generated by voltage level shifters which comprise of inverters coupled in a feedback configuration (Fig.7.12). Two inverters in a stacked totem-pole like structure provide the supply connections to a third inverter, whose output swings between the positive voltage, Vdd, and the negative voltage, Vss. When the output is Vdd, the inverter's

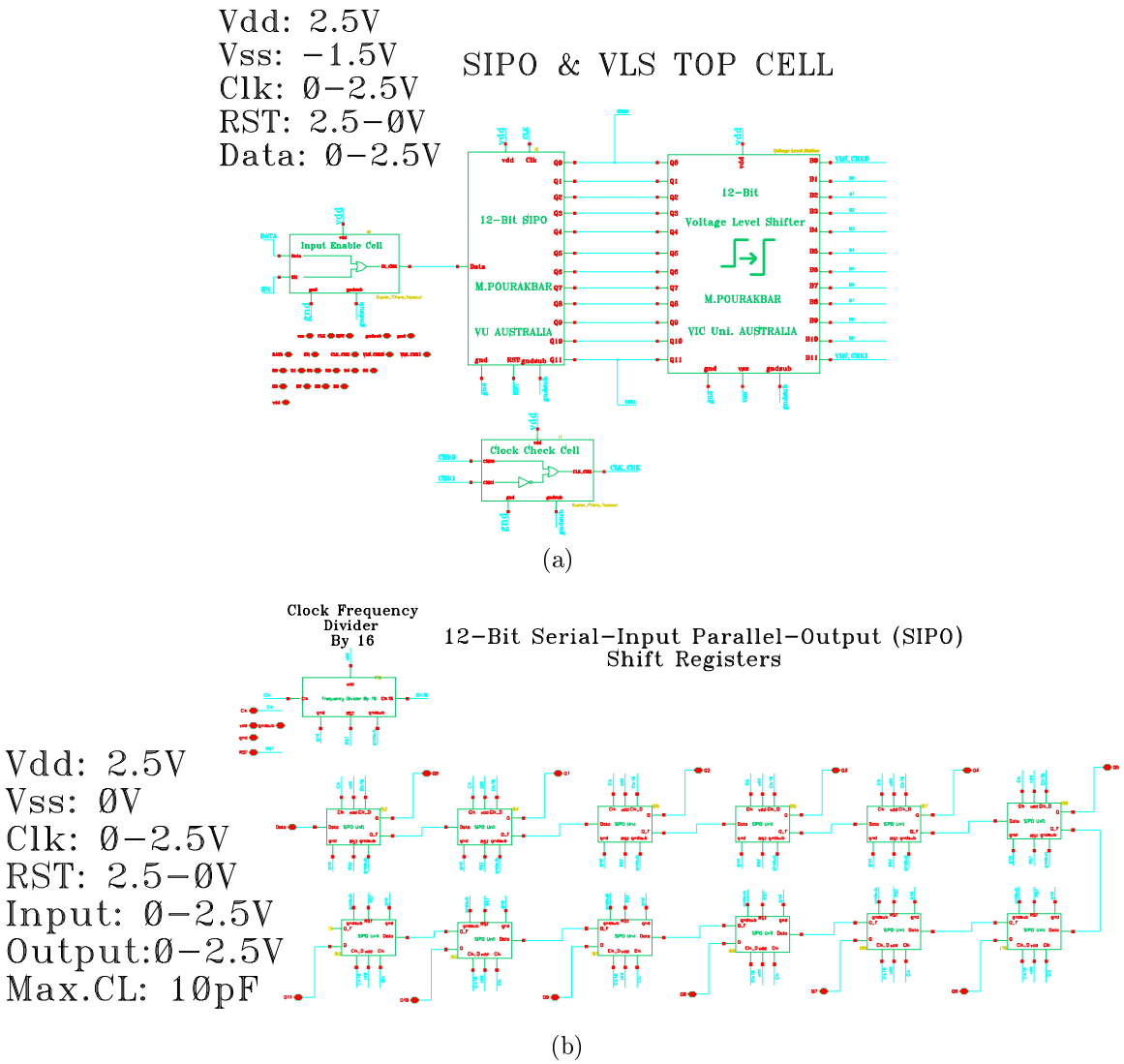


Figure. 7.11: 12-bit serial-to-parallel interface (SPI): (a) top-cell schematic (b) 12-bit serial-input parallel-output (SIPO) schematic (SIPO blocks are modified D flip-flops).

supplies are Vdd and 0V (Gnd); when the output is Vss then the inverter's supplies are 0V and Vss. Moreover, proper buffering techniques along with a wide-hysteresis Schmitt-Trigger circuit are used for all digital signal pads. The final layout of the SOI chip is shown in Fig.7.13.

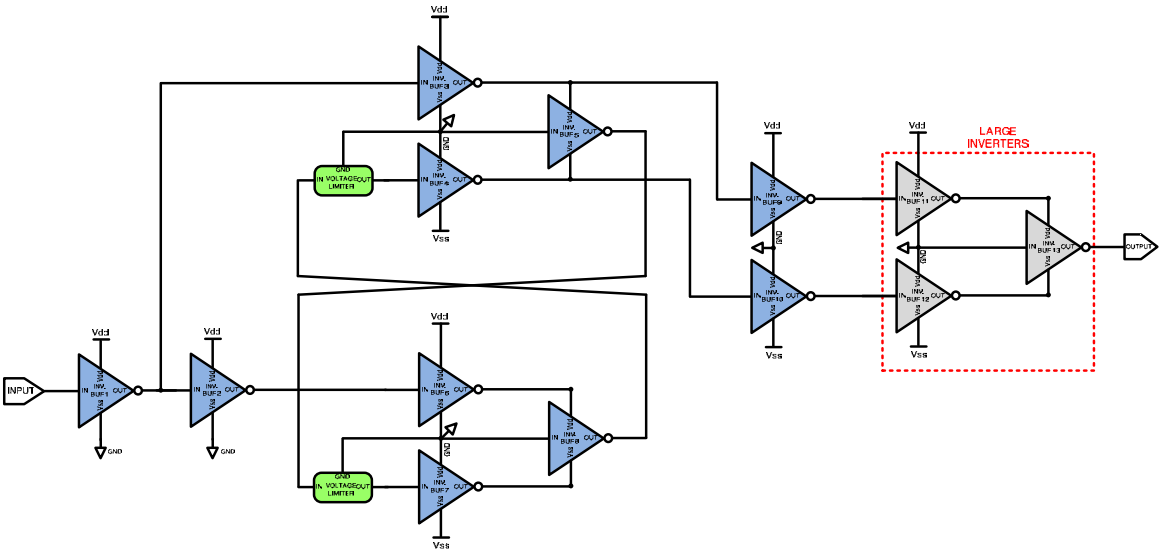


Figure. 7.12: Voltage level shifter schematic: blue: inverter buffers, gray: large size inverter buffers, green: voltage increasing limiter.

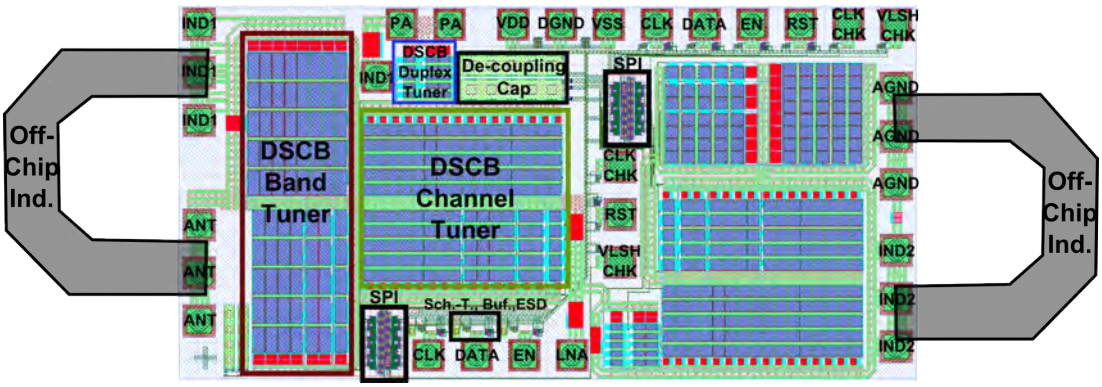


Figure. 7.13: Final layout of the SOI duplex filter.

7.2.2 High-Q Laminated Inductor Design

High-Q PCB inductors based on RT/Duriod 5880 material with a relative permittivity of 2.2 are designed. A flip chip connection with the solder ball approach was chosen due to low cost. The inductor structure including two solder balls adhered to each terminal was simulated in Agilent ADS Momentum. Fig. 7.14 illustrates the inductor layout and Table 7.4 summarises the physical parameters and simulated data of the inductor.

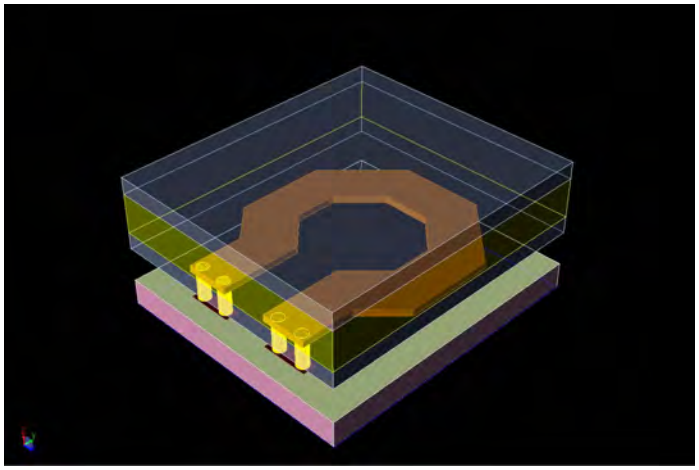


Figure. 7.14: 3D structural geometry of the laminated inductor.

Table 7.4: Parameters of 3D-EM simulated Inductor.

Parameter	**Inductor**
L (nH)	1.34
Q**-Factor**	120.20
SRF (GHz)	18.74
Width & Spacing (μm)	354.30 & 371.2
Outer Diameter (mm)	1.58

7.2.3 Simulation Results

The prototype test circuit was implemented in a 130nm partially-depleted SOI technology, the die occupies an area of $2.4mm^2$ dominated by the DSCBs. Fig. 7.15 shows the microphotograph of the chip. Due to the lead time and cost in flip-chip assembly, the rest of this section is devoted to post-layout simulation results of the circuit. Special care was taken to minimise the parasitics effects and the coupling between Tx and Rx to stop signal leakage bypassing the filters. The PA was connected to the top of the chip and the LNA to the bottom with the antenna on the lower left side. Fig. 7.16 shows the simulated Tx to Rx isolation as the filter is tuned across the specified LTE frequency bands. As expected, the low-isolation device creates two nulls at f_{tx} and f_{rx}. The critical Tx null depth exceeds $35dB$ and the Rx null depth

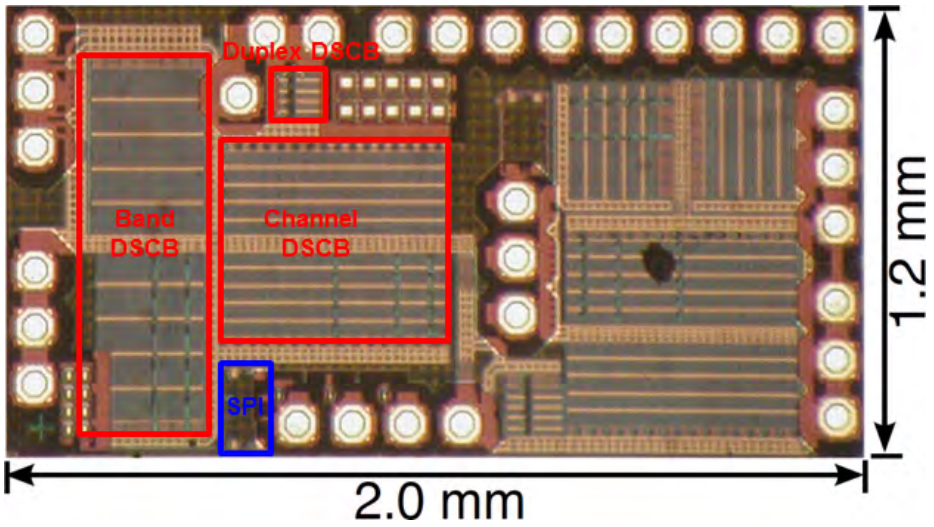
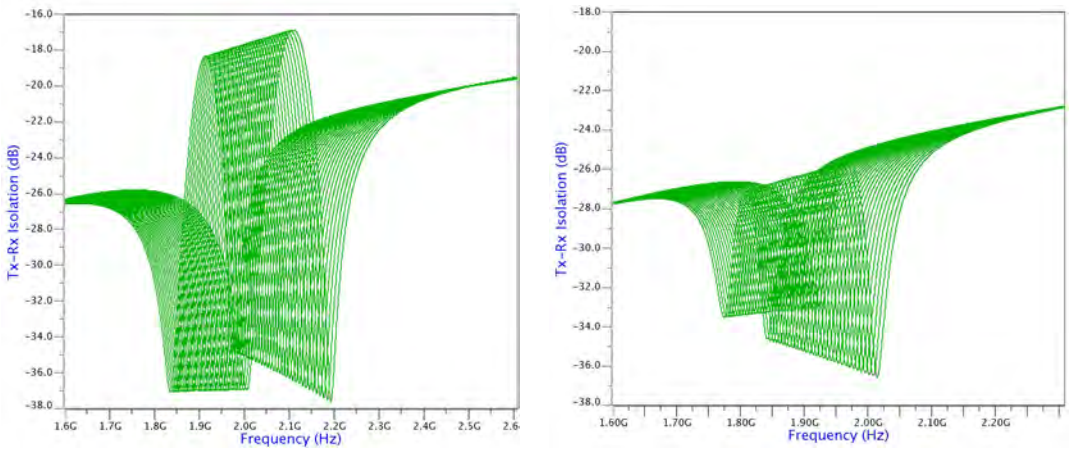


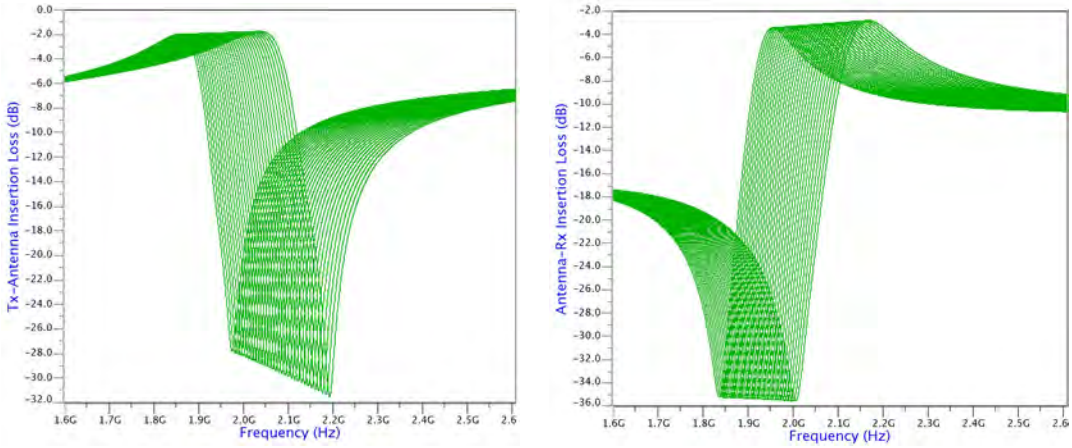
Figure. 7.15: Die microphotograph of the quad-band tunable SOI duplex filter.

exceeds $33dB$; well above the $20dB$ requirement. The simulation results indicate that the DSCBs provide larger tuning range than the specified bandwidth in both cases. Targeting the LTE1, the insertion loss from PA port to the antenna is better than $2dB$, which is $1dB$ higher than the calculations for component $Qs = 100$ shown in Chapter 4 (see Table 4.1). To a certain extent the Tx insertion loss can be reduced by lowering impedance levels and trading off some of the (excess) Rx null depth. The Rx band has $3.4dB$ insertion loss, as shown in Fig. 7.17. The use of the coil saving architecture in the HFN circuit often leads to increased Rx insertion loss. Finally, the circuit was simulated for different LTE frequency bands as summarised in Table 7.5. The reduced duplexing offset of band 2 and band 3 (80MHz and 95MHz respectively) shows up as increased insertion loss. This problem does not necessarily make the LID non-competitive, since commercial SAW and FBAR duplex filters also have the same tendency.



(a) (b)

Figure. 7.16: Tx to Rx isolation (a) LTE1 ($f_d = 190MHz$) (b) LTE2 ($f_d = 80MHz$).



(a) (b)

Figure. 7.17: Frequency, LTE1 : (a) Tx-to-Ant path (b) Ant-to-Rx path.

Table 7.5: Performance of the low-isolation device for different LTE frequency bands.

	Quad-Band LTE Low-Isolation Device			
Parameter	**Band 1**	**Band 2**	**Band 3**	**Band 7**
IL_{Tx}	2dB	3.4dB	3.1dB	2.6dB
ISO_{Tx}	37dB	33dB	34dB	35dB
IL_{Rx}	3.4dB	3.6dB	3.7dB	1.9dB
ISO_{Rx}	35dB	35dB	33dB	>38dB
$TuningRange$	225MHz	160MHz	160MHz	215MHz

7.3 Triple-band SOS Duplex Filter

A triple-band low-isolation device to cover LTE band 1,2, and 3 was designed. Fig.7.18 illustrates the building blocks of the chip. A 250nm Silicon-on-Sapphire (SOS) process

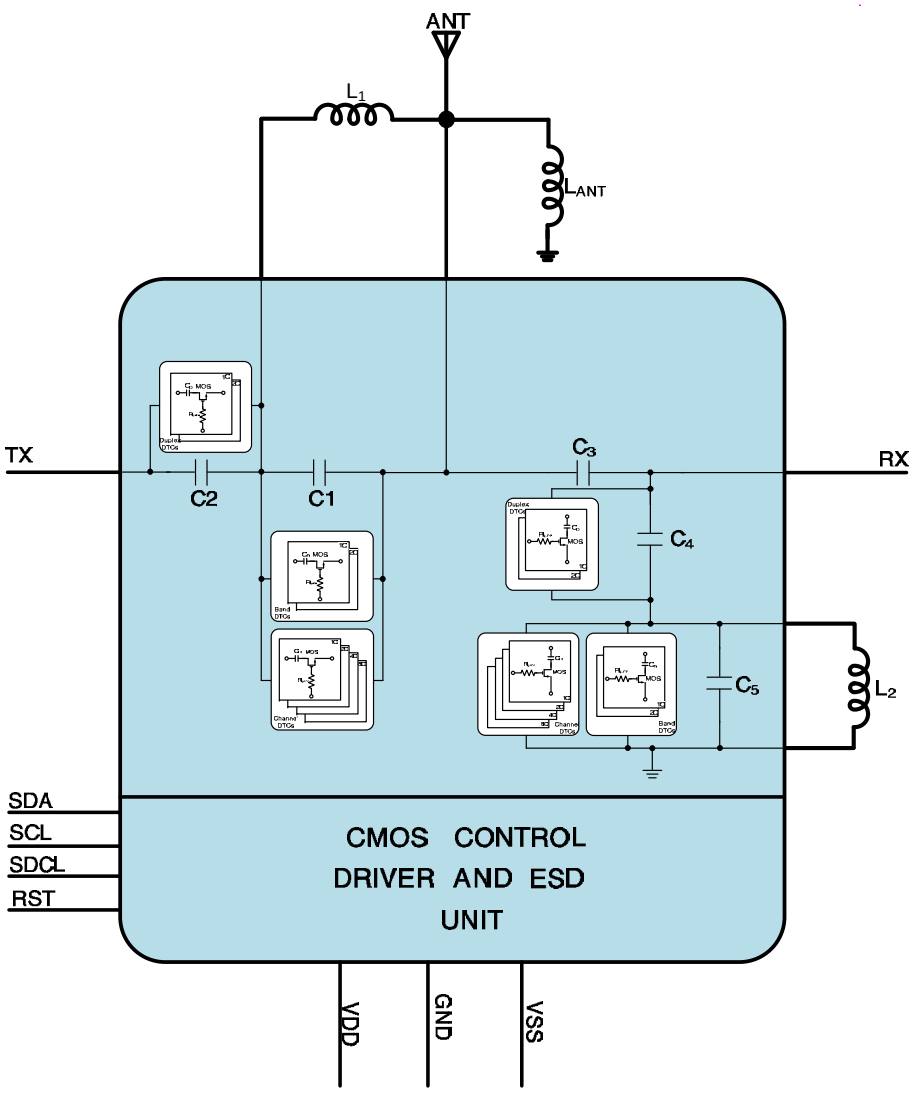


Figure. 7.18: Multi-band tunable SOS duplex filter.

was chosen due to a generously free access by Peregrine Semiconductor. The FOM is 480fs for this process, almost two times higher than the SOI process of the previous

section, hence higher switching losses and/or a reduced tuning range are anticipated. Here, the frequency adjustment range is more than halved by not including band 7. The DSCBs are re-designed for sufficient Q-factor and capacitance ratio to cover the reduced number of LTE bands. The frequency band selection, the channel selection, and the duplex distance are tuned by a 2-bit, 4-bit, and 2-bit DSCBs, respectively. In this design, the channel, band, and duplex DSCBs have a $(\frac{C_{on}}{C_{off}})$ of 4.4, 1.8, and 2.7, respectively. The designed DSCBs have the $Q_{off} > 100$, $Q_{on} > 34$. A stacked configuration of five FETs is used here.

A CMOS control driver is included on the chip. It includes an SPI, ESD protection circuits, de-coupling capacitors, wide-hysteresis Schmitt-Trigger circuits, and adequate buffer circuitries. Fig.7.19 shows the final chip layout.

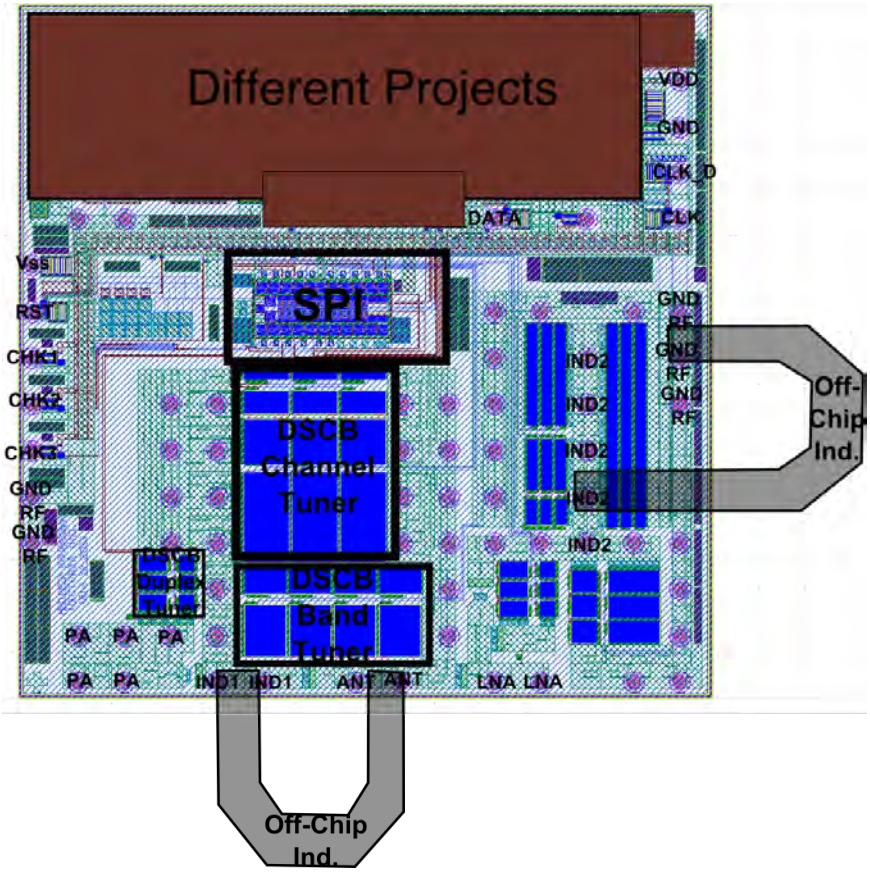


Figure. 7.19: Final layout of the SOS duplex filter.

7.3.1 Simulation Results

The triple-band duplex filter was fabricated in SOS 250nm Peregrine process, the die occupies an area of $6mm^2$ dominated by the DSCBs and wide track routings to accommodate more bond pads. Fig.7.20 displays the die photograph. The chip was defined for flip-chip mounting, however, the multi-project silicon wafer (MPW) was not post-processed for solder bumping. This was found to be too costly at the University since the die needs to be singulated first then gold stud bumps are manually placed by a third-party company. No experimental work could therefore be done for the chip. An attempt at wire bonding was unsuccessful due to the small area of the pads. Only post-layout simulation results are given.

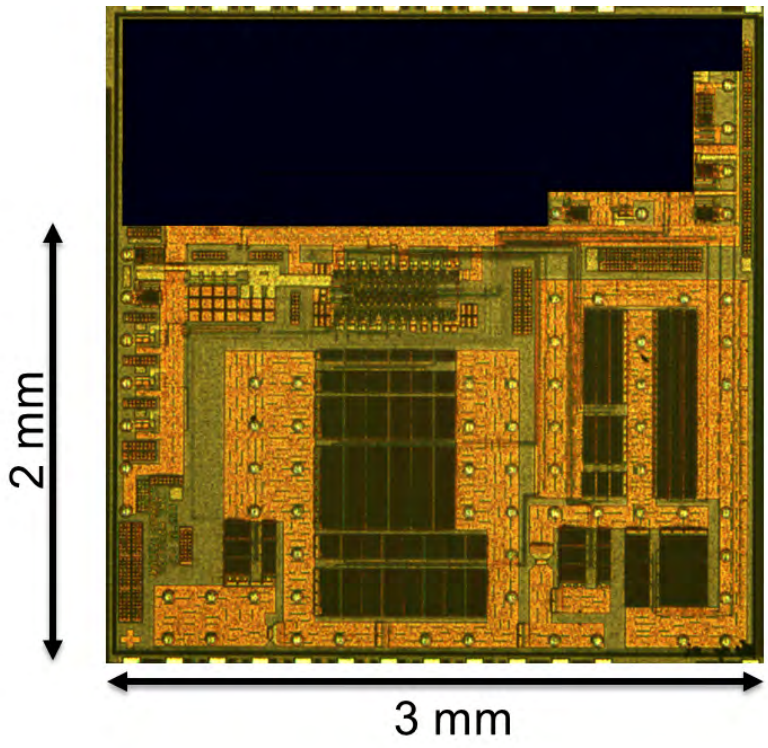


Figure. 7.20: Die microphotograph of the triple-band tunable SOS duplex filter.

Fig.7.21 shows the simulated frequency response of the filters tuned for the LTE1. Two null-depths of 29dB and 32dB were achieved. These are well above the target

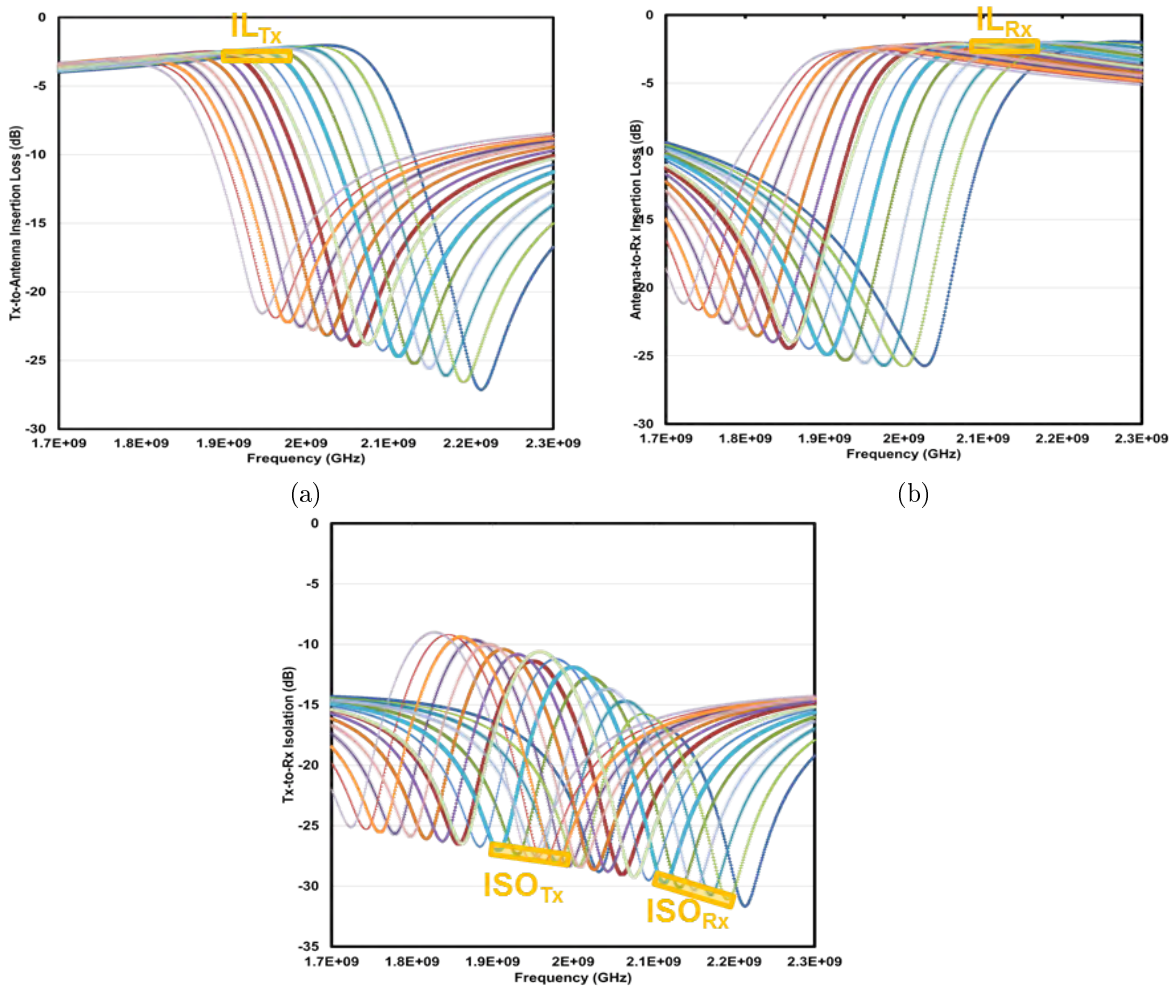


Figure. 7.21: Frequency response of the filters in LTE1 : (a) Tx-to-Ant path (b) Ant-to-Rx path (c) Tx-to-Rx path.

isolation for the LID across the specified frequency band. The insertion loss of better than 2.5dB was obtained for both the Tx and the Rx band, a slight improvement on the previous SOI circuit. LTE2 has a small f_d of 80MHz making it the most difficult band. A worse-case IL_{Tx} and ISO_{Rx} of 3.8dB and 19.3dB were simulated, respectively. Table 7.6 summarises the simulation results for the three different LTE frequency bands.

Table 7.6: Performance of the LID for different LTE frequency bands.

	Triple-Band LTE LID		
Parameter	**Band 1**	**Band 2**	**Band 3**
IL_{Tx}	2.1dB	3.8dB	3.2dB
ISO_{Tx}	29dB	19.3dB	20dB
IL_{Rx}	2.4dB	2.8dB	2.6dB
ISO_{Rx}	32dB	25.5dB	27.7dB
$TuningRange$	320MHz	250MHz	250MHz

7.4 Summary

In this chapter, the impacts of die-to-substrate interconnections on a laminated inductor are investigated. Solder ball and copper pillar significantly reduce the contact resistance between the silicon die and the PCB substrate. The simulation results show that an inductor of $1.06nH$ designed on a thermoset substrate material and adhered to a silicon chip via a couple of solder bumps, can achieve the quality factor of 100. This inductor might be directly used inside a package for the tunable LIDs.

Two LC-based multi-band tunable low-isolation devices were presented. The first prototype was implemented in a 130nm SOI process and provides an isolation exceeding 30dB at both Tx and Rx frequencies for each of four specified LTE bands (1, 2, 3, and 7). The fabricated circuit occupies an area of 2.0mm×1.2mm.

The second prototype was demonstrated in an older technology, 250nm SOS. The FET switch FOM effectively reduces the tuning range by one band. Simulations show that the circuit can meet the isolation requirement of an LID covering three LTE bands (1, 2, and 3). The insertion loss was better than 2.5dB across LTE1. The size of the fabricated circuit is 3.0mm×2.0mm.

The reported isolations can be further improved by applying an additional cancellation technique in an adaptive duplex solution. A summary of the measurement and simulation results for the described LIDs are compared with some alternative duplexer technologies in the next chapter.

Chapter 8

Conclusion

Nowadays, the LTE mobile communication standard is widely adopted throughout the world. This new standard creates more design challenges for handset manufacturers in order to offer compatible mobile phones while maintaining low build cost. Currently, the handset industry uses fixed frequency bandwidth components for each of the supported bands. In frequency division duplexing (FDD) systems, one such component is the duplexer. This is a series of highly frequency selective SAW/FBAR band-pass filters that are designed to isolate the sensitive receiver circuits from the high-power transmitter output. These not only demonstrate low-noise, high-linearity features but also have bulky size and require an additional off-chip inductor at their balanced port. As indicated in Chapter 2 there are now 32 FDD bands in operation somewhere in the world. To provide support for the many operating bands in the LTE system, a set of duplexing filters and an RF switch are required for each frequency band. In addition, a duplexer is required for each antenna in a MIMO system. These drawbacks in traditional handset design provide the motivation to develop alternate wideband tunable adaptive duplexer solutions for LTE handsets.

Chapter 3 reviewed current and proposed duplexer structures concluding with the the wideband adaptive architecture of [53]. The need for multiple switched duplexers is eliminated by using a low isolation device (LID) combined with a double

loop cancellation process. The goal of this Thesis was to develop a suitable LID. In operation, the LID needs to create an initial isolation of about 15∼20dB and then an active double-loop cancelling technique is used to further increase transmit-to-receive isolation. The cancelling circuit can form up to two nulls at separate frequencies by controlling the gain and phase settings of the loop coefficients. The transmit data and a pilot signal are used to control the cancelling loops. The original work used a wideband circulator to create the initial isolation. Such a device is suitable for a base station when the antenna system is always matched. However, this would not be suitable for hand-held devices due to the undetermined impedance of the antenna. In this work, the circulator is replaced by a tunable set of duplexing filters which enable the scheme to cover multiple channels and frequency bands.

This thesis investigated two possible bandpass-bandstop networks, a low frequency (passband) network (LFN) and a high frequency network (HFN). The theory developed in Chapter 4 showed the performance of the two networks is dominated by the impedance level of the network elements and the Q of the primary resonant circuit which must be high particularly when the duplexing offset is small. The impedance level of the components determines the trade off between stop-band isolation and pass-band insertion loss. It also determines the voltage enhancement, caused by network resonances, which has a major impact on the switch design for the fabricated solutions. High voltages in the OFF state require a large number of stacked devices to share the voltage, which is significantly easier when the devices are implemented on an insulating substrate, such as Silicon-on-Sapphire (SOS) or Silicon-on-Insulator (SOI). The use of dual circuits provides more impedance level choices and therefore trade-offs between voltage and current levels within the components.

Chapter 5 briefly described the SOI and SOS processes and compared them to normal bulk CMOS. The $R_{on} \times C_{off}$ figure of merit (FOM) for a FET switch was introduced as was the biasing and stacking operation required for high voltage operation. Low FOM's are preferable and the SOI process had the best performance. Simulations of an eight transistor stack illustrated voltage sharing in the OFF state

and distortion generation in the ON state.

In Chapter 6, both a fully-integrated LID and a discrete LID were designed and tested, targeting LTE band 1. The former is a digitally tunable LC-based duplex filter fabricated in 250-nm SOS process; it measured $19dB$ of isolation at the transmit frequency and $14dB$ of isolation at the receive frequency while achieving the required tuning range of $60MHz$ for LTE1. However the insertion loss was poor particularly on the receiver side ($\approx 5dB$). SOI/SOS inductors have higher Q than their CMOS counterparts, but in this application the Q's are far short of what is needed. Off-chip inductors are thus necessary to reach targeted performance. The discrete solution used off-chip passives and commercial off-the-shelf digitally tuned capacitors (DTC) mounted on a PCB. The null-depths were improved to below $-25dB$ and the insertion loss reduced to $3.6dB$. The commercial DTCs were not optimised for this application and further improvements can be expected by custom designing the switches and using good Figure of Merit Transistors.

Today's smart phones need to operate in different operating bands and standards due to roaming purpose. Therefore, multi-band duplexers are fruitful. In Chapter 7, two partially-integrated solutions for multi-band tunable LIDs were proposed. The first prototype is a quad-band tunable LID which supports four common LTE bands (1,2,3, and 7). It was implemented using a 130-nm partially-depleted SOI process. The simulation results showed that the isolation exceeded 30dB at both Tx and Rx frequencies for each intended LTE band. The circuit was fabricated and occupies an area of $2.4mm^2$. The second prototype was a cut-down version of the previous chip (only triple-band) which covered LTE 1,2,3. The 250-nm SOS process used for implementation had a poorer FOM which restricted the tuning range. The simulated isolation was almost 30dB for LTE1. However, it was degraded to about 19dB for LTE2 with the smaller duplex offset of 85MHz.

Table 8.1 compares some alternative duplexer technologies. The circulator used in [53] is wideband (1 octave) but is very bulky. Small circulators such as in [88] have a narrow bandwidths (7%) making them unsuitable for the larger duplex offsets

(10%). Couplers have a wide bandwidth but suffer from a high insertion loss on the coupled port [89], reducing this is at the expense of increasing the loss on the direct port. A 3dB coupler has a minimum of 3dB loss on both ports. Hybrid balancing networks have a wide bandwidth [40]. However, like couplers, there is a 3dB loss in the balancing network. There is also the problem of maintaining balance at both Tx and Rx frequencies concurrently. Dual antennas, if they are closely spaced, have narrow bandwidths [20]. Larger spacing increases bandwidth and real-estate. Filtering techniques are less affected by antenna mismatch compared to couplers and circulators. SAW devices have good isolation and insertion loss but are not tunable [90]. The solutions proposed here are tunable, but have higher insertion loss than the SAW devices they are meant to replace. The PCB solution is competitive in terms of IL as predicted by EM-simulations, but the measured results missed the target by 1dB on the Tx side.

Table 8.1: Performance summary and comparison.

Ref.		**Circulator [88]**	**Coupler [89]**	**EBD [40]**	**Dual Ant. [20]**	**SAW Dup. [90]**	**This work**					
Tech.		Ferrite	0.18-um CMOS	90-nm CMOS	LC Matching FR4 PCB	Surface Acoustic Wave	Lumped LC 250-nm SOS		Lumped LC FR4 PCB		Quad-band SOI	Triple-band SOS
Freq. Range (MHz)		1880-2025	600-1300	1700-2200	2420-2500	1950-2140	1920-2170		1830-2220		1710-2170	1710-2690
IL	**Tx**	0.25dB	0.8dB	4.7dB†	0dB	1.8+0.9*= 2.7dB	**Sim.**	**Meas.**	**Sim.**	**Meas.**	**Sim.‡**	**Sim.‡**
							3.8dB	3.8dB	2.6dB	3.7dB	2.0dB	2.1dB
	Rx		16dB	>3.8dB†		2.4+0.9*= 3.3dB	4.8dB	5.8dB	3.5dB	3.8dB	3.4dB	2.4dB
ISO	**Tx**	23dB	>20dB	70dB	>15dB	50dB	17.5dB	19dB	28dB	25dB	35dB	29dB
	Rx			40dB		42dB	13.5dB	14dB	28dB	31dB	37dB	32dB
Tuning Range (%)		NO	NO	29.4	NO	NO	3.0	4.8	8.2-11	12	11.5	16.4
Size (mm^2)		412	0.09§	2.52	1155	3.2	2.42		121¶		2.4	6

*Assumes Peregrine PE42694 SP9T switch and 0.3dB PCB loss.
†Assumes antenna balun with 0.8dB loss.
§Core size without the capacitors in PCB.
¶Core size with de-embedded SMA launches and traces.
‡Simulation results for LTE band 1.

8.1 Future Work

- Clearly the two multi-band integrated solutions fabricated using the SOI and the SOS processes (Chapter 7) need to be tested. Enough funding and proper assembly methods to do this are necessary.

- The HFN network generally has greater insertion loss compared to the LFN network. This is because the single inductor HFN involved a compromise of replacing what should have been a quarter-wave transmission line with a capacitor. Fig. 8.1 shows both the design used in this work (same as Fig 4.10) and the design with an additional inductor, which should lead to improved HFN performance. Note the inductor between antenna and ground (Fig. 8.1 top) will be absorbed into the antenna tuner.

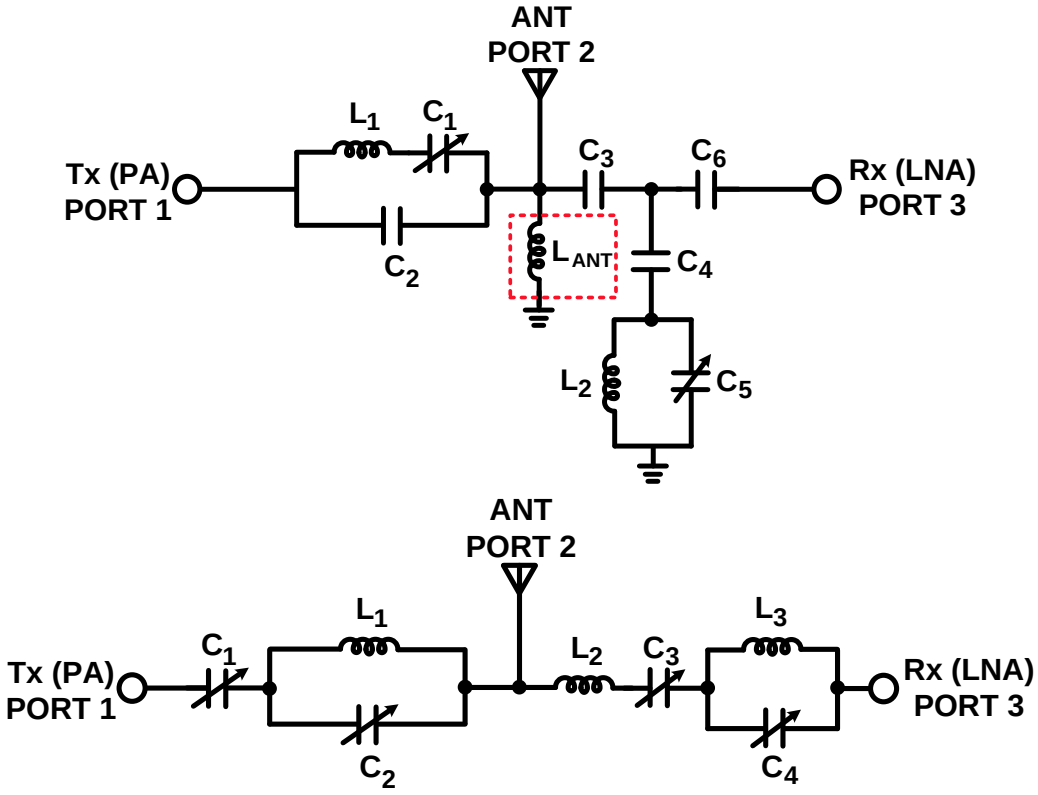


Figure. 8.1: Tunable duplex filters with the coil-saving HFN (top) and the proposed non-coil saving HFN (bottom).

- More isolation nulls are needed to accommodate different carrier-aggregation (CA) scenarios. A possible solution is to cascade more LFN/HFN networks in each transmission path. For instance, a tunable duplex filter topology for a CA scenario with two transmit and two receive frequencies is shown in Fig. 8.2. The structure creates two isolation nulls in both the Tx and the Rx bands.

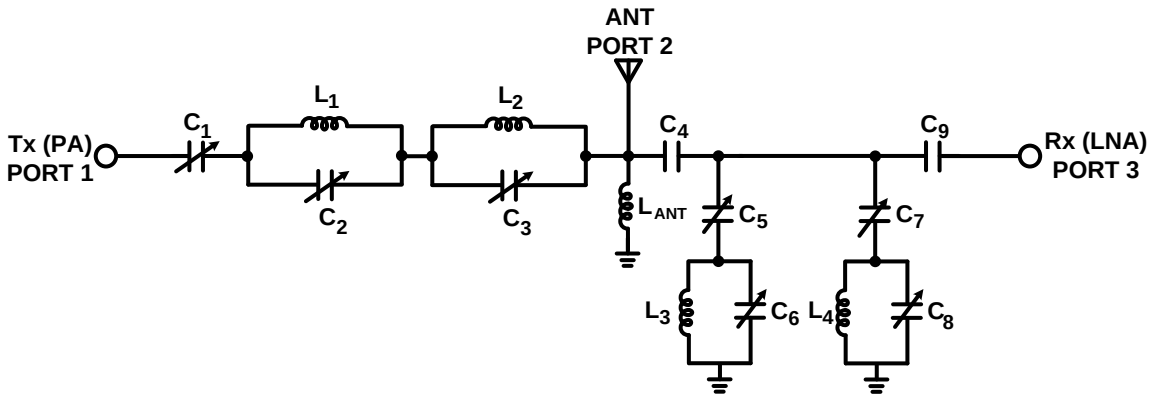


Figure. 8.2: Proposed tunable duplex filters structure to support a carrier-aggregation scenarios ((f_{Tx1}, f_{Tx2}) and (f_{Rx1}, f_{Rx2})).

- Other Ph.D. students have designed the gain-phaser adjusters for the cancelling loops and the pilot sub-system for the adaptive duplexer. Integration of these with the LID in a single silicon chip is the ultimate aim.

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